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AX8052F143

SoC Ultra-Low Power RF-Microcontroller for RF Carrier Frequencies in the Range 27 - 1050 MHz

ON Semiconductor®

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OVERVIEW

Features

SoC Ultra−low Power Advanced Narrow−band RF−microcontroller for Wireless Communication Applications

- QFN40 Package
- Supply Range 1.8 V − 3.6 V
- −40°C to 85°C
- Ultra−low Power Consumption:
  - CPU Active Mode 150 μA/MHz
  - Sleep Mode with 256 Byte RAM Retention and Wake−up Timer running 900 nA
  - Sleep Mode 4 kByte RAM Retention and Wake−up Timer running 1.5 μA
  - Sleep Mode 8 kByte RAM Retention and Wake−up Timer running 2.2 μA
  - Radio RX−mode
    6.5 mA @ 169 MHz
    9.5 mA @ 868 MHz and 433 MHz
  - Radio TX−mode at 868 MHz
    7.5 mA @ 0 dBm
    16 mA @ 10 dBm
    48 mA @ 16 dBm

AX8052

- Ultra−low Power MCU Core Compatible with Industry Standard 8052 Instruction Set
- Down to 500 nA Wake−up Current
- Single Cycle/Instruction for many Instructions
- 64 kByte In−system Programmable FLASH
- Code Protection Lock
- 8.25 kByte SRAM
- 3−wire (1 dedicated, 2 shared) In−circuit Debug Interface
- Three 16−bit Timers with ΣΔ Output Capability
- Two 16−bit Wakeup Timers
- Two Input Captures
- Two Output Compares with PWM Capability
- 10−bit 500 ksample/s Analog−to−Digital Converter
- Temperature Sensor
- Two Analog Comparators
- Two UARTs
- One General Purpose Master/Slave SPI
- Two Channel DMA Controller
- Multi−megabit/s AES Encryption/Decryption Engine, supports AES−128, AES−192 and AES−256 with True Random Number Generator (TRNG)
  NOTE: The AES Engine and the TRNG require Software Enabling and Support.
- Ultra−low Power 10 kHz/640 Hz Wakeup Oscillator, with Automatic Calibration against a Precise Clock
- Internal 20 MHz RC Oscillator, with Automatic Calibration against a Precise Clock for Flexible System Clocking
- Low Frequency Tuning Fork Crystal Oscillator for Accurate Low Power Time Keeping
- Brown−out and Power−on−Reset Detection

High Performance Narrow−band RF Transceiver compatible to AX5043 (FSK/MSK/4−FSK/GFSK/GMSK/ASK/AFSK/FM/PSK)

- Receiver
  - Carrier Frequencies from 27 to 1050 MHz
  - Data Rates from 0.1 kbps to 125 kbps
  - Optional Forward Error Correction (FEC)
  - Sensitivity without FEC
    −135 dBm @ 0.1 kbps, 868 MHz, FSK
    −126 dBm @ 1 kbps, 868 MHz, FSK
    −117 dBm @ 10 kbps, 868 MHz, FSK
    −107 dBm @ 100 kbps, 868 MHz, FSK
    −105 dBm @ 125 kbps, 868 MHz, FSK

    −138 dBm @ 0.1 kbps, 868 MHz, PSK
    −130 dBm @ 1 kbps, 868 MHz, PSK
    −120 dBm @ 10 kbps, 868 MHz, PSK
    −109 dBm @ 100 kbps, 868 MHz, PSK
    −108 dBm @ 125 kbps, 868 MHz, PSK

- Sensitivity with FEC
  −137 dBm @ 0.1 kbps, 868 MHz, FSK
  −122 dBm @ 5 kbps, 868 MHz, FSK
  −111 dBm @ 50 kbps, 868 MHz, FSK
- High Selectivity Receiver with up to 47 dB Adjacent Channel Rejection
- 0 dBm Maximum Input Power
- ±10% Data−rate Error Tolerance
- Support for Antenna Diversity with External Antenna Switch
- Short Preamble Modes allow the Receiver to work with as little as 16 Preamble Bits
- Fast State Switching Times
  200 μs TX → RX Switching Time
  62 μs RX → TX Switching Time

- Transmitter
  - Carrier Frequencies from 27 to 1050 MHz
  - Data−rates from 0.1 kbps to 125 kbps
  - High Efficiency, High Linearity Integrated Power Amplifier
  - Maximum Output Power
    16 dBm @ 868 MHz
    16 dBm @ 433 MHz
    16 dBm @ 169 MHz
  - Power Level programmable in 0.5 dB Steps
  - GFSK Shaping with BT=0.3 or BT=0.5
  - Unrestricted Power Ramp Shaping

- RF Frequency Generation
  - Configurable for Usage in 27 MHz −1050 MHz Bands
  - RF Carrier Frequency and FSK Deviation Programmable in 1 Hz Steps
  - Ultra Fast Settling RF Frequency Synthesizer for Low−power Consumption
  - Fully Integrated RF Frequency Synthesizer with VCO Auto−ranging and Band−width Boost Modes for Fast Locking
  - Configurable for either Fully Integrated VCO, Internal VCO with External Inductor or Fully External VCO
  - Configurable for either Fully Integrated or External Synthesizer Loop Filter for a Large Range of Bandwidths
  - Channel Hopping up to 2000 hops/s
  - Automatic Frequency Control (AFC)

- Flexible Antenna Interface
  - Integrated RX/TX Switching with Differential Antenna Pins
  - Mode with Differential RX Pins and Single−ended TX Pin for Usage with External PAs and for Maximum PA Efficiency at Low Output Power

- Wakeup−on−Radio
  - 640 Hz or 10 kHz Lowest Power Wake−up Timer
  - Wake−up Time Interval programmable between 98 μs and 102 s

- Sophisticated Radio Controller
  - Antenna Diversity and RX/TX Switch Control
  - Fully Automatic Packet Reception and Transmission without Micro−controller Intervention
  - Supports HDLC, Raw, Wireless M−Bus Frames and Arbitrary Defined Frames
  - Automatic Channel Noise Level Tracking
  - μs Resolution Timestamps for Exact Timing (eg. for Frequency Hopping Systems)
  - 256 Byte Micro−programmable FIFO, optionally supports Packet Sizes > 256 Bytes
  - Three Matching Units for Preamble Byte, Sync−word and Address
  - Ability to store RSSI, Frequency Offset and Data−rate Offset with the Packet Data
  - Multiple Receiver Parameter Sets allow the use of more aggressive Receiver Parameters during Preamble, dramatically shortening the Required Preamble Length at no Sensitivity Degradation

- Advanced Crystal Oscillator (RF Reference Oscillator)
  - Fast Start−up and Lowest Power Steady−state XTAL Oscillator for a Wide Range of Crystals
  - Integrated Tuning Capacitors
  - Possibility of Applying an External Clock Reference (TCXO)

Applications

27 – 1050 MHz Licensed and Unlicensed Radio Systems

- Internet of Things
- Automatic meter reading (AMR)
- Security applications
- Building automation
- Wireless networks
- Messaging Paging
- Compatible with: Wireless M−Bus, POCSAG, FLEX, KNX, Sigfox, Z−Wave, enocean
- Regulatory Regimes: EN 300 220 V2.3.1 including the Narrow−band 12.5 kHz, 20 kHz and 25 kHz Definitions; EN 300 422; FCC Part 15.247; FCC Part 15.249; FCC Part 90 6.25 kHz, 12.5 kHz and 25 kHz

BLOCK DIAGRAM

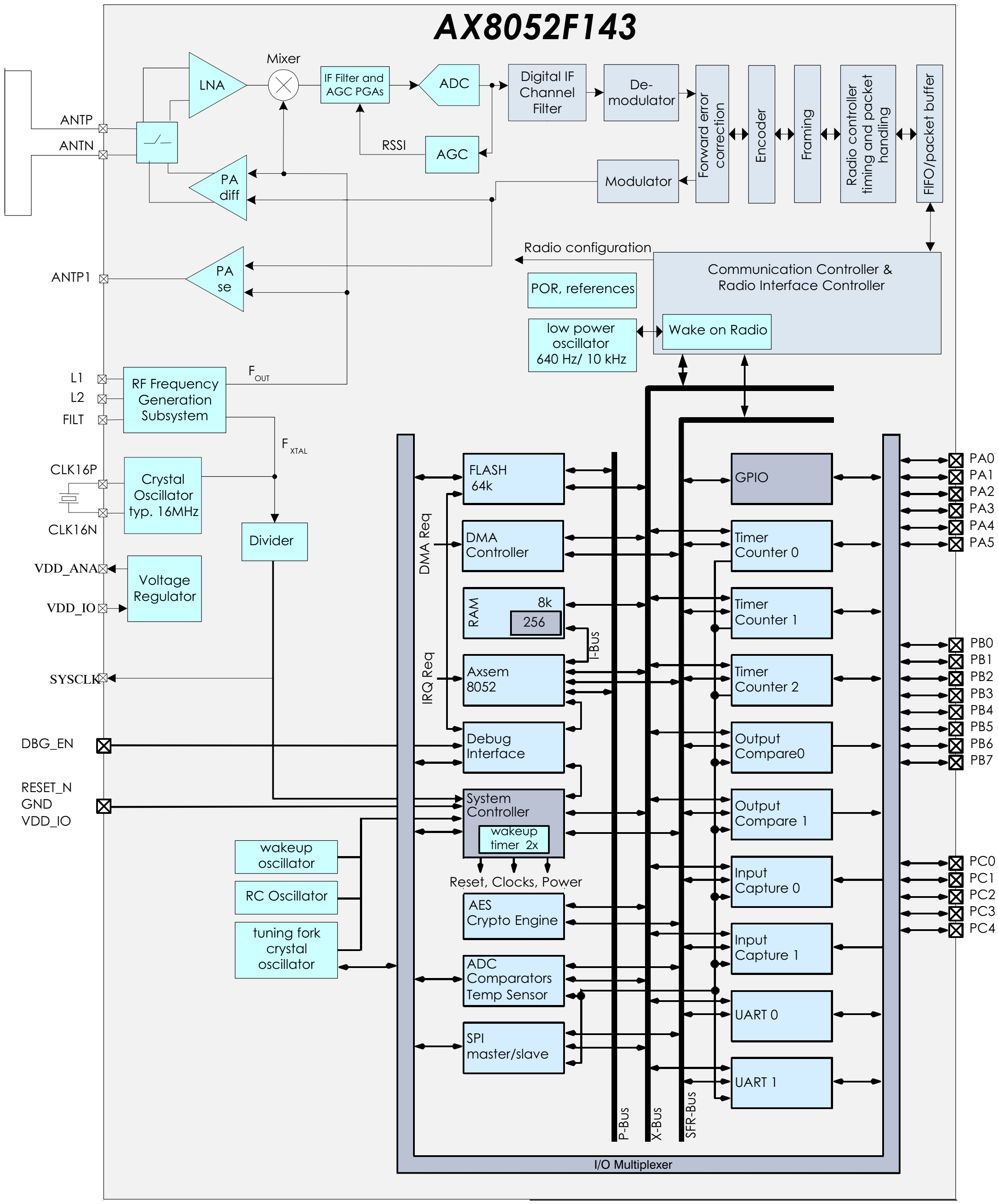

Figure 1. Functional Block Diagram of the AX8052F143

Table 1. PIN FUNCTION DESCRIPTIONS

Symbol	Pin(s)	Type	Description
VDD_ANA	1	P	Analog power output, decouple to neighboring GND
GND	2	P	Ground, decouple to neighboring VDD_ANA
ANTP	3	A	Differential antenna input/output
ANTN	4	A	Differential antenna input/output
ANTP1	5	A	Single−ended antenna output
GND	6	P	Ground, decouple to neighboring VDD_ANA
VDD_ANA	7	P	Analog power output, decouple to neighboring GND
GND	8	P	Ground
FILT	9	A	Optional synthesizer filter
L2	10	A	Optional synthesizer inductor
L1	11	A	Optional synthesizer inductor
SYSCLK	12	I/O/PU	System clock output
PC4	13	I/O/PU	General purpose IO
PC3	14	I/O/PU	General purpose IO
PC2	15	I/O/PU	General purpose IO
PC1	16	I/O/PU	General purpose IO
PC0	17	I/O/PU	General purpose IO
PB0	18	I/O/PU	General purpose IO
PB1	19	I/O/PU	General purpose IO
PB2	20	I/O/PU	General purpose IO
PB3	21	I/O/PU	General purpose IO
PB4	22	I/O/PU	General purpose IO
PB5	23	I/O/PU	General purpose IO
PB6	24	I/O/PU	General purpose IO, DBG_DATA
PB7	25	I/O/PU	General purpose IO, DBG_CLK
DBG_EN	26	I/PD	In−circuit debugger enable
RESET_N	27	I/PU	Optional reset pin. If this pin is not used it must be connected to VDD_IO
GND	28	P	Ground
VDD_IO	29	P	Unregulated power supply
PA0	30	I/O/A/PU	General purpose IO
PA1	31	I/O/A/PU	General purpose IO
PA2	32	I/O/A/PU	General purpose IO
PA3	33	I/O/A/PU	General purpose IO
PA4	34	I/O/A/PU	General purpose IO
PA5	35	I/O/A/PU	General purpose IO
VDD_IO	36	P	Unregulated power supply
TST1	37	A	Must be connected to GND
TST2	38	A	Must be connected to GND
CLK16N	39	A	Crystal oscillator input/output (RF reference oscillator)
CLK16P	40	A	Crystal oscillator input/output (RF reference oscillator)
GND	Center pad	P	Ground on center pad of QFN, must be connected

A = analog input
I = digital input signal
O = digital output signal
PU = pull−up
I/O = digital input/output signal
N = not to be connected
P = power or ground
PD = pull−down

All digital inputs are Schmitt trigger inputs, digital input and output levels are LVCMOS/LVTTL compatible. Port A Pins (PA0 − PA7) must not be driven above VDD_IO, all other digital inputs are 5 V tolerant. Pull−ups are programmable for all GPIO pins.

Alternate Pin Functions

GPIO Pins are shared with dedicated Input/Output signals of on−chip peripherals. The following table lists the available functions on each GPIO pin.

Table 2. ALTERNATE PIN FUNCTIONS

GPIO	Alternate Functions				
PA0	T0OUT	IC1	ADC0		
PA1	T0CLK	OC1	ADC1		
PA2	OC0	U1RX	ADC2	COMPI00	
PA3	T1OUT		ADC3	LPXTALP	
PA4	T1CLK	COMPO0	ADC4	LPXTALN	
PA5	IC0	U1TX	ADC5	COMPI10	
PB0	U1TX	IC1	EXTIRQ0		
PB1	U1RX	OC1			
PB2	IC0	T2OUT			PWRAMP
PB3	OC0	T2CLK	EXTIRQ1	DSWAKE	ANTSEL
PB4	U0TX	T1CLK			
PB5	U0RX	T1OUT			
PB6	DBG_DATA				
PB7	DBG_CLK				
PC0	SSEL	T0OUT	EXTIRQ0		
PC1	SSCK	T0CLK	COMPO1		
PC2	SMOSI	U0TX			
PC3	SMISO	U0RX	COMPO0		
PC4	COMPO1	ADCTRIG	EXTIRQ1		

Pinout Drawing

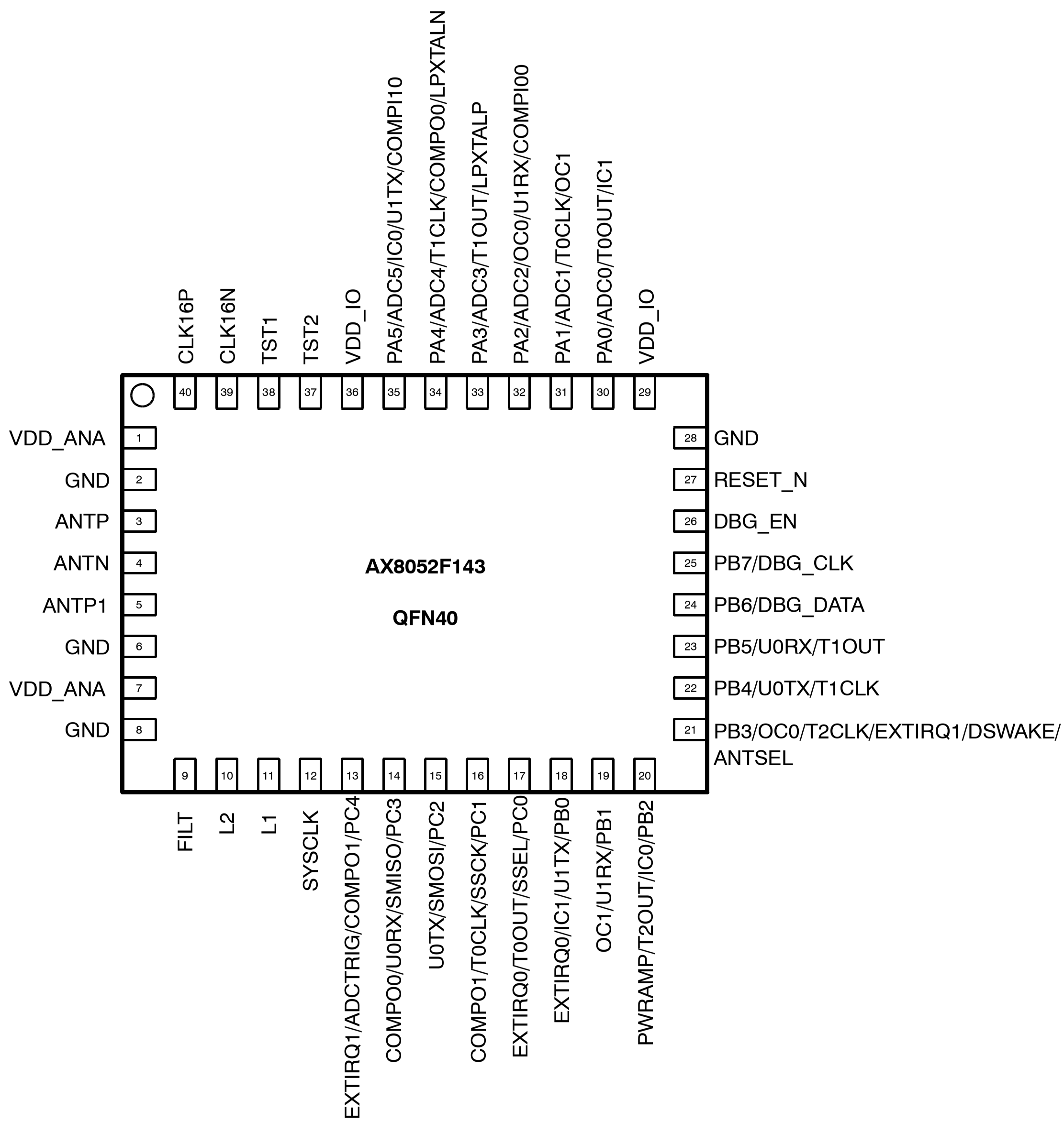

Figure 2. Pinout Drawing (Top View)

SPECIFICATIONS

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Condition	Min	Max	Units
VDD_IO	Supply voltage		–0.5	5.5	V
IDD	Supply current			200	mA
P_{tot}	Total power consumption			800	mW
P_i	Absolute maximum input power at receiver input	ANTP and ANTN pins in RX mode		10	dBm
I_{I1}	DC current into any pin except ANTP, ANTN, ANTP1		–10	10	mA
I_{I2}	DC current into pins ANTP, ANTN, ANTP1		–100	100	mA
I_O	Output Current			40	mA
V_{ia}	Input voltage ANTP, ANTN, ANTP1 pins		–0.5	5.5	V
	Input voltage digital pins		–0.5	5.5	V
V_{es}	Electrostatic handling	HBM	–2000	2000	V
T_{amb}	Operating temperature		–40	85	°C
T_{stg}	Storage temperature		–65	150	°C
T_j	Junction Temperature			150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Table 4. SUPPLIES

Sym	Description	Condition	Min	Typ	Max	Units
T_{AMB}	Operational ambient temperature		–40	27	85	°C
VDD_{IO}	I/O and voltage regulator supply voltage		1.8	3.0	3.6	V
VDD_{IO_R1}	I/O voltage ramp for reset activation; Note 1	Ramp starts at VDD_IO ≤ 0.1 V	0.1			V/ms
VDD_{IO_R2}	I/O voltage ramp for reset activation; Note 1	Ramp starts at 0.1 V < VDD_IO < 0.7 V	3.3			V/ms
V_{BOUT}	Brown–out threshold	Note 2		1.3		V
I_{DS}	Deep Sleep current			100		nA
I_{SL256P}	Sleep current, 256 Bytes RAM retained	Wakeup from dedicated pin		500		nA
I_{SL256}	Sleep current, 256 Bytes RAM retained	Wakeup Timer running at 640 Hz		900		nA
I_{SL4K}	Sleep current, 4.25 kBytes RAM retained	Wakeup Timer running at 640 Hz		1.5		μA
I_{SL8K}	Sleep current, 8.25 kBytes RAM retained	Wakeup Timer running at 640 Hz		2.2		μA
I_{RX}	Current consumption RX RF frequency generation subsystem: Internal VCO and internal loop–fiter	868 MHz, datarate 6 kbps		9.5		mA
		169 MHz, datarate 6 kbps		6.5		
		868 MHz, datarate 100 kbps		11		
		169 MHz, datarate 100 kbps		7.5		
$I_{TX-DIFF}$	Current consumption TX differential	868 MHz, 16 dBm, FSK, Note 3 RF frequency generation subsystem: Internal VCO and internal loop–filter Antenna configuration: Differential PA, internal RX/TX switch		48		mA

1. If VDD_IO ramps cannot be guaranteed, an external reset circuit is recommended, see the AX8052 Application Note: Power On Reset
2. Digital circuitry is functional down to typically 1 V.
3. Measured with optimized matching networks.

Table 4. SUPPLIES

Sym	Description	Condition	Min	Typ	Max	Units
I_{RX-SE}	Current consumption TX single ended	868 MHz, 0 dBm, FSK, Note 3 RF frequency generation subsystem: Internal VCO and internal loop−filter Antenna configuration: Single ended PA, external RX/TX switching		7.5		mA
I_{MCU}	Microcontroller running power consumption	All peripherals disabled		150		μA/ MHz
I_{VSUP}	Voltage supervisor	Run and standby mode		85		μA
I_{LPXTAL}	Crystal oscillator current (RF reference oscillator)	16 MHz		160		μA
I_{LFXTAL}	Low frequency crystal oscillator current	32 kHz		700		nA
I_{RCOSC}	Internal oscillator current	20 MHz		210		μA
I_{LPOSC}	Internal Low Power Oscillator current	10 kHz		650		nA
		640 Hz		210		nA
I_{ADC}	ADC current	311 kSample/s, DMA 5 MHz		1.1		mA
I_{WOR}	Typical wake−on−radio duty cycle current	1s, 100 kbps		6		μA

1. If VDD_IO ramps cannot be guaranteed, an external reset circuit is recommended, see the AX8052 Application Note: Power On Reset
2. Digital circuitry is functional down to typically 1 V.
3. Measured with optimized matching networks.

For information on current consumption in complex modes of operation tailored to your application, see the software AX−RadioLab.

Note on current consumption in TX mode

To achieve best output power the matching network has to be optimized for the desired output power and frequency. As a rule of thumb a good matching network produces about 50% efficiency with the AX8052F143 power amplifier although over 90% are theoretically possible. A typical matching network has between 1 dB and 2 dB loss (P_{loss}). The theoretical efficiencies are the same for the single ended PA (ANTP1) and differential PA (ANTP and ANTN) therefore only one current value is shown in the table below. We recommend to use the single ended PA for low output power and the differential PA for high power. The differential PA is internally multiplexed with the LNA on pins ANTP and ANTN. Therefore constraints for the RX matching have to be considered for the differential PA matching.

The current consumption can be calculated as

$$I_{TX}[mA] = \frac{1}{PA_{efficiency}} \times 10^{\frac{P_{out}[dBm] + P_{loss}[dB]}{10}} \div 1.8V + I_{offset}$$

I_{offset} is about 6 mA for the fully integrated VCO at 400 MHz to 1050 MHz, and 3 mA for the VCO with external inductor at 169 MHz. The following table shows calculated current consumptions versus output power for P_{loss} = 1 dB, $PA_{efficiency}$ = 0.5, I_{offset}= 6 mA at 868 MHz and I_{offset}= 3.5 mA at 169 MHz.

Table 5. CURRENT CONSUMPTION VS. OUTPUT POWER

Pout [dBm]	I_{txcalc} [mA]	
	868 MHz	169 MHz
0	7.5	4.5
1	7.9	4.9
2	8.4	5.4
3	9.0	6.0
4	9.8	6.8
5	10.8	7.8
6	12.1	9.1
7	13.7	10.7
8	15.7	12.7
9	18.2	15.2
10	21.3	18.3
11	25.3	22.3
12	30.3	27.3
13	36.7	33.7
14	44.6	41.6
15	54.6	51.6

Both AX8052F143 power amplifiers run from the regulated VDD_ANA supply and not directly from the battery. This has the advantage that the current and output power do not vary much over supply voltage and temperature.

Table 6. LOGIC

Symbol	Description	Condition	Min	Typ	Max	Units
Digital Inputs						
V_{T+}	Schmitt trigger low to high threshold point	VDD_IO = 3.3 V		1.55		V
V_{T-}	Schmitt trigger high to low threshold point			1.25		V
V_{IL}	Input voltage, low				0.8	V
V_{IH}	Input voltage, high		2.0			V
V_{IPA}	Input voltage range, Port A		−0.5		VDD_IO	V
V_{IPBC}	Input voltage range, Ports B, C		−0.5		5.5	V
I_L	Input leakage current		−10		10	μA
R_{PU}	Programmable Pull−Up Resistance			65		kΩ
Digital Outputs						
I_{OH}	Output Current, high Ports PA, PB and PC	V_{OH} = 2.4 V	8			mA
I_{OL}	Output Current, low Ports PA, PB and PC	V_{OL} = 0.4 V	8			mA
I_{OH}	Output Current, high Pin SYSCLK	V_{OH} = 2.4 V	4			mA
I_{OL}	Output Current, low Pin SYSCLK	V_{OL} = 0.4 V	4			mA
I_{OZ}	Tri−state output leakage current		−10		10	μA

AC Characteristics

Table 7. CRYSTAL OSCILLATOR (RF REFERENCE OSCILLATOR)

Symbol	Description	Condition	Min	Typ	Max	Units
f_{XTAL}	Crystal or frequency	Note 1, 2, 3	10	16	50	MHz
gm_{osc}	Oscillator transconductance range	Self−regulated see note 4	0.2		20	mS
C_{osc}	Programmable tuning capacitors at pins CLK16N and CLK16P	AX5043_XTALCAP = 0x00 default		3		pF
		AX5043_XTALCAP = 0x01		8.5		pF
		AX5043_XTALCAP = 0xFF		40		pF
$C_{osc-lsb}$	Programmable tuning capacitors, increment per LSB of AX5043_XTALCAP	AX5043_XTALCAP = 0x01 – 0xFF		0.5		pF
f_{ext}	External clock input (TCXO)	Note 2, 3, 5	10	16	50	MHz
RIN_{osc}	Input DC impedance		10			kΩ
$NDIV_{SYSCLK}$	Divider ratio $f_{SYSCLK} = F_{XTAL} / NDIV_{SYSCLK}$		2^0	2^4	2^{10}	

1. Tolerances and start−up times depend on the crystal used. Depending on the RF frequency and channel spacing the IC must be calibrated to the exact crystal frequency using the readings of the register AX5043_TRKFREQ.
2. The choice of crystal oscillator or TCXO frequency depends on the targeted regulatory regime for TX, see separate documentation on meeting regulatory requirements.
3. To avoid spurious emission, the crystal or TCXO reference frequency should be chosen so that the RF carrier frequency is not an integer multiple of the crystal or TCXO frequency.
4. The oscillator transconductance is regulated for fastest start−up time during start−up and for lowest power curing steady state oscillation. This means that values depend on the crystal used.
5. If an external clock or TCXO is used, it should be input via an AC coupling at pin CLK16P with the oscillator powered up and AX5043_XTALCAP = 000000. For detailed TCXO network recommendations depending on the TCXO output swing refer to the AX5043 Application Note: Use with a TCXO Reference Clock.

Table 8. LOW−POWER OSCILLATOR (TRANSCEIVER WAKE ON RADIO CLOCK)

Symbol	Description	Condition	Min	Typ	Max	Units
$f_{osc-slow}$	Oscillator frequency slow mode LPOSC FAST = 0 in AX5043_LPOSCCONFIG register	No calibration	480	640	800	Hz
		Internal calibration vs. crystal clock has been performed	630	640	650	
$f_{osc-fast}$	Oscillator frequency fast mode LPOSC FAST = 1 in AX5043_LPOSCCONFIG register	No calibration	7.6	10.2	12.8	kHz
		Internal calibration vs. crystal clock has been performed	9.8	10.2	10.8	

Table 9. RF FREQUENCY GENERATION SUBSYSTEM (SYNTHESIZER)

Symbol	Description	Condition	Min	Typ	Max	Units
f_{REF}	Reference frequency	The reference frequency must be chosen so that the RF carrier frequency is not an integer multiple of the reference frequency	10	16	50	MHz
Dividers						
$NDIV_{ref}$	Reference divider ratio range	Controlled directly with bits REFDIV in register AX5043_PLLVCODIV	2^0		2^3	
$NDIV_m$	Main divider ratio range	Controlled indirectly with register AX5043_FREQ	4.5		66.5	
$NDIV_{RF}$	RF divider range	Controlled directly with bit RFDIV in register AX5043_ PLLVCODIV	1		2	
Charge Pump						
I_{CP}	Charge pump current	Programmable in increments of 8.5 μA via register AX5043_PLLCPI	8.5		2168	μA
Internal VCO (VCOSEL = 0)						
f_{RF}	RF frequency range	RFDIV = 1	400		525	MHz
		RFDIV = 0	800		1050	
f_{step}	RF frequency step	RFDIV = 1 f_{REF} = 16.000000 MHz		0.98		Hz
BW	Synthesizer loop bandwidth	The synthesizer loop bandwidth an start−up time can be programmed with the registers AX5043_PLLLOOP and AX5043_PLLCPI. For recommendations see the AX5043 Programming Manual, the AX−RadioLab software and AX5043 Application Notes on compliance with regulatory regimes.	50		500	kHz
T_{start}	Synthesizer start−up time if crystal oscillator and reference are running		5		25	μs
PN868	Synthesizer phase noise 868 MHz f_{REF} = 48 MHz	10 kHz from carrier		−95		dBc/Hz
		1 MHz from carrier		−120		
PN433	Synthesizer phase noise 433 MHz f_{REF} = 48 MHz	10 kHz from carrier		−105		dBc/Hz
		1 MHz from carrier		−120		
VCO with external inductors (VCOSEL = 1, VCO2INT = 1)						
f_{RFrng_lo}	RF frequency range For choice of L_{ext} values as well as VCO gains see Figure 3 and Figure 4	RFDIV = 1	27		262	MHz
f_{RFrng_hi}		RFDIV = 0	54		525	
PN169	Synthesizer phase noise 169 MHz L_{ext}=47 nH (wire wound 0603) AX5043_RFDIV = 0, f_{REF}= 16 MHz Note: phase noises can be improved with higher f_{REF}	10 kHz from carrier		−97		dBc/Hz
		1 MHz from carrier		−115		

Table 9. RF FREQUENCY GENERATION SUBSYSTEM (SYNTHESIZER)

Symbol	Description	Condition	Min	Typ	Max	Units
External VCO (VCOSEL = 1, VCO2INT = 0)						
f_{RF}	RF frequency range fully external VCO	Note: The external VCO frequency needs to be 2 x f_{RF}	27		1000	MHz
V_{amp}	Differential input amplitude at L1, L2 terminals			0.7		V
V_{inL}	Input voltage levels at L1, L2 terminals		0		1.8	V
V_{ctrl}	Control voltage range	Available at FILT in external loop filter mode	0		1.8	V

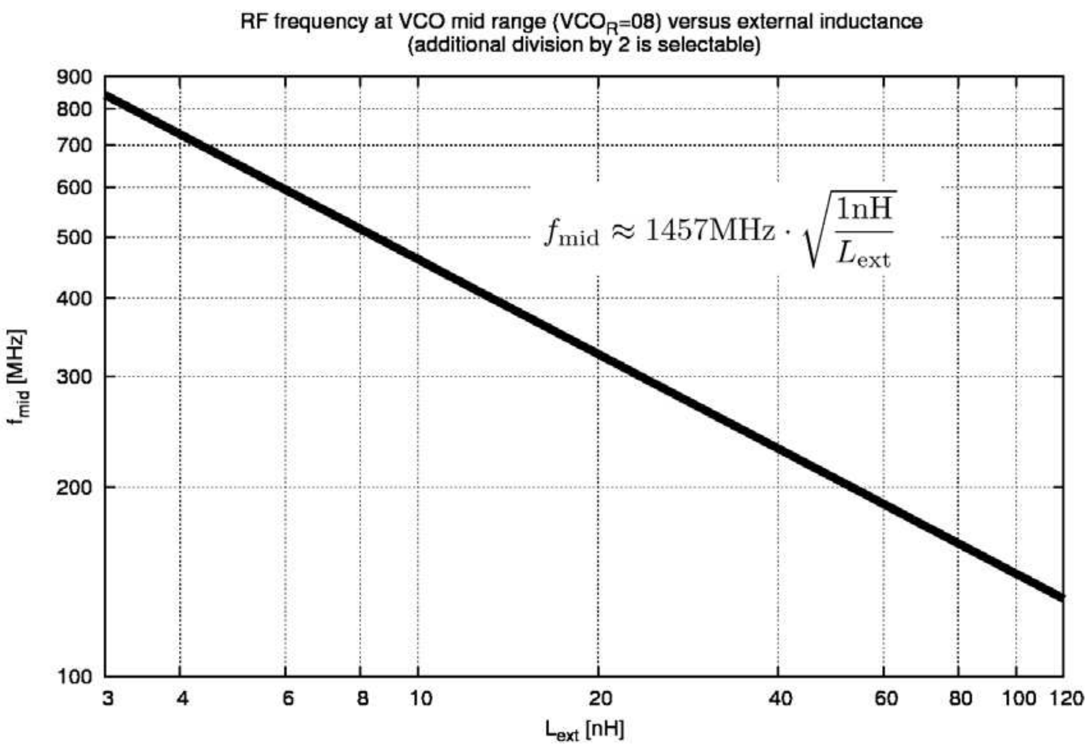

Figure 3. VCO with External Inductors: Typical Frequency vs. L_{ext}

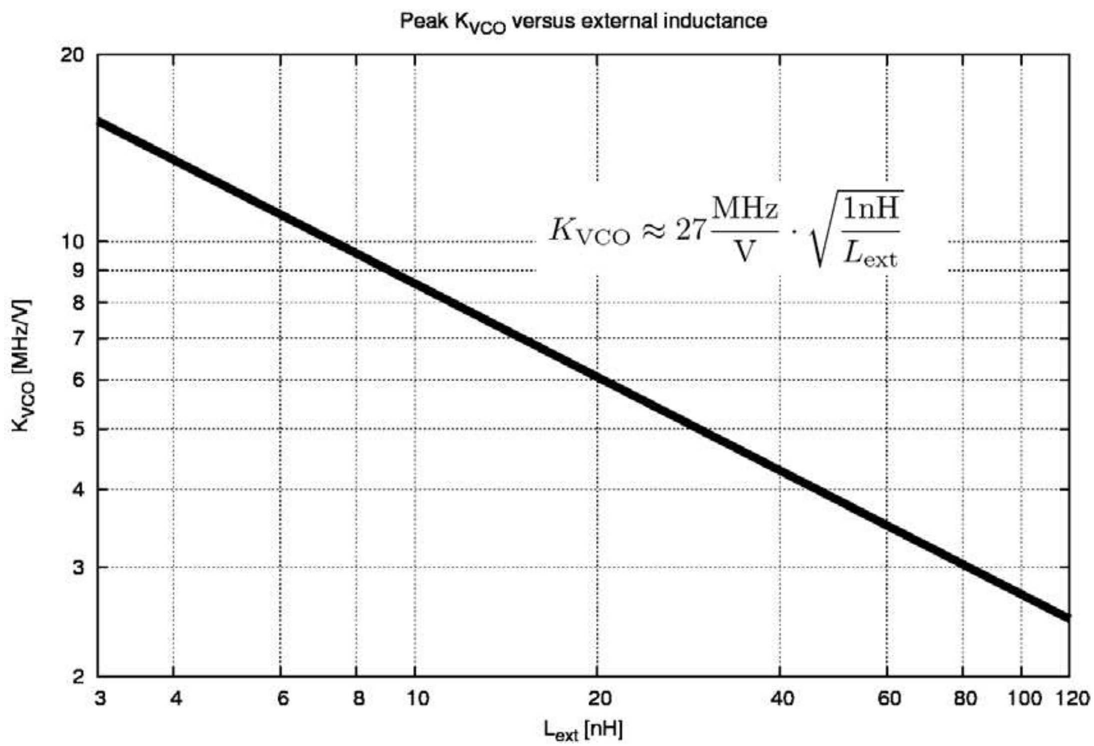

Figure 4. VCO with External Inductors: Typical K_{VCO} vs. L_{ext}

The following table shows the typical frequency ranges for frequency synthesis with external VCO inductor for different inductor values.

Table 10.

Lext [nH]	Freq [MHz] RFDIV = 0	Freq [MHz] RFDIV = 1	PLL Range
8.2	482	241	0
8.2	437	219	15
10	432	216	0
10	390	195	15
12	415	208	0
12	377	189	15
15	380	190	0
15	345	173	15
18	345	173	0
18	313	157	15
22	308	154	0
22	280	140	14
27	285	143	0
27	258	129	15
33	260	130	0
33	235	118	15
39	245	123	0
39	223	112	14
47	212	106	0
47	194	97	14
56	201	101	0
56	182	91	15
68	178	89	0
68	161	81	15
82	160	80	1
82	146	73	14
100	149	75	1
100	136	68	14
120	136	68	0
120	124	62	14

For tuning or changing of ranges a capacitor can be added in parallel to the inductor.

Table 11. TRANSMITTER

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate		0.1		125	kbps
PTX	Transmitter power @ 868 MHz	Differential PA, 50 Ω single ended measurement at an SMA connector behind the matching network, Note 2	−10		16	dBm
	Transmitter power @ 433 MHz		−10		16	
	Transmitter power @ 169 MHz		−10		16	
PTX_{step}	Programming step size output power	Note 1			0.5	dB
dTX_{temp}	Transmitter power variation vs. temperature	−40°C to +85°C Note 2		± 0.5		dB
dTX_{Vdd}	Transmitter power variation vs. VDD_IO	1.8 to 3.6 V Note 2		± 0.5		dB
Padj	Adjacent channel power GFSK BT = 0.5, 500 Hz deviation, 1.2 kbps, 25 kHz channel spacing, 10 kHz channel BW	868 MHz		−44		dBc
		433 MHz		−51		
$PTX_{868-harm2}$	Emission @ 2nd harmonic	868 MHz, Note 2		−40		dBc
$PTX_{868-harm3}$	Emission @ 3rd harmonic			−60		
$PTX_{433-harm2}$	Emission @ 2nd harmonic	433 MHz, Note 2		−40		dBc
$PTX_{433-harm3}$	Emission @ 3rd harmonic			−40		

1. $P_{out} = \frac{\text{AX5043\_TXPWRCOEFFB}}{2^{12}-1} \times P_{max}$
2. 50 Ω single ended measurements at an SMA connector behind the matching network. For recommended matching networks see Applications section.

Table 12. RECEIVER SENSITIVITIES

The table lists typical input sensitivities (without FEC) in dBm at the SMA connector with the complete matching network for BER=10^{-3} at 433 or 868 MHz.

Data rate [kbps]		FSK h = 0.66	FSK h = 1	FSK h = 2	FSK h = 4	FSK h = 5	FSK h = 8	FSK h = 16	PSK
0.1	Sensitivity [dBm]	−135	−134.5	−132.5	−133	−133.5	−133	−132.5	−138
	RX Bandwidth [kHz]	0.2	0.2	0.3	0.5	0.6	0.9	2.1	0.2
	Deviation [kHz]	0.033	0.05	0.1	0.2	0.25	0.4	0.8	
1	Sensitivity [dBm]	−126	−125	−123	−123.5	−124	−123.5	−122.5	−130
	RX Bandwidth [kHz]	1.5	2	3	6	7	11	21	1
	Deviation [kHz]	0.33	0.5	1	2	2.5	4	8	
10	Sensitivity [dBm]	−117	−116	−113	−114	−113.5	−113		−120
	RX Bandwidth [kHz]	15	20	30	50	60	110		10
	Deviation [kHz]	3.3	5	10	20	25	40		
100	Sensitivity [dBm]	−107	−105.5						−109
	RX Bandwidth [kHz]	150	200						100
	Deviation [kHz]	33	50						
125	Sensitivity [dBm]	−105	−104						−108
	RX Bandwidth [kHz]	187.5	200						125
	Deviation [kHz]	42.3	62.5						

1. Sensitivities are equivalent for 1010 data streams and PN9 whitened data streams.
2. RX bandwidths < 0.9 kHz cannot be achieved with an 48 MHz TCXO. A 16 MHz TCXO was used for all measurements at 0.1 kbps.

Table 13. RECEIVER

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate		0.1		125	kbps
IS_{BER868}	Input sensitivity at BER = 10^{-3} for 868 MHz operation, continuous data, without FEC	FSK, h = 0.5, 100 kbps		−106		dBm
		FSK, h = 0.5, 10 kbps		−116		
		FSK, 500 Hz deviation, 1.2 kbps		−126		
		PSK, 100 kbps		−109		
		PSK, 10 kbps		−120		
		PSK, 1 kbps		−130		
$IS_{BER868FEC}$	Input sensitivity at BER = 10^{-3}, for 868 MHz operation, continuous data, with FEC	FSK, h = 0.5, 50 kbps		−111		dBm
		FSK, h = 0.5, 5 kbps		−122		
		FSK, 0.1 kbps		−137		
IS_{PER868}	Input sensitivity at PER = 1%, for 868 MHz operation, 144 bit packet data, without FEC	FSK, h = 0.5, 100 kbps		−103		dBm
		FSK, h = 0.5, 10 kbps		−115		
		FSK, 500 Hz deviation, 1.2 kbps		−125		
IS_{WOR868}	Input sensitivity at PER = 1% for 868 MHz operation, WOR−mode, without FEC	FSK, h= 0.5, 100 kpbs		−102		dBm
IL	Maximum input level	Full selectivity		0		dBm
		FSK, reduced selectivity		10		
CP_{1dB}	Input referred compression point	2 tones separated by 100 kHz		−35		dBm
RSSIR	RSSI control range	FSK, 500 Hz deviation, 1.2 kbps	−126		−46	dB
$RSSIS_1$	RSSI step size	Before digital channel filter; calculated from register AX5043_AGCCOUNTER		0.625		dB
$RSSIS_2$	RSSI step size	Behind digital channel filter; calculated from registers AX5043_AGCCOUNTER, AX5043_TRKAMPL		0.1		dB
$RSSIS_3$	RSSI step size	Behind digital channel filter; reading register AX5043_RSSI		1		dB
SEL_{868}	Adjacent channel suppression	25 kHz channels , Note 1		45		dB
		100 kHz channels, Note 1		47		
BLK_{868}	Blocking at ± 10 MHz offset	Note 2		78		dB
R_{AFC}	AFC pull−in range	The AFC pull−in range can be programmed with the AX5043_MAXRFOFFSET registers. The AFC response time can be programmed with the AX5043_FREQGAIND register.	± 15			%
R_{DROFF}	Bitrate offset pull−in range	The bitrate pull−in range can be programmed with the AX5043_MAXDROFFSET registers.	± 10			%

1. Interferer/Channel @ BER = 10^{-3}, channel level is +3 dB above the typical sensitivity, the interfering signal is CW; channel signal is modulated with shaping
2. Channel/Blocker @ BER = 10^{-3}, channel level is +3 dB above the typical sensitivity, the blocker signal is CW; channel signal is modulated with shaping

Table 14. RECEIVER AND TRANSMITTER SETTLING PHASES

Symbol	Description	Condition	Min	Typ	Max	Units
T_{xtal}	XTAL settling time	Powermodes: POWERDOWN to STANDBY Note that T_{xtal} depends on the specific crystal used.		0.5		ms
T_{synth}	Synthesizer settling time	Powermodes: STANDBY to SYNTHTX or SYNTHRX		40		μs
T_{tx}	TX settling time	Powermodes: SYNTHTX to FULLTX T_{tx} is the time used for power ramping, this can be programmed to be 1 x t_{bit}, 2 x t_{bit}, 4 x t_{bit} or 8 x t_{bit}. Note 1	0	1 x t_{bit}	8 x t_{bit}	μs
T_{rx_init}	RX initialization time			150		μs
T_{rx_rssi}	RX RSSI acquisition time (after T_{rx_init})	Powermodes: SYNTHRX to FULLRX Modulation (G)FSK Note 1		80 + 3 x t_{bit}		μs
$T_{rx\_preamble}$	RX signal acquisition time to valid data RX at full sensitivity/selectivity (after T_{rx_init})			9 x t_{bit}		

1. t_{bit} depends on the datarate, e.g. for 10 kbps t_{bit} = 100 μs

Table 15. OVERALL STATE TRANSITION TIMES

Symbol	Description	Condition	Min	Typ	Max	Units
T_{tx_on}	TX startup time	Powermodes: STANDBY to FULLTX Note 1	40	40 + 1 x t_{bit}		μs
T_{rx_on}	RX startup time	Powermodes: STANDBY to FULLRX		190		μs
T_{rx_rssi}	RX startup time to valid RSSI	Powermodes: STANDBY to FULLRX Modulation (G)FSK Note 1		270 + 3 x t_{bit}		μs
T_{rx_data}	RX startup time to valid data at full sensitivity/selectivity			190 + 9 x t_{bit}		μs
T_{rxtx}	RX to TX switching	Powermodes: FULLRX to FULLTX		62		μs
T_{txrx}	TX to RX switching (to preamble start)	Powermodes: FULLTX to FULLRX		200		
T_{hop}	Frequency hop	Switch between frequency defined in register AX5043_FREQA and AX5043_FREQB		30		μs

1. t_{bit} depends on the datarate, e.g. for 10 kbps t_{bit} = 100 μs

Table 16. LOW FREQUENCY CRYSTAL OSCILLATOR

Symbol	Description	Condition	Min	Typ	Max	Units
f_{LPXTAL}	Crystal frequency			32	150	kHz
gm_{lpxosc}	Transconductance oscillator	LPXOSCGM = 00110		3.5		μs
		LPXOSCGM = 01000		4.6		
		LPXOSCGM = 01100		6.9		
		LPXOSCGM = 10000		9.1		
RIN_{lpxosc}	Input DC impedance		10			MΩ

Table 17. INTERNAL LOW POWER OSCILLATOR

Symbol	Description	Condition	Min	Typ	Max	Units
f_{LPOSC}	Oscillation Frequency	LPOSCFAST = 0 Factory calibration applied. Over the full temperature and voltage range	630	640	650	Hz
		LPOSCFAST = 1 Factory calibration applied Over the full temperature and voltage range	10.08	10.24	10.39	kHz

Table 18. INTERNAL RC OSCILLATOR

Symbol	Description	Condition	Min	Typ	Max	Units
$f_{LFRCPOSC}$	Oscillation Frequency	Factory calibration applied. Over the full temperature and voltage range	19.8	20	20.2	MHz

Table 19. MICROCONTROLLER

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{SYSCLKL}$	SYSCLK Low		27			ns
$T_{SYSCLKH}$	SYSCLK High		21			ns
$T_{SYSCLKP}$	SYSCLK Period		47			ns
T_{FLWR}	FLASH Write Time	2 Bytes		20		μs
T_{FLPE}	FLASH Page Erase	1 kBytes		2		ms
T_{FLE}	FLASH Secure Erase	64 kBytes		10		ms
T_{FLEND}	FLASH Endurance: Erase Cycles		10 000	100 000		Cycles
$T_{FLRETroom}$	FLASH Data Retention	25°C See Figure 5 for the lower limit set by the memory qualification	100			Years
$T_{FLREThot}$		85°C See Figure 5 for the lower limit set by the memory qualification	10			

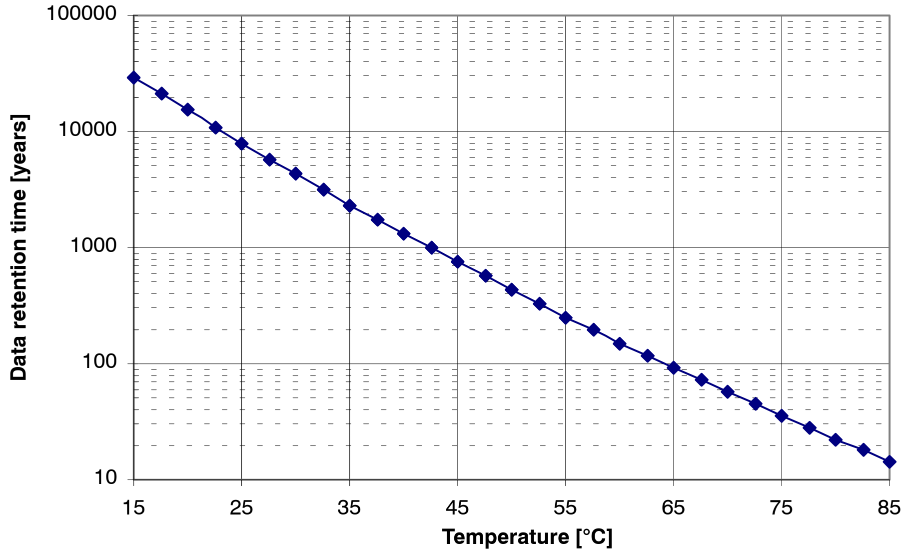

Figure 5. FLASH Memory Qualification Limit for Data Retention after 10k Erase Cycles

Table 20. ADC / COMPARATOR / TEMPERATURE SENSOR

Symbol	Description	Condition	Min	Typ	Max	Units
ADCSR	ADC sampling rate GPADC mode		30		500	kHz
ADCSR_T	ADC sampling rate temperature sensor mode		10	15.6	30	kHz
ADCRES	ADC resolution			10		Bits
V_{ADCREF}	ADC reference voltage & comparator internal reference voltage		0.95	1	1.05	V
Z_{ADC00}	Input capacitance				2.5	pF
DNL	Differential nonlinearity			± 1		LSB
INL	Integral nonlinearity			± 1		LSB
OFF	Offset			3		LSB
GAIN_ERR	Gain error			0.8		%
ADC in Differential Mode						
V_{ABS_DIFF}	Absolute voltages & common mode voltage in differential mode at each input		0		VDD_IO	V
V_{FS_DIFF01}	Full swing input for differential signals	Gain x1	−500		500	mV
V_{FS_DIFF10}		Gain x10	−50		50	mV
ADC in Single Ended Mode						
V_{MID_SE}	Mid code input voltage in single ended mode			0.5		V
V_{IN_SE00}	Input voltage in single ended mode		0		VDD_IO	V
V_{FS_SE01}	Full swing input for single ended signals	Gain x1	0		1	V
Comparators						
V_{COMP_ABS}	Comparator absolute input voltage		0		VDD_IO	V
V_{COMP_COM}	Comparator input common mode		0		VDD_IO − 0.8	V
$V_{COMPOFF}$	Comparator input offset voltage				20	mV
Temperature Sensor						
T_{RNG}	Temperature range		−40		85	°C
T_{RES}	Temperature resolution			0.1607		°C/LSB
T_{ERR_CAL}	Temperature error	Factory calibration applied	−2		2	°C

CIRCUIT DESCRIPTION

The AX8052F143 is a true single chip narrow−band, ultra−low power RF−microcontroller SoC for use in licensed and unlicensed bands ranging from 70 MHz to 1050 MHz. The on−chip transceiver consists of a fully integrated RF front−end with modulator and demodulator. Base band data processing is implemented in an advanced and flexible communication controller that enables user friendly communication.

The AX8052F143 contains a high speed microcontroller compatible to the industry standard 8052 instruction set. It contains 64 kBytes of FLASH and 8.25 kBytes of internal SRAM.

The AX8052F143 features 3 16−bit general purpose timers with ΣΔ capability, 2 output compare units for generating PWM signals, 2 input compare units to record timings of external signals, 2 16−bit wakeup timers, a watchdog timer, 2 UARTs, a Master/Slave SPI controller, a 10−bit 500 kSample/s A/D converter, 2 analog comparators, a temperature sensor, a 2 channel DMA controller, and a dedicated AES crypto controller. Debugging is aided by a dedicated hardware debug interface controller that connects using a 3−wire protocol (1 dedicated wire, 2 shared with GPIO) to the PC hosting the debug software.

While the radio carrier/LO synthesizer can only be clocked by the crystal oscillator (carrier stability requirements dictate a high stability reference clock in the MHz range), the microcontroller and its peripherals provide extremely flexible clocking options. The system clock that clocks the microcontroller, as well as peripheral clocks, can be selected from one of the following clock sources: the crystal oscillator, an internal high speed 20MHz oscillator, an internal low speed 640 Hz/10 kHz oscillator, or the low frequency crystal oscillator. Prescalers offer additional flexibility with their programmable divide by a power of two capability. To improve the accuracy of the internal oscillators, both oscillators may be slaved to the crystal oscillator.

AX8052F143 can be operated from a 1.8 V to 3.6 V power supply over a temperature range of –40°C to 85°C, it consumes 4 – 51 mA for transmitting, depending on the output power, 6.8 – 11 mA for receiving.

The AX8052F143 features make it an ideal interface for integration into various battery powered solutions such as ticketing or as transceiver for telemetric applications e.g. in sensors. As primary application, the transceiver is intended for UHF radio equipment in accordance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220−1 and the US Federal Communications Commission (FCC) standard Title 47 CFR part 15 as well as Part 90. Additionally AX8052F143 is suited for systems targeting compliance with Wireless M−Bus standard EN 13757−4:2005. Wireless M−Bus frame support (S, T, R) is built−in.

The AX8052F143 sends and receives data in frames. This standard operation mode is called Frame Mode. Pre and post ambles as well as checksums can be generated automatically.

AX8052F143 supports any data rate from 0.1 kbps to 125 kbps for FSK, MSK, 4−FSK, GFSK, GMSK and ASK modulations. To achieve optimum performance for specific data rates and modulation schemes several register settings to configure the AX8052F143 are necessary, they are outlined in the following, for details see the AXSEM RadioLab software which calculates the necessary register settings and the AX5043 Programming Manual.

The receiver supports multi−channel operation for all data rates and modulation schemes.

Microcontroller

The AX8052 microcontroller core executes the industry standard 8052 instruction set. Unlike the original 8052, many instructions are executed in a single cycle. The system clock and thus the instruction rate can be programmed freely from DC to 20 MHz.

Memory Architecture

The AX8052F143 Microcontroller features the highest bandwidth memory architecture of its class. Figure 6 shows the memory architecture. Three bus masters may initiate bus cycles:

- The AX8052 Microcontroller Core
- The Direct Memory Access (DMA) Engine
- The Advanced Encryption Standard (AES) Engine

Bus targets include:

- Two individual 4 kBytes RAM blocks located in X address space, which can be simultaneously accessed and individually shut down or retained during sleep mode
- A 256 Byte RAM located in internal address space, which is always retained during sleep mode
- A 64 kBytes FLASH memory located in code space.
- Special Function Registers (SFR) located in internal address space accessible using direct address mode instructions
- Additional Registers located in X address space (X Registers)

The upper half of the FLASH memory may also be accessed through the X address space. This simplifies and makes the software more efficient by reducing the need for generic pointers.

NOTE: Generic pointers include, in addition to the address, an address space tag.

SFR Registers are also accessible through X address space, enabling indirect access to SFR registers. This allows driver code for multiple identical peripherals (such as UARTs or Timers) to be shared.

The 4 word × 16 bit fully associative cache and a pre−fetch controller hide the latency of the FLASH.

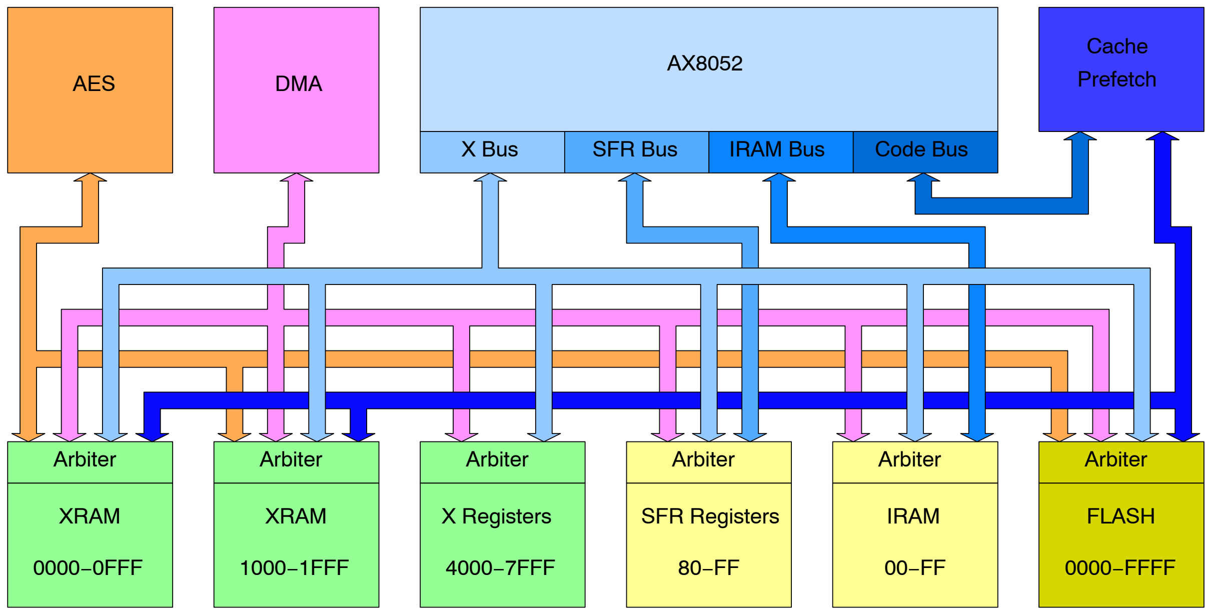

Figure 6. AX8052 Memory Architecture

The AX8052 Memory Architecture is fully parallel. All bus masters may simultaneously access different bus targets during each system clock cycle. Each bus target includes an arbiter that resolves access conflicts. Each arbiter ensures that no bus master can be starved.

Both 4 kBytes RAM blocks may be individually retained or switched off during sleep mode. The 256 Byte RAM is always retained during sleep mode.

The AES engine accesses memory 16 bits at a time. It is therefore slightly faster to align its buffers on even addresses.

Memory Map

The AX8052, like the other industry standard 8052 compatible microcontrollers, uses a Harvard architecture. Multiple address spaces are used to access code and data. Figure 7 shows the AX8052 memory map.

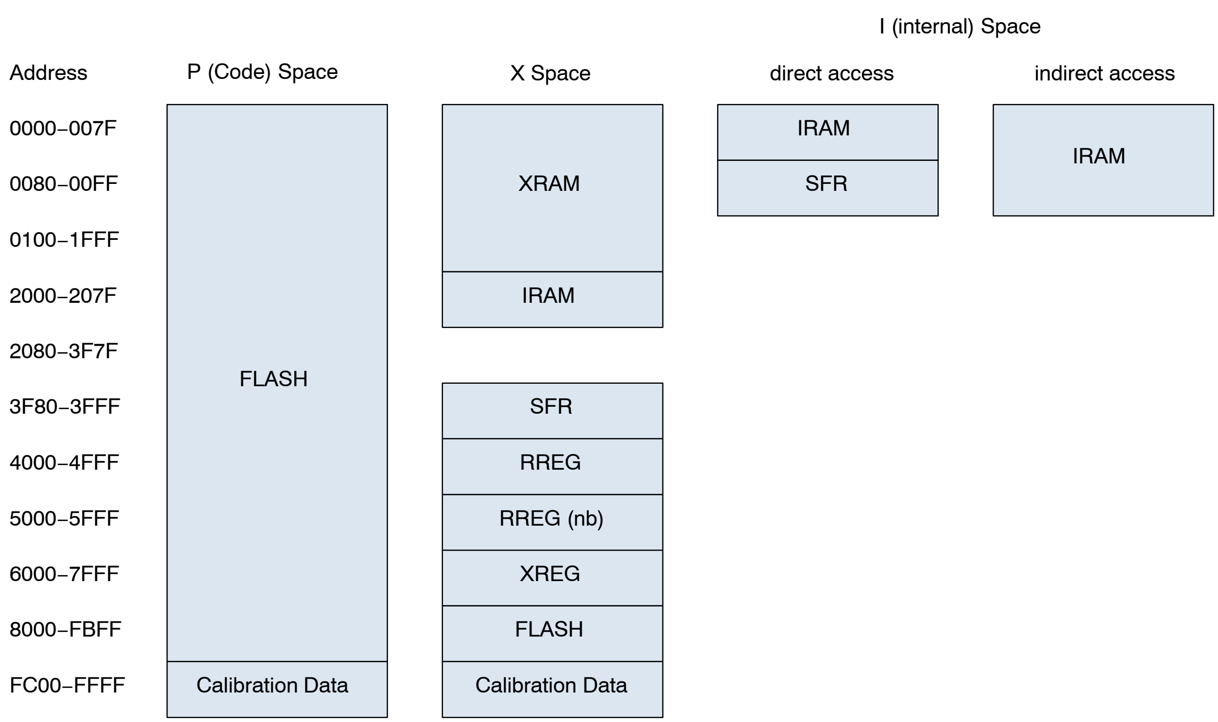

Figure 7. AX8052 Memory Architecture

The AX8052 uses P or Code Space to access its program. Code space may also be read using the MOVC instruction.

Smaller amounts of data can be placed in the Internal (see Note) or Data Space. A distinction is made in the upper half of the Data Space between direct accesses (MOV reg,addr; MOV addr,reg) and indirect accesses (MOV reg,@Ri; MOV @Ri,reg; PUSH; POP); Direct accesses are routed to the Special Function Registers, while indirect accesses are routed to the internal RAM.

NOTE: The origin of Internal versus External (X) Space is historical. External Space used to be outside of the chip on the original 8052 Microcontrollers.

Large amounts of data can be placed in the External or X Space. It can be accessed using the MOVX instructions. Special Function Registers, as well as additional Microcontroller Registers (XREG) and the Radio Registers (RREG) are also mapped into the X Space.

Detailed documentation of the Special Function Registers (SFR) and additional Microcontroller Registers can be found in the AX8052 Programming Manual.

The Radio Registers are documented in the AX5043 Programming Manual. Register Addresses given in the AX5043 Programming Manual are relative to the beginning of RREG, i.e. 0x4000 must be added to these addresses. It is recommended that the AXSEM provided ax8052f143.h header file is used; Radio Registers are prefixed with AX5043_ in the ax8052f143.h header file to avoid clashes of same−name Radio Registers with AX8052 registers.

Normally, accessing Radio Registers through the RREG address range is adequate. Since Radio Register accesses have a higher latency than other AX8052 registers, the AX8052 provides a method for non−blocking access to the Radio Registers. Accessing the RREG (nb) address range initiates a Radio Register access, but does not wait for its completion. The details of mechanism is documented in the Radio Interface section of the AX8052 Programming Manual.

The FLASH memory is organized as 64 pages of 1 kBytes each. Each page can be individually erased. The write word size is 16 Bits. The last 1 kByte page is dedicated to factory calibration data and should not be overwritten.

Power Management

The microcontroller power mode can be selected independently from the transceiver. The microcontroller supports the following power modes:

Table 21. POWER MANAGEMENT

PCON register	Name	Description
00	RUNNING	The microcontroller and all peripherals are running. Current consumption depends on the system clock frequency and the enabled peripherals and their clock frequency.
01	STANDBY	The microcontroller is stopped. All register and memory contents are retained. All peripherals continue to function normally. Current consumption is determined by the enabled peripherals. STANDBY is exited when any of the enabled interrupts become active.
10	SLEEP	The microcontroller and its peripherals, except GPIO and the system controller, are shut down. Their register settings are lost. The internal RAM is retained. The external RAM is split into two 4 kByte blocks. Software can determine individually for both blocks whether contents of that block are to be retained or lost. SLEEP can be exited by any of the enabled GPIO or system controller interrupts. For most applications this will be a GPIO or wakeup timer interrupt.
11	DEEPSLEEP	The microcontroller, all peripherals and the transceiver are shut down. Only 4 bytes of scratch RAM are retained. DEEPSLEEP can only be exited by tying the PB3 pin low.

Clocking

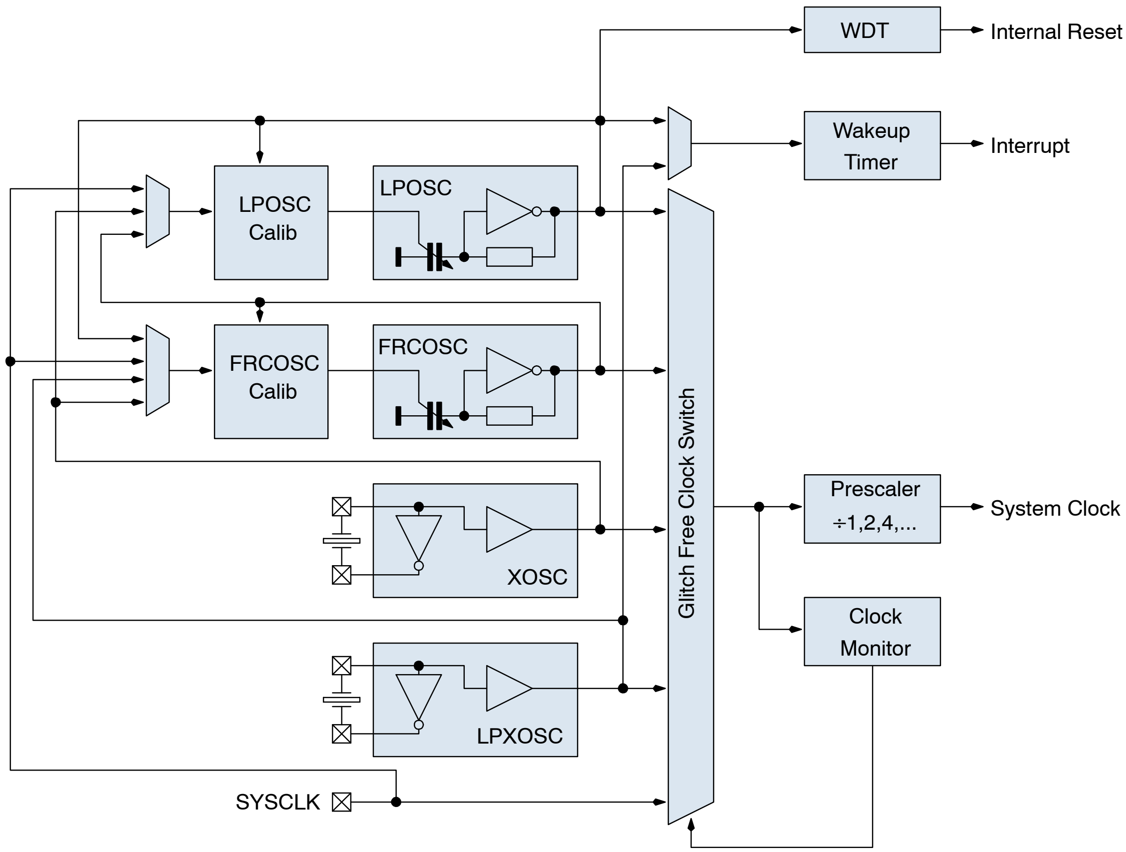

Figure 8. Clock System Diagram

The system clock can be derived from any of the following clock sources:

- The crystal oscillator (RF reference oscillator, typically 16 MHz, via SYSCLK)
- The low speed crystal oscillator (typical 32 kHz tuning fork)
- The internal high speed RC (20 MHz) oscillator
- The internal low power (640 Hz/10 kHz) oscillator

An additional pre−scaler allows the selected oscillator to be divided by a power of two. After reset, the microcontroller starts with the internal high speed RC oscillator selected and divided by two. I.e. at start−up, the microcontroller runs with 10 MHz ± 10%. Clocks may be switched any time by writing to the CLKCON register. In order to prevent clock glitches, the switching takes approximately $2 \cdot (T_1+T_2)$, where T_1 and T_2 are the periods of the old and the new clock. Switching may take longer if the new oscillator first has to start up. Internal oscillators start up instantaneously, but crystal oscillators may take a considerable amount of time to start the oscillation. CLKSTAT can be read to determine the clock switching status.

A programmable clock monitor resets the CLKCON register when no system clock transitions are found during a programmable time interval, thus reverts to the internal RC oscillator.

Both internal oscillators can be slaved to one of the crystal oscillators to increase the accuracy of the oscillation frequency. While the reference oscillator runs, the internal oscillator is slaved to the reference frequency by a digital frequency locked loop. When the reference oscillator is switched off, the internal oscillator continues to run unslaved with the last frequency setting.

Reset and Interrupts

After reset, the microcontroller starts executing at address 0x0000. Several events can lead to resetting the microcontroller core:

- POR or hardware RESET_N pin activated and released
- Leaving SLEEP or DEEPSLEEP mode
- Watchdog Reset
- Software Reset

The reset cause can be determined by reading the PCON register.

The microcontroller supports 22 interrupt sources. Each interrupt can be individually enabled and can be programmed to have one of two possible priorities. The interrupt vectors are located at 0x0003, 0x000B,…, 0x00AB.

Debugging

A hardware debug unit considerably eases debugging compared to other 8052 microcontrollers. It allows to reliably stop the microcontroller at breakpoints even if the stack is smashed. The debug unit communicates with the host PC running the debugger using a 3 wire interface. One wire is dedicated (DBG_EN), while two wires are shared with GPIO pins (PB6, PB7). When DBG_EN is driven high, PB6 and PB7 convert to debug interface pins and the GPIO functionality is no longer available. A pin emulation feature however allows bits PINB[7:6] to be set and PORTB[7:6] and DIRB[7:6] to be read by the debugger software. This allows for example switches or LEDs connected to the PB6, PB7 pins to be emulated in the debugger software whenever the debugger is active.

In order to protect the intellectual property of the firmware developer, the debug interface can be locked using a developer−selectable 64−bit key. The debug interface is then disabled and can only be enabled with the knowledge of this 64−bit key. Therefore, unauthorized persons cannot read the firmware through the debug interface, but debugging is still possible for authorized persons. Secure erase can be initiated without key knowledge; secure erase ensures that the main FLASH array is completely erased before erasing the key, reverting the chip into factory state.

The DebugLink peripheral looks like an UART to the microcontroller, and allows exchange of data between the microcontroller and the host PC without disrupting program execution.

Timer, Output Compare and Input Capture

The AX8052F143 features three general purpose 16−bit timers. Each timer can be clocked by the system clock, any of the available oscillators, or a dedicated input pin. The timers also feature a programmable clock inversion, a programmable prescaler that can divide by powers of two, and an optional clock synchronization logic that synchronizes the clock to the system clock. All three counters are identical and feature four different counting modes, as well as a ΣΔ mode that can be used to output an analog value on a dedicated digital pin only employing a simple RC lowpass filter.

Two output compare units work in conjunction with one of the timers to generate PWM signals.

Two input capture units work in conjunction with one of the timers to measure transitions on an input signal.

For software timekeeping, two additional 16−bit wakeup timers with 4 16−bit event registers are provided, generating an interrupt on match events.

UART

The AX8052F143 features two universal asynchronous receiver transmitters. They use one of the timers as baud rate generator. Word length can be programmed from 5 to 9 bits.

SPI Master/Slave Controller

The AX8052F143 features a master/slave SPI controller. Both 3 and 4 wire SPI variants are supported. In master mode, any of the on−chip oscillators or the system clock may be selected as clock source. An additional prescaler with divide by two capability provides additional clocking flexibility. Shift direction, as well as clock phase and inversion, are programmable.

ADC, Analog Comparators and Temperature Sensor

The AX8052F143 features a 10−bit, 500 kSample/s Analog to Digital converter. Figure 9 shows the block diagram of the ADC. The ADC supports both single ended and differential measurements. It uses an internal reference of 1 V. ×1, ×10 and ×0.1 gain modes are provided. The ADC may digitize signals on PA0…PA7, as well as VDD_IO and an internal temperature sensor. The user can define four channels which are then converted sequentially and stored in four separate result registers. Each channel configuration consists of the multiplexer and the gain setting.

The AX8052F143 contains an on−chip temperature sensor. Built−in calibration logic allows the temperature sensor to be calibrated in °C, °F or any other user defined temperature scale.

The AX8052F143 also features two analog comparators. Each comparator can either compare two voltages on dedicated PA pins, or one voltage against the internal 1 V reference. The comparator output can be routed to a dedicated digital output pin or can be read by software. The comparators are clocked with the system clock.

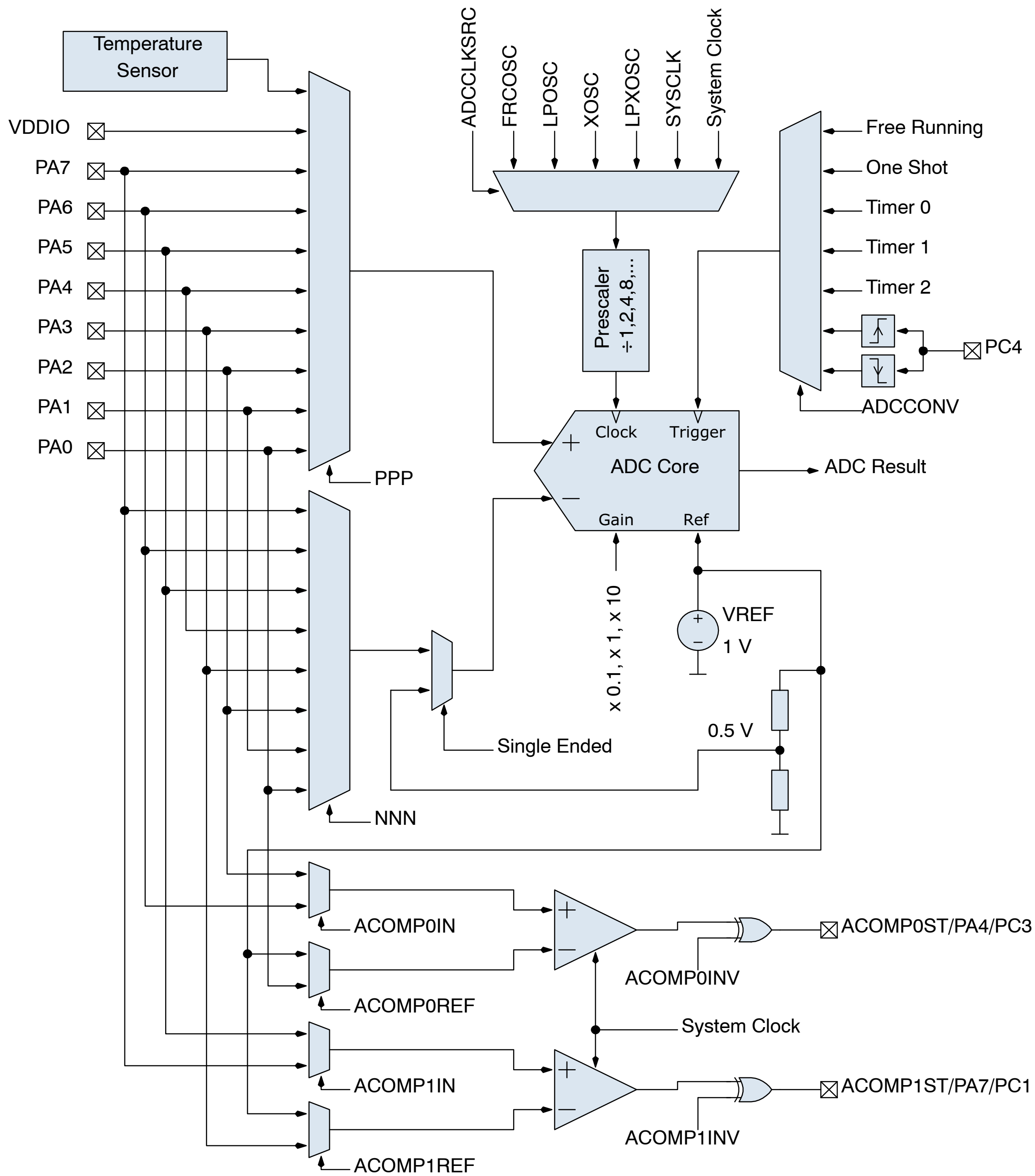

Figure 9. ADC Block Diagram

DMA Controller

The AX8052F143 features a dual channel DMA engine. Each DMA channel can either transfer data from XRAM to almost any peripheral on chip, or from almost any peripheral to XRAM. Both channels may also be cross−linked for memory−memory transfers. The DMA channels use buffer descriptors to find the buffers where data is to be retrieved or placed, thus enabling very flexible buffering strategies.

The DMA channels access XRAM in a cycle steal fashion. They access XRAM whenever XRAM is not used by the microcontroller. Their priority is lower than the microcontroller, thus interfering very little with the microcontroller. Additional logic prevents starvation of the DMA controller.

AES Engine

The AX8052F143 contains a dedicated engine for the government mandated Advanced Encryption Standard (AES). It features a dedicated DMA engine and reads input data as well as key stream data from the XRAM, and writes output data into a programmable buffer in the XRAM. The round number is programmable; the chip therefore supports AES−128, AES−192, and AES−256, as well as higher security proprietary variants. Keystream (key expansion) is performed in software, adding to the flexibility of the AES engine. ECB (electronic codebook), CFB (cipher feedback) and OFB (output feedback) modes are directly supported without software intervention.

Crystal Oscillator and TCXO Interface (RF Reference Oscillator)

The AX8052F143 is normally operated with an external TCXO, which is required by most narrow−band regulation with a tolerance of 0.5 ppm to 1.5 ppm depending on the regulation. The on−chip crystal oscillator allows the use of an inexpensive quartz crystal as the RF generation subsystem's timing reference when possible from a regulatory point of view.

A wide range of crystal frequencies can be handled by the crystal oscillator circuit. As the reference frequency impacts both the spectral performance of the transmitter as well as the current consumption of the receiver, the choice of reference frequency should be made according to the regulatory regime targeted by the application. Application Notes for usage of AX5043 in compliance with various regulatory regimes also apply to AX8052F143.

The crystal or TCXO reference frequency should be chosen so that the RF carrier frequency is not an integer multiple of the crystal or TCXO frequency.

The oscillator circuit is enabled by programming the AX5043_PWRMODE register. At power−up it is enabled.

To adjust the circuit's characteristics to the quartz crystal being used, without using additional external components, the tuning capacitance of the crystal oscillator can be programmed. The transconductance of the oscillator is automatically regulated, to allow for fastest start−up times together with lowest power operation during steady−state oscillation.

The integrated programmable tuning capacitor bank makes it possible to connect the oscillator directly to pins CLK16N and CLK16P without the need for external capacitors. It is programmed using bits XTALCAP[5:0] in register AX5043_XTALCAP.

To synchronize the receiver frequency to a carrier signal, the oscillator frequency could be tuned using the capacitor bank however, the recommended method to implement frequency synchronization is to make use of the high resolution RF frequency generation sub−system together with the Automatic Frequency Control, both are described further down.

Alternatively a single ended reference (TXCO, CXO) may be used. The CMOS levels should be applied to CLK16P via an AC coupling with the crystal oscillator enabled. For detailed TCXO network recommendations depending on TCXO output swing refer to the AX5043 Application Note: Use with a TCXO Reference Clock.

Low Power Oscillator and Wake on Radio (WOR) Mode

The AX8052F143 transceiver features an internal lowest power fully integrated oscillator. In default mode the frequency of oscillation is 640 Hz ± 1.5%, in fast mode it is 10.2 kHz ± 1.5%.

If Wake on Radio Mode is enabled, the receiver wakes up periodically at a user selectable interval, and checks for a radio signal on the selected channel. If no signal is detected, the receiver shuts down again. If a radio signal is detected, and a valid packet is received, the microcontroller is alerted by asserting an interrupt.

SYSCLK Output

The SYSCLK pin outputs the RF reference clock signal divided by a programmable integer. Divisions from 1 to 2048 are possible. For divider ratios > 1 the duty cycle is 50%. Bits SYSCLK[3:0] in the AX5043_PINCFG1 register set the divider ratio. The SYSCLK output can be disabled.

Power−on−Reset (POR) and RESET_N Input

AX8052F143 has an integrated power−on−reset block which is edge sensitive to VDD_IO. For many common application cases no external reset circuitry is required. However, if VDD_IO ramps cannot be guaranteed, an external reset circuit is recommended. For detailed recommendations and requirements see the AX8052 Application Note: Power On Reset.

After POR or reset all registers are set to their default values.

The RESET_N pin contains a weak pull−up. However, it is strongly recommended to connect the RESET_N pin to VDD_IO if not used, for additional robustness.

The AX8052F143 can be reset by software as well. The microcontroller is reset by writing 1 to the SWRESET bit of the PCON register. The transceiver can be reset by first writing 1 and then 0 to the RST bit in the AX5043_PWRMODE register.

Ports

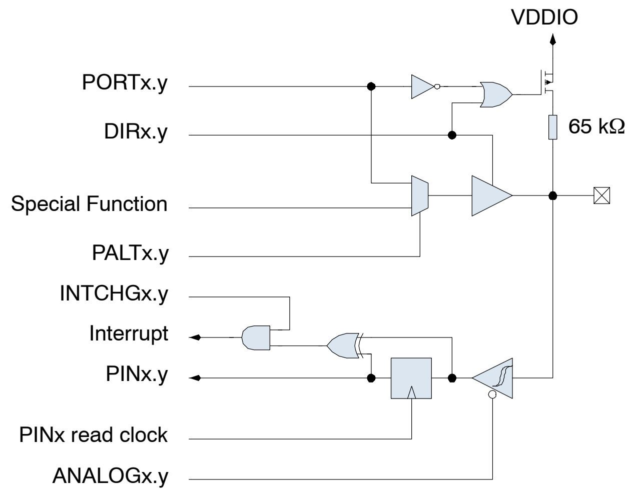

Figure 10. Port Pin Schematic

Figure 10 shows the GPIO logic. The DIR register bit determines whether the port pin acts as an output (1) or an input (0).

If configured as an output, the PALT register bit determines whether the port pin is connected to a peripheral output (1), or used as a GPIO pin (0). In the latter case, the PORT register bit determines the port pin drive value.

If configured as an input, the PORT register bit determines whether a pull−up resistor is enabled (1) or disabled (0). Inputs have chmitt−trigger characteristic. Port A inputs may be disabled by setting the ANALOGA register bit; this prevents additional current consumption if the voltage level of the port pin is mid−way between logic low and logic high, when the pin is used as an analog input.

Port A, B and C pins may interrupt the microcontroller if their level changes. The INTCHG register bit enables the interrupt. The PIN register bit reflects the value of the port pin. Reading the PIN register also resets the interrupt if interrupt on change is enabled.

PWRAMP and ANTSEL

PWRAMP functionality is available on PB2 if PALTRADIO bit 6 and DIRB bit 2 are set. ANTSEL functionality is available on PB3 if PALTRADIO bit 7 and DIRB bit 3 are set. If these pins should be set to high−impedance, it must be done by clearing the corresponding DIRB bit, not by setting AX5043_PINFUNCPWRAMP or AX5043_PINFUNCANTSEL to Z.