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Not Recommended for New Designs

BCM® Bus Converter

B048x160y24A

Unregulated DC-DC Converter

FEATURES

- 48 Vdc – 16.0 Vdc 240 W Bus Converter
- High efficiency (>94%) reduces system power consumption
- High power density (>817 W/in^3) reduces power system footprint by >40%
- Contains built-in protection features:
  - Undervoltage
  - Overvoltage Lockout
  - Overcurrent Protection
  - Short circuit Protection
  - Overtemperature Protection
- Provides enable/disable control, internal temperature monitoring
- Can be paralleled to create multi-kW arrays

TYPICAL APPLICATIONS

- High End Computing Systems
- Automated Test Equipment
- High Density Power Supplies
- Communications Systems

DESCRIPTION

The VI Chip® bus converter is a high efficiency (>94%) Sine Amplitude Converter™ (SAC™) operating from a 38 to 55 Vdc primary bus to deliver an isolated, unregulated 12.7 to 18.3 output. The Sine Amplitude Converter offers a low AC impedance beyond the bandwidth of most downstream regulators; therefore capacitance normally at the load can be located at the input to the Sine Amplitude Converter. Since the transformation ratio of the B048x160y24A is 1/3, the capacitance value can be reduced by a factor of 9x, resulting in savings of board area, materials and total system cost.

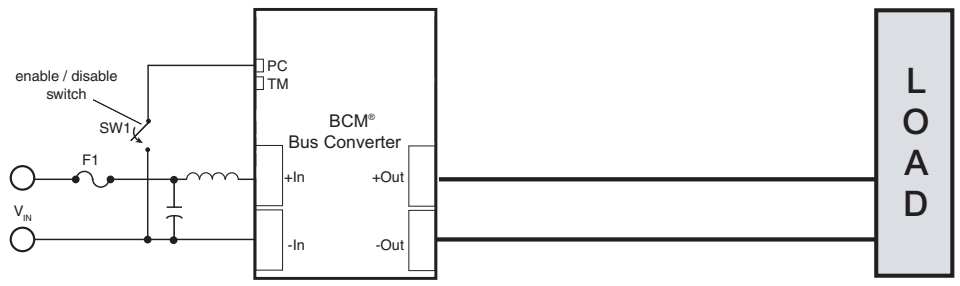
The B048x160y24A is provided in a VI Chip package compatible with standard pick-and-place and surface mount assembly processes. The co-molded VI Chip package provides enhanced thermal management due to a large thermal interface area and superior thermal conductivity. The high conversion efficiency of the B048x160y24A increases overall system efficiency and lowers operating costs compared to conventional approaches.

PART NUMBERING

PART NUMBER	PACKAGE STYLE	PRODUCT GRADE
B048 **x** 160 **y** 24A	**F** = J-Lead	**T** = -40° to 125°C
	T = Through hole	**M** = -55° to 125°C

For Storage and Operating Temperatures see Section 6.0 General Characteristics

TYPICAL APPLICATION



1.0 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

	MIN	MAX	UNIT
+IN to –IN	-1	60	V
VIN slew rate (operational)	-1	1	V/µs
Isolation voltage, input to output		2250	V
+OUT to –OUT	-0.5	30	V

	MIN	MAX	UNIT
Output current transient (< = 10 ms, < = 10% DC)	-3	23	A
Output current average	-2	15	A
PC to –IN	-0.3	20	V
TM to –IN	-0.3	7	V

2.0 ELECTRICAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T_C < 100°C (T-Grade)**; All other specifications are at **T_C = 25°C** unless otherwise noted.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
POWERTRAIN						
Input voltage range, continuous	V_{IN_DC}		**38**		**55**	V
Input voltage range, transient	V_{IN_TRANS}	Full current or power supported, 50 ms max, 10% duty cycle max	**38**		**55**	V
Quiescent current	I_Q	Disabled, PC Low		5.0	**7.0**	mA
V_{IN} to V_{OUT} time	$T_{ON}1$	V_{IN} = 48 V, PC floating	600	730	900	ms
No load power dissipation	P_{NL}	V_{IN} = 48 V, T_C = 25°C		4.4	5.6	W
		V_{IN} = 48 V	**1.9**		**8.5**	
		V_{IN} = 38 V to 55 V, T_C = 25°C			7	
		V_{IN} = 38 V to 55 V			**10**	
Inrush current peak	I_{INR_P}	Worse case of: V_{IN} = 55 V, C_{OUT} = 800 µF, R_{LOAD} = 1040 mΩ		13	**20**	A
DC input current	I_{IN_DC}	At P_{OUT} = 240 W			**5.5**	A
Transformation ratio	K	K = V_{OUT}/V_{IN}, at no load		1/3		V/V
Output power (average)	P_{OUT_AVG}				**240**	W
Output power (peak)	P_{OUT_PK}	10 ms max, P_{OUT_AVG} ≤ 240 W			**360**	W
Output current (average)	I_{OUT_AVG}				**15**	A
Output current (peak)	I_{OUT_PK}	10 ms max, I_{OUT_AVG} ≤ 15 A			**23**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 48 V, I_{OUT} = 15 A; T_C = 25°C	94.5	95.3		%
		V_{IN} = 38 V to 55 V, I_{OUT} = 15 A; T_C = 25°C	90.0			
		V_{IN} = 48 V, I_{OUT} = 8 A; T_C = 25°C	93.8	94.8		
Efficiency (hot)	η_{HOT}	V_{IN} = 48 V, I_{OUT} = 15 A; T_C = 100°C	94.4	95.0		%
Efficiency (over load range)	$\eta_{20\%}$	3 A < I_{OUT} < 15 A	**82.0**			%
Output resistance	R_{OUT_COLD}	I_{OUT} = 15 A, T_C = -40°C	11.0	22.1	31.0	mΩ
	R_{OUT_AMB}	I_{OUT} = 15 A, T_C = 25°C	19.0	26.6	33.0	mΩ
	R_{OUT_HOT}	I_{OUT} = 15 A, T_C = 100°C	24.0	30.2	35.0	mΩ
Switching frequency	F_{SW}		**1.56**	1.65	**1.74**	MHz
Output voltage ripple	V_{OUT_PP}	C_{OUT} = 0 F, I_{OUT} = 15 A, V_{IN} = 48 V, 20 MHz BW, Section 10		250	**350**	mV
Output inductance (parasitic)	L_{OUT_PAR}	Frequency up to 30 MHz, Simulated J-lead model		600		pH
Output capacitance (internal)	C_{OUT_INT}	Effective value at 16.0 V_{OUT}		4		µF
Output capacitance (external)	C_{OUT_EXT}		**0**		**800**	µF

2.0 ELECTRICAL CHARACTERISTICS (CONT.)

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
PROTECTION						
Input overvoltage lockout threshold	V_{IN_OVLO+}		**55.1**	59.0	**60**	V
Input overvoltage recovery threshold	V_{IN_OVLO-}		**55.1**	56.0	**60**	V
Input overvoltage lockout hysteresis	$V_{IN\_OVLO\_HYST}$			1.2		V
Overvoltage lockout response time	T_{OVLO}			8		µs
Fault recovery time	$T_{AUTO\_RESTART}$		**240**	300	**380**	ms
Input undervoltage lockout threshold	V_{IN_UVLO-}		**28.5**	31.1	**37.4**	V
Input undervoltage recovery threshold	V_{IN_UVLO+}		**28.5**	33.7	**37.4**	V
Input undervoltage lockout hysteresis	$V_{IN\_UVLO\_HYST}$			1.6		V
Undervoltage lockout response time	T_{UVLO}			8		µs
Output overcurrent trip threshold	I_{OCP}		**16**	31	**44**	A
Output overcurrent response time constant	T_{OCP}	Effective internal RC filter		7.7		ms
Short circuit protection trip threshold	I_{SCP}		**35**			A
Short circuit protection response time	T_{SCP}			1		µs
Thermal shutdown threshold	T_{J_OTP}		**125**			°C

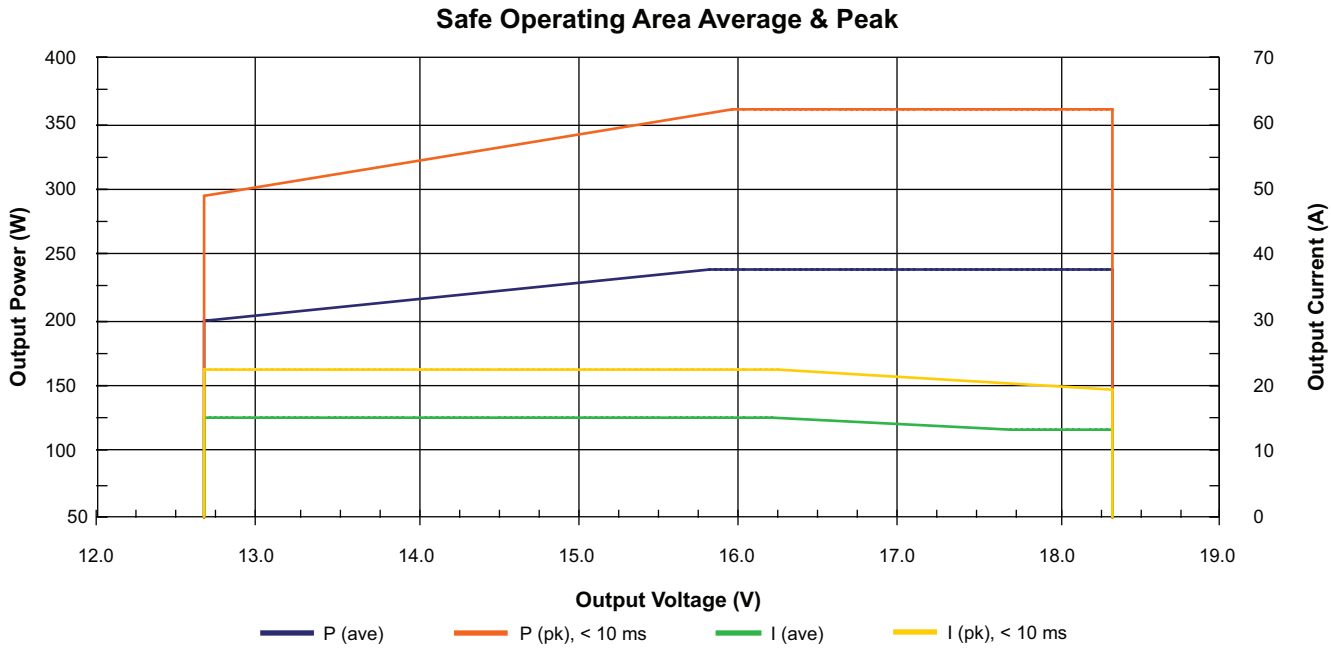


Figure 1 — *Safe operating area*

3.0 SIGNAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C < T_C < 100°C (T-Grade); All other specifications are at T_C = 25°C unless otherwise noted.

PRIMARY CONTROL : PC

- The PC pin enables and disables the BCM. When held low, the BCM is disabled.
- In an array of BCM modules, PC pins should be interconnected to synchronize start up and permit start up into full load conditions.
- PC pin outputs 5 V during normal operation. PC pin internal bias level drops to 2.5 V during fault mode, provided V_{IN} remains in the valid range.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Regular Operation	PC voltage	V_{PC}		**4.7**	5.0	**5.3**	V
		PC available current	I_{PC_OP}		**2.0**	3.5	**5.0**	mA
	Standby	PC source (current)	I_{PC_EN}		**50**	100		µA
		PC resistance (internal)	R_{PC_INT}	Internal pull down resistor	**50**	150	**400**	kΩ
	Transition	PC capacitance (internal)	C_{PC_INT}	Section 7			**1100**	pF
	Start Up	PC load resistance	R_{PC_S}	To permit regular operation	**60**			kΩ
DIGITAL INPUT / OUPUT	Start Up	PC time to start	$T_{ON}1$		**400**	550	**620**	ms
	Regular Operation	PC enable threshold	V_{PC_EN}		**2.0**	2.5	**3.0**	V
	Standby	PC disable duration	$T_{PC\_DIS\_T}$	Minimum time before attempting re-enable	**1**			s
	Transition	PC threshold hysteresis	V_{PC_HYSTER}			50		mV
		PC enable to V_{OUT} time	T_{ON2}	V_{IN} = 48 V for at least T_{ON1} ms	50	100	150	µs
		PC disable to standby time	$T_{PC\text{-}DIS}$			4	**10**	µs
		PC fault response time	T_{FR_PC}	From fault to PC = 2 V		100		µs

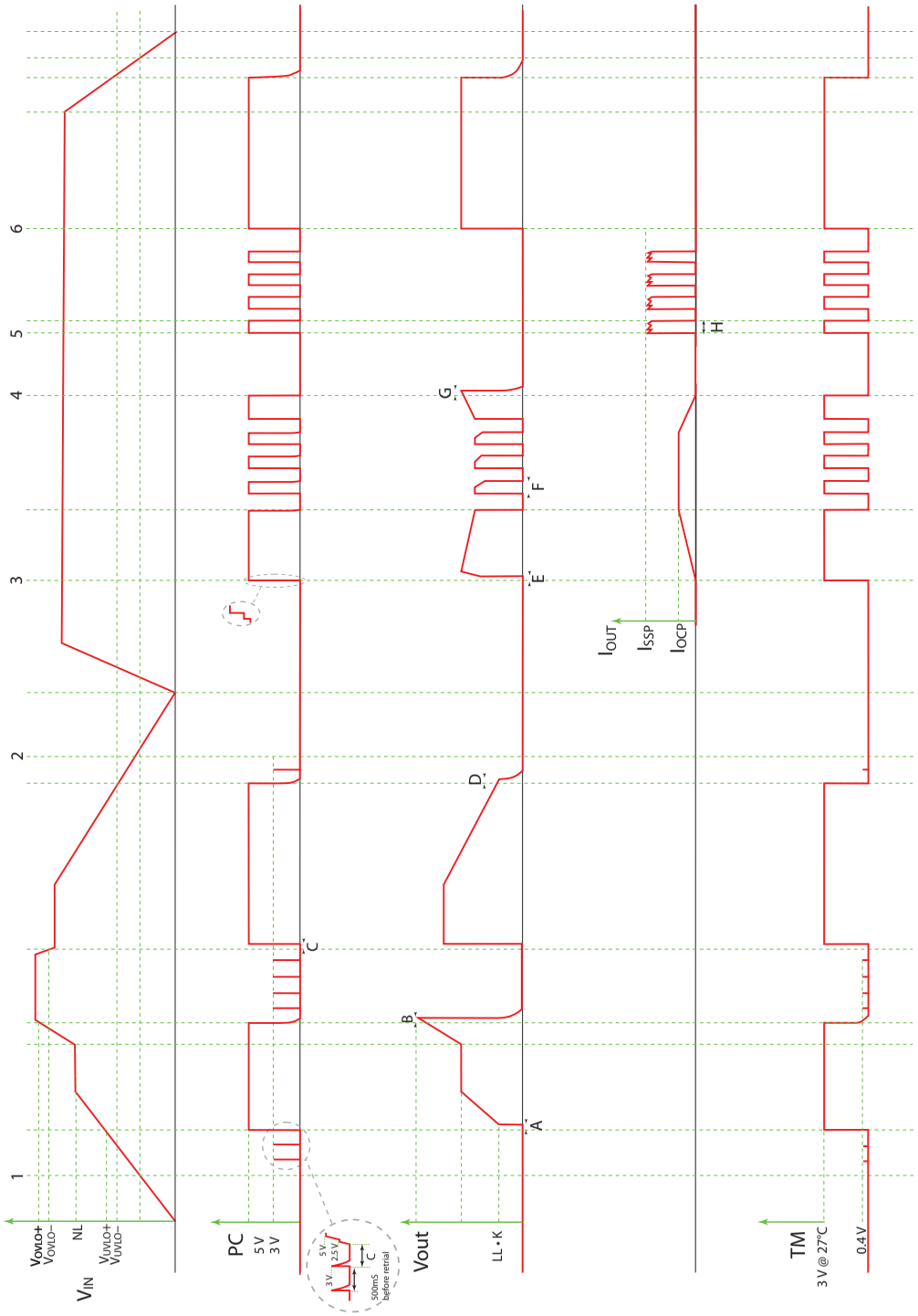
TEMPERATURE MONITOR : TM

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Regular Operation	TM voltage range	V_{TM}		**2.12**		**4.04**	V
		TM voltage reference	V_{TM_AMB}	T_J controller = 27°C	2.95	3.00	3.05	V
		TM available current	I_{TM}		**100**			µA
		TM gain	A_{TM}			10		mV/°C
		TM voltage ripple	V_{TM_PP}	C_{TM} = 0 pF, V_{IN} = 48 V, I_{OUT} = 15 A		120	**200**	mV
DIGITAL OUTPUT (FAULT FLAG)	Transition	TM capacitance (external)	C_{TM_EXT}				**50**	pF
		TM fault response time	T_{FR_TM}	From fault to TM = 1.5 V		10		µs
	Standby	TM voltage	V_{TM_DIS}			0		V
		TM pull down (internal)	R_{TM_INT}	Internal pull down resistor	**25**	40	**50**	kΩ

RESERVED : RSV

Reserved for factory use. No connection should be made to this pin.

4.0 TIMING DIAGRAM



Notes:
– Timing and signal amplitudes are not to scale
– Error pulse width is load dependent

A: T_{ON1}
B: T_{OVLO}*
C: $T_{AUTO\_RESTART}$
D: T_{UVLO}
E: T_{ON2}
F: T_{OCP}
G: T_{PC-DIS}
H: T_{SCP}**

1: Controller start
2: Controller turn off
3: PC release
4: PC pulled low
5: PC released on output SC
6: SC removed

*Min value switching off
**From detection of error to power train shut down

5.0 APPLICATION CHARACTERISTICS

The following values, typical of an application environment, are collected at T_C = 25°C unless otherwise noted. See associated figures for general trend data.

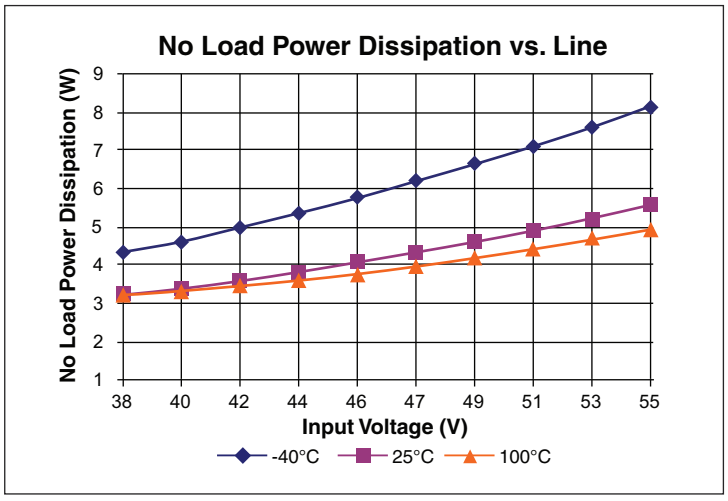


Figure 2 — *No load power dissipation vs. V_{IN}*

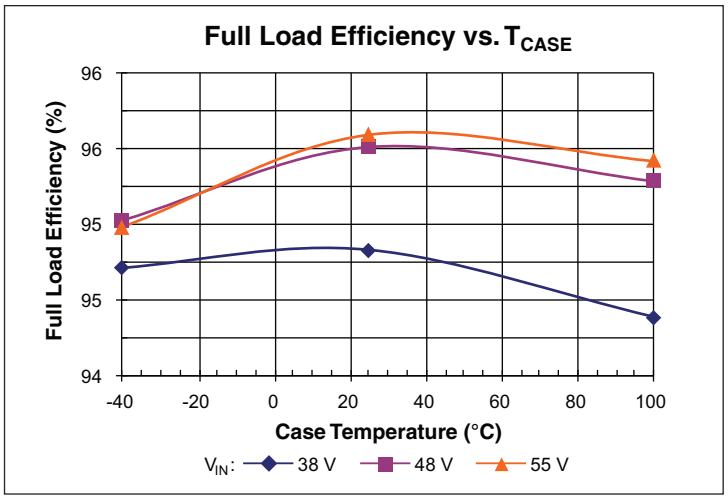


Figure 3 — *Full load efficiency vs. temperature; V_{IN}*

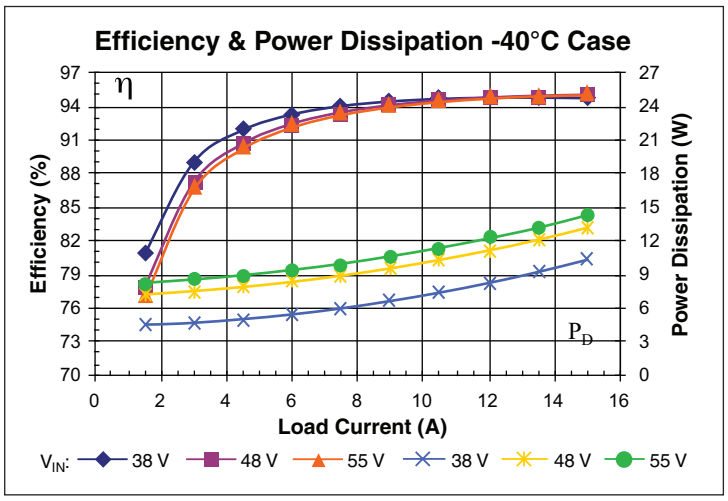


Figure 4 — *Efficiency and power dissipation at T_C = -40°C*

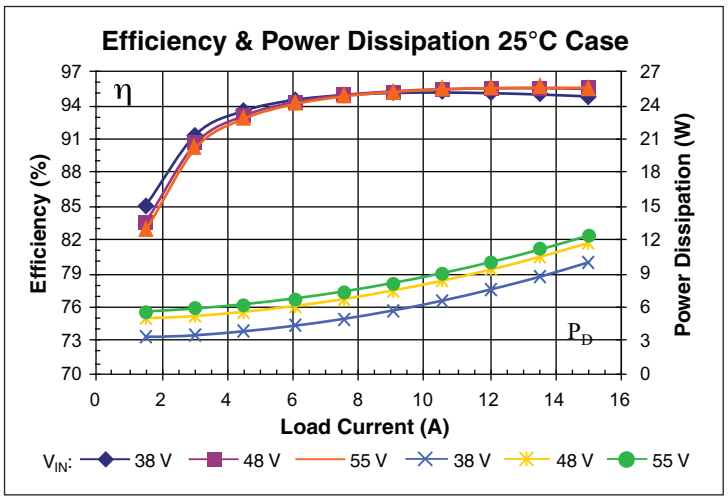


Figure 5 — *Efficiency and power dissipation at T_C = 25°C*

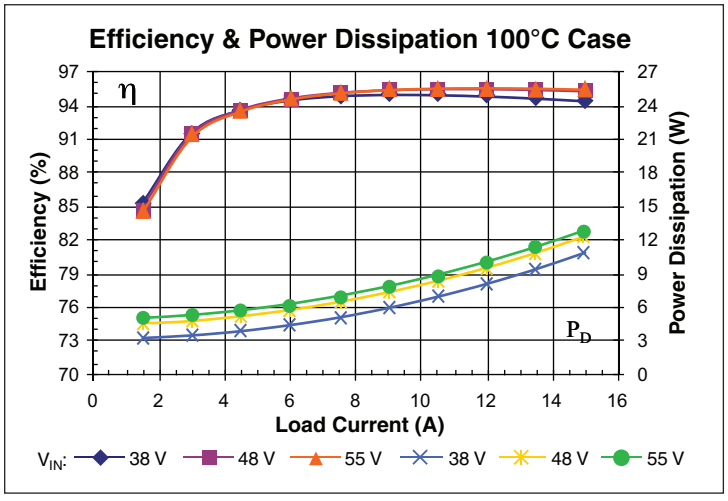


Figure 6 — *Efficiency and power dissipation at T_C = 100°C*

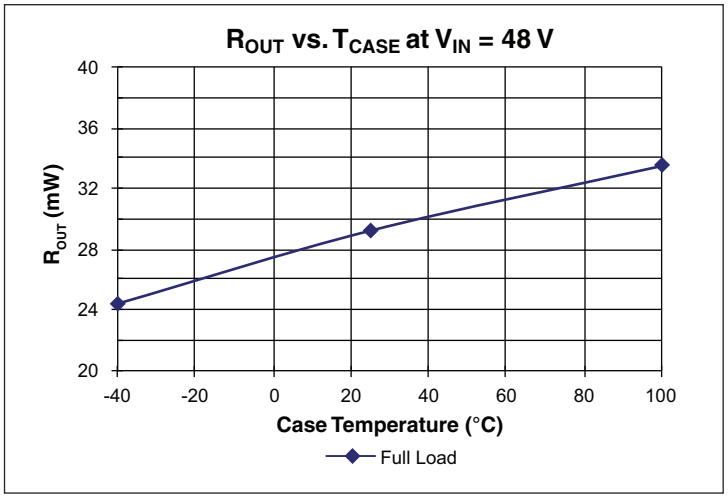


Figure 7 — *R_{OUT} vs. temperature*

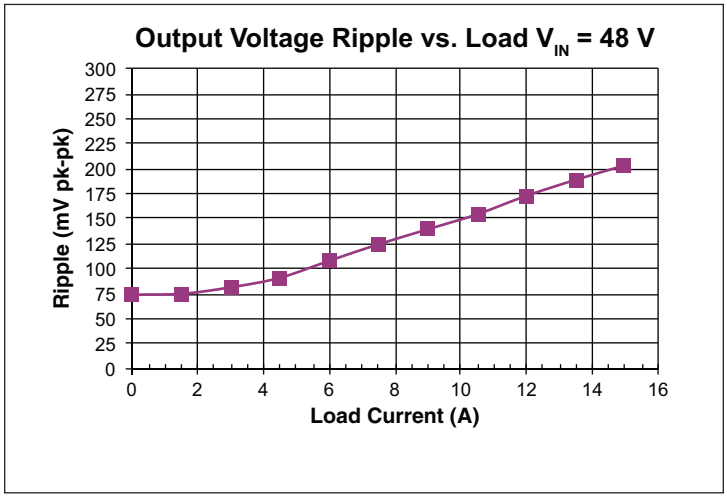


Figure 8 — *V_{RIPPLE} vs. I_{OUT} ; No external C_{OUT}, Board mounted module, scope setting : 20 MHz analog BW*

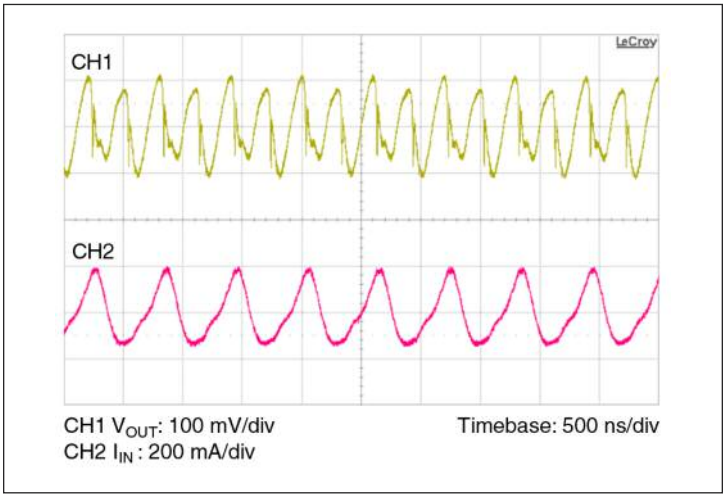


Figure 9 — *Full load ripple, 330 µF C_{IN}; No external C_{OUT}. Board mounted module, scope setting : 20 MHz analog BW*

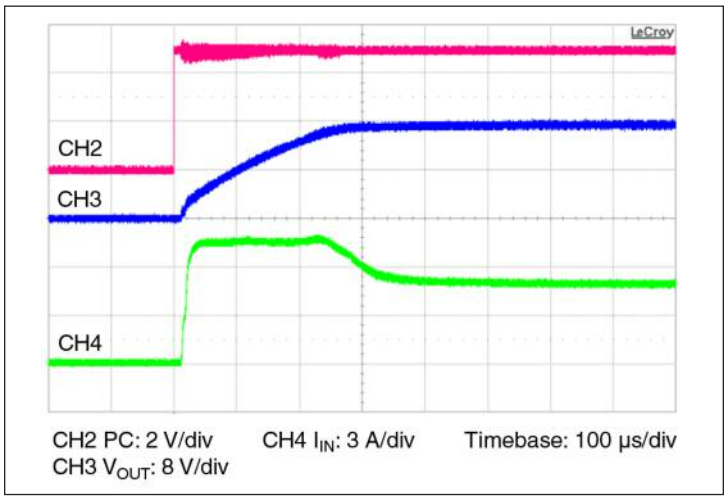


Figure 10 — *Start up from application of PC; V_{IN} pre-applied C_{OUT} = 800 µF*

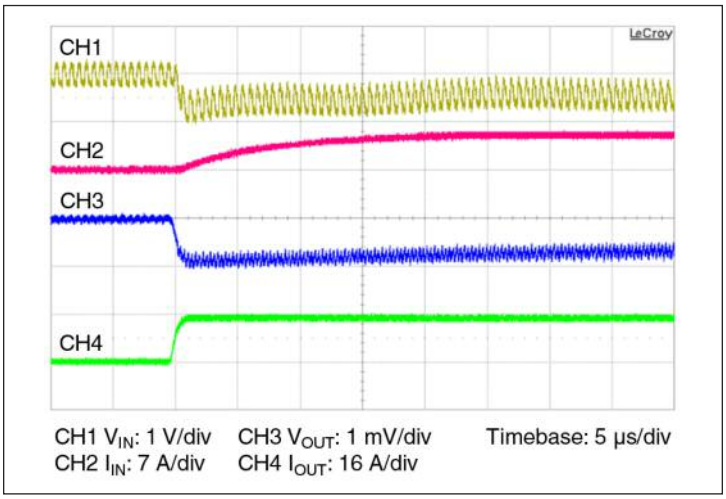


Figure 11 — *0 A– 15 A transient response: C_{IN} = 330 µF, I_{IN} measured prior to C_{IN}, no external C_{OUT}*

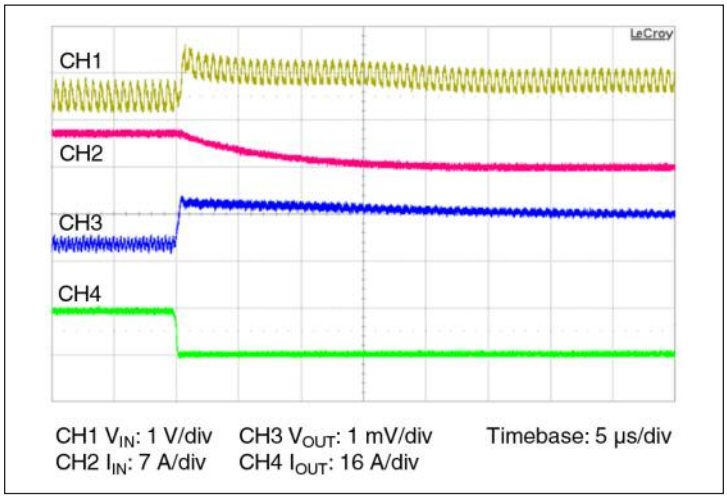


Figure 12 — *15 A – 0 A transient response: C_{IN} = 330 µF, I_{IN} measured prior to C_{IN}, no external C_{OUT}*

6.0 GENERAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T_J < 125°C (T-Grade)**; All other specifications are at **T_J = 25°C** unless otherwise noted.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
MECHANICAL						
Length	L		32.25 / [1.270]	32.50 / [1.280]	32.75 / [1.289]	mm/[in]
Width	W		21.75 / [0.856]	22.00 / [0.866]	22.25 / [0.876]	mm/[in]
Height	H		6.48 / [0.255]	6.73 / [0.265]	6.98 / [0.275]	mm/[in]
Volume	Vol	No heat sink		4.81 / [0.294]		cm^3/[in^3]
Weight	W			14.5 / [0.512]		g/[oz]
Lead finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
THERMAL						
Operating temperature	T_J	B048x160y24A (T-Grade)	-40		125	°C
		BCM48BF160M240A00 (M-Grade)	-55		125	°C
Thermal resistance	ϕ_{JC}	Isothermal heatsink and isothermal internal PCB		1		°C/W
Thermal capacity				5		Ws/°C
ASSEMBLY						
Peak compressive force applied to case (Z-axis)		Supported by J-lead only			6	lbs
					5.41	lbs / in^2
Storage temperature	T_{ST}	B048x160y24A (T-Grade)	-40		125	°C
		BCM48BF160M240A00 (M-Grade)	-65		125	°C
Moisture sensitivity level	MSL	MSL 6, 4 hours out of bag maximum				
		MSL 5				
ESD withstand	ESD_{HBM}	Human Body Model, "JEDEC JESD 22-A114D.01" Class 1D	1000			V
	ESD_{CDM}	Charge Device Model, "JEDEC JESD 22-C101-D"	400			
SOLDERING						
Peak temperature during reflow		MSL 6, 4 hours out of bag maximum			245	°C
		MSL 5			225	°C
Peak time above 217°C				60	90	s
Peak heating rate during reflow				1.5	3	°C/s
Peak cooling rate post reflow				1.5	6	°C/s
SAFETY						
Working voltage (IN – OUT)	V_{IN_OUT}				**60**	VDC
Isolation voltage (hipot)	V_{HIPOT}		**2,250**			VDC
Isolation capacitance	C_{IN_OUT}	Unpowered unit	**2500**	**3200**	**3800**	pF
Isolation resistance	R_{IN_OUT}	At 500 Vdc	**10**			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer Profile		4.6		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		5.8		MHrs
Agency approvals / standards		cTUVus				
		cURus				
		CE Marked for Low Voltage Directive and ROHS recast directive, as applicable.				

7.0 USING THE CONTROL SIGNALS PC, TM

Primary Control (PC) pin can be used to accomplish the following functions:

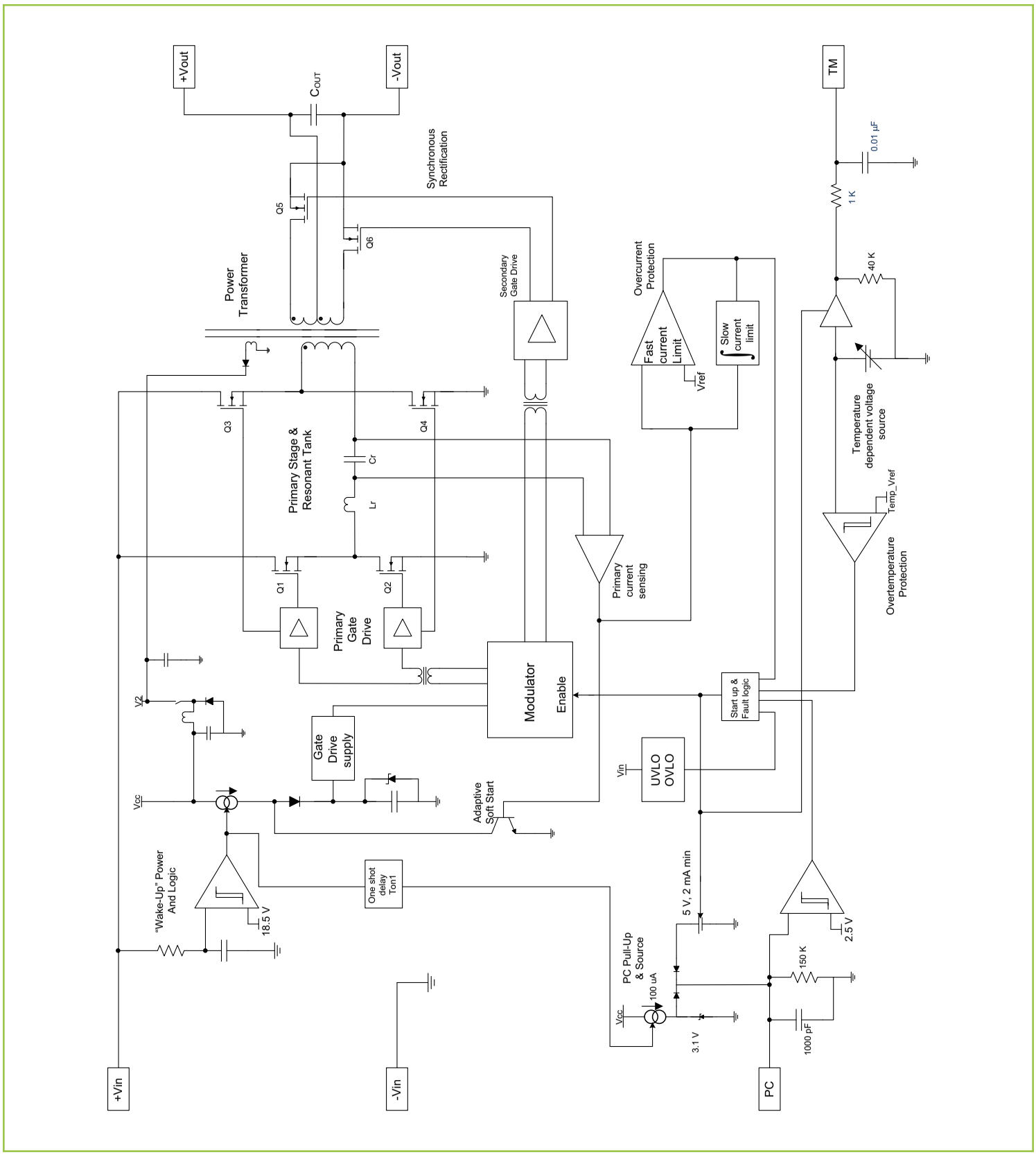
- Logic enable and disable for module: Once T_{on1} time has been satisfied, a PC voltage greater than Vpc_en will cause the module to start. Bringing PC lower than Vpc_dis will cause the module to enter standby.
- Auxiliary voltage source: Once enabled in regular operational conditions (no fault), each BCM module PC provides a regulated 5 V, 3.5 mA voltage source.
- Synchronized start up: In an array of parallel modules, PC pins should be connected to synchronize start up across units. This permits the maximum load and capacitance to scale by the number of paralleled modules.
- Output disable: PC pin can be actively pulled down in order to disable the module. Pull down impedance shall be lower than 60 Ω.
- Fault detection flag: The PC 5 V voltage source is internally turned off as soon as a fault is detected.
- Note that PC can not sink significant current during a fault condition. The PC pin of a faulted module will not cause interconnected PC pins of other modules to be disabled.

Temperature Monitor (TM) pin provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- Monitor the control IC temperature: The temperature in Kelvin is equal to the voltage on the TM pin scaled by 100. (i.e. 3.0 V = 300 K = 27°C). If a heat sink is applied, TM can be used to protect the system thermally.
- Fault detection flag: The TM voltage source is internally turned off as soon as a fault is detected. For system monitoring purposes microcontroller interface faults are detected on falling edges of TM signal.

8.0 B048x160y24A BLOCK DIAGRAM



9.0 SINE AMPLITUDE CONVERTER™ POINT OF LOAD CONVERSION

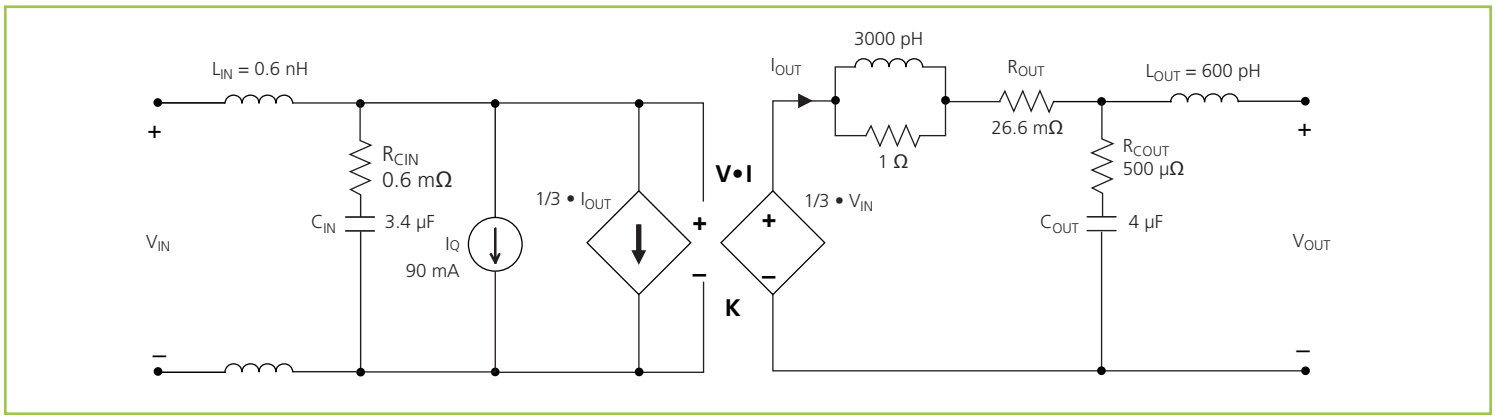


Figure 13 — *VI Chip® module AC model*

The Sine Amplitude Converter (SAC™) uses a high frequency resonant tank to move energy from input to output. (The resonant tank is formed by Cr and leakage inductance Lr in the power transformer windings as shown in the BCM module Block Diagram. See Section 8). The resonant LC tank, operated at high frequency, is amplitude modulated as a function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving power density.

The B048x160y24A SAC can be simplified into the preceeding model.

At no load:

$$V_{OUT} = V_{IN} \bullet K \quad (1)$$

K represents the "turns ratio" of the SAC.
Rearranging Eq (1):

$$K = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

In the presence of load, V_{OUT} is represented by:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{OUT} \quad (3)$$

and I_{OUT} is represented by:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K} \quad (4)$$

R_{OUT} represents the impedance of the SAC, and is a function of the R_{DSON} of the input and output MOSFETs and the winding resistance of the power transformer. I_Q represents the quiescent current of the SAC control, gate drive circuitry, and core losses.

The use of DC voltage transformation provides additional interesting attributes. Assuming that $R_{OUT} = 0\ \Omega$ and $I_Q = 0$ A, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with V_{IN}.

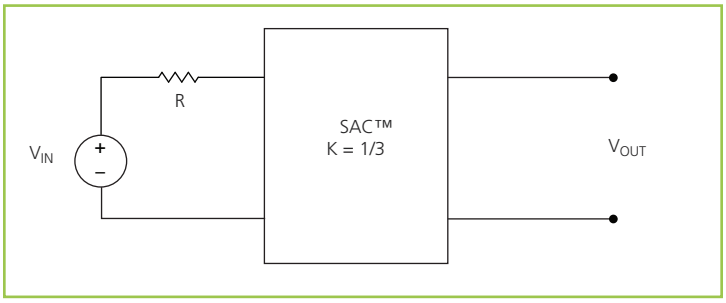


Figure 14 — *K = 1/3 Sine Amplitude Converter™ with series input resistor*

The relationship between V_{IN} and V_{OUT} becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \bullet R) \bullet K \quad (5)$$

Substituting the simplified version of Eq. (4) (I_Q is assumed = 0 A) into Eq. (5) yields:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R \bullet K^2 \quad (6)$$

This is similar in form to Eq. (3), where R_{OUT} is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the input side of the SAC is effectively scaled by K^2 with respect to the output.

Assuming that R = 1 Ω, the effective R as seen from the secondary side is 111.1 mΩ, with K = 1/3 .

A similar exercise should be performed with the additon of a capacitor or shunt impedance at the input to the SAC. A switch in series with V_{IN} is added to the circuit. This is depicted in Figure 15.

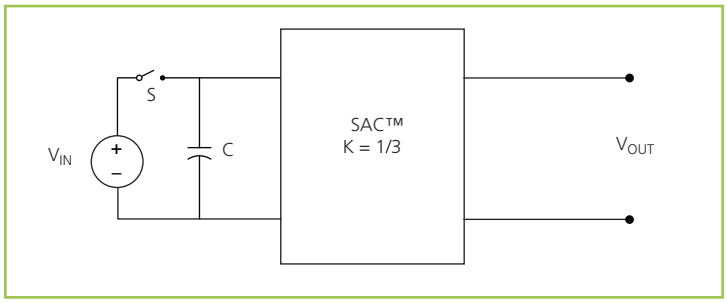


Figure 15 — *Sine Amplitude Converter™ with input capacitor*

A change in V_{IN} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{IN}}{dt} \quad (7)$$

Assume that with the capacitor charged to V_{IN}, the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{OUT} \bullet K \quad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{OUT} = \frac{C}{K^2} \bullet \frac{dV_{OUT}}{dt} \quad (9)$$

The equation in terms of the output has yielded a K^2 scaling factor for C, specified in the denominator of the equation. A K factor less than unity results in an effectively larger capacitance on the output when expressed in terms of the input. With a K = 1/3 as shown in Figure 15, C = 1 µF would appear as C = 9 µF when viewed from the output.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM® module are:

- No load power dissipation (P_{NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss (R_{OUT}): refers to the power loss across the BCM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{R_{OUT}} \quad (10)$$

Therefore,

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{R_{OUT}} \quad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{R_{OUT}}}{P_{IN}} \quad (12)$$

$$= \frac{V_{IN} \bullet I_{IN} - P_{NL} - (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}$$

$$= 1 - \left(\frac{P_{NL} + (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}\right)$$

10.0 INPUT AND OUTPUT FILTER DESIGN

A major advantage of SAC™ systems versus conventional PWM converters is that the transformers do not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieve power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

1. Guarantee low source impedance:

   To take full advantage of the BCM module's dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be as high as 1 µF in series with 0.3 Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

2. Further reduce input and/or output voltage ripple without sacrificing dynamic response:

   Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the module multiplied by its K factor. This is illustrated in Figures 11 and 12.

3. Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures:

   The module input/output voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even during this condition, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it. A criterion for protection is the maximum amount of energy that the input or output switches can tolerate if avalanched.

Total load capacitance at the output of the BCM module shall not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the module. At frequencies <500 kHz the module appears as an impedance of R_{OUT} between the source and load.

Within this frequency range, capacitance at the input appears as effective capacitance on the output per the relationship defined in Eq. 5.

$$C_{OUT} = \frac{C_{IN}}{K^2} \qquad \text{Eq. 6}$$

This enables a reduction in the size and number of capacitors used in a typical system.

11.0 THERMAL CONSIDERATIONS

VI Chip® products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input / output conditions, thermal management and environmental conditions. Maintaining the top of the B048x160y24A case to less than 100ºC will keep all junctions within the VI Chip module below 125ºC for most applications.

The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.

It is not recommended to use a VI Chip module for an extended period of time at full load without proper heat sinking.

12.0 CURRENT SHARING

The performance of the SAC™ topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- Apply same input / output filters (if present) to each unit.

For further details see AN:016 Using BCM Bus Converters in High Power Arrays.

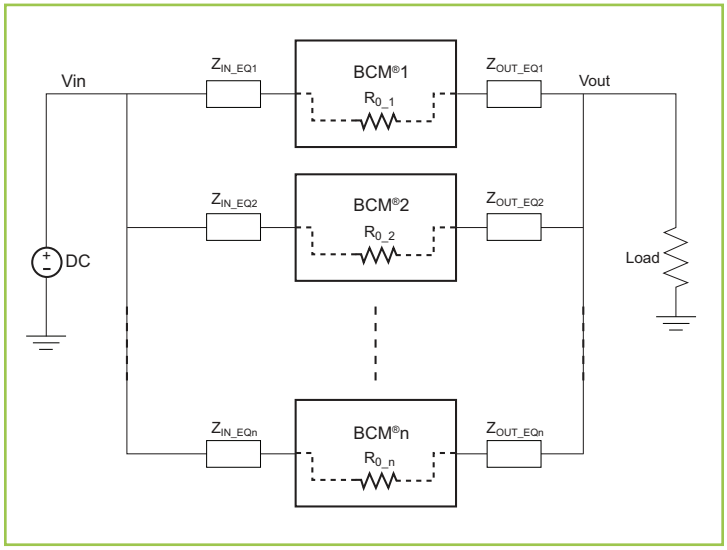


Figure 16 — *BCM module array*

13.0 FUSE SELECTION

In order to provide flexibility in configuring power systems VI Chip® modules are not internally fused. Input line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than maximum current of BCM module)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: <= 10A Littlefuse Nano^2 Fuse.

14.0 REVERSE OPERATION

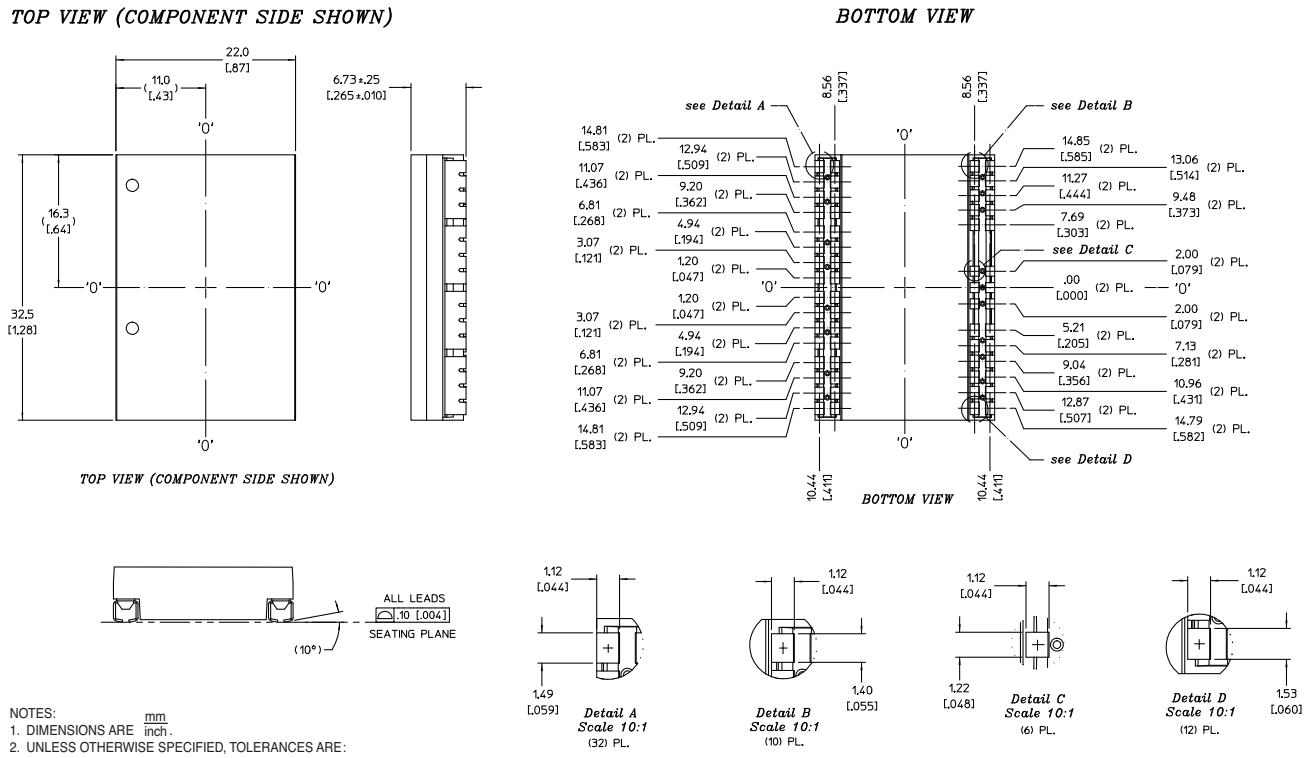
BCM® modules are capable of reverse power operation. Once the unit is started, energy will be transferred from secondary back to the primary whenever the secondary voltage exceeds VIN • K. The module will continue operation in this fashion for as long as no faults occur.

The B048x160y24A has not been qualified for continuous operation in a reverse power condition. Furthermore fault protections which help protect the module in forward operation will not fully protect the module in reverse operation.

Transient operation in reverse is expected in cases where there is significant energy storage on the output and transient voltages appear on the input. Transient reverse power operation of less than 10 ms, 10% duty cycle is permitted and has been qualified to cover these cases.

15.1 J-LEAD PACKAGE MECHANICAL DRAWING

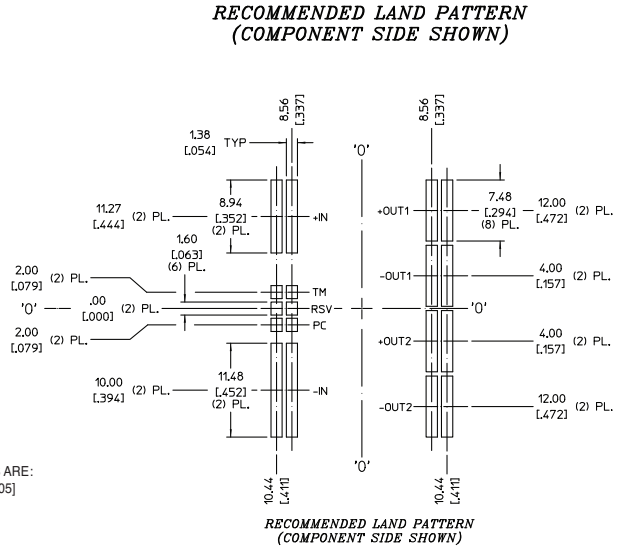
mm
(inch)



NOTES:
1. DIMENSIONS ARE mm / inch.
2. UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
   .X / [.XX] = +/-0.25 / [.01]; .XX / [.XXX] = +/-0.13 / [.005]
3. PRODUCT MARKING ON TOP SURFACE

DXF and PDF files are available on vicorpower.com

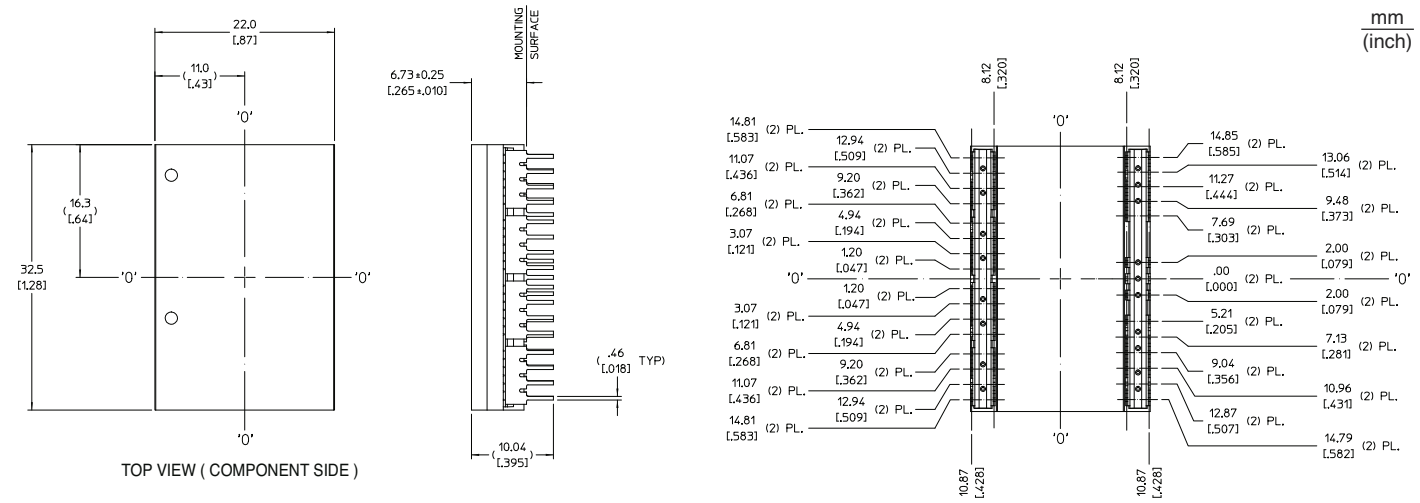
15.2 J-LEAD PACKAGE RECOMMENDED LAND PATTERN



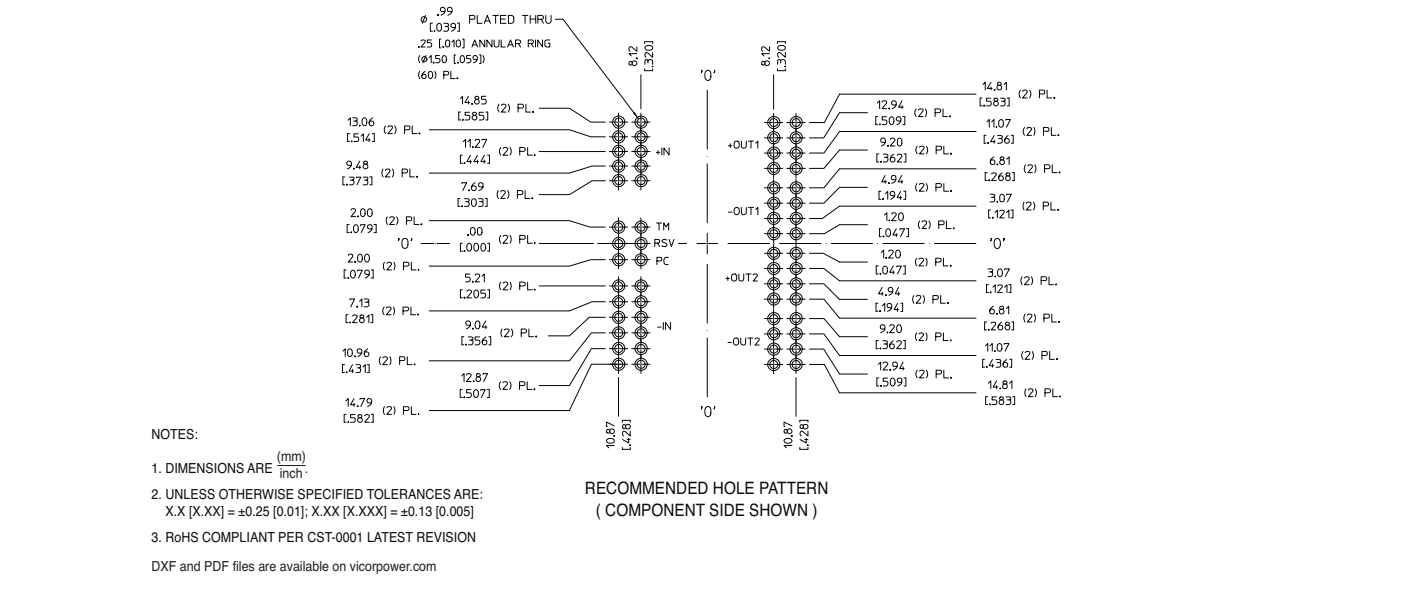
NOTES:
1. DIMENSIONS ARE mm / inch.
2. UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
   .X / [.XX] = +/-0.25 / [.01]; .XX / [.XXX] = +/-0.13 / [.005]
3. PRODUCT MARKING ON TOP SURFACE

DXF and PDF files are available on vicorpower.com

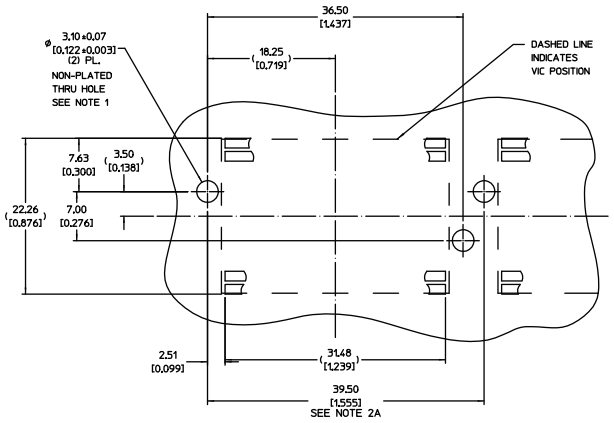
15.3 THROUGH-HOLE PACKAGE MECHANICAL DRAWING



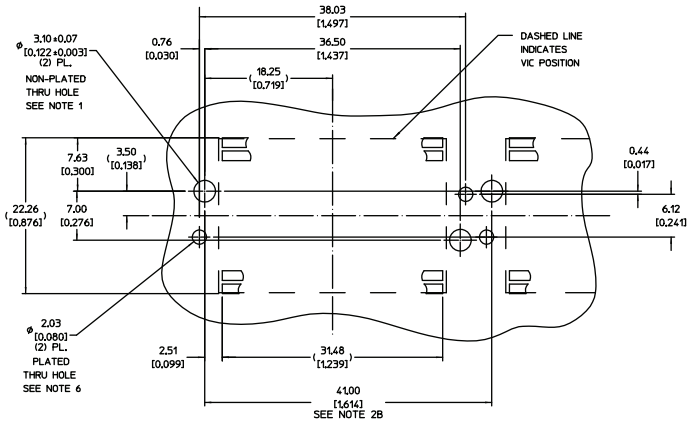
15.4 THROUGH-HOLE PACKAGE RECOMMENDED LAND PATTERN



15.5 RECOMMENDED HEAT SINK PUSH PIN LOCATION



(NO GROUNDING CLIPS)

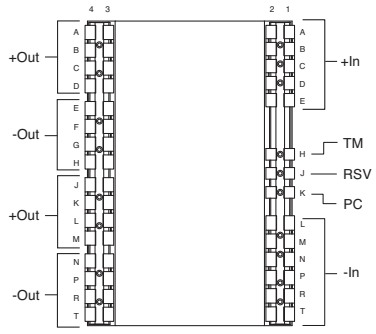


(WITH GROUNDING CLIPS)

Notes:

1. Maintain 3.50 (0.138) Dia. keep-out zone free of copper, all PCB layers.
2. (A) Minimum recommended pitch is 39.50 (1.555). This provides 7.00 (0.275) component edge-to-edge spacing, and 0.50 (0.020) clearance between Vicor heat sinks.
   (B) Minimum recommended pitch is 41.00 (1.614). This provides 8.50 (0.334) component edge-to-edge spacing, and 2.00 (0.079) clearance between Vicor heat sinks.
3. VI Chip® module land pattern shown for reference only; actual land pattern may differ. Dimensions from edges of land pattern to push–pin holes will be the same for all full-size VI Chip® products.
4. RoHS compliant per CST–0001 latest revision.
5. Unless otherwise specified: Dimensions are mm (inches) tolerances are: x.x (x.xx) = ±0.3 (0.01) x.xx (x.xxx) = ±0.13 (0.005)
6. Plated through holes for grounding clips (33855) shown for reference, heat sink orientation and device pitch will dictate final grounding solution.

15.6 BCM MODULE PIN CONFIGURATION



Bottom View

Signal Name	Designation
+In	A1-E1, A2-E2
–In	L1-T1, L2-T2
TM	H1, H2
RSV	J1, J2
PC	K1, K2
+Out	A3-D3, A4-D4, J3-M3, J4-M4
–Out	E3-H3, E4-H4, N3-T3, N4-T4

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