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To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

RENESAS

HAT2173H

Silicon N Channel Power MOS FET
Power Switching

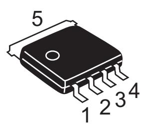
REJ03G0030-0200
Rev.2.00
Sep 26, 2005

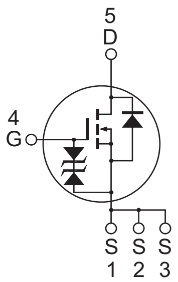
Features

- High speed switching
- Capable of 8 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 12 mΩ typ. (at V_{GS} = 10 V)

Outline

RENESAS Package code: PTZZ0005DA-A)
(Package name: LFPAK)





1, 2, 3 Source
4 Gate
5 Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$ Note1	100	A
Body-drain diode reverse drain current	I_{DR}	25	A
Avalanche current	I_{AP} Note 2	25	A
Avalanche energy	E_{AR} Note 2	62.5	mJ
Channel dissipation	Pch Note3	30	W
Channel to Case Thermal Resistance	θch-C	4.17	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. Tc = 25°C

Electrical Characteristics

(Ta = 25°C)

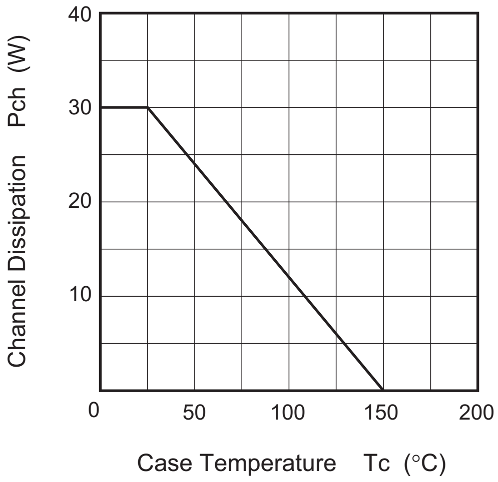
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 100 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	4.0	—	6.0	V	V_{DS} = 10 V, I_D = 20 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	12	15	mΩ	I_D = 12.5 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	13	17.5	mΩ	I_D = 12.5 A, V_{GS} = 8 V Note4
Forward transfer admittance	$\|y_{fs}\|$	27	45	—	S	I_D = 12.5 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	4350	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	520	—	pF	
Reverse transfer capacitance	Crss	—	150	—	pF	
Gate resistance	Rg	—	0.5	—	Ω	
Total gate charge	Qg	—	61	—	nC	V_{DD} = 50 V, V_{GS} = 10 V, I_D = 25 A
Gate to source charge	Qgs	—	23	—	nC	
Gate to drain charge	Qgd	—	14.5	—	nC	
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	V_{GS} = 10 V, I_D = 12.5 A, V_{DD} ≅ 30 V, R_L = 2.4 Ω, Rg = 4.7 Ω
Rise time	t_r	—	15	—	ns	
Turn-off delay time	$t_{d(off)}$	—	37	—	ns	
Fall time	t_f	—	5.7	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.82	1.07	V	IF = 25 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	55	—	ns	IF = 25 A, V_{GS} = 0, di_F/ dt = 100 A/ µs

Notes: 4. Pulse test

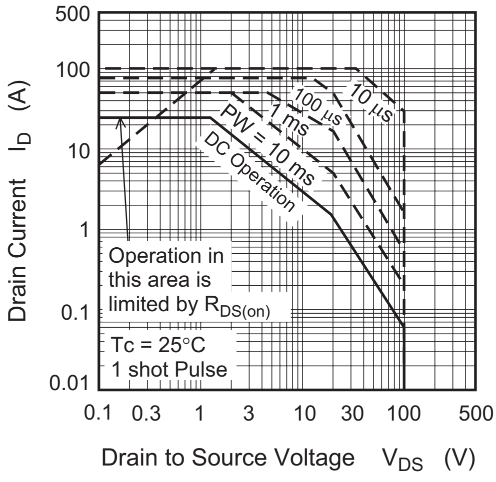
RENESAS

Main Characteristics

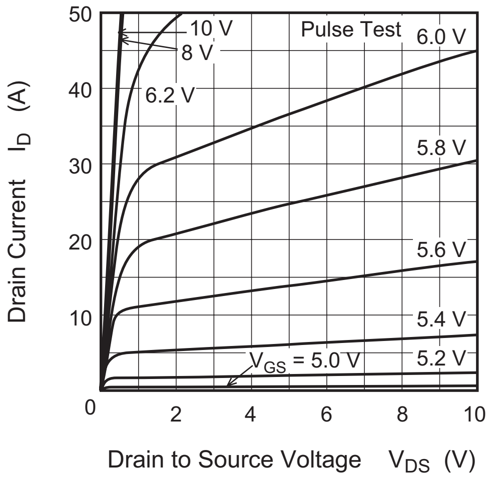
Power vs. Temperature Derating



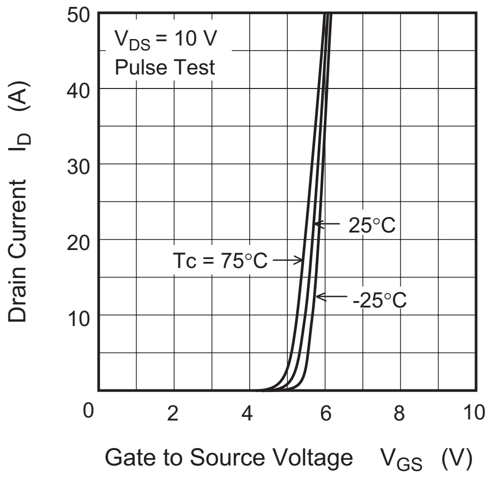
Maximum Safe Operation Area



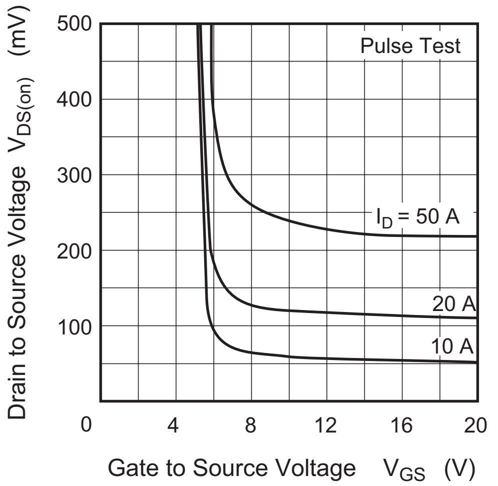
Typical Output Characteristics



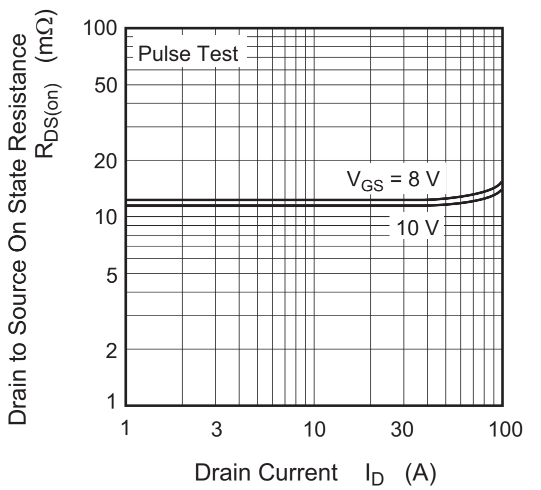
Typical Transfer Characteristics

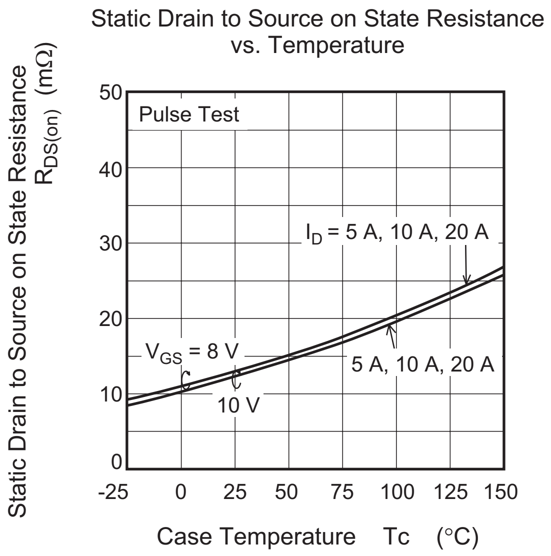


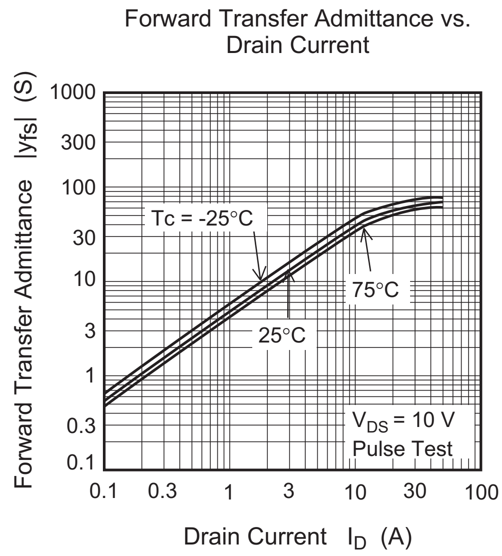
Drain to Source Saturation Voltage vs. Gate to Source Voltage

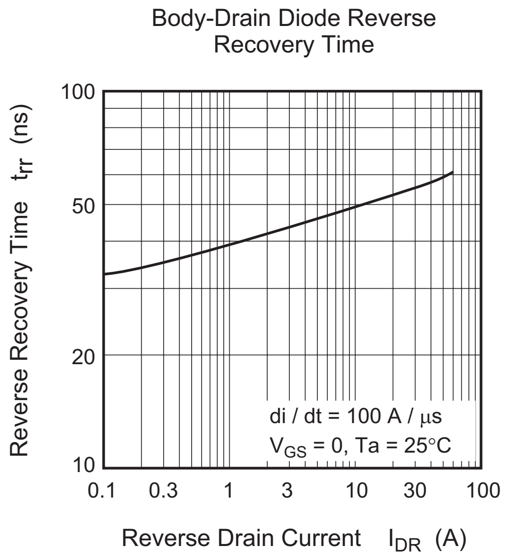


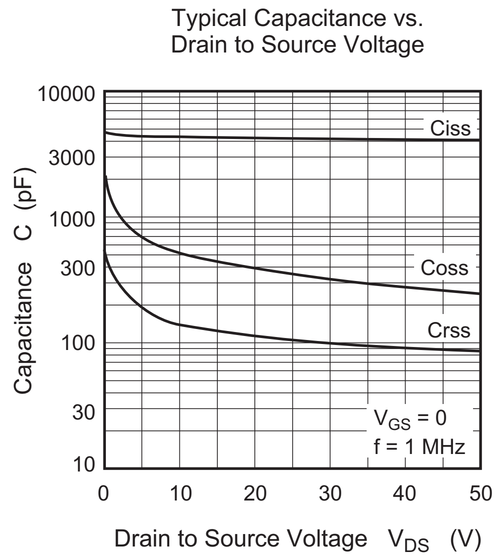
Static Drain to Source on State Resistance vs. Drain Current

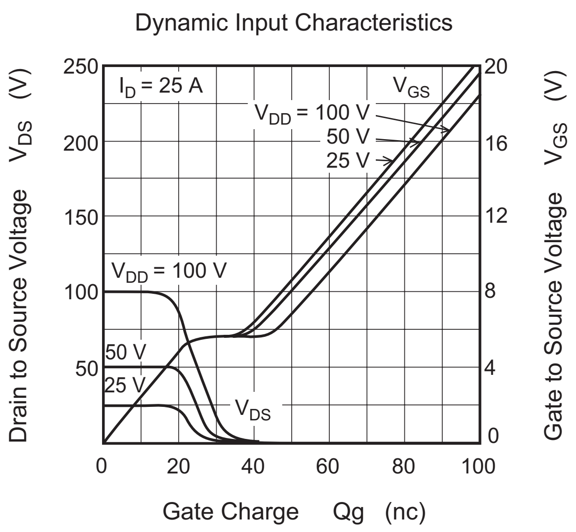


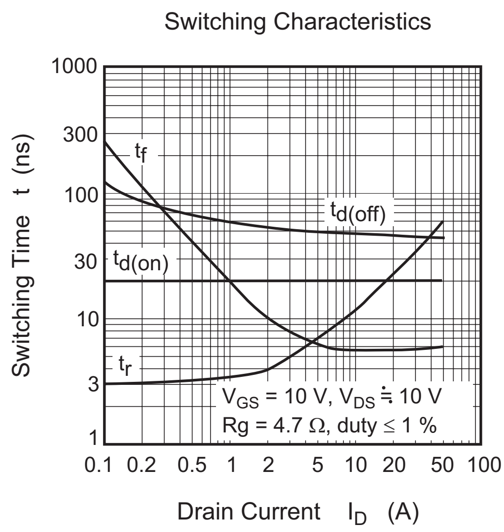

Static Drain to Source on State Resistance
vs. Temperature
Static Drain to Source on State Resistance
RDS(on) (mΩ)
Pulse Test
ID = 5 A, 10 A, 20 A
VGS = 8 V
10 V
5 A, 10 A, 20 A
Case Temperature Tc (°C)


Forward Transfer Admittance vs.
Drain Current
Forward Transfer Admittance |yfs| (S)
Tc = -25°C
75°C
25°C
VDS = 10 V
Pulse Test
Drain Current ID (A)

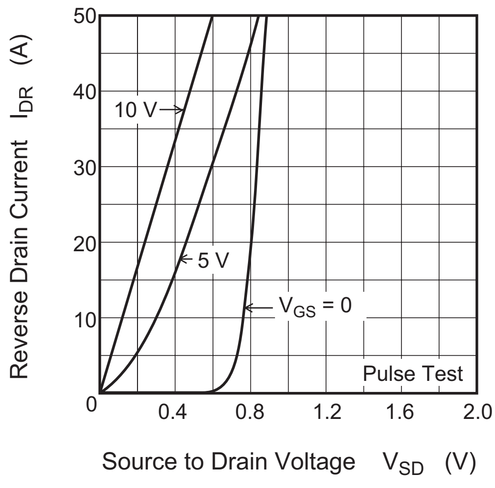

Body-Drain Diode Reverse
Recovery Time
Reverse Recovery Time trr (ns)
di / dt = 100 A / μs
VGS = 0, Ta = 25°C
Reverse Drain Current IDR (A)


Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Drain to Source Voltage VDS (V)

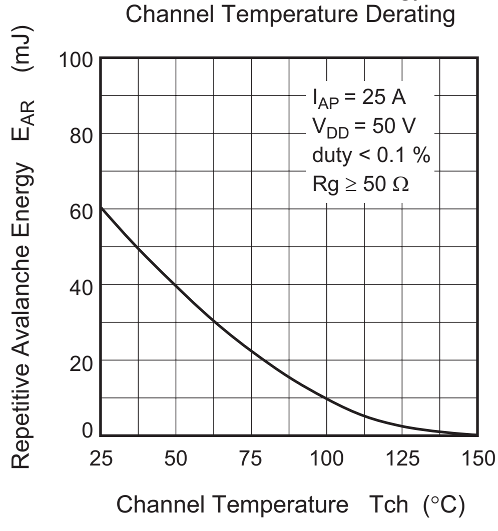

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
ID = 25 A
VGS
VDD = 100 V
50 V
25 V
VDD = 100 V
50 V
25 V
VDS
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
tf
td(off)
td(on)
tr
VGS = 10 V, VDS ≒ 10 V
Rg = 4.7 Ω, duty ≤ 1 %
Drain Current ID (A)

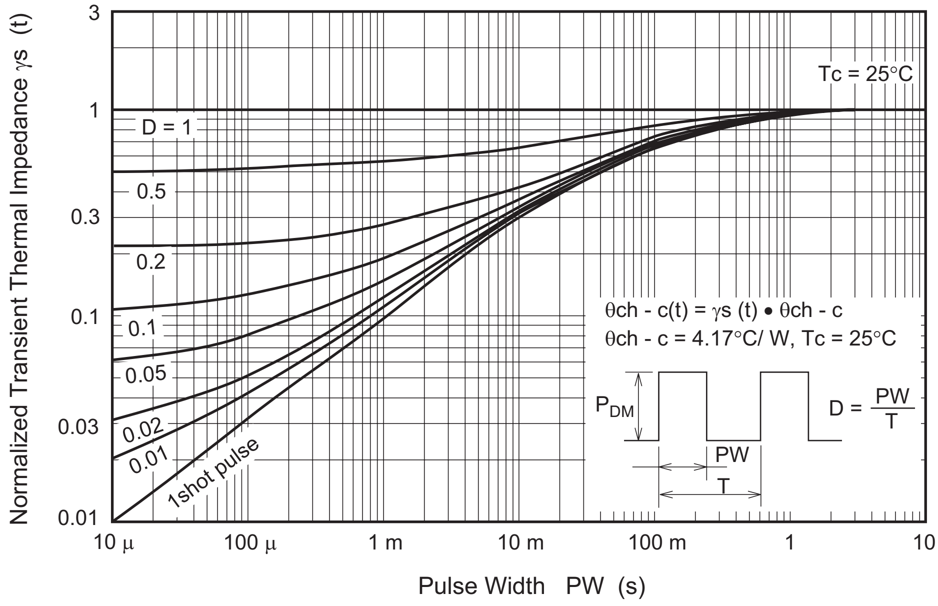
Reverse Drain Current vs.
Source to Drain Voltage



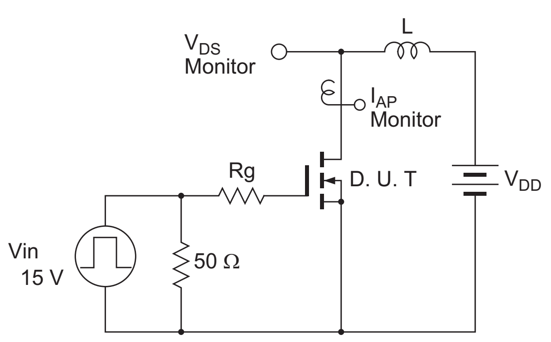
Maximum Avalanche Energy vs.
Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

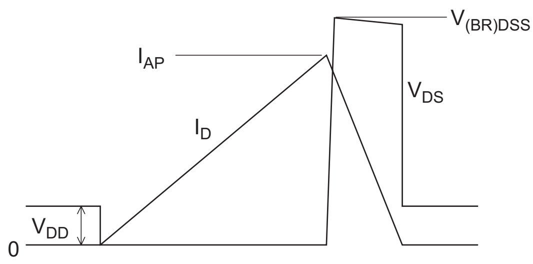


Avalanche Test Circuit

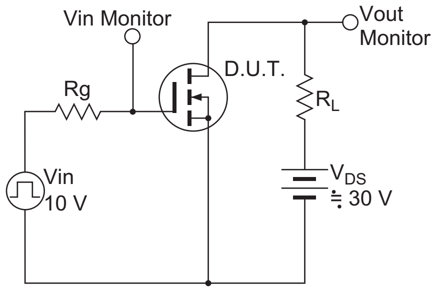


Avalanche Waveform

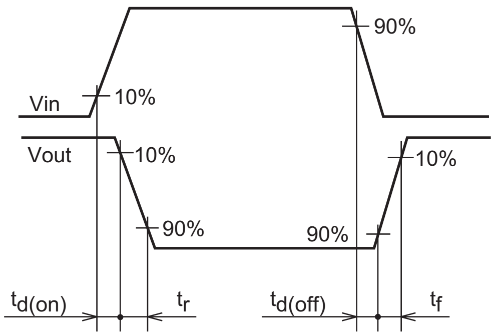
$$E_{AR} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



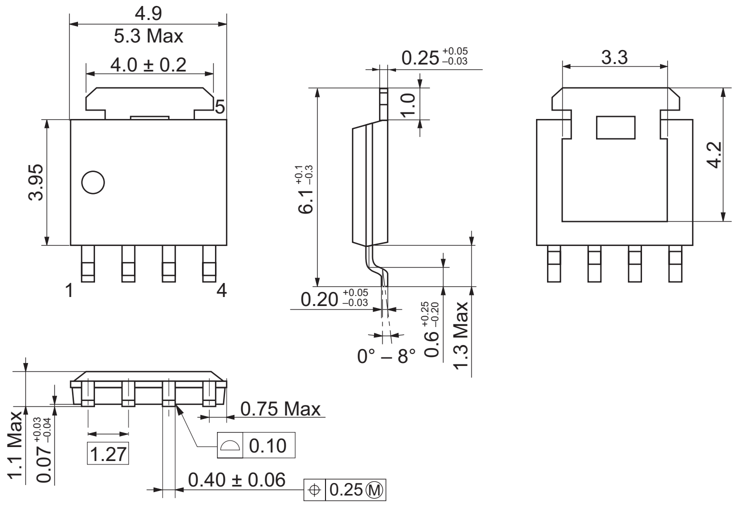
Switching Time Waveform



Package Dimensions

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
SC-100	PTZZ0005DA-A	LFPAK	0.080g

Unit: mm



(Ni/Pd/Au plating)

Ordering Information

Part Name	Quantity	Shipping Container
HAT2173H-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

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