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Complementary wireless module WLAN / BT

Standard Laminate SiP Module

Series/Type:	**R078 (WL1837) / D7020**
Ordering code:	**B30931D7020Y918**
Date:	2014-12-9
Version:	1.3

1. Overview

This document details the specifications and features of R078 (WL1837) / D7020 SiP module. The R078 (WL1837) / D7020 SiP module is based on Texas Instruments WL1837 IC, specifically WL183x Data Sheet version 1.4, such that the SiP module specification is subject to any subsequent changes in applicable Texas Instruments documentation and software.

The R078 (WL1837) / D7020 contains the WL1837 SoC, 2.4GHz and 5 GHz SPDT switches, 2.4GHz and 5GHz band pass filters / diplexer and necessary passive components for WLAN and BT in a highly integrated solution.

1.1 Features

- WLAN, BT, BLE on a single chip provide universal connectivity in small PCB footprint.
- Provides efficient direct connection to battery by employing several integrated switched mode power supplies (DC2DC).
- Based on 45nm CMOS technology using proven core technology.
- Seamless integration with TI OMAP™ Application Processors.
- WLAN and Bluetooth cores software and hardware are compatible with prior WL127x and WL128x offerings, for smooth migration to Device.
- Shared HCI transport for BT/BLE over UART and SDIO for WLAN.
- Downloadable patches and firmware enables new features to be added for all functional block's.
- Temperature detection and compensation mechanism ensures minimal variation in the RF performance over the entire temperature range.
- Bluetooth 4.0, BLE and all audio processing features work in parallel and include full coexistence with WLAN

1.2 Applications

Mobile phone and mobile computer device applications.

1.3 General Description

The R078 (WL1837) / D7020 is a highly integrated WLAN, BT, BLE device that forms a complete standalone communication system. The WL1837 is a highly integrated single-chip CMOS (45-nm process) incorporates the core functionality of the WL1271/3 and WL1281/3 devices.

The device is the 8th-generation WLAN/BT/BLE devices from Texas Instruments. As such, the WL1837 is based upon proven core technology and complements the TI integrated devices for connectivity portfolio.

R078 (WL1837) / D7020 is ideal for use in mobile phone and mobile computer device applications due to its low current, small area and cellular phone coexistence-friendly features.

1.4 Terms and abbreviations

BPF – Band-Pass Filter
BT – Bluetooth
FE – Front-End (refers to FE IC and BPF)
GND – Ground
HCI – Host Controller Interface
IC – Integrated Circuit
I/O – Input/Output interfaces
LDO – Low Drop-Out (voltage regulator)
PCB – Printed Circuit Board
Q – Quality factor
RF – Radio Frequency
RX – Receive
SiP – System in Package
SoC – System on Chip
TX – Transmit
Vbat – Battery Voltage
VIO – external pre-existing 1.8V IO power supply
WLAN – Wireless Local Area Network

1.5 Reference documents

- Texas Instruments WL183x_Data_Manual_Rev_1_4.pdf

2 Functional Block Features

2.1 Functional Block Diagram

Figure 2-1 shows a high-level view of R078 (WL1837) / D7020 along with its various configurations.

The flexibility of the R078 (WL1837) / D7020 based on WL1837 enables easy integration with various host-system topologies.

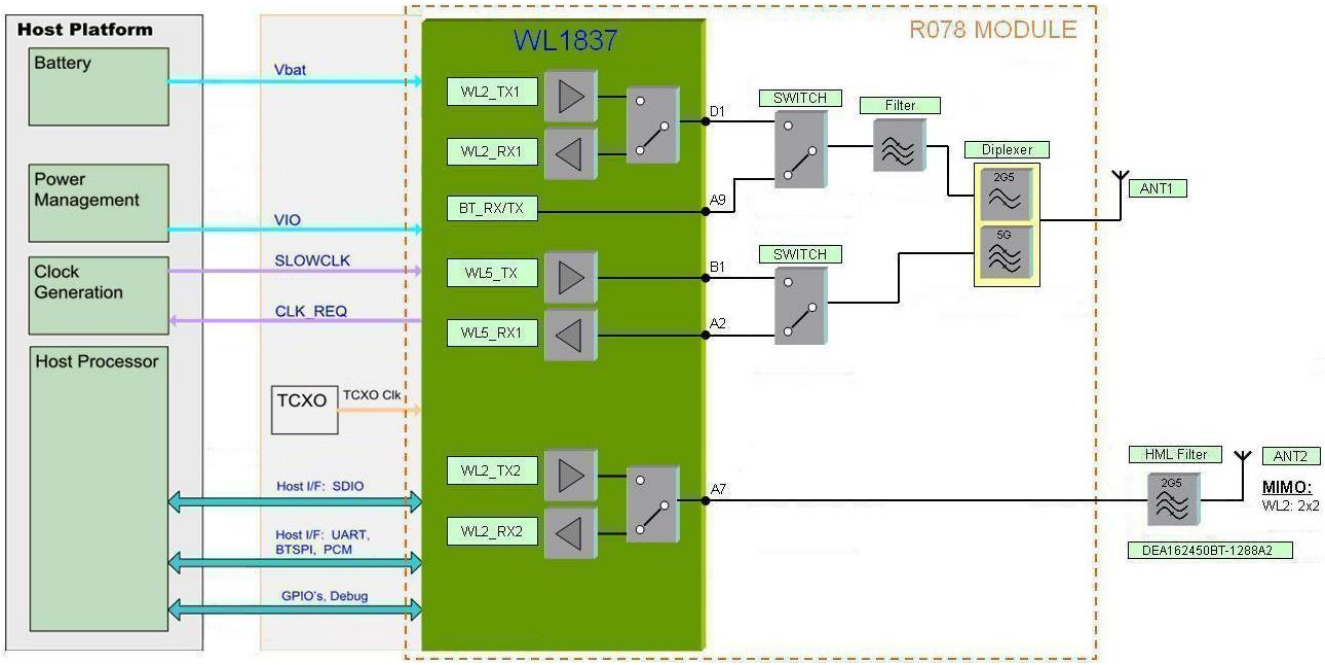

Figure 2-1 High-Level System Diagram

2.2 WLAN Features

- Integrated 2.4 & 5GHz power amplifiers for complete WLAN solution
- WLAN MAC Baseband Processor and RF transceiver - IEEE802.11a/b/g/n compliant
- WLAN 2.4 / 5 GHz SISO (20 / 40 MHz channels), 2.4 GHz MIMO (20 MHz channels).
- Baseband Processor
  - IEEE Std 802.11a/b/g data rates and IEEE Std 802.11n data rates with 20 or 40 MHz SISO and 20 MHz MIMO.
- Fully calibrated system. No production calibration required.
- Medium-Access Controller (MAC)
  - Embedded ARM™ Central Processing Unit (CPU)
  - Hardware-Based Encryption/Decryption Using 64-, 128-, and 256-Bit WEP, TKIP or AES Keys,
  - Supports requirements for Wi-Fi Protected Access (WPA and WPA2.0) and IEEE Std 802.11i [Includes Hardware-Accelerated Advanced-Encryption Standard (AES)]
  - Designed to work with IEEE Std 802.1x
- New advanced co-existence scheme with BT/BLE
- 2.4/5.0 GHz Radio
  - Internal LNA, PA and RF switch
  - Supports: IEEE Std 802.11a, 802.11b, 802.11g and 802.11n
- Supports 4 bit SDIO host interface, including high speed (HS) and V3 modes

2.3 Bluetooth Features

- Supports Bluetooth 4.0 BLE
- Includes concurrent operation and built-in coexistence and prioritization handling of BT, BLE, audio processing and WLAN
- Dedicated Audio processor supporting on chip SBC encoding + A2DP:
  - Assisted A2DP (A3DP) support - SBC Encoding implemented internally
  - Assisted WB-Speech (AWBS) support - modified SBC codec implemented internally

2.4 BLE Features

- Fully compliant with BT4.0 BLE dual mode standard
- Support for all roles and role-combinations, mandatory as well as optional
- Supports up to 10BLE connection
- Independent buffering for LE allows having large number of multiple connections without affecting BR/EDR performance

3 Detailed Description

3.1 Host Interfaces

3.1.1 Device Host Interface Options

The following table summarizes the Host Controller interface options. All interfaces operate independently.

Table 3-1 Host Controller Interface options

WLAN	Shared HCI for BT	BT Voice/Audio
WLAN HS SDIO	Over UART	BT PCM

The Device incorporates UART module dedicated to the BT shared-transport Host Controller Interface (HCI) transport layer. The HCI interface is used to transport commands, events, and ACL between the Bluetooth device and its host using HCI data packets.

This acts as a shared transport for BT/BLE functional blocks.

3.1.2 WLAN SDIO Transport Layer

The SDIO is the host interface for WLAN. The interface between the host and the D7020 uses an SDIO interface and supports a maximum clock rate of 50MHz.

The Device SDIO also supports the following features of the SDIO V3 specification:

- 4 bit data bus
- Synchronous and Asynchronous In-Band-Interrupt
- Default and High-Speed (50MHz) timing
- Sleep/wake commands

SDIO timing specifications are given in specification section at end of document.

3.1.3 HCI UART Shared Transport Layers for BT

The HCI UART supports most baud rates (including all PC rates) for all fast clock frequencies - up to maximum of 4 Mbps. After power up the baud rate is set for 115.2 kbps, irrespective of fast clock frequency. The baud rate can then be changed by using a VS command. The Device responds with a Command Complete Event (still at 115.2 kbps), after which the baud rate change takes place.

HCI hardware includes the following features:

- Receiver detection of break, idle, framing, FIFO overflow, and parity error conditions.
- Transmitter underflow detection.
- CTS/RTS hardware flow control.
- 4 wire (H4)

Parameter	Value
Bit rate	*115.2 kbps*
Data length	8 bits
Stop bit	1
Parity	None

Table 3-2 UART Default Setting

3.1.3.1 UART 4 Wire Interface - H4

The interface includes four signals: TXD, RXD, CTS and RTS. Flow control between the host and the Device is byte-wise by hardware.

Flow control is obtained by the following:

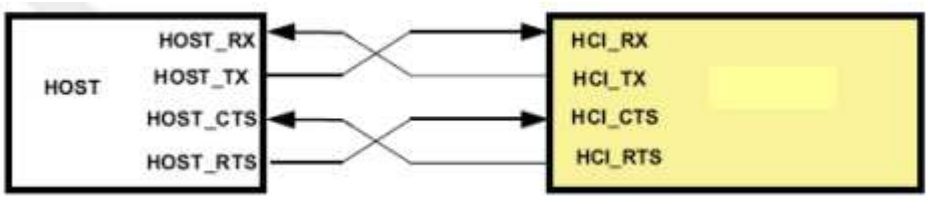

Figure 3-1 HCI UART Connection

When the RX buffer of the Device passes the “flow control” threshold, it will set the HCI_RTS signal high to stop transmission from the host.

When the CTS signal is set high, the Device will stop its transmission on the interface. In case CTS is set high in the middle of transmitting a byte, the Device will finish transmitting the byte and stop the transmission.

3.1.3.2 BT function Firmware Low Power Mode Protocols

The Device includes a mechanism that handles the transition between operating mode and deep sleep low-power mode. The protocol is done via the UART and is known as eHCILL (enhanced HCI Low Level) power management protocol.

This protocol is backward compatible with the TI BT HCILL Protocol, so a Host that implements the HCILL does not need to change anything in order to work with the Device. The "Enhanced" portion of the HCILL introduces changes that allow a simpler host implementation of this protocol. See SWRA288 eHCILL Four-Wire Power Management Protocol.

3.1.4 BT Audio CODEC Interface

3.1.4.1 Overview

The CODEC interface is a fully dedicated programmable serial port, supporting the following:

- Two voice channels
- Master / slave modes
- Coding schemes: u-Law, A-Law, Linear, Transparent and SBC (for Assisted WBS operation)
- Long & short frames
- Different data sizes, order and positions
- Enlarged interface options to support a wider variety of Codecs

3.1.4.2 PCM Hardware Interface

The PCM interface is one implementation of the codec interface. It contains the following four lines:

- Clock--configurable direction (input or output)
- Frame Sync--configurable direction (input or output)
- Data In--Input
- Data Out--Output/Tri state

The Device can be either the master of the interface where it generates the clock and the frame-sync signals, or slave where it receives these two signals. The PCM interface is fully configured by means of a VS command.

For slave mode, clock input frequencies between 64KHz and 12 MHz are supported..

For master mode, the Device can generate any clock frequency between 64 kHz and 6 MHz.

3.1.4.3 PCM Data Format

The data format is fully configurable:

- The data length can be from 8 to 320 bits, in 1 bit increments, when working with two channels, or up to 640 bits when using 1 channel. The data length can be set independently for each channel.
- The data position within a frame is also configurable with 1-clock (bit) resolution, and can be set independently (relative to the edge of the Frame Sync signal) for each channel.
- The Data_IN and Data_OUT bit order can be configured independently. For example; Data_IN can start with MSB while Data_OUT starts with LSB. Each channel is separately configurable. The inverse bit order (i.e. LSB first) is supported only for sample sizes up to 24 bits.
- The data in and data out size do not necessarily have to be the same length.
- The Data_OUT line is configured as a „high-Z" output between data words. Data_OUT can also be set for permanent high-Z, irrespective of data out. This allows the Device to be a bus slave in a multi-slave PCM environment. At power up, Data_OUT is configured as high-Z.

3.1.4.4 PCM Frame-Idle Period

The CODEC interface has the capability for frame-idle periods, where the PCM clock can “take a break” and become ‘0’ at the end of the PCM frame, after all data has been transferred.

The Device supports frame-idle periods both as master and slave of the PCM bus.

When Device is the master of the interface, the frame-idle period is configurable. There are 2 configurable parameters:

- Clk_Idle_Start - Indicates the number of PCM clock cycles from the beginning of the frame till the beginning of the idle period. After Clk_Idle_Start clock cycles, the clock becomes ‘0’.
- Clk_Idle_End - Indicates the time from the beginning of the frame till the end of the idle period. This time is given in multiples of PCM clock periods.

The delta between Clk_Idle_Start and Clk_Idle_End is the clock idle period.

e.g. For PCM clock rate = 1 MHz, frame sync period = 10 kHz, Clk_Idle_Start = 60, Clk_Idle_End = 90. Between each two-frame sync there are 70 clock cycles (instead of 100). The clock idle period starts 60 clock cycles after the beginning of the frame and lasts 90-60=30 clock cycles. This means that the idle period ends 100-90=10 clock cycles before the end of the frame. The data transmission must end prior to the beginning of the idle period.

3.1.5 Two Channel PCM Bus Example

In the following figure, a 2-channel PCM bus is shown where the two channels have different word sizes and arbitrary positions in the bus' frame. (FT stands for Frame Timer).

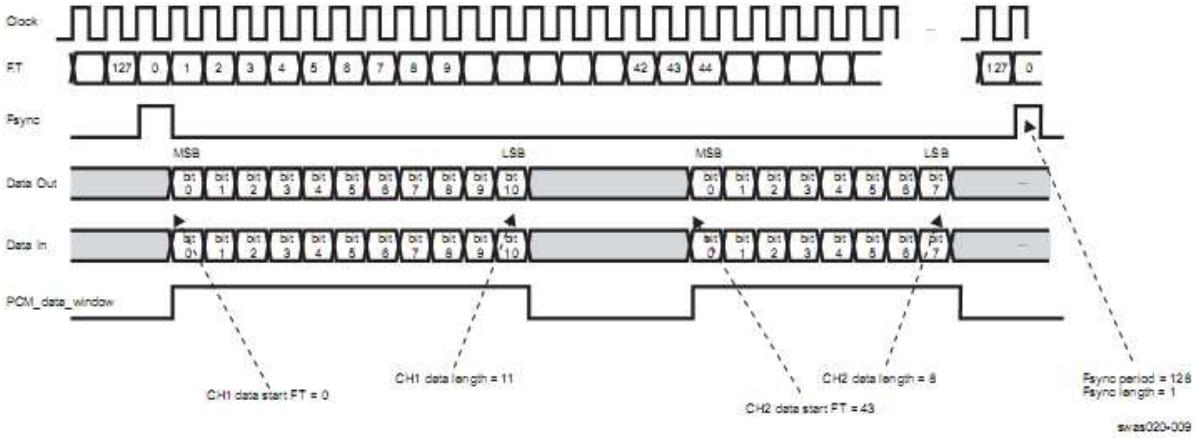

Figure 3-2 2 Channels PCM Bus Timing

3.1.6 PCM Audio Encoding

The Device CODEC interface can use one of four audio coding patterns:

- A-Law (8-bit)
- µ-Law (8-bit)
- Linear (8 or 16-bit)
- SBC (16-bit)

Two BT voice channels are not supported when SBC encoding is selected.

3.1.6.1 BT PCM Clock Mismatch Handling

In BT RX, the Device receives RF voice packets and writes these to the CODEC I/F. If the Device receives data faster than the CODEC I/F output allows, an overflow occurs. In this case, the Device BT function has 2 possible behavior modes: "allow overflow" and "don't allow overflow".

- If overflow is allowed, the Device BT function continues receiving data and overwrites any data not yet sent to the CODEC.
- If overflow is not allowed, RF voice packets received when buffer is full, are discarded.

When the Bluetooth functional block is master on the PCM and slave on the Bluetooth network, the Bluetooth functional block can measure the drift between the two clocks and apply compensation to the PCM clock in order to avoid underrun and overrun scenarios

3.1.6.2 BT Inter-IC Sound (BT I2S over PCM bus)

The Device can be configured as an Inter-IC Sound (I2S) serial interface to a I2S CODEC device. In this mode, the Device audio CODEC interface is configured as a bi-directional, full duplex interface, with two time slots per frame: Time slot 0 is used for the left channel audio data and time slot 1 for the right channel audio data. Each time slot is configurable up to 40 serial clock cycles in length and the frame is configurable up to 80 serial clock cycles in length.

3.2 Clocks and Power Management

3.2.1 Slow Clock / RTC clock

The slow clock is a free-running clock of 32.768 KHz which is supplied from an external clock source. It is connected to the RTC_CLK pin and is a digital square-wave signal in the range of 0-1.8V nom.

3.2.2 Fast Clock System

3.2.2.1 Fast clock using external crystal

The devices incorporate an internal crystal oscillator circuit for supporting a cost optimized crystal based fast clock scheme. Connection is as shown:

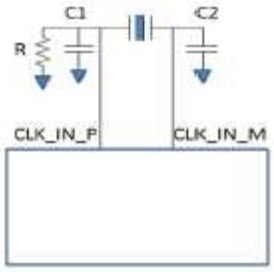

Figure 3-3 XTAL Connection

C1 = C2. Typically 8 - 22pF. Refer to Crystal manufacturer's recommendations.
R = 390K ohm (+/- 5% tolerance).

NOTE : this arrangement does not support 5GHz band functions.

3.2.2.2 Fast Clock using external oscillator

CLK_IN_P is the main system fast clock and must meet the specifications as described in "Fast clock specifications" at the end of this document.

The clock must be one of the specified frequencies and the device incorporates an internal mechanism to detect this. The clock can be AC or DC coupled, sine or square wave.

Crystal operation is supported as shown:

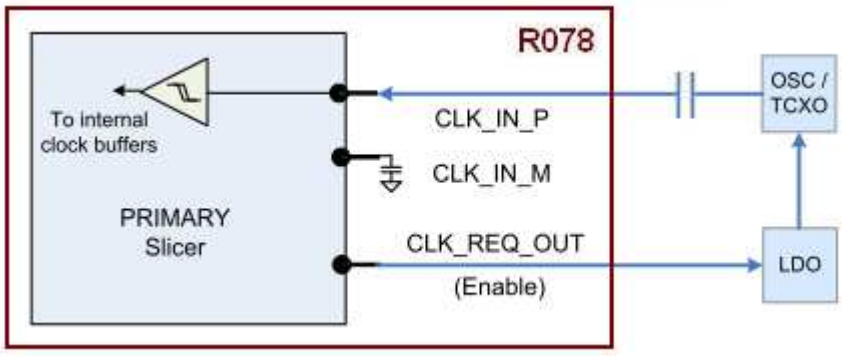

Figure 3-4 Fast Clock Block Diagram

3.2.3 Power Management

3.2.3.1 Block Diagram - internal DC2DC's

The Device incorporates three internal DC2DC's (switched-mode power supplies) to provide efficient internal and external supplies, derived from Vbat.

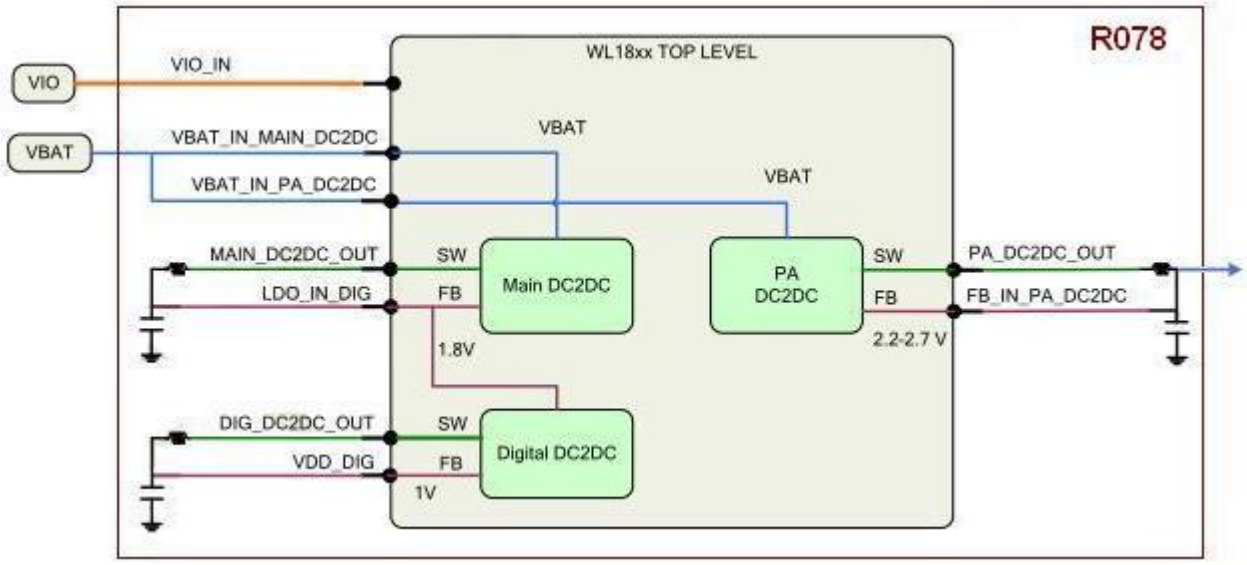

Figure 3-5 Internal DC2DC's

3.2.4 Reset / Power up system

After Vbat and VIO are fed to Device and while BT_EN, WLAN_EN are de-asserted (LOW), the device is in Shutdown state.

While in Shutdown state all functional blocks, internal DC2DC's and LDO's will be disabled. The power supplied to the functional blocks is cut off.

When one of the two signals BT_EN or WLAN_EN are asserted (High) a Power On Reset (POR) is performed.

Stable Slow Clock, VIO and Vbat are pre-requisites for successful POR.

3.2.4.1 Chip Top-level Power Up Sequence

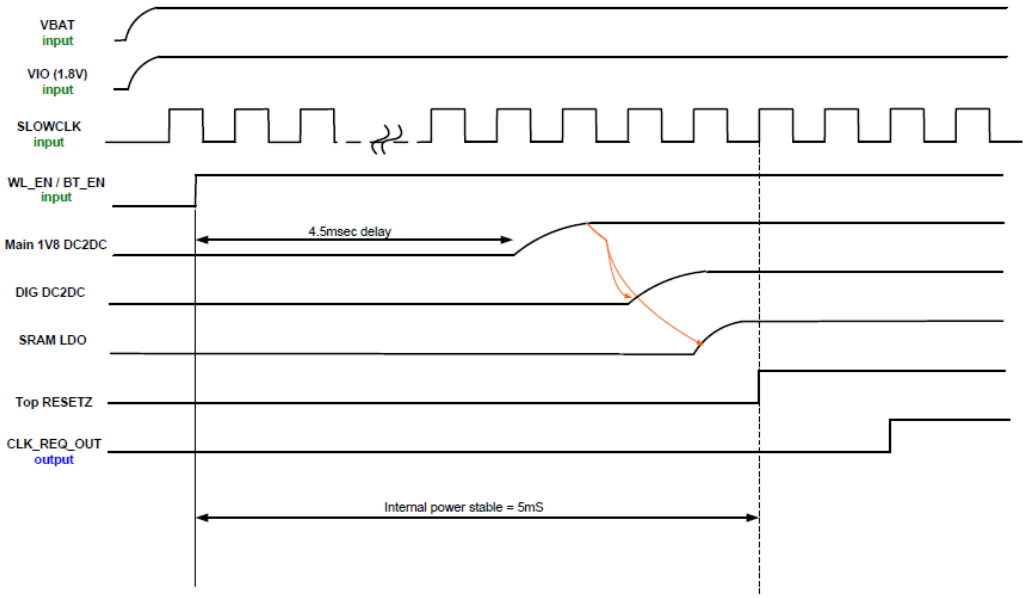

Figure 3-6 Chip Top-level Power Up Sequence

3.2.4.2 WLAN Power Up Sequence

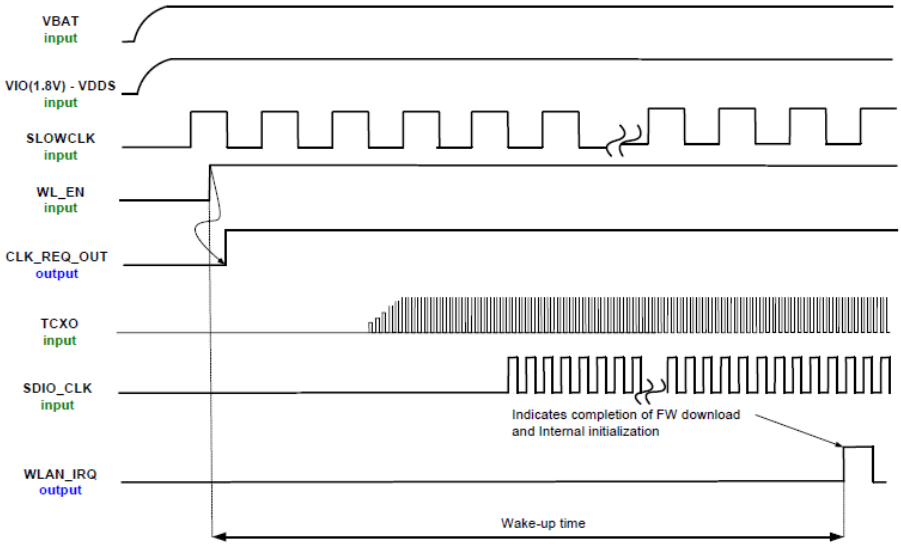

Figure 3-7 WLAN Power Up Sequence

3.2.4.3 BT/BLE Power Up Sequence

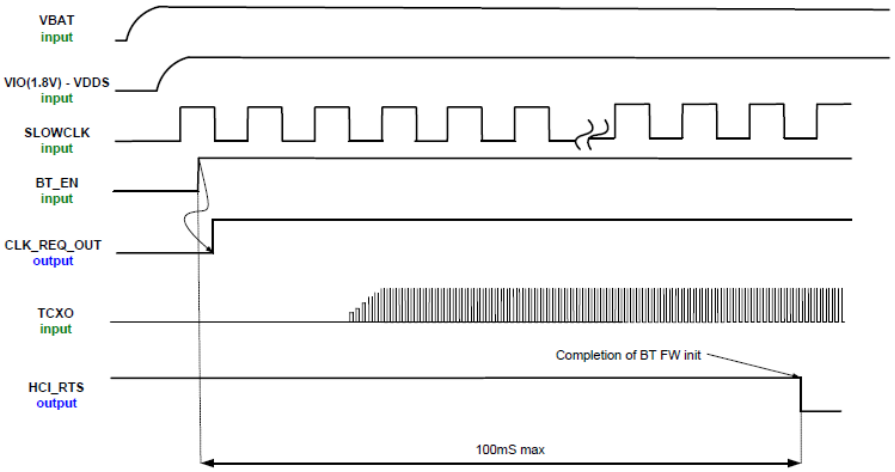

Figure 3-8 BT Power Up Sequence

3.3 WLAN Functional Block

3.3.1 WLAN MAC

R078 (WL1837) / D7020 MAC implements the IEEE standard 802.11 MAC sub-layer using both dedicated hardware and embedded firmware. The MAC hardware implements real-time functions, including access protocol management, encryption and decryption.

3.3.2 WLAN Baseband Processor

R078 (WL1837) / D7020 baseband processor implements the IEEE 802.11a/b/g/n PHY sub layers and has been optimized to perform well in conditions of high multipath and noise.

3.3.3 WLAN RF Radio

R078 (WL1837) / D7020 WLAN radio is a highly integrated radio processor designed for 802.11a/b/g/n applications, including internal front-end PA's.

3.3.4 Coexistence BT/BLE - WLAN

R078 (WL1837) / D7020 has been designed to support simultaneous operation of each of the major on-chip core functions. This operational coexistence is based on extensive frequency planning for each of the on-chip core functions, as well as a sophisticated MAC co-ordination scheme between Bluetooth and WLAN subsystems that allows operation in the same ISM frequency band.

3.3.5 WLAN RF Configuration and Power Options

The R078 (WL1837) / D7020 includes all RF switches, band pass filters and diplexer for complete WLAN (SISO) and BT RF system. Optional MIMO configuration is also supported with external band pass filter.

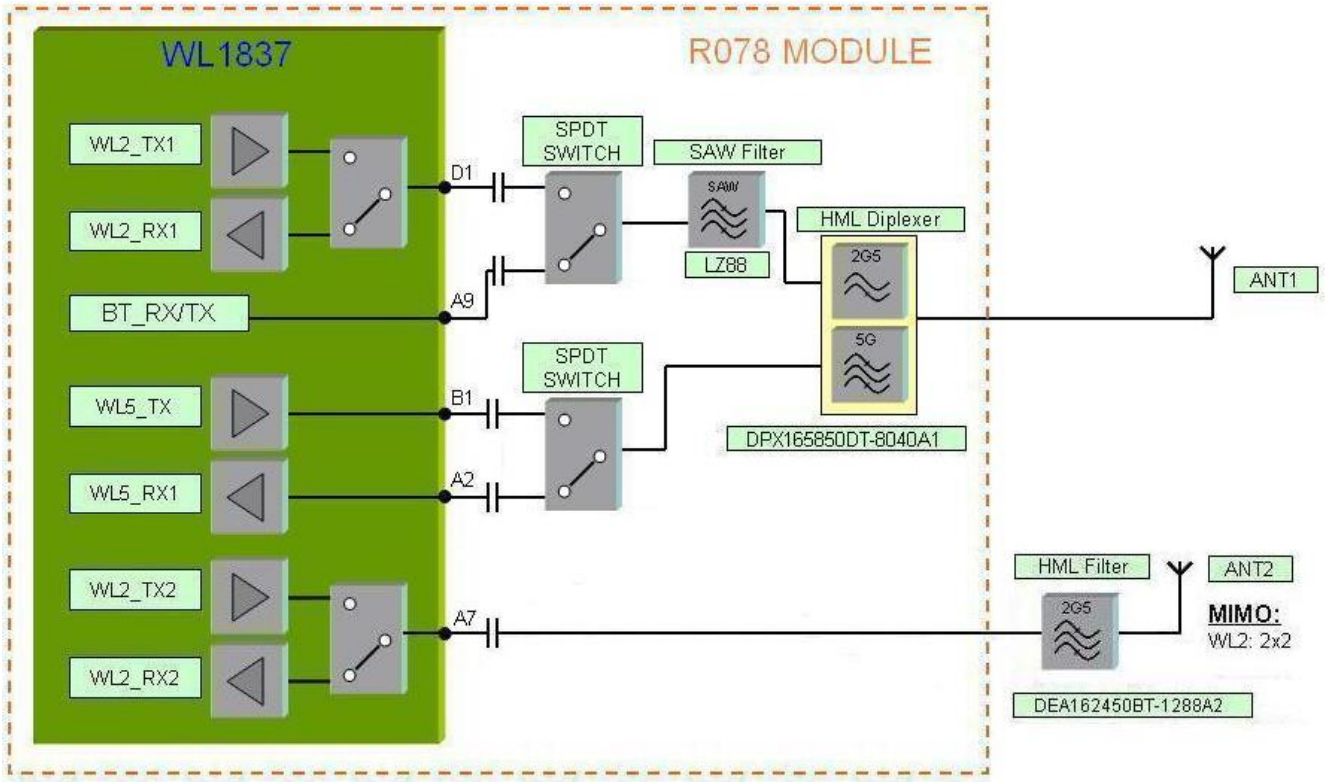

Figure 3-9 R078 (WL1837) / D7020 SISO/MIMO configuration options

3.3.5.1 MIMO and SISO options (WL1837 device)

The diagram above shows WLAN and BT pins in standard SISO application and also for optional MIMO.

Standard configuration for SISO:

- WLAN 2.4/5GHz + BT
- WLAN/BT 2.4GHz simultaneous RX/RX

Optional configuration for MIMO:

- WLAN 2.4/5GHz + BT
- WLAN/BT 2.4GHz simultaneous RX/RX
- WLAN 2.4GHz MIMO

3.4 Bluetooth Functional Block

3.4.1 BT Digital Radio Processor (DRP)

The Device uses 8th-generation TI Bluetooth technology, with new features and improved radio performance.

3.4.2 BT Receiver

The receiver uses near-zero-IF architecture to convert the RF signal to baseband data. Received signal from the external antenna is input to an internal RF switch and a differential LNA (low-noise amplifier).

This signal is then passed to a mixer which down-converts the signal to an IF, followed by a filter and amplifier. The signal is then quantized by a sigma-delta ADC. The quantized signal is further processed to reduce the interference level.

The demodulator digitally down-converts the signal to zero IF and recovers the data stream by an adaptive decision mechanism. The demodulator includes EDR processing with state-of-the-art performance. It includes a maximum-likelihood sequence estimator (MLSE) for improved performance of basic-rate BR sensitivity, and adaptive equalization to enhance EDR modulation.

3.4.3 BT Transmitter

The transmitter is based on an all-digital sigma-delta PLL with a digitally controlled oscillator (DCO) as the RF frequency clock. The modulation is achieved by directly modulating the digital PLL. The power amplifier is also digitally controlled.

For EDR modulation, the transmitter uses a Polar-Modulation technique. In this mode, in addition to the frequency modulation that controls the direct-modulated ADPLL, an amplitude control modulates the PA, using the Digital-Transmitter block. This block receives the input bit-stream and converts these signals to phase-modulated control-words. The phase-modulated digital signal is then processed to provide frequency-modulation control to the ADPLL.

3.4.4 Class 1.5 Application

Device provides on-chip support for Class 2 and Class 1.5 applications. Class 1.5 is the normal operating mode after the initialization script has been sent to the Device.

It is called Class 1.5 as Device can transmit more than 4dBm on any BT modulation.

Refer to Bluetooth RF Performance specifications at end of document for more information.

3.4.5 Advanced Audio features

The Device includes Audio and Voice Processor (AVPR) targeted for off-loading the host CPU from coding voice/audio samples when running A2DP and WBS profiles.

3.4.5.1 Assisted Wideband (WB) speech

- Encode/Decode 16kHz PCM audio samples to/from 64kbps SBC frames
- Fully compliant with the BT SIG Wideband speech profile

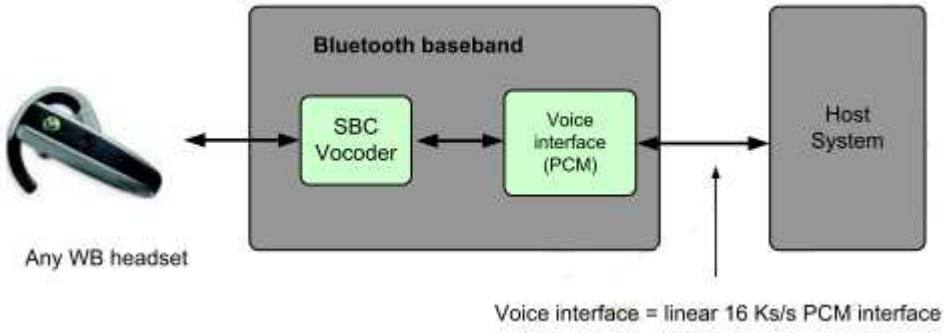

Figure 3-10 Device Wideband speech support

3.4.5.2 Assisted A2DP

- Encode 44.1/48kHz PCM audio samples to Low/Mid/High Quality A2DP stream
- Fully compliant with the BT SIG A2DP profile

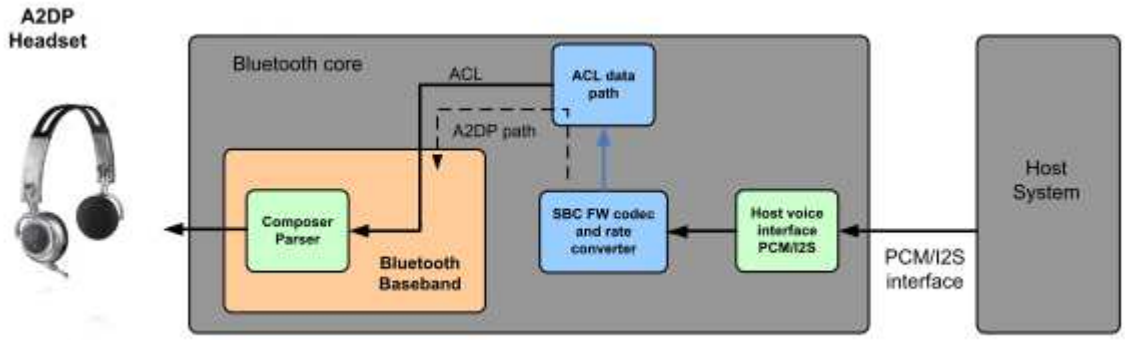

Figure 3-11 Device Assisted A2DP

3.5 Terminal Assignements

The view is from top side:

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
12	GND	BT_AUD_FSYNC_SB_DATA	GND	VIO	GND	GND	GND	GND	NC	NC	NC	NC	GND	GND	12
11	GND	BT_AUD_IN_SB_CLK	GND	GND	GND	SDIO_D2_WL	SDIO_CLK_WL	GND	BT_AUD_OUT	GND	NC	GND	GND	NC	11
10	GND	BT_AUD_CLK	GND	FUNC2_BT	GND	SDIO_D3_WL	SDIO_D0_WL	GND	DC2DC_REQ_MODE_SOC	CLK_REQ_OUT	GND	GND	GND	GND	10
9	GND	GND	GND	FUNC1_BT	GND	SDIO_CMD_WL	SDIO_D1_WL	GND	SLOW_CLK	NC	NC	GND	GND	NC	9
8	WLAN_BG2	GND	NC	NC	GND	GND	GND	COEX_MWS_BT_WL_TX_O	COEX_MWS_FRAME_SYNC	NC	NC	GND	GND	NC	8
7	GND	GND	NC	GND	GND	COEX_MWS_ACTIVE	RX_SW_FEM_WL	COEX_MWS_RX_PRI	NC	NC	GND	GND	GND	NC	7
6	NC	GND	PBIAS_TESTP_W	GND	GND	DC2DC_REQ_OUT_SOC	WLAN_IRQ	UART_DEBUG	GPIO_2	NC	NC	GND	GND	NC	6
5	GND	GND	PDET_TESTM_W	GND	GND	GND	WLAN_EN_SOC	FEM_PA_EN_WL	NC	GPIO_1	GND	GND	GND	GND	5
4	GND	GND	NC	GND	BT_EN_SOC	BT_HCI_RX	BT_HCI_TX	BT_HCI_RTS	BT_HCI_CTS	GPIO_3	GND	VBAT1	VBAT2	VBAT3	4
3	11abg_ANT_1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	3
2	GND	GND	GND	GND	GND	CLK_IN_P	CLK_IN_M	GND	GND	GND	GND	GND	GND	GND	2
1	GND	GND	GND	GND	GND	GND	GND	GND	PA_DC2DC_IN	PA_DC2DC_OUT	GND	GND	GND	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

DIGITAL
RF
Power
GND
CLOCK
DIGITAL High Speed
Not Used NC

Top view

Figure 3-12 Terminal Assignements

3.6 Terminal Functions

Pin names and pin numbers in bracket apply to WSP pin out.

Table 3-3 Terminal Functions

Module Pin Name (WSP Pin Name)	Module Pin No. (WSP ball no.)	I/O Type	Shut Down state	Default after POR	Buffer Type [mA]	Description
WLAN pins: I/O signals						
SDIO_CLK_WL (SDIO_CLK_WL)	G11 (E11)	IN	HiZ	HiZ		WLAN SDIO clock. Must be driven by the host.
SDIO_CMD_WL(SDIO_CMD_WL)	F9 (D8)	IN	HiZ	HiZ		WLAN SDIO command in. Host must pull up.
SDIO_D0_WL (SDIO_D0_WL)	G10 (E10)	I/O	HiZ	HiZ		WLAN SDIO data bit 0. Host must pull up.
SDIO_D1_WL (SDIO_D1_WL)	G9 (E9)	I/O	HiZ	HiZ		WLAN SDIO data bit 1. Host must pull up.
SDIO_D2_WL (SDIO_D2_WL)	F11 (D11)	I/O	HiZ	HiZ		WLAN SDIO data bit 2. Host must pull up.
SDIO_D3_WL (SDIO_D3_WL)	F10 (D10)	I/O	HiZ	PU		WLAN SDIO data bit 3. Changes state to PU at WL_EN or BT_EN assertion for card detect. Later disabled by the SW during init. Host must pull up.
WLAN_IRQ (IRQ_WL)	G6 (E3)	OUT	PD	Drive 0		SDIO available, interrupt out. Active high. To use WL_RS232_TX/RX lines, need to pull up with 10K resistor.
GPIO_1 (GPIO1)	K5 (H1)	I/O	PD	PD		Option: WL_RS232_TX (when IRQ_WL = 1 at power up)
GPIO_2 (GPIO2)	J6 (H2)	I/O	PD	PD		Option: WL_RS232_RX (when IRQ_WL = 1 at power up)
GPIO_3 (UART_DBG_WL)	K4 (G4)	OUT	PU	PU		WLAN logger Option: GPIO3
FEM_PA_EN_WL (GPIO13)	H5 (F2)					NC
RX_SW_FEM_WL (SW_CTRL_BG_IO1)	G7 (F3)					NC
PBIAS_TESTP_W (PABIAS_OUT_FEM_TESTP_WL)	C6 (C7)	ANA				NC
PDET_TESTM_W (PDET_IN_FEM_TESTM_WL)	C5 (C6)	ANA				NC
WLAN Pins: RF antenna						
11abg_ANT_1	A3	RF				WLAN ABG / BT RX and TX 50Ω input and output. No external matching required.
WLAN_BG2	A8	RF				Second 2.4GHz WLAN BG input and output for MIMO functionality. Requires external RF filter.
BT pins: I/O Signals						
BT_HCI_RX (HCI_RX_BT)	F4 (E7)	IN	PU	PU		HCI UART RX from host. Shared HCI I/F for BT. NC if not used.
BT_HCI_TX (HCI_TX_BT)	G4 (F7)	OUT	PU	PU		HCI UART TX to host. Shared HCI I/F.NC if not used.

Module Pin Name (WSP Pin Name)	Module Pin No. (WSP ball no.)	I/O Type	Shut Down state	Default after POR	Buffer Type [mA]	Description
BT_HCI_RTS (HCI_RTS_BT)	H4 (G6)	OUT	PU	PU		HCI UART RTS to host. Shared HCI I/F. NC if not used.
BT_HCI_CTS (HCI_CTS_BT)	J4 (F6)	IN	PU	PU		HCI UART CTS from host. Shared HCI I/F. NC if not used.
UART_DEBUG (UART_DEBUG_BT)	H6 (G2)	OUT	PU	PU		BT UART debug (logger). NC if not used.
FUNC1_BT (FUNC1_BT)	D9 (E8)	OUT	PD	PD		Optional: BT_HOST_WAKE_UP signal to wake-up the HOST from BT. NC if not used.
FUNC2_BT (FUNC2_BT)	D10 (B11)	IN	PD	PD		Optional: BT_WAKE_UP Bluetooth wakeup from HOST. NC if not used.
BT_AUD_CLK (AUD_CLK_BT)	B10 (G11)	OUT	PD	PD		BT PCM/I2S bus clock. NC if not used.
BT_AUD_FSYNC_SB_DATA (AUD_FSYNC_BT)	B12 (H11)	OUT	PD	PD		BT PCM/I2S bus frame sync. NC if not used.
BT_AUD_IN_SB_CLK (AUD_IN_BT)	B11 (G9)	IN	PD	PD		BT PCM/I2S bus data input. NC if not used.
BT_AUD_OUT (AUD_OUT_BT)	J11 (G10)	OUT	PD	PD		BT PCM/I2S bus data output. NC if not used.
JTAG pins						
JTAG_TCK	C8 (F11)	IN	PD	PD		JTAG_TCK NC if not used
JTAG_TMS	C7 (F8)	IN	PD	PD		JTAG_TMS NC if not used
JTAG_TDI	C4 (F9)	IN	PD	PD		JTAG_TDI NC if not used
JTAG_TDO	D8 (F10)	OUT	PD	PD		JTAG_TDO NC if not used
Clock pins						
CLK_IN_P	F2 (E4)	ANA				FREF/TCXO input for all functional blocks
CLK_IN_M	G2 (E5)	ANA				Connect to GND
SLOW_CLK (RTC_CLK)	J9 (H8)	ANA				Sleep clock 32.768 kHz
CLK_REQ_OUT	K10 (K11)	OUT	PD	PD		Request external fast clock NC if not used.
Enable pins						
BT_EN_SOC (BT_EN)	E4 (E2)	IN	PD	PD		High = enable
WLAN_EN_SOC (WLAN_EN)	G5 (E1)	IN	PD	PD		High = enable
Power management pins						
VBAT1	M4	POW				Battery voltage
VBAT2	N4	POW				Battery voltage
VBAT3	P4	POW				Battery voltage
VIO	D12	POW				1.8V I/O power supply
PA_DC2DC_IN	J1	POW				PA power supply input, with internal PA_DC2DC connect to pin PA_DC2DC_OUT K1.
PA_DC2DC_OUT	K1	POW				DC2DC output for PA supply, with internal PA_DC2DC connect to pin PA_DC2DC_IN J1.
DC2DC_REQ_OUT_SOC (NU)	F6 (D3)					NC
DC2DC_REQ_MODE_SOC (NU)	J10 (J10)					NC

Module Pin Name (WSP Pin Name)	Module Pin No. (WSP ball no.)	I/O Type	Shut Down state	Default after POR	Buffer Type [mA]	Description
Co-existence signals						
COEX_MWS_RX_PRI (COEX_MWS_UART_RX)	H7 (G5)		PU	PU		General purpose IO. NC if not used.
COEX_MWS_BT_WL_TX_O (COEX_MWS_UART_TX)	H8 (G7)		PU	PU		General purpose IO. NC if not used.
COEX_MWS_ACTIVE (COEX_MWS_PRE_TX)	F7 (G8)		PU	PU		General purpose IO. NC if not used.
COEX_MWS_FRAME_SYNC (COEX_MWS_FRAME_SYNC)	J8 (H7)		PU	PU		General purpose IO. NC if not used.
Not used pins						
NU	A6					NC
NU	J5					NC
NU	J7					NC
NU	J12					NC
NU	K6					NC
NU	K7					NC
NU	K8					NC
NU	K9					NC
NU	K12					NC
NU	L6					NC
NU	L8					NC
NU	L9					NC
NU	L11					NC
NU	L12					NC
NU	M12					NC
NU	P6					NC
NU	P7					NC
NU	P8					NC
NU	P9					NC
NU	P11					NC
Ground pins						
GND	A1	GND				
GND	A2	GND				
GND	A4	GND				
GND	A5	GND				
GND	A7	GND				
GND	A9	GND				
GND	A10	GND				
GND	A11	GND				
GND	A12	GND				
GND	B1	GND				
GND	B2	GND				
GND	B3	GND				
GND	B4	GND				
GND	B5	GND				

Module Pin Name (WSP Pin Name)	Module Pin No. (WSP ball no.)	I/O Type	Shut Down state	Default after POR	Buffer Type [mA]	Description
GND	B6	GND				
GND	B7	GND				
GND	B8	GND				
GND	B9	GND				
GND	C1	GND				
GND	C2	GND				
GND	C3	GND				
GND	C9	GND				
GND	C10	GND				
GND	C11	GND				
GND	C12	GND				
GND	D1	GND				
GND	D2	GND				
GND	D3	GND				
GND	D4	GND				
GND	D5	GND				
GND	D6	GND				
GND	D7	GND				
GND	D11	GND				
GND	E1	GND				
GND	E2	GND				
GND	E3	GND				
GND	E5	GND				
GND	E6	GND				
GND	E7	GND				
GND	E8	GND				
GND	E9	GND				
GND	E10	GND				
GND	E11	GND				
GND	E12	GND				
GND	F1	GND				
GND	F3	GND				
GND	F5	GND				
GND	F8	GND				
GND	F12	GND				
GND	G1	GND				
GND	G3	GND				
GND	G8	GND				
GND	G12	GND				

Module Pin Name (WSP Pin Name)	Module Pin No. (WSP ball no.)	I/O Type	Shut Down state	Default after POR	Buffer Type [mA]	Description
GND	H1	GND				
GND	H2	GND				
GND	H3	GND				
GND	H9	GND				
GND	H10	GND				
GND	H11	GND				
GND	H12	GND				
GND	J2	GND				
GND	J3	GND				
GND	K2	GND				
GND	K3	GND				
GND	K11	GND				
GND	L1	GND				
GND	L2	GND				
GND	L3	GND				
GND	L4	GND				
GND	L5	GND				
GND	L7	GND				
GND	L10	GND				
GND	M1	GND				
GND	M2	GND				
GND	M3	GND				
GND	M5	GND				
GND	M6	GND				
GND	M7	GND				
GND	M8	GND				
GND	M9	GND				
GND	M10	GND				
GND	M11	GND				
GND	N1	GND				
GND	N2	GND				
GND	N3	GND				
GND	N5	GND				
GND	N6	GND				
GND	N7	GND				
GND	N8	GND				
GND	N9	GND				
GND	N10	GND				
GND	N11	GND				

Module Pin Name (WSP Pin Name)	Module Pin No. (WSP ball no.)	I/O Type	Shut Down state	Default after POR	Buffer Type [mA]	Description
GND	N12	GND				
GND	P1	GND				
GND	P2	GND				
GND	P3	GND				
GND	P5	GND				
GND	P10	GND				
GND	P12	GND				

4 Design Goal Specifications

Section Disclaimer

This Specification is based upon the Texas Instruments WL183x Data Sheet version 1.4, and is subject to any subsequent changes in applicable Texas Instruments documentation and software.

Any parameter marked TBD indicates that this is yet to be determined by TDK design/testing. Any parameter marked TBC indicates that this is yet to be determined in an update of Texas Instruments documentation.

4.1 General Chip Requirements and Operation

All parameters are measured as follows unless stated otherwise: VIO=1.8V

4.1.1 Absolute Maximum Ratings (1)

			Value	Unit
VBAT(2)			-0.5 to 5.5(4)	V
VIO			-0.5 to 2.1	V
Input voltage to Analog pins (3)			-0.5 to 2.1	V
Input voltage to all other pins			-0.5 to (VDD_IO + 0.5V)	V
Operating ambient temperature range			-40 to +85(5)	°C
ESD Stress Voltage (6)	Human Body Model (7)	RF pins	>500	V
		Other	>1000	V
	Charged Device Model (8)	RF pins	>300	V
		Other	>250	V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The following signals are from the VBAT group: VBAT1, VBAT2, VBAT3

(3) Analog pins: WLAN_BG2, 11abg_ANT_1.

(4) 5.5V up to 10s cumulative in 7 years. 5V cumulative to 250s, 4.8V cumulative to 2.33 years – all includes charging dips and peaks.

(5) Operating free-air temperature range. The device can be reliably operated for 7 years at $T_{ambient}$ of 85°C, assuming 25% active mode and 75% sleep mode (15,400 cumulative active power-on hours).

(6) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.

(7) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500V HBM is possible if necessary precautions are taken. Pins listed as 1000V may actually have higher performance.

(8) Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250V CDM is possible if necessary precautions are taken. Pins listed as 250 V may actually have higher performance.