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# **CTVS – Ceramic transient voltage suppressors**

SMD multilayer transient voltage suppressors,  
high-speed series

**Series/Type:**

Date: February 2016

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**Multilayer varistors (MLVs)**

**High-speed series**

**SMD**

**EPCOS type designation system for high-speed series, single chips**

CT	0402	V150	HS	G
<p><b>Construction:</b> CT <math>\triangleq</math> Single chip with nickel barrier termination (AgNiSn)</p>				
<p><b>Case sizes:</b> 0402 0603</p>				
<p><b>Maximum RMS operating voltage (<math>V_{RMS}</math>):</b> S5 <math>\triangleq</math> 4 V S14 <math>\triangleq</math> 14 V L25 <math>\triangleq</math> 25 V</p> <p><b>Or:</b> <b>Indication of the varistor voltage:</b> V150 <math>\triangleq</math> 150 V V275 <math>\triangleq</math> 275 V</p>				
<p><b>Internal coding</b></p>				
<p><b>Taping mode:</b> G <math>\triangleq</math> 180-mm reel, 7" G2 <math>\triangleq</math> 330-mm reel, 13"</p>				

## Multilayer varistors (MLVs)

### High-speed series

#### SMD

#### EPCOS type designation system for high-speed series, array

CA	05	M2	S10	T	100H	G
<b>Construction:</b> CA $\triangleq$ Chip array with nickel barrier termination (AgNiSn)						
<b>Case sizes:</b> 05 $\triangleq$ 0508 array 06 $\triangleq$ 0612 array						
<b>Number of elements per component:</b> M2 $\triangleq$ Array with two elements P4 $\triangleq$ Array with four elements						
<b>Maximum RMS operating voltage (<math>V_{RMS}</math>):</b> S10 $\triangleq$ 10 V S14 $\triangleq$ 14 V <b>Typical varistor voltage (<math>V_v</math>):</b> V150 $\triangleq$ 150 V						
<b>Internal coding</b>						
<b>High-speed series</b> 100H $\triangleq$ Matched capacitance varistor (MCV array with $C_{yp} = 10 \cdot 10^0 = 10$ pF) HS $\triangleq$ 4-fold array						
<b>Taping mode:</b> G $\triangleq$ 180-mm reel, 7"						

## Multilayer varistors (MLVs)

### High-speed series

### SMD

#### Description

The high-speed series comprises a range of multilayer ceramic varistors for protection against ESD on data lines.

#### Features

- ESD protection level acc. to ISO 10605, IEC 61000-4-2 level 4
- Capacitance ratings down to 0.6 pF
- Low insertion loss
- Low leakage current
- No signal distortion
- Long-term ESD stability
- Bidirectional protection
- RoHS-compatible
- Suitable for lead-free soldering
- PSpice simulation models available

#### Applications

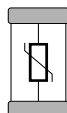
- ESD protection for high-speed data lines such as USB 2.0, firewire, IEEE 1394 interfaces, RF antennas, RF modules
- Selected types for ESD protection for high-speed automotive data lines (e.g. CAN bus, FlexRay)
- ESD protection for I/O ports of video and audio lines
- Integrated solutions for connectors in mobile communication and handheld devices

#### Design

- Multilayer technology
- Flammability rating better than UL 94 V-0
- Termination (see “Soldering directions”):
  - CT and CA types with nickel barrier terminations (AgNiSn), recommended for lead-free soldering, and compatible with tin/lead solder.

#### Single chip

Internal circuit



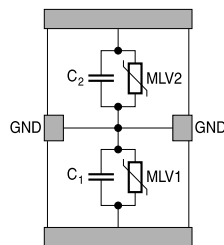
MLV0006-H

Available case sizes:

EIA	Metric
0402	1005
0603	1608

#### Matched capacitance varistor array (MCV array)

Internal circuit



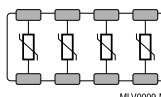
MLV0420-N

Available case sizes:

EIA	Metric	Version
0508	1220	2-fold array

#### 4-fold array

Internal circuit



MLV0009-MJ

Available case sizes:

EIA	Metric	Version
0508	1220	4-fold array
0612	1632	4-fold array

**Multilayer varistors (MLVs)**
**High-speed series**
SMD
**General technical data for single chips**

Maximum RMS operating voltage		$V_{RMS,max}$	4 ... 25	V
Maximum DC operating voltage		$V_{DC,max}$	5.5 ... 32	V
Contact discharge ESD capability	to IEC 61000-4-2	$V_{ESD,contact}$	8	kV
Air discharge ESD capability	to IEC 61000-4-2	$V_{ESD,air}$	15	kV
Maximum surge current	(8/20 $\mu$ s)	$I_{surge,max}$	1 ... 5	A
Typical capacitance	(1 MHz, 1 V)	$C_{typ}$	0.6 ... 15	pF
Maximum clamping voltage		$V_{clamp,max}$	66 ... 290	V
Operating temperature	for 0402	$T_{op}$	-40/+85	°C
Operating temperature	for 0603	$T_{op}$	-55/+125	°C
Operating temperature	for 0603, automotive types	$T_{op}$	-55/+150	°C
Storage temperature	for 0402	LCT/UCT	-40/+125	°C
Storage temperature	for 0603	LCT/UCT	-55/+150	°C
Response time		$t_{resp}$	< 0.5	ns

**General technical data for arrays**

Maximum RMS operating voltage		$V_{RMS,max}$	10 ... 14	V
Maximum DC operating voltage		$V_{DC,max}$	12 ... 16	V
Contact discharge ESD capability	to IEC 61000-4-2	$V_{ESD,contact}$	8	kV
Air discharge ESD capability	to IEC 61000-4-2	$V_{ESD,air}$	15	kV
Maximum surge current	(8/20 $\mu$ s)	$I_{surge,max}$	1 ... 5	A
Typical capacitance for 4-fold array	(1 MHz, 1 V)	$C_{typ}$	4 x 3 ... 4 x 10	pF
Typical capacitance for MCV array	(1 MHz, 1 V)	$C_{typ}$	Matched capacitance 2 x 10 ( $\Delta$ C between elements < 3%)	pF
Maximum clamping voltage		$V_{clamp,max}$	59 ... 350	V
Operating temperature	for 4-fold arrays	$T_{op}$	-40/+125	°C
Operating temperature	for MCV arrays	$T_{op}$	-55/+125	°C
Storage temperature	for 4-fold arrays	LCT/UCT	-40/+125	°C
Storage temperature	for MCV arrays	LCT/UCT	-55/+150	°C
Response time		$t_{resp}$	< 0.5	ns

**Multilayer varistors (MLVs)**
**High-speed series**
**SMD**
**Electrical specifications and ordering codes for single chips**
**Maximum ratings ( $T_{op,max}$ )**

Type	Ordering code	$V_{RMS,max}$ V	$V_{DC,max}$ V	$I_{surge,max}$ (8/20 $\mu$ s) A	$W_{max}$ (ESD) <sup>1)</sup> mJ	$T_{op,max}$ $^{\circ}$ C
<b>Single chip</b>						
CT0402S5ARFG	B72590T7050S160	4	5.5	-	-	+85
CT0603S5ARFG	B72500T7050S160	4	5.5	-	-	+125
CT0402S14AHSG	B72590T8140S160	14	16	2	30	+85
CT0402V150HSG	B72590T8151V060	14	16	1	30	+85
CT0402V150RFG	B72590T7151V060	14	16	-	-	+85
CT0402V275RFG	B72590T7271V060	14	16	-	-	+85
CT0402V90RFG	B72590T7900V060	14	16	-	-	+85
CT0603S14AHSG	B72500T8140S160	14	16	5	30	+125
CT0603S14AHSG_E	B72500E8140S160	14	16	5	30	+150 <sup>2)</sup>
CT0603V150RFG	B72500T7151V060	14	16	-	-	+125
CT0603V150RFG_E	B72500E7151V060	14	16	-	-	+150 <sup>2)</sup>
CT0603L25HSG	B72500T8250L060	25	32	5	50	+125
CT0603L25HSG_E	B72500E8250L060	25	32	5	50	+150 <sup>2)</sup>

**Characteristics ( $T_A = 25^{\circ}$ C)**

Type	$V_V$ (1 mA) V	$\Delta V_V$ %	$V_{clamp,max}$ V	$I_{clamp}$ (8/20 $\mu$ s) A	$C_{typ}$ (1 MHz, 1 V) pF	$C_{max}$ (1 MHz, 1 V) pF
<b>Single chip</b>						
CT0402S5ARFG	255	$\pm 15$	-	-	0.6	1
CT0603S5ARFG	255	$\pm 15$	-	-	0.6	1
CT0402S14AHSG	28	$\pm 20$	66	1	10	15
CT0402V150HSG	150	$\pm 35$	290	1	2	3
CT0402V150RFG	150	$\pm 35$	-	-	2	3
CT0402V275RFG	275	$\pm 30$	-	-	1.5	2
CT0402V90RFG	105	$\pm 15$	-	-	2.2	3
CT0603S14AHSG	28	$\pm 20$	66	1	15	30
CT0603S14AHSG_E	28	$\pm 20$	66	1	15	30
CT0603V150RFG	150	$\pm 35$	-	-	3	5
CT0603V150RFG_E	150	$\pm 35$	290	1	3	5
CT0603L25HSG	61	$\pm 15$	120	1	10	15
CT0603L25HSG_E	61	$\pm 15$	120	1	10	15

**Note:**

Typ CT0603S14AHSG\_E, CT0603V150RFG\_E and CT0603L25HSG\_E are qualified acc. to AEC-Q200 with  $T_{op} = 150^{\circ}$ C.

1) To IEC 61000-4-2, level 4

2) Qualified acc. to AEC-Q200

**Multilayer varistors (MLVs)**
**High-speed series**
**SMD**
**Electrical specifications and ordering codes for arrays**
**Maximum ratings ( $T_{op,max}$ )**

Type	Ordering code	$V_{RMS,max}$ V	$V_{DC,max}$ V	$I_{surge,max}$ (8/20 $\mu$ s) A	$W_{max}$ (ESD) <sup>1)</sup> mJ	$T_{op,max}$ $^{\circ}$ C
<b>2-fold array</b>						
CA05M2S10T100HG	B72812Q1120S160	10	12	5	-	+125 <sup>2)</sup>
<b>4-fold array</b>						
CA05P4S14THSG	B72714A8140S160	14	16	2	30	+85
CA06P4V150THSG	B72724A8151V062	14	16	1	30	+85

**Characteristics ( $T_A = 25\text{ }^{\circ}$ C)**

Type	$V_V$ (1 mA) V	$\Delta V_V$ %	$V_{clamp,max}$ V	$I_{clamp}$ (8/20 $\mu$ s) A	$C_{typ}$ (1 MHz, 1 V) pF	$C_{max}$ (1 MHz, 1 V) pF
<b>2-fold array</b>						
CA05M2S10T100HG	26	$\pm 20$	60	1	10	15
<b>4-fold array</b>						
CA05P4S14THSG	28	$\pm 15$	59	1	10	15
CA06P4V150THSG	150	$\pm 20$	350	1	3	5

**Further characteristics**

Type	Absolute capacitance deviation between array elements <sup>3)</sup> %	Maximum relative capacitance change %/ K	Dissipation factor $\tan \delta$ (@ 1 MHz, 1 $V_{RMS}$ , 25 $^{\circ}$ C)	$P_{diss,max}$ mW	$V_{LD}$ (300 ms) V	$V_{jump}$ (60 s) V
<b>2-fold array</b>						
CA05M2S10T100HG	$\leq 3$	0.1	$< 50 \cdot 10^{-3}$	3	27	28

1) To IEC 61000-4-2, level 4

2) Qualified acc. to AEC-Q200

3) Absolute value of  $(C_1 - C_2) / \text{minimum } (C_1, C_2)$ , with  $C_1, C_2$  denoting the two individual capacitances of the 2-fold array.



## Multilayer varistors (MLVs)

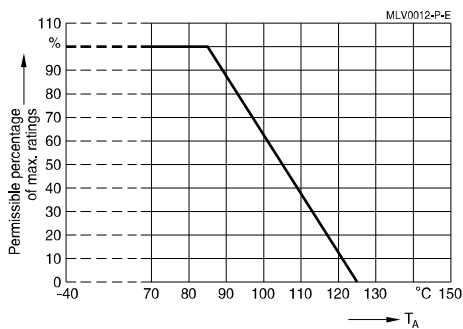
### High-speed series

#### SMD

#### Temperature derating

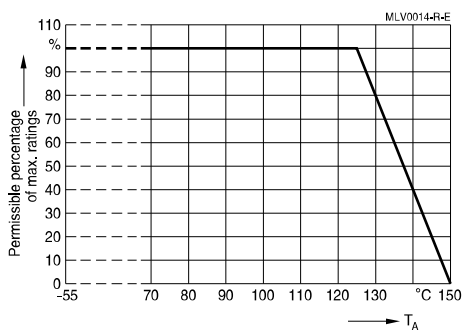
Climatic category:

–40/+85 °C for chip size 0402 single chip and 4-fold arrays



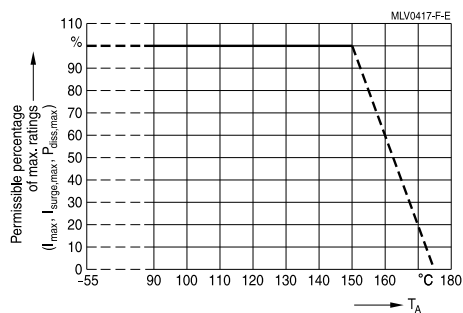
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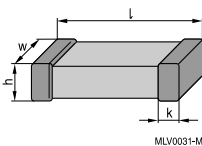
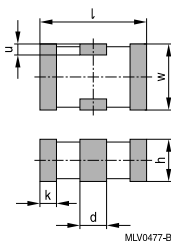
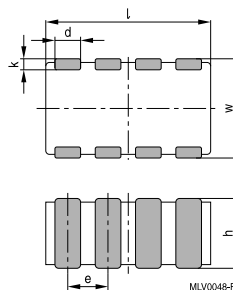
–55/+125 °C for chip size 0603 single chip and MCV arrays



Climatic category:

–55/+150 °C for chip size 0603 single chip, only automotive types



**Multilayer varistors (MLVs)**
**High-speed series**
**SMD**
**Dimensional drawings**
**Single chip**

**2-fold MCV array**

**4-fold array**

**Dimensions in mm**

Case size EIA / mm	l	w	h	d	e	k	u
0201 / 0603 Single chip	0.60 ±0.03	0.30 ±0.03	0.33 max.	-	-	0.15 ±0.05	-
0402 / 1005 Single chip	1.00 ±0.15	0.50 ±0.10	0.6 max.	-	-	0.10 ... 0.30	-
0508 / 1220 2-fold MCV array	2.00 ±0.20	1.25 ±0.15	0.9 max.	0.50 ±0.20	-	0.30 ±0.20	0.20 ±0.10
0508 / 1220 4-fold array	2.00 ±0.20	1.25 ±0.20	0.9 max.	0.30 ±0.10	0.50 ±0.10	0.20 +0.2/-0.1	-
0603 / 1608 Single chip	1.60 ±0.15	0.80 ±0.10	0.9 max.	-	-	0.10 ... 0.40	-
0612 / 1632 4-fold array	3.20 ±0.20	1.60 ±0.15	0.9 max.	0.40 ±0.15	0.80 ±0.15	0.20 ±0.10	-

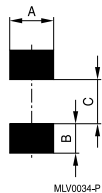
## Multilayer varistors (MLVs)

### High-speed series

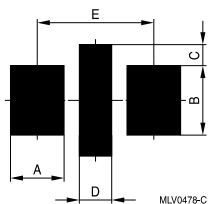
#### SMD

#### Recommended solder pad layout

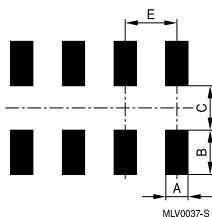
##### Single chip



##### 2-fold MCV array



##### 4-fold array



Dimensions in mm

Case size EIA / mm		A	B	C	D	E
0201 / 0603	Single chip	0.30	0.25	0.30	-	-
0402 / 1005	Single chip	0.60	0.60	0.50	-	-
0508 / 1220	2-fold MCV array	1.00	1.30	0.40	0.60	2.16
0508 / 1220	4-fold array	0.35	0.90	0.40	-	0.50
0603 / 1608	Single chip	1.00	1.00	1.00	-	-
0612 / 1632	4-fold array	0.50	0.70	1.20	-	0.76

**Multilayer varistors (MLVs)**
**High-speed series**
SMD
**Delivery mode**

EIA case size	Taping	Reel size mm	Packing unit pcs.	Type	Ordering code
<b>2-fold array</b>					
0508	Cardboard	180	4000	CA05M2S10T100HG	B72812Q1120S160
<b>4-fold array</b>					
0508	Cardboard	180	4000	CA05P4S14THSG	B72714A8140S160
0612	Blister	180	3000	CA06P4V150THSG	B72724A8151V062
<b>Single chip</b>					
0402	Cardboard	180	10000	CT0402S14AHSG	B72590T8140S160
0402	Cardboard	180	10000	CT0402S5ARFG	B72590T7050S160
0402	Cardboard	180	10000	CT0402V150HSG	B72590T8151V060
0402	Cardboard	180	10000	CT0402V150RFG	B72590T7151V060
0402	Cardboard	180	10000	CT0402V275RFG	B72590T7271V060
0402	Cardboard	180	10000	CT0402V90RFG	B72590T7900V060
0603	Cardboard	180	4000	CT0603L25HSG	B72500T8250L060
0603	Cardboard	180	4000	CT0603L25HSG_E	B72500E8250L060
0603	Cardboard	180	4000	CT0603S14AHSG	B72500T8140S160
0603	Cardboard	180	4000	CT0603S14AHSG_E	B72500E8140S160
0603	Cardboard	180	4000	CT0603S5ARFG	B72500T7050S160
0603	Cardboard	180	4000	CT0603V150RFG	B72500T7151V060
0603	Cardboard	180	4000	CT0603V150RFG_E	B72500E7151V060

## Multilayer varistors (MLVs)

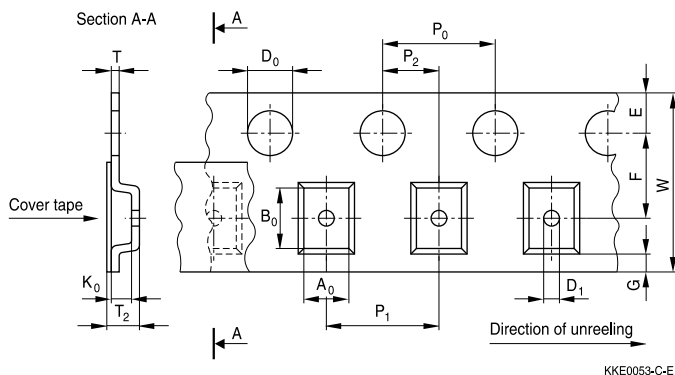
### High-speed series

#### SMD

#### Taping and packing

#### 1 Taping and packing for SMD components

#### 1.1 Blister tape (taping to IEC 60286-3)



KKE0053-C-E

#### Dimensions in mm

	8-mm tape					12-mm tape		Tolerance
	Case size (inch/mm)					Case size (inch/mm)		
			0508/ 1220	0612/ 1632	1012/ 2532			
	0603/ 1608	0506/ 1216	0805/ 2012	1206/ 3216	1210/ 3225	1812/ 4532	2220/ 5750	
A <sub>0</sub>	0.9 ±0.10	1.50	1.50	1.80	2.80	3.50	5.10	±0.20
B <sub>0</sub>	1.75 ±0.10	1.80	2.30	3.40	3.50	4.80	6.00	±0.20
K <sub>0</sub>	1.0	0.80	1.80			3.40		max.
T	0.30					0.30		max.
T <sub>2</sub>	1.3	1.20	2.50			3.90		max.
D <sub>0</sub>	1.50					1.50		+0.10/-0
D <sub>1</sub>	0.3					1.50		min.
P <sub>0</sub>	4.00					4.00		±0.10 <sup>1)</sup>
P <sub>2</sub>	2.00					2.00		±0.05
P <sub>1</sub>	4.00					8.00		±0.10
W	8.00					12.00		±0.30
E	1.75					1.75		±0.10
F	3.50					5.50		±0.05
G	0.75					0.75		min.

1) ≤±0.2 mm over 10 sprocket holes.

## Multilayer varistors (MLVs)

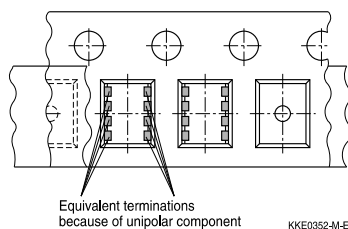
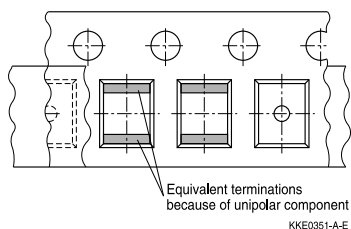
### High-speed series

#### SMD

#### Part orientation in tape pocket for blister tape

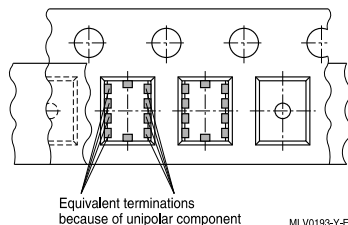
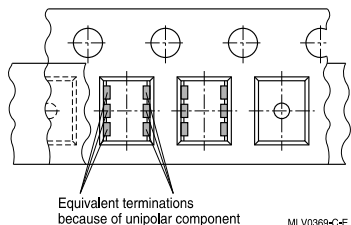
For discrete chip, EIA case sizes 0603, 0805, 1206, 1210, 1812 and 2220

For array, EIA case size 0612



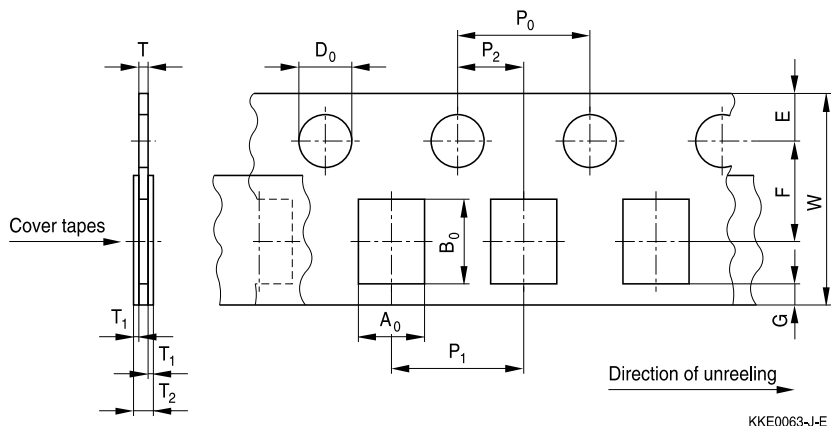
For arrays, EIA case sizes 0506 and 1012

For filter array, EIA case size 0508



#### Additional taping information

Reel material	Polystyrol (PS)
Tape material	Polystyrol (PS) or Polycarbonat (PC) or PVC
Tape break force	min. 10 N
Top cover tape strength	min. 10 N
Top cover tape peel force	0.1 to 1.0 N for 8-mm tape and 0.1 to 1.3 N for 12-mm tape at a peel speed of 300 mm/min
Tape peel angle	Angle between top cover tape and the direction of feed during peel off: 165° to 180°
Cavity play	Each part rests in the cavity so that the angle between the part and cavity center line is no more than 20°

**Multilayer varistors (MLVs)**
**High-speed series**
**SMD**
**1.2 Cardboard tape (taping to IEC 60286-3)**

**Dimensions in mm**

	8-mm tape						Tolerance
	Case size (inch/mm)					Case size (inch/mm)	
	0201/0603	0402/1005	0405/1012	0603/1608	1003/2508	0508/1220	
A <sub>0</sub>	0.38 ±0.05	0.60	1.05	0.95	1.00	1.60	±0.20
B <sub>0</sub>	0.68 ±0.05	1.15	1.60	1.80	2.85	2.40	±0.20
T	0.42 ±0.02	0.60	0.75	0.95	0.95	0.95	max.
T <sub>2</sub>	0.4 min.	0.70	0.90	1.10	1.10	1.10	max.
D <sub>0</sub>	1.50 ±0.1	1.50				1.50	+0.10/-0
P <sub>0</sub>	4.00						±0.10 <sup>2)</sup>
P <sub>2</sub>	2.00						±0.05
P <sub>1</sub>	2.00 ±0.05	2.00	4.00	4.00	4.00	4.00	±0.10
W	8.00						±0.30
E	1.75						±0.10
F	3.50						±0.05
G	0.75						min.

2) ≤0.2 mm over 10 sprocket holes.

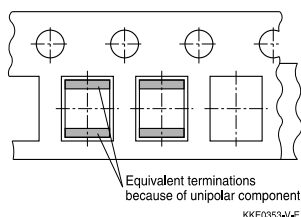
## Multilayer varistors (MLVs)

### High-speed series

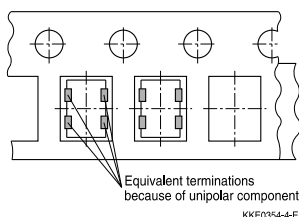
#### SMD

#### Part orientation in tape pocket for cardboard tape

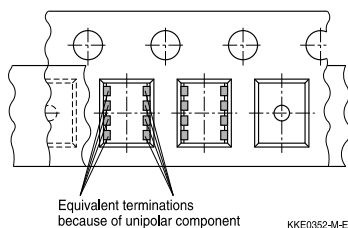
For discrete chip, EIA case sizes 0201, 0402, 0603 and 1003



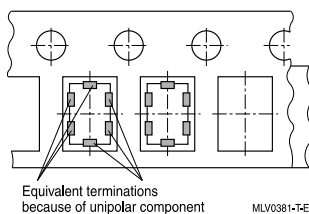
For array, EIA case size 0405



For array, EIA case size 0508



For filter array, EIA case size 0405



#### Additional taping information

Reel material	Polystyrol (PS)
Tape material	Cardboard
Tape break force	min. 10 N
Top cover tape strength	min. 10 N
Top cover tape peel force	0.1 to 1.0 N at a peel speed of 300 mm/min
Tape peel angle	Angle between top cover tape and the direction of feed during peel off: 165° to 180°
Cavity play	Each part rests in the cavity so that the angle between the part and cavity center line is no more than 20°

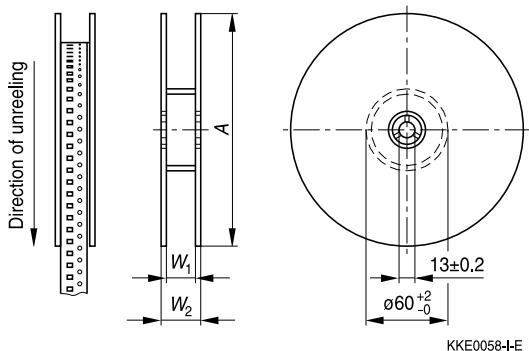


## Multilayer varistors (MLVs)

### High-speed series

#### SMD

### 1.3 Reel packing

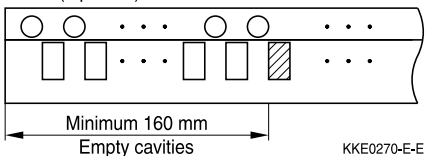


#### Dimensions in mm

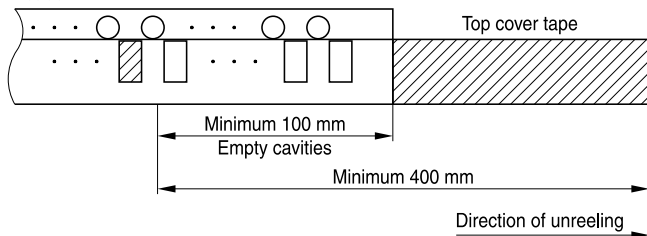
	8-mm tape		12-mm tape	
	180-mm reel	330-mm reel	180-mm reel	330-mm reel
A	180 +0/-3	330 +0/-2.0	180 +0/-3	330 +0/-2.0
W <sub>1</sub>	8.4 +1.5/-0	8.4 +1.5/-0	12.4 +1.5/-0	12.4 +1.5/-0
W <sub>2</sub>	14.4 max.	14.4 max.	18.4 max.	18.4 max.

#### Leader, trailer

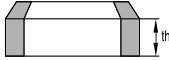
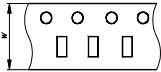


Trailer (tape end)



Leader



**Multilayer varistors (MLVs)**
**High-speed series**
**SMD**
**1.4 Packing units for discrete chip and array chip**

Case size inch/mm	 Chip thickness th			 Ø 180-mm reel	 Ø 330-mm reel
		Cardboard tape W	Blister tape W	pcs.	pcs.
0201/0603	0.33 mm	8 mm	–	15000	–
0402/1005	0.6 mm	8 mm	–	10000	50000
0405/1012	0.7 mm	8 mm	–	5000	–
0506/1216	0.5 mm	–	8 mm	4000	–
0508/1220	0.9 mm	8 mm	8 mm	4000	–
0603/1608	0.9 mm	8 mm	8 mm	4000	16000
0612/1632	0.7 mm	–	8 mm	3000	–
0805/2012	0.7 mm	–	8 mm	3000	–
	0.9 mm	–	8 mm	3000	12000
	1.3 mm	–	8 mm	3000	12000
1003/2508	0.9 mm	8 mm	–	4000	–
1012/2532	1.0 mm	–	8 mm	2000	–
1206/3216	0.9 mm	–	8 mm	3000	–
	1.3 mm	–	8 mm	3000	12000
	1.4 mm	–	8 mm	2000	8000
	1.6 mm	–	8 mm	2000	8000
1210/3225	0.9 mm	–	8 mm	3000	–
	1.3 mm	–	8 mm	3000	12000
	1.4 mm	–	8 mm	2000	8000
	1.6 mm	–	8 mm	2000	8000
1812/4532	1.3 mm	–	12 mm	1500	–
	1.4 mm	–	12 mm	1000	–
	1.6 mm	–	12 mm	1000	4000
	2.0 mm	–	12 mm	–	3000
	2.3 mm	–	12 mm	–	3000
2220/5750	1.3 mm	–	12 mm	1500	–
	1.4 mm	–	12 mm	1000	–
	1.6 mm	–	12 mm	1000	–
	2.0 mm	–	12 mm	–	3000
	2.3 mm	–	12 mm	–	3000
	2.7 mm	–	12 mm	600	–
	3.0 mm	–	12 mm	600	–

**Multilayer varistors (MLVs)****High-speed series****SMD****2 Delivery mode for leaded SHCV varistors**

Standard delivery mode for SHCV types is bulk. Alternative taping modes (AMMO pack or taped on reel) are available upon request.

Packing units for:

Type	Pieces
SR6	2000
SR1 / SR2	1000

For types not listed in this data book please contact EPCOS.

## Multilayer varistors (MLVs)

### High-speed series

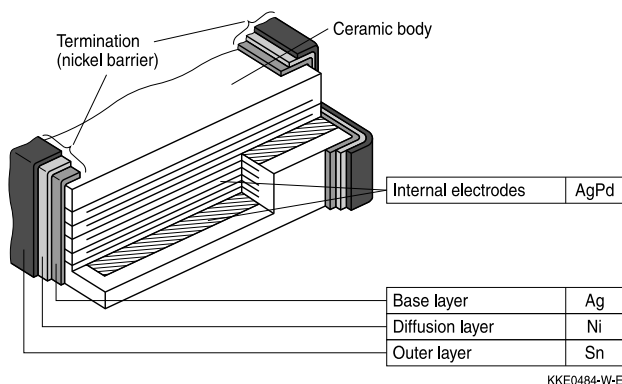
#### SMD

### Soldering directions

#### 1 Terminations

##### 1.1 Nickel barrier termination

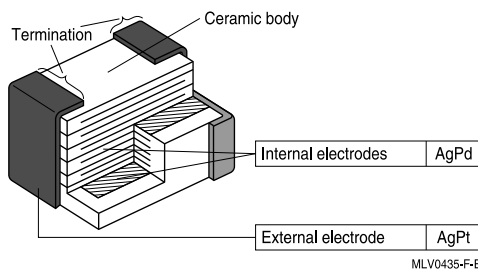
The nickel barrier layer of the silver/nickel/tin termination prevents leaching of the silver base metallization layer. This allows great flexibility in the selection of soldering parameters. The tin prevents the nickel layer from oxidizing and thus ensures better wetting by the solder. The nickel barrier termination is suitable for all commonly-used soldering methods, including lead-free soldering.



Multilayer CTVS: Structure of nickel barrier termination

##### 1.2 Silver-platinum termination

Silver-platinum terminations are mainly used for the large EIA case sizes 1812 and 2220. The silver-platinum termination is approved for reflow soldering, SnPb soldering and lead-free soldering with a silver containing solder paste. In case of SnPb soldering, a solder paste Sn62Pb36Ag2 is recommended. For lead-free reflow soldering, a solder paste SAC, e.g. Sn95.5Ag3.8Cu0.7, is recommended.



Multilayer varistor: Structure of silver-platinum termination

## Multilayer varistors (MLVs)

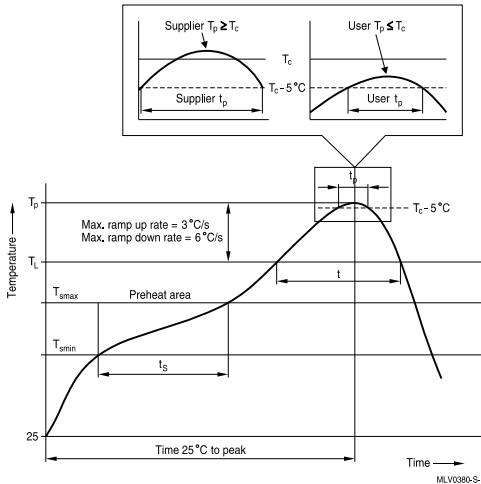
### High-speed series

### SMD

## 2 Recommended soldering temperature profiles

### 2.1 Reflow soldering temperature profile

#### Recommended temperature characteristic for reflow soldering following JEDEC J-STD-020D



Profile feature		Sn-Pb eutectic assembly	Pb-free assembly
Preheat and soak			
- Temperature min	$T_{smin}$	100 °C	150 °C
- Temperature max	$T_{smax}$	150 °C	200 °C
- Time	$t_{smin}$ to $t_{smax}$	60 ... 120 s	60 ... 180 s
Average ramp-up rate	$T_{smax}$ to $T_p$	3 °C/ s max.	3 °C/ s max.
Liquidous temperature	$T_L$	183 °C	217 °C
Time at liquidous	$t_L$	60 ... 150 s	60 ... 150 s
Peak package body temperature	$T_p$ <sup>1)</sup>	220 °C ... 235 °C <sup>2)</sup>	245 °C ... 260 °C <sup>2)</sup>
Time ( $t_p$ ) <sup>3)</sup> within 5 °C of specified classification temperature ( $T_c$ )		20 s <sup>3)</sup>	30 s <sup>3)</sup>
Average ramp-down rate	$T_p$ to $T_{smax}$	6 °C/ s max.	6 °C/ s max.
Time 25 °C to peak temperature		maximum 6 min	maximum 8 min

1) Tolerance for peak profile temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.

2) Depending on package thickness. For details please refer to JEDEC J-STD-020D.

3) Tolerance for time at peak profile temperature ( $t_p$ ) is defined as a supplier minimum and a user maximum.

**Note:** All temperatures refer to topside of the package, measured on the package body surface.  
Number of reflow cycles: 3

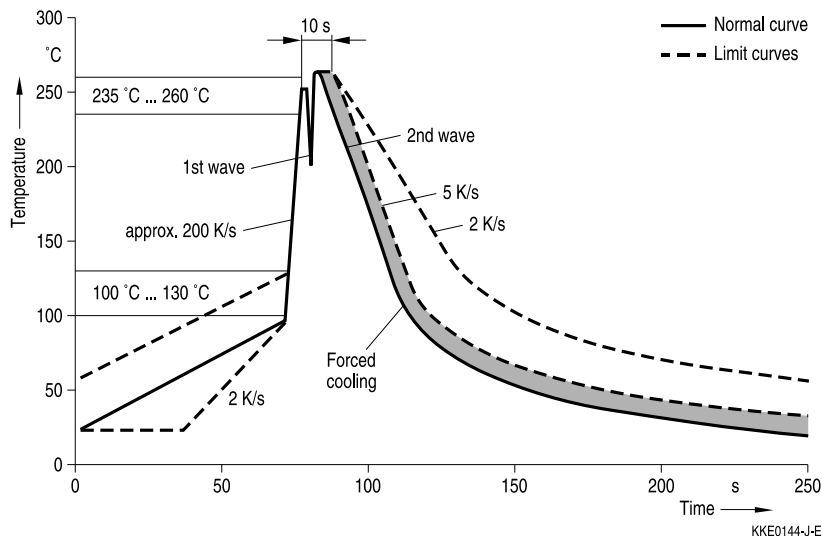
## Multilayer varistors (MLVs)

### High-speed series

#### SMD

### 2.2 Wave soldering temperature profile

Temperature characteristics at component terminal with dual-wave soldering



### 2.3 Lead-free soldering processes

EPCOS multilayer CTVS with AgNiSn termination are designed for the requirements of lead-free soldering processes only.

Soldering temperature profiles to JEDEC J-STD-020D, IEC 60068-2-58 and ZVEI recommendations.

## 3 Recommended soldering methods - type-specific releases by EPCOS

### 3.1 Overview

Type	EIA case size	Reflow soldering		Wave soldering	
		SnPb	Lead-free	SnPb	Lead-free
CT... / CD...	0201/ 0402	Approved	Approved	No	No
CT... / CD...	0603 ... 2220	Approved	Approved	Approved	Approved
CN...K2	1812, 2220	Approved	Approved	No	No
Arrays	0405 ... 1012	Approved	Approved	No	No
ESD/EMI filters	0405, 0508	Approved	Approved	No	No
SHCV	-	No	No	Approved	Approved

## Multilayer varistors (MLVs)

### High-speed series

#### SMD

### 3.2 Nickel barrier and AgPt terminated multilayer MLVs

All EPCOS MLVs with nickel barrier and AgPt termination are suitable and fully qualified for lead-free soldering. The nickel barrier layer is 100% matte tin-plated.

### 3.3 Silver-platinum terminated MLVs

The silver-platinum termination is approved for reflow soldering, SnPb soldering and lead-free with a silver containing solder paste. In case of SnPb soldering, a solder paste Sn62Pb36Ag2 is recommended. For lead-free reflow soldering, a solder paste SAC, e.g. Sn95.5Ag3.8Cu0.7, is recommended.

### 3.4 Tinned iron wire

All EPCOS SHCV types with tinned termination are approved for lead-free and SnPb soldering.

## 4 Solder joint profiles / solder quantity

### 4.1 Nickel barrier termination

If the meniscus height is too low, that means the solder quantity is too low, the solder joint may break, i.e. the component becomes detached from the joint. This problem is sometimes interpreted as leaching of the external terminations.

If the solder meniscus is too high, i.e. the solder quantity is too large, the vise effect may occur. As the solder cools down, the solder contracts in the direction of the component. If there is too much solder on the component, it has no leeway to evade the stress and may break, as in a vise.

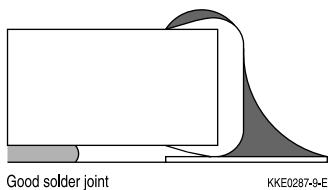
The figures below show good and poor solder joints for dual-wave and infrared soldering.

**Multilayer varistors (MLVs)**

**High-speed series**

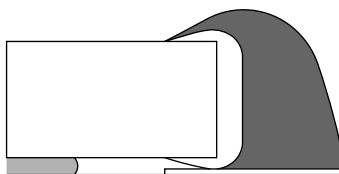
**SMD**

**4.1.1 Solder joint profiles for nickel barrier termination - dual-wave soldering**



Good solder joint

KKE0287-9-E

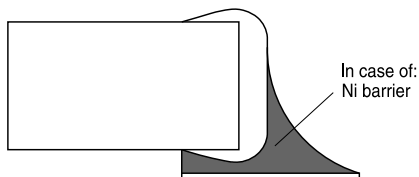


Too much solder  
Pad geometry too large,  
not soldered in preferred direction

KKE0288+4-E

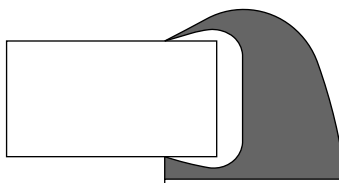
Good and poor solder joints caused by amount of solder in dual-wave soldering.

**4.1.2 Solder joint profiles for nickel barrier termination / silver-platinum termination - reflow soldering**



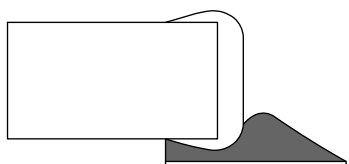
Good solder joint

MLV0196-B-E



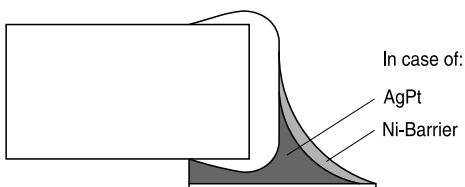
Too much solder  
Pad geometry too large

KKE0071-A-E



Poor wetting

KKE0072+4-E



Good solder joint

MLV0549-M-E

Good and poor solder joints caused by amount of solder in reflow soldering.



**Multilayer varistors (MLVs)**
**High-speed series**
SMD
**5 Solderability tests**

Test	Standard	Test conditions Sn-Pb soldering	Test conditions Pb-free soldering	Criteria/ test results
Wettability	IEC 60068-2-58	Immersion in 60/40 SnPb solder using non-activated flux at 215 ±3 °C for 3 ±0.3 s	Immersion in Sn96.5Ag3.0Cu0.5 solder using non- or low activated flux at 245 ±5 °C for 3 ±0.3 s	Covering of 95% of end termination, checked by visual inspection
Leaching resistance	IEC 60068-2-58	Immersion in 60/40 SnPb solder using mildly activated flux without preheating at 260 ±5 °C for 10 ±1 s	Immersion in Sn96.5Ag3.0Cu0.5 solder using non- or low activated flux without preheating at 255 ±5 °C for 10 ±1 s	No leaching of contacts
Thermal shock (solder shock)		Dip soldering at 300 °C/5 s	Dip soldering at 300 °C/5 s	No deterioration of electrical parameters. Capacitance change: $ \Delta C/C_0  \leq 15\%$
Tests of resistance to soldering heat for SMDs	IEC 60068-2-58	Immersion in 60/40 SnPb for 10 s at 260 °C	Immersion in Sn96.5Ag3.0Cu0.5 for 10 s at 260 °C	Change of varistor voltage: $ \Delta V/V (1 \text{ mA})  \leq 5\%$
Tests of resistance to soldering heat for radial leaded components (SHCV)	IEC 60068-2-20	Immersion of leads in 60/40 SnPb for 10 s at 260 °C	Immersion of leads in Sn96.5Ag3.0Cu0.5 for 10 s at 260 °C	Change of varistor voltage: $ \Delta V/V (1 \text{ mA})  \leq 5\%$ Change of capacitance X7R: $\leq -5/+10\%$

## Multilayer varistors (MLVs)

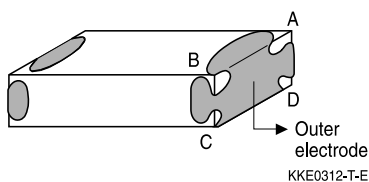
### High-speed series

#### SMD

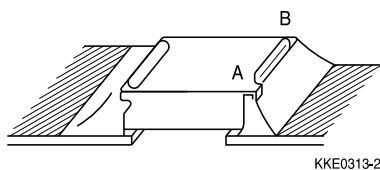
#### Note:

#### Leaching of the termination

Effective area at the termination might be lost if the soldering temperature and/or immersion time are not kept within the recommended conditions. Leaching of the outer electrode should not exceed 25% of the chip end area (full length of the edge A-B-C-D) and 25% of the length A-B, shown below as mounted on substrate.



As a single chip



As mounted on substrate

## 6 Notes for proper soldering

### 6.1 Preheating and cooling

- According to JEDEC J-STD-020D. Please refer to section 2 of this chapter.

### 6.2 Repair/ rework

Manual soldering with a soldering iron must be avoided, hot-air methods are recommended for rework purposes.

### 6.3 Cleaning

All environmentally compatible agents are suitable for cleaning. Select the appropriate cleaning solution according to the type of flux used. The temperature difference between the components and cleaning liquid must not be greater than 100 °C. Ultrasonic cleaning should be carried out with the utmost caution. Too high ultrasonic power can impair the adhesive strength of the metalized surfaces.

### 6.4 Solder paste printing (reflow soldering)

An excessive application of solder paste results in too high a solder fillet, thus making the chip more susceptible to mechanical and thermal stress. Too little solder paste reduces the adhesive strength on the outer electrodes and thus weakens the bonding to the PCB. The solder should be applied smoothly to the end surface.