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With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Ceramic transient voltage suppressors

SMD multilayer transient voltage suppressors, high-speed series

The following products presented in this data sheet are being withdrawn.

Ordering Code	Substitute Product	Date of Withdrawal	Deadline Last Orders	Last Shipments
B72762A8151V060		2012-11-09	2013-03-01	2013-06-01
B72762A8140S160		2012-11-09	2013-03-01	2013-06-01

For further information please contact your nearest EPCOS sales office, which will also support you in selecting a suitable substitute. The addresses of our worldwide sales network are presented at www.epcos.com/sales.

EPCOS AG is a TDK Group Company.

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EPCOS type designation system for high-speed series

CA	04	P2	S	14	T	HS	G

Construction:
CT ≙ Single chip with nickel barrier termination (AgNiSn)
CA ≙ Chip array with nickel barrier termination (AgNiSn)

Case sizes:
0201 ≙ 0201 single chip
0402 ≙ 0402 single chip
0603 ≙ 0603 single chip
04 ≙ 0405 array
05 ≙ 0508 array
06 ≙ 0612 array

Number of elements per component:
– ≙ Single chip
P2 ≙ Array with 2 elements
P4 ≙ Array with 4 elements

Tolerance of the varistor voltage:
L ≙ ±15%
S ≙ Special tolerance
V ≙ Special tolerance

Maximum RMS operating voltage (V_{RMS}):
14 ≙ 14 V

Typical varistor voltage (V_v):
150 ≙ 150 V

Internal coding

High-speed series

Taping mode:
G ≙ 180-mm reel

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Features

- ESD protection level acc. to ISO 10605, IEC 61000-4-2 level 4
- Bidirectional protection
- Capacitance ratings down to 2 pF
- Low insertion loss
- Low leakage current
- No signal distortion
- RoHS-compatible
- Suitable for lead-free soldering

Applications

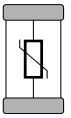
- ESD protection for high-speed data lines such as USB 2.0, firewire, etc.
- ESD protection for I/O ports of video and audio lines
- Integrated solutions for connectors in mobile communication and handheld devices

Design

- Multilayer technology
- Lack of plastic or epoxy encapsulation for flammability rating better than UL 94 V-0
- Termination (see “Soldering directions”):
  - CT and CA types with nickel barrier terminations (AgNiSn), recommended for lead-free soldering, and compatible with tin/lead solder.

Single chip

Internal circuit



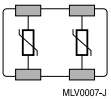
MLV0006-H

Available case sizes:

EIA	Metric
0201	0603
0402	1005
0603	1608

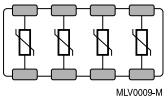
Array

Internal circuit



MLV0007-J

2-fold array



MLV0009-M

4-fold array

Available case sizes:

EIA	Metric	Version
0405	1014	2-fold array
0508	1220	4-fold array
0612	1632	4-fold array

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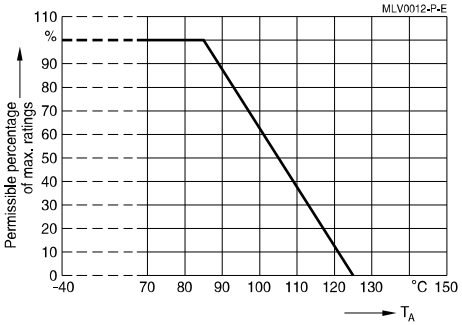
General technical data

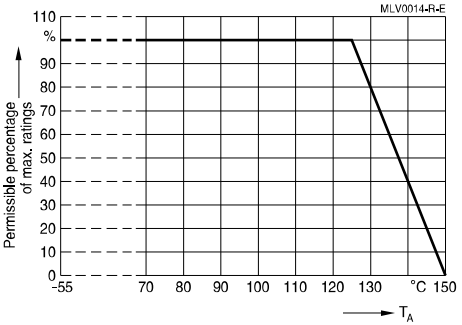
Maximum RMS operating voltage		$V_{RMS,max}$	4 ... 25	V
Maximum DC operating voltage		$V_{DC,max}$	5.5 ... 32	V
Contact discharge ESD capability	to IEC 61000-4-2	$V_{ESD,contact}$	8	kV
Air discharge ESD capability	to IEC 61000-4-2	$V_{ESD,air}$	15	kV
Maximum surge current	(8/20 µs)	$I_{surge,max}$	1 ... 5	A
Typical capacitance	(1 MHz, 1 V)	C_{typ}	2 ... 15	pF
Maximum clamping voltage	(8/20 µs)	$V_{clamp,max}$	59 ... 350	V
Operating temperature	for 0201, 0402 and arrays	T_{op}	−40/+85	°C
Operating temperature	for 0603	T_{op}	−55/+125	°C
Storage temperature	for 0201, 0402 and arrays	LCT/UCT	−40/+125	°C
Storage temperature	for 0603	LCT/UCT	−55/+150	°C

Temperature derating

Climatic category:
−40/+85 °C for chip size 0201, 0402 and arrays



Climatic category:
−55/+125 °C for chip size 0603



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Electrical specifications and ordering codes

Maximum ratings ($T_{op,max}$)

Type	Ordering code	$V_{RMS,max}$ V	$V_{DC,max}$ V	$I_{surge,max}$ (8/20 µs) A	W_{max} (ESD)[1] mJ	$T_{op,max}$ °C
2-fold array						
CA04P2S14THSG	B72762A8140S160	14	16	1	30	+85
CA04P2V150THSG	B72762A8251V060	14	16	1	30	+85
4-fold array						
CA05P4S14THSG	B72714A8140S160	14	16	2	30	+85
CA06P4V150THSG	B72724A8151V062	14	16	1	30	+85
Single chip						
CT0201S4AHSG	B72440T8040S160	4	5.5	-	-	+85
CT0402S14AHSG	B72590T8140S160	14	16	2	30	+85
CT0402V150HSG	B72590T8151V060	14	16	1	30	+85
CT0603S14AHSG	B72500T8140S160	14	16	5	30	+125
CT0603L25HSG	B72500T8250L060	25	32	5	50	+125

Characteristics (T_A = 25 °C)

Type	$V_{V,min}$ (1 mA) V	$V_{V,max}$ (1 mA) V	$V_{clamp,max}$ V	I_{clamp} (8/20 µs) A	C_{typ} (1 MHz, 1 V) pF	C_{max} (1 MHz, 1 V) pF
2-fold array						
CA04P2S14THSG	23	33	66	1	10	15
CA04P2V150THSG	-	175	350	1	3	5
4-fold array						
CA05P4S14THSG	24	32	59	1	10	15
CA06P4V150THSG	-	175	350	1	3	5
Single chip						
CT0201S4AHSG	21	39	70	1	-	10
CT0402S14AHSG	23	33	66	1	10	15
CT0402V150HSG	-	200	290	1	2	3
CT0603S14AHSG	23	33	66	1	15	30
CT0603L25HSG	51.9	70.1	120	1	10	15

1) To IEC 61000-4-2, level 4

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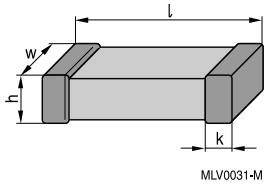
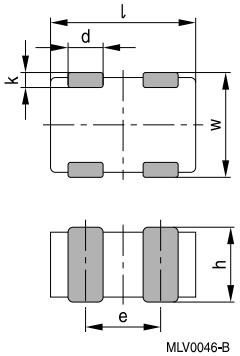
Dimensional drawings

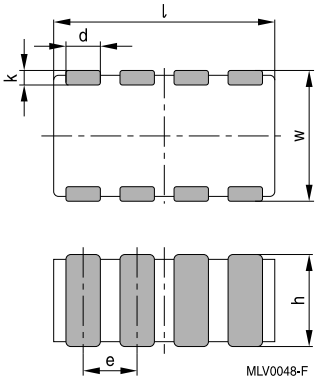
Single chip



2-fold array



4-fold array



Dimensions in mm

Case size EIA / mm	l	w	h	d	e	k
0201 / 0603	0.60 ±0.03	0.30 ±0.03	0.33 max.	-	-	0.15 ±0.05
0402 / 1005	1.00 ±0.15	0.50 ±0.10	0.6 max.	-	-	0.10 ... 0.30
0405 / 1014	1.37 ±0.15	1.00 +0/−0.15	0.7 max.	0.36 ±0.10	0.64 ±0.10	0.20 ±0.10
0508 / 1220	2.00 ±0.20	1.25 ±0.20	0.9 max.	0.30 ±0.10	0.50 ±0.10	0.20 +0.2/−0.1
0603 / 1608	1.60 ±0.15	0.80 ±0.10	0.9 max.	-	-	0.10 ... 0.40
0612 / 1632	3.20 ±0.20	1.60 ±0.15	0.9 max.	0.40 ±0.15	0.80 ±0.15	0.20 ±0.10

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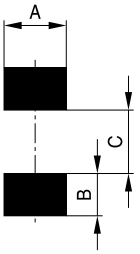
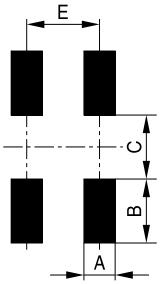
Recommended solder pad layout

Single chip



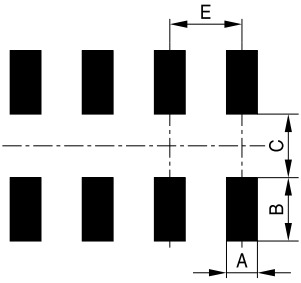
MLV0034-P

2-fold array



MLV0035-Q

4-fold array



MLV0037-S

Dimensions in mm

Case size EIA / mm		A	B	C	E
0201 / 0603	Single chip	0.30	0.25	0.30	-
0402 / 1005	Single chip	0.60	0.60	0.50	-
0603 / 1608	Single chip	1.00	1.00	1.00	-
0405 / 1014	2-fold array	0.40	0.55	0.28	0.64
0508 / 1220	4-fold array	0.35	0.90	0.40	0.50
0612 / 1632	4-fold array	0.50	0.70	1.20	0.76

Delivery mode

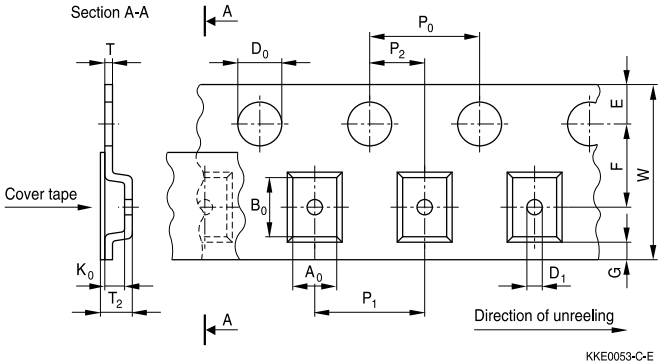
EIA case size	Taping	Reel size mm	Packing unit pcs.	Type	Ordering code
2-fold array					
0405	Cardboard	180	5000	CA04P2S14THSG	B72762A8140S160
0405	Cardboard	180	5000	CA04P2V150THSG	B72762A8251V060
4-fold array					
0508	Cardboard	180	4000	CA05P4S14THSG	B72714A8140S160
0612	Blister	180	3000	CA06P4V150THSG	B72724A8151V062
Single chip					
0201	Cardboard	180	15000	CT0201S4AHSG	B72440T8040S160
0402	Cardboard	180	10000	CT0402S14AHSG	B72590T8140S160
0402	Cardboard	180	10000	CT0402V150HSG	B72590T8151V060
0603	Cardboard	180	4000	CT0603L25HSG	B72500T8250L060
0603	Cardboard	180	4000	CT0603S14AHSG	B72500T8140S160

SMD

Taping and packing

1 Taping and packing for SMD components

1.1 Blister tape (the taping to IEC 60286-3)



Dimensions in mm

	8-mm tape					12-mm tape		16-mm tape		Tolerance
	Case size (inch/mm)					Case size (inch/mm)		Case size (inch/mm)		
			0508/ 1220	0612/ 1632	1012/ 2532					
	0603/ 1608	0506/ 1216	0805/ 2012	1206/ 3216	1210/ 3225	1812/ 4532	2220/ 5750	3225	4032	
A_0	0.9 ±0.10	1.50	1.60	1.90	2.80	3.50	5.10	7.00	8.60	±0.20
B_0	1.75 ±0.10	1.80	2.40	3.50	3.50	4.80	6.00	8.70	10.60	±0.20
K_0	1.0	0.80	1.80			2.60		5.00		max.
T	0.30					0.30		0.30		max.
T_2	1.3	1.20	2.50			3.50		5.50		max.
D_0	1.50					1.50		1.50		+0.10/−0
D_1	1.00					1.50		1.50		min.
P_0	4.00					4.00		4.00		±0.10[1)]
P_2	2.00					2.00		2.00		±0.05
P_1	4.00					8.00		12.00		±0.10
W	8.00					12.00		16.00		±0.30
E	1.75					1.75		1.75		±0.10
F	3.50					5.50		7.50		±0.05
G	0.75					0.75		0.75		min.

1) ≤±0.2 mm over 10 sprocket holes.

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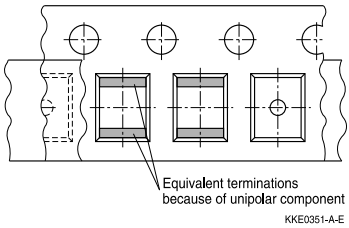
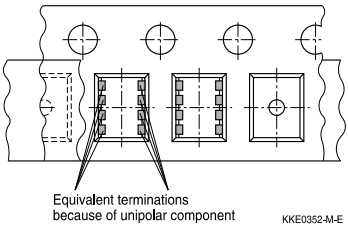
Part orientation in tape pocket for blister tape

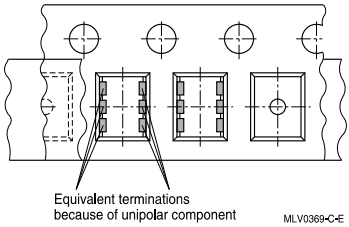
For discrete chip, case sizes 0603, 0805, 1206, 1210, 1812 and 2220



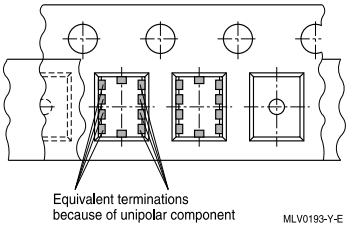
For array, case sizes 0612



For arrays 0506 and 1012



For filter array, case size 0508



Additional taping information

Reel material	Polystyrol (PS)
Tape material	Polystyrol (PS) or Polycarbonat (PC) or PVC
Tape break force	min. 10 N
Top cover tape strength	min. 10 N
Top cover tape peel force	0.2 to 0.6 N for 8-mm tape and 0.2 to 0.8 N for 12-mm tape at a peel speed of 300 mm/min
Tape peel angle	Angle between top cover tape and the direction of feed during peel off: 165° to 180°
Cavity play	Each part rests in the cavity so that the angle between the part and cavity center line is no more than 20°

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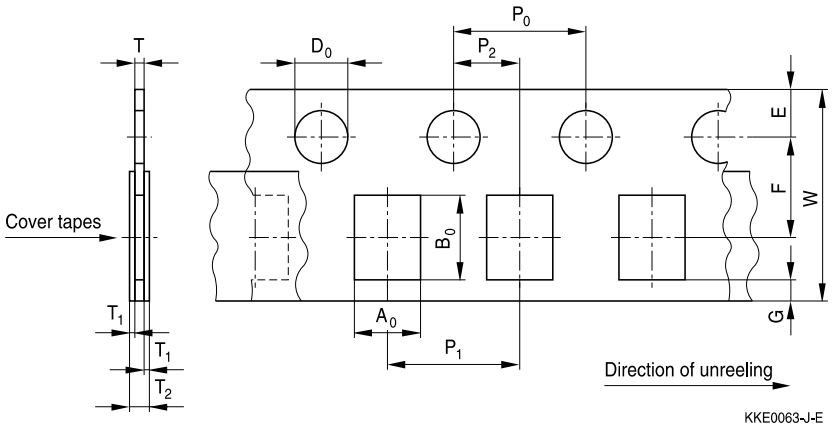
1.2 Cardboard tape (taping to IEC 60286-3)



Dimensions in mm

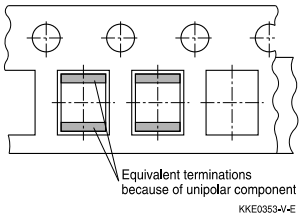
	8-mm tape						Tolerance
	Case size (inch/mm)					Case size (inch/mm)	
	0201/0603	0402/1005	0405/1012	0603/1608	1003/2508	0508/1220	
A_0	0.38 ±0.05	0.60	1.05	0.95	1.00	1.60	±0.20
B_0	0.68 ±0.05	1.15	1.60	1.80	2.85	2.40	±0.20
T	0.35 ±0.02	0.60	0.75	0.95	1.00	0.95	max.
T_2	0.4 min.	0.70	0.90	1.10	1.10	1.12	max.
D_0	1.50 ±0.1	1.50				1.50	+0.10/−0
P_0	4.00						±0.10[2)]
P_2	2.00						±0.05
P_1	2.00 ±0.05	2.00	4.00	4.00	4.00	4.00	±0.10
W	8.00						±0.30
E	1.75						±0.10
F	3.50						±0.05
G	1.35	0.75					min.

2) ≤0.2 mm over 10 sprocket holes.

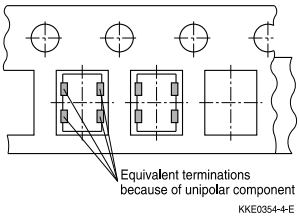
SMD

Part orientation in tape pocket for cardboard tape

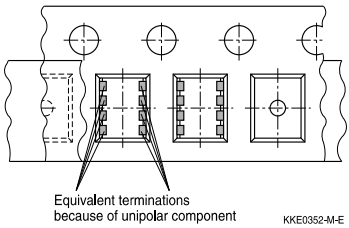
For discrete chip case sizes 0201, 0402, 0603 and 1003



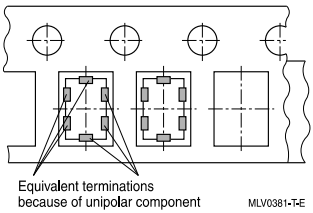
For array case size 0405



For array case size 0508



For filter array, case size 0405

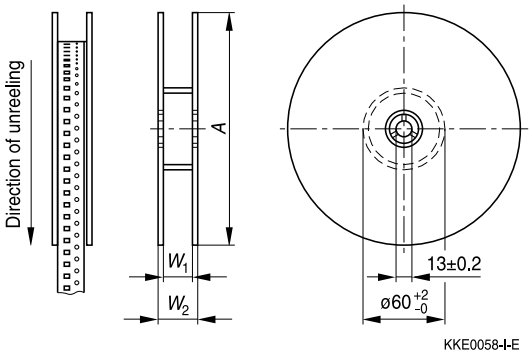


Additional taping information

Reel material	Polystyrol (PS)
Tape material	Cardboard
Tape break force	min. 10 N
Top cover tape strength	min. 10 N
Top cover tape peel force	0.1 to 0.65 N at a peel speed of 300 mm/min
Tape peel angle	Angle between top cover tape and the direction of feed during peel off: 165° to 180°
Cavity play	Each part rests in the cavity so that the angle between the part and cavity center line is no more than 20°

SMD

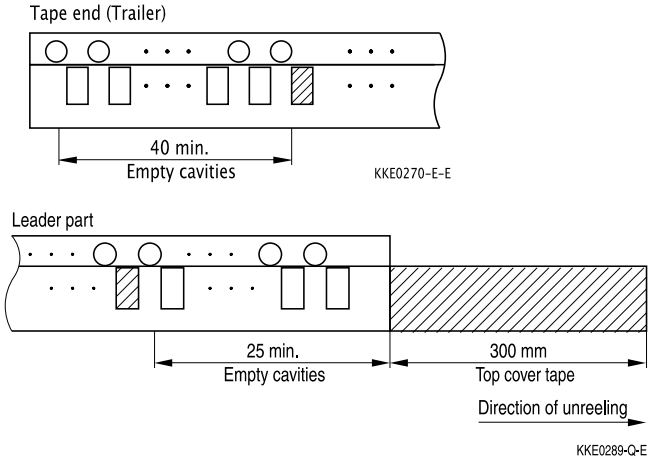
1.3 Reel packing



Dimensions in mm

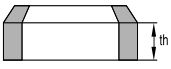
	8-mm tape		12-mm tape		16-mm tape
	180-mm reel	330-mm reel	180-mm reel	330-mm reel	330-mm reel
A	180 −3/+0	330 −2.0	180 −3/+0	330 −2.0	330 −2.0
W_1	8.4 +1.5/−0	8.4 +1.5/−0	12.4 +1.5/−0	12.4 +1.5/−0	16.4 +1.5/−0
W_2	14.4 max.	14.4 max.	18.4 max.	18.4 max.	22.4 max.

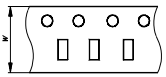
Leader, trailer

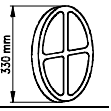


SMD

1.4 Packing units for discrete chip and array chip







Case size inch/mm	Chip thickness th	Cardboard tape W	Blister tape W	∅ 180-mm reel pcs.	∅ 330-mm reel pcs.
0201/0603	0.33 mm	8 mm	–	15000	–
0402/1005	0.6 mm	8 mm	–	10000	–
0405/1012	0.7 mm	8 mm	–	5000	–
0506/1216	0.5 mm	–	8 mm	4000	–
0508/1220	0.9 mm	8 mm	8 mm	4000	–
0603/1608	0.9 mm	8 mm	8 mm	4000	16000
0612/1632	0.9 mm	–	8 mm	3000	–
0805/2012	0.7 mm	–	8 mm	3000	–
	0.9 mm	–	8 mm	3000	12000
	1.3 mm	–	8 mm	3000	–
1003/2508	0.9 mm	8 mm	–	4000	–
1012/2532	1.0 mm	–	8 mm	2000	–
1206/3216	0.9 mm	–	8 mm	3000	–
	1.3 mm	–	8 mm	3000	–
	1.4 mm	–	8 mm	2000	–
	1.6 mm	–	8 mm	2000	–
1210/3225	0.9 mm	–	8 mm	3000	–
	1.3 mm	–	8 mm	3000	–
	1.4 mm	–	8 mm	2000	–
	1.6 mm	–	8 mm	2000	–
1812/4532	1.3 mm	–	12 mm	1500	–
	1.4 mm	–	12 mm	1000	–
	1.6 mm	–	12 mm	–	4000
	2.3 mm	–	12 mm	–	3000
2220/5750	1.3 mm	–	12 mm	1500	–
	1.4 mm	–	12 mm	1000	–
	2.0 mm	–	12 mm	–	3000
	2.3 mm	–	12 mm	–	3000
3225	3.2 mm	–	16 mm	–	1000
	4.5 mm	–	16 mm	–	1000
4032	3.2 mm	–	16 mm	–	1000
	4.5 mm	–	16 mm	–	1000

2 Delivery mode for leaded SHCV varistors

Standard delivery mode for SHCV types is bulk. Alternative taping modes (AMMO pack or taped on reel) are available upon request.

Packing units for:

Type	Pieces
SR6	2000
SR1 / SR2	1000

For types not listed in this data book please contact EPCOS.

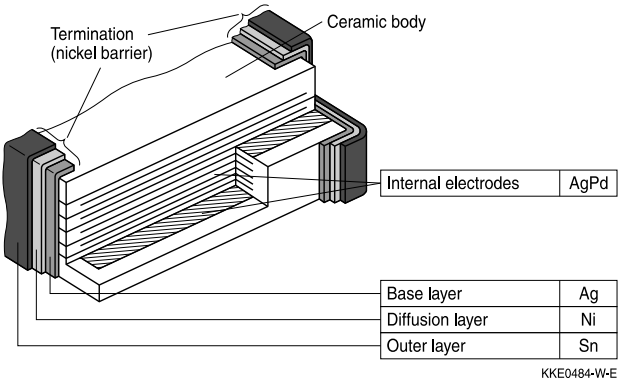
SMD

Soldering directions

1 Terminations

1.1 Nickel barrier termination

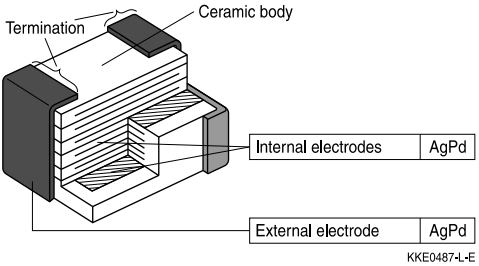
The nickel barrier layer of the silver/nickel/tin termination prevents leaching of the silver base metallization layer. This allows great flexibility in the selection of soldering parameters. The tin prevents the nickel layer from oxidizing and thus ensures better wetting by the solder. The nickel barrier termination is suitable for all commonly-used soldering methods.



Multilayer CTVS: Structure of nickel barrier termination

1.2 Silver-palladium termination

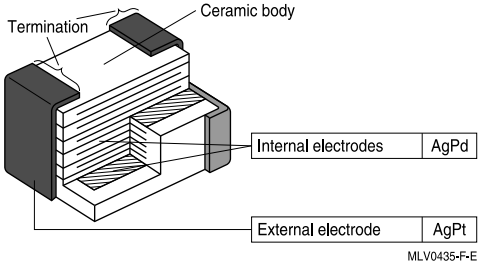
Silver-palladium terminations are used for the large case sizes 1812 and 2220 and for chips intended for conductive adhesion. This metallization improves the resistance of large chips to thermal shock.
In case of conductive adhesion, the silver-palladium metallization reduces susceptibility to corrosion. Silver-palladium termination can be used for smaller case sizes (only chip) for hybrid applications as well. The silver-palladium termination is not approved for lead-free soldering.



Multilayer varistor: Structure of silver-palladium termination

1.3 Silver-platinum termination

Silver-platinum terminations are mainly used for the large case sizes 1812 and 2220. The silver-platinum termination is approved for reflow soldering, SnPb soldering and lead-free soldering with a silver containing solder paste. In case of SnPb soldering, a solder paste Sn62Pb36Ag2 is recommended. For lead-free reflow soldering, a solder paste SAC, e.g. Sn95.5Ag3.8Cu0.7, is recommended.

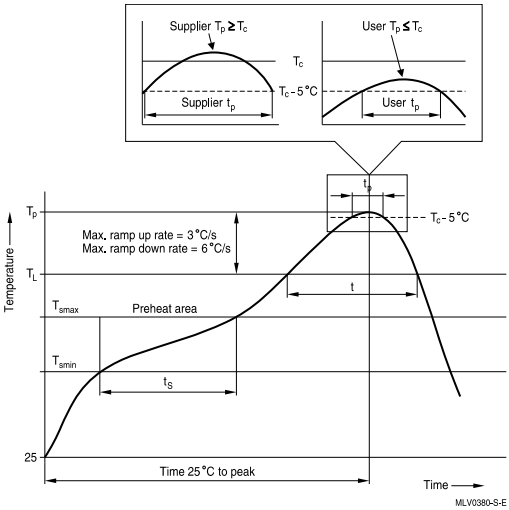


Multilayer varistor: Structure of silver-platinum termination

2 Recommended soldering temperature profiles

2.1 Reflow soldering temperature profile

Recommended temperature characteristic for reflow soldering following JEDEC J-STD-020D



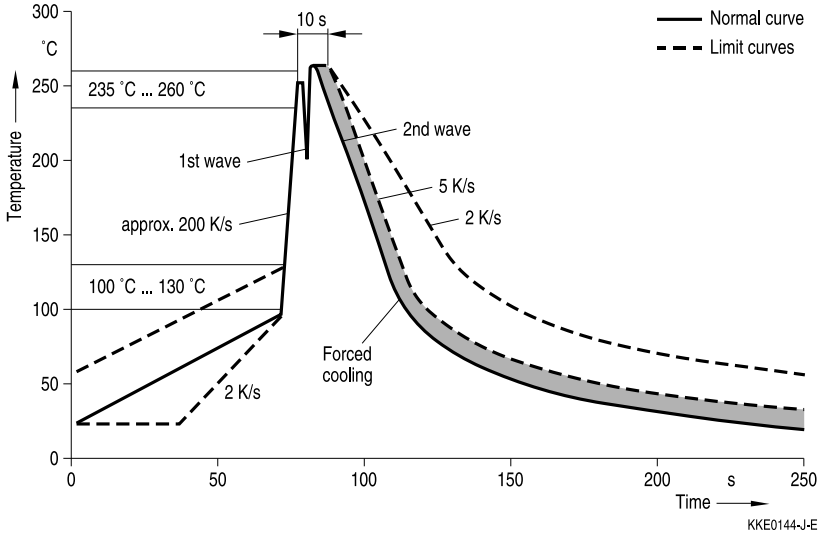
Profile feature		Sn-Pb eutectic assembly	Pb-free assembly
Preheat and soak			
- Temperature min	T_{smin}	100 °C	150 °C
- Temperature max	T_{smax}	150 °C	200 °C
- Time	t_{smin} to t_{smax}	60 ... 120 s	60 ... 180 s
Average ramp-up rate	T_{smax} to T_p	3 °C/ s max.	3 °C/ s max.
Liquidous temperature	T_L	183 °C	217 °C
Time at liquidous	t_L	60 ... 150 s	60 ... 150 s
Peak package body temperature	T_p [1]	220 °C ... 235 °C [2]	245 °C ... 260 °C [2]
Time (t_P) [3] within 5 °C of specified classification temperature (T_c)		20 s [3]	30 s [3]
Average ramp-down rate	T_p to T_{smax}	6 °C/ s max.	6 °C/ s max.
Time 25 °C to peak temperature		maximum 6 min	maximum 8 min

1) Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.
2) Depending on package thickness. For details please refer to JEDEC J-STD-020D.
3) Tolerance for time at peak profile temperature (t_P) is defined as a supplier minimum and a user maximum.

Note: All temperatures refer to topside of the package, measured on the package body surface. Number of reflow cycles: 3

2.2 Wave soldering temperature profile

Temperature characteristics at component terminal with dual-wave soldering



2.3 Lead-free soldering processes

EPCOS multilayer CTVS with AgNiSn termination are designed for the requirements of lead-free soldering processes only.
Soldering temperature profiles to JEDEC J-STD-020D, IEC 60068-2-58 and ZVEI recommendations.

3 Recommended soldering methods - type-specific releases by EPCOS

3.1 Overview

		Reflow soldering		Wave soldering	
Type	Case size	SnPb	Lead-free	SnPb	Lead-free
CT... / CD...	0201/ 0402	Approved	Approved	No	No
CT... / CD...	0603 ... 2220	Approved	Approved	Approved	Approved
CN...	0603 ... 2220	Approved	No	Approved	No
CN...K2	1812, 2220	Approved	Approved	No	No
Arrays	0405 ... 1012	Approved	Approved	No	No
ESD/EMI filters	0405, 0508	Approved	Approved	No	No
CU	3225, 4032	Approved	Approved	Approved	Approved
SHCV	-	No	No	Approved	Approved

3.2 Nickel barrier and AgPt terminated multilayer CTVS

All EPCOS MLVs with nickel barrier and AgPt termination are suitable and fully qualiyfied for lead-free soldering. The nickel barrier layer is 100% matte tin-plated.

3.3 Silver-palladium terminated MLVs

AgPd-terminated MLVs are mainly designed for conductive adhesion technology on hybrid material. Additionally MLVs with AgPd termination are suitable for reflow and wave soldering with SnPb solder.

Note:
Lead-free soldering is not approved for MLVs with AgPd termination.

3.4 Silver-platinum terminated MLVs

The silver-platinum termination is approved for reflow soldering, SnPb soldering and lead-free with a silver containing solder paste. In case of SnPb soldering, a solder paste Sn62Pb36Ag2 is recommended. For lead-free reflow soldering, a solder paste SAC, e.g. Sn95.5Ag3.8Cu0.7, is recommended.

3.5 Tinned copper alloy

All EPCOS CU types with tinned termination are approved for lead-free and SnPb soldering.

3.6 Tinned iron wire

All EPCOS SHCV types with tinned termination are approved for lead-free and SnPb soldering.

4 Solder joint profiles / solder quantity

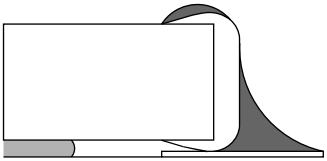
4.1 Nickel barrier termination

If the meniscus height is too low, that means the solder quantity is too low, the solder joint may break, i.e. the component becomes detached from the joint. This problem is sometimes interpreted as leaching of the external terminations.

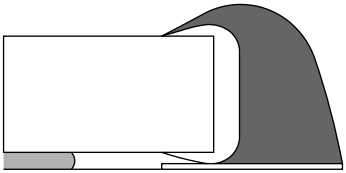
If the solder meniscus is too high, i.e. the solder quantity is too large, the vise effect may occur. As the solder cools down, the solder contracts in the direction of the component. If there is too much solder on the component, it has no leeway to evade the stress and may break, as in a vise.

The figures below show good and poor solder joints for dual-wave and infrared soldering.

4.1.1 Solder joint profiles for nickel barrier termination - dual-wave soldering



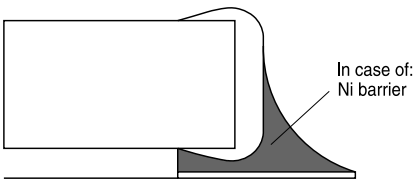
Good solder joint KKE0287-9-E



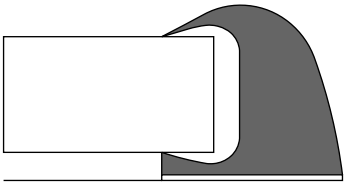
Too much solder
Pad geometry too large,
not soldered in preferred direction KKE0288-H-E

Good and poor solder joints caused by amount of solder in dual-wave soldering.

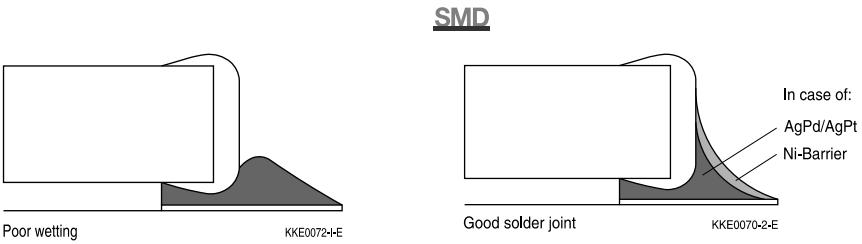
4.1.2 Solder joint profiles for nickel barrier termination / silver-palladium / silver-platinum termination - reflow soldering



Good solder joint MLV0196-B-E

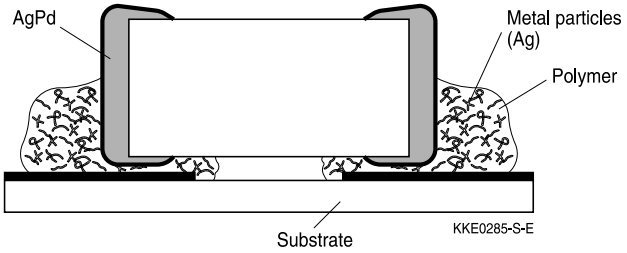


Too much solder
Pad geometry too large KKE0071-A-E



Good and poor solder joints caused by amount of solder in reflow soldering.

5 Conductive adhesion



Attaching surface-mounted devices (SMDs) with electrically conductive adhesives is a commercially attractive method of component connection to supplement or even replace conventional soldering methods.

Electrically conductive adhesives consist of a non-conductive plastic (epoxy resin, polyimide or silicon) in which electrically conductive metal particles (gold, silver, palladium, nickel, etc) are embedded. Electrical conduction is effected by contact between the metal particles.

Adhesion is particularly suitable for meeting the demands of hybrid technology. The adhesives can be deposited ready for production requirements by screen printing, stamping or by dispensers. As shown in the following table, conductive adhesion involves two work operations fewer than soldering.

Reflow soldering	Wave soldering	Conductive adhesion
Screen-print solder paste	Apply glue dot	Screen-print conductive adhesive
Mount SMD	Mount SMD	Mount SMD
Predry solder paste	Cure glue	Cure adhesive
Reflow soldering	Wave soldering	Inspect
Wash	Wash	
Inspect	Inspect	

A further advantage of adhesion is that the components are subjected to virtually no temperature shock at all. The curing temperatures of the adhesives are between 120 °C and 180 °C, typical curing times are between 30 minutes and one hour.

The bending strength of glued chips is, in comparison with that of soldered chips, higher by a factor of at least 2, as is to be expected due to the elasticity of the glued joints.

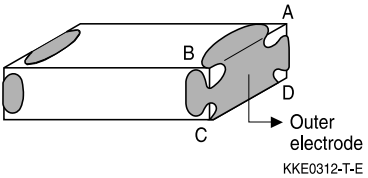
The lower conductivity of conductive adhesive may lead to higher contact resistance and thus result in electrical data different to those of soldered components. Users must pay special attention to this in RF applications.

6 Solderability tests

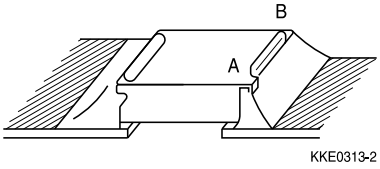
Test	Standard	Test conditions Sn-Pb soldering	Test conditions Pb-free soldering	Criteria/ test results
Wettability	IEC 60068-2-58	Immersion in 60/40 SnPb solder using non-activated flux at 215 ± 3 °C for 3 ± 0.3 s	Immersion in Sn96.5Ag3.0Cu0.5 solder using non- or low activated flux at 245 ± 5 °C for 3 ± 0.3 s	Covering of 95% of end termination, checked by visual inspection
Leaching resistance	IEC 60068-2-58	Immersion in 60/40 SnPb solder using mildly activated flux without preheating at 260 ± 5 °C for 10 ±1 s	Immersion in Sn96.5Ag3.0Cu0.5 solder using non- or low activated flux without preheating at 255 ± 5 °C for 10 ±1 s	No leaching of contacts
Thermal shock (solder shock)		Dip soldering at 300 °C/5 s	Dip soldering at 300 °C/5 s	No deterioration of electrical parameters. Capacitance change: ≤ ±15%
Tests of resistance to soldering heat for SMDs	IEC 60068-2-58	Immersion in 60/40 SnPb for 10 s at 260 °C	Immersion in Sn96.5Ag3.0Cu0.5 for 10 s at 260 °C	Change of varistor voltage: ≤ ±5%
Tests of resistance to soldering heat for radial leaded components (SHCV)	IEC 60068-2-20	Immersion of leads in 60/40 SnPb for 10 s at 260 °C	Immersion of leads in Sn96.5Ag3.0Cu0.5 for 10 s at 260 °C	Change of varistor voltage: ≤ ±5% Change of capacitance X7R: ≤ −5/+10%

Note:
Leaching of the termination

Effective area at the termination might be lost if the soldering temperature and/or immersion time are not kept within the recommended conditions. Leaching of the outer electrode should not exceed 25% of the chip end area (full length of the edge A-B-C-D) and 25% of the length A-B, shown below as mounted on substrate.



As a single chip



As mounted on substrate

7 Notes for proper soldering

7.1 Preheating and cooling

- According to JEDEC J-STD-020D. Please refer to chapter 2.

7.2 Repair / rework

Manual soldering with a soldering iron must be avoided, hot-air methods are recommended for rework purposes.

7.3 Cleaning

All environmentally compatible agents are suitable for cleaning. Select the appropriate cleaning solution according to the type of flux used. The temperature difference between the components and cleaning liquid must not be greater than 100 °C. Ultrasonic cleaning should be carried out with the utmost caution. Too high ultrasonic power can impair the adhesive strength of the metallized surfaces.

7.4 Solder paste printing (reflow soldering)

An excessive application of solder paste results in too high a solder fillet, thus making the chip more susceptible to mechanical and thermal stress. Too little solder paste reduces the adhesive strength on the outer electrodes and thus weakens the bonding to the PCB. The solder should be applied smoothly to the end surface.

7.5 Adhesive application

Thin or insufficient adhesive causes chips to loosen or become disconnected during curing. Low viscosity of the adhesive causes chips to slip after mounting. It is advised to consult the manufacturer of the adhesive on proper usage and amounts of adhesive to use.

7.6 Selection of flux

Used flux should have less than or equal to 0.1 wt % of halogenated content, since flux residue after soldering could lead to corrosion of the termination and/or increased leakage current on the surface of the component. Strong acidic flux must not be used. The amount of flux applied should be carefully controlled, since an excess may generate flux gas, which in turn is detrimental to solderability.

7.7 Storage of CTVSs

Solderability is guaranteed for one year from date of delivery for multilayer varistors, CeraDiodes and ESD/EMI filters (half a year for chips with AgPd and AgPt terminations) and two years for SHCV and CU components, provided that components are stored in their original packages.

Storage temperature: −25 °C to +45 °C

Relative humidity: ≤75% annual average, ≤95% on 30 days a year

The solderability of the external electrodes may deteriorate if SMDs and leaded components are stored where they are exposed to high humidity, dust or harmful gas (hydrogen chloride, sulfurous acid gas or hydrogen sulfide).

Do not store SMDs and leaded components where they are exposed to heat or direct sunlight. Otherwise the packing material may be deformed or SMDs/ leaded components may stick together, causing problems during mounting.

After opening the factory seals, such as polyvinyl-sealed packages, it is recommended to use the SMDs or leaded components as soon as possible.

7.8 Placement of components on circuit board

Especially in the case of dual-wave soldering, it is of advantage to place the components on the board before soldering in that way that their two terminals do not enter the solder bath at different times.
Ideally, both terminals should be wetted simultaneously.

7.9 Soldering cautions

- An excessively long soldering time or high soldering temperature results in leaching of the outer electrodes, causing poor adhesion and a change of electrical properties of the varistor due to the loss of contact between electrodes and termination.
- Wave soldering must not be applied for MLVs designated for reflow soldering only.
- Keep the recommended down-cooling rate.

7.10 Standards

CECC 00802

IEC 60068-2-58

IEC 60068-2-20

JEDEC J-STD-020D

SMD

Symbols and terms

Symbol	Term
$C_{line,typ}$	Typical capacitance per line
C_{max}	Maximum capacitance
C_{min}	Minimum capacitance
C_{nom}	Nominal capacitance
ΔC_{nom}	Tolerance of nominal capacitance
C_{typ}	Typical capacitance
$f_{cut\text{-}off,min}$	Minimum cut-off frequency
I	Current
I_{clamp}	Clamping current
I_{leak}	Leakage current
$I_{leak,typ}$	Typical leakage current
I_{PP}	Peak pulse current
$I_{surge,max}$	Maximum surge current (also termed peak current)
LCT	Lower category temperature
L_{typ}	Typical inductance
$P_{diss,max}$	Maximum power dissipation
P_{PP}	Peak pulse power
R_{ins}	Insulation resistance
R_{min}	Minimum resistance
R_S	Resistance per line
T_A	Ambient temperature
T_{op}	Operating temperature
T_{stg}	Storage temperature
t_r	Duration of equivalent rectangular wave
t_{resp}	Response time
UCT	Upper category temperature
V	Voltage
$V_{BR,min}$	Minimum breakdown voltage
$V_{clamp,max}$	Maximum clamping voltage
$V_{DC,max}$	Maximum DC operating voltage (also termed working voltage)
$V_{ESD,air}$	Air discharge ESD capability
$V_{ESD,contact}$	Contact discharge ESD capability
V_{jump}	Maximum jump start voltage