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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Operational Amplifiers

Low Noise Operational Amplifiers

BA2107G BA2115xxx

General Description

The BA2107/BA2115 are single and dual operational amplifier with high gain and high slew rate(4v/μs). The BA2107/BA2115 have good performance of input referred noise voltage(7 $nV/\sqrt{Hz}$) and total harmonic distortion(0.008%). These are suitable for Audio applications.

Features

- High Voltage Gain
- Low Input Referred Noise Voltage
- Low Total Harmonic Distortion
- Wide Operating Supply Voltage

Application

- Audio Application
- Potable Equipment
- Consumer Electronics

Key Specification

- Wide Operating Supply Voltage (split supply): ±1.0V to ±7.0V
- Operating Temperature Range: -40°C to +85°C
- Slew Rate: 4V/μs(Typ)
- Total Harmonic Distortion : 0.008%(Typ)
- Input Referred Noise Voltage : 7 $nV/\sqrt{Hz}$ (Typ)

Packages

	W(Typ)xD(Typ) xH(Max)
SSOP5	2.90mm x 2.80mm x 1.25mm
SOP8	5.00mm x 6.20mm x 1.71mm
SOP-J8	4.90mm x 6.00mm x 1.65mm
MSOP8	2.90mm x 4.00mm x 0.90mm

Simplified Schematic

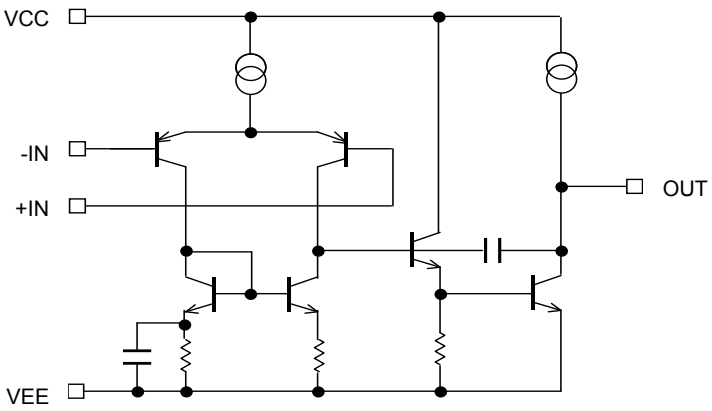
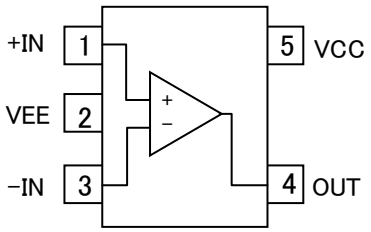


Figure 1. Simplified Schematic

○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

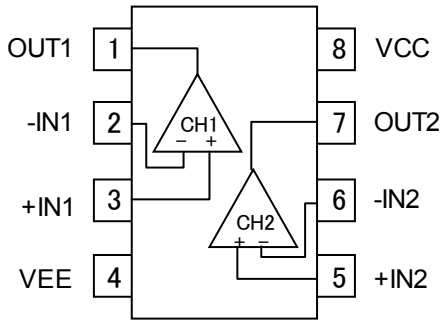
Pin Configuration

SSOP5



Pin No.	Pin Name
1	+IN1
2	VEE
3	-IN1
4	OUT
5	VCC

SOP8, SOP-J8, MSOP8



Pin No.	Pin Name
1	OUT1
2	-IN1
3	+IN1
4	VEE
5	+IN2
6	-IN2
7	OUT2
8	VCC

Package			
SSOP5	SOP8	SOP-J8	MSOP8
BA2107G	BA2115F	BA2115FJ	BA2115FVM

Ordering Information

B A 2 1 x x x x x - x x

Part Number
BA2107G
BA2115xxx

Package
G : SSOP5
F : SOP8
FJ : SOP-J8
FVM : MSOP8

Packaging and forming specification
E2: Embossed tape and reel (SOP8/SOP-J8)
TR: Embossed tape and reel (SSOP5/MSOP8)

Line-up

Operating Temperature Range	Operating Supply Voltage (split supply)	Supply Current (Typ)	Slew Rate (Typ)	Package		Orderable Part Number
-40°C to +85°C	±1.0V to ±7.0V	3.5mA	4V/µs	SSOP5	Reel of 3000	BA2107G-TR
				SOP8	Reel of 2500	BA2115F-E2
				SOP-J8	Reel of 2500	BA2115FJ-E2
				MSOP8	Reel of 3000	BA2115FVM-TR

Absolute Maximum Ratings (T_A=25℃)

○BA2107, BA2115

Parameter	Symbol		Ratings	Unit
Supply Voltage	VCC-VEE		+14	V
Power Dissipation	P_D	SSOP5	0.67(Note 1,4)	W
		SOP8	0.78(Note 2,4)	
		SOP-J8	0.67(Note 1,4)	
		MSOP8	0.59(Note 3,4)	
Differential Input Voltage (Note 5)	C		+14	V
Input Common-mode Voltage Range	V_{ICM}		(VEE-0.3) to (VEE+14)	V
Input Current(Note 6)	I_I		-10	mA
Operating Supply Voltage	V_{opr}		2 to 14(±1 to ±7)	V
Operating Temperature	T_{opr}		-40 to +85	℃
Storage Temperature	T_{stg}		-55 to 150	℃
Maximum Junction Temperature	T_{Jmax}		+150	℃

(Note 1) To use at temperature above T_A=25℃ reduce 5.4mW/℃
(Note 2) To use at temperature above T_A=25℃ reduce 6.2mW/℃
(Note 3) To use at temperature above T_A=25℃ reduce 4.8mW/℃
(Note 4) Mounted on a FR4 glass epoxy PCB 70mm×70mm×1.6mm (copper foil area less than 3%).
(Note 5) The voltage difference between inverting input and non-inverting input is the differential input voltage.
Then input terminal voltage is set to more than VEE.
(Note 6) An excessive input current will flow when input voltages of more than VCC+0.6V or less than VEE-0.6V are applied.
The input current can be set to less than the rated current by adding a limiting resistor.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

Electrical Characteristics

○BA2107 (Unless otherwise specified VCC=+2.5V, VEE=-2.5V, T_A=25°C)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Input Offset Voltage (Note 7)	V_{IO}	-	1	6	mV	VOUT=0V, V_{ICM}=0V
Input Offset Current (Note 7)	I_{IO}	-	2	200	nA	VOUT=0V, V_{ICM}=0V
Input Bias Current (Note 8)	I_B	-	150	400	nA	VOUT=0V, V_{ICM}=0V
Supply Current	I_{CC}	-	1.8	3.0	mA	Av=0dB, R_L=∞, +IN=0V
Maximum Output Voltage(High)	V_{OH}	4.5	4.8	-	V	R_L≧2.5kΩ, V_{OHmin}=VCC-0.5V
		-	11.6	-		R_L≧10kΩ, VCC=12V, VEE=0V V_{RL}=6V, V_{OH}=VCC-0.4V
		-	15.5	-		R_L≧10kΩ, VCC=16V, VEE=0V V_{RL}=8V, V_{OH}=VCC-0.5V
Maximum Output Voltage(Low)	V_{OL}	0.5	0.2	-	V	R_L≧2.5kΩ, V_{OLmin}=VEE+0.5V
		-	0.4	-		R_L≧10kΩ, VCC=12V, VEE=0V V_{RL}=6V, V_{OL}=VEE+0.4V
		-	0.5	-		R_L≧10kΩ, VCC=16V, VEE=0V V_{RL}=8V, V_{OL}=VEE+0.5V
Output Source Current	I_{SOURCE}	-	1.4	-	mA	-
Output Sink Current	I_{SINK}	-	90	-	mA	-
Large Signal Voltage Gain	Av	60	80	-	dB	R_L≧10kΩ, VOUT=2.5±2V V_{ICM}=2.5V
Input Common-mode Voltage Range	V_{ICM}	±1.5	-	-	V	(VEE+1.0V) - (VCC-1.0V)
Common-mode Rejection Ratio	CMRR	60	74	-	dB	V_{ICM}=-1.5V to +1.5V
Power Supply Rejection Ratio	PSRR	60	80	-	dB	VEE=0V, VCC=2V to 16V
Slew Rate	SR	-	4	-	V/μs	Av=0dB, +IN=2V_{P-P}
Gain Bandwidth Product	GBW	-	12	-	MHz	f=10kHz
Unity Gain Frequency	f_T	-	3.4	-	MHz	0dB cross frequency
Input Referred Noise Voltage	V_N	-	7	-	nV/$\sqrt{Hz}$	R_S=600Ω, DIN-AUDIO
		-	0.9	-	μVrms	R_S=600Ω, DIN-AUDIO
Total Harmonic Distortion	THD+N	-	0.008	-	%	Av=20dB, f=1kHz, DIN-AUDIO

(Note 7) Absolute value

(Note 8) Current direction: Since first input stage is composed with PNP transistor, input bias current flows out from IC.

○BA2115 (Unless otherwise specified VCC=+2.5V, VEE=-2.5V, T_A=25°C)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Input Offset Voltage (Note 9)	V_{IO}	-	1	6	mV	VOUT=0V, V_{ICM}=0V
Input Offset Current (Note 9)	I_{IO}	-	2	200	nA	VOUT=0V, V_{ICM}=0V
Input Bias Current (Note 10)	I_B	-	150	400	nA	VOUT=0V, V_{ICM}=0V
Supply Current	I_{CC}	-	3.5	5	mA	Av=0dB, R_L=∞, All Op-Amps +IN=0V
Maximum Output Voltage(High)	V_{OH}	4.5	4.8	-	V	R_L≧2.5kΩ, V_{OHmin}=VCC-0.5V
		-	11.6	-		R_L≧10kΩ, VCC=12V, VEE=0V V_{RL}=6V, V_{OH}=VCC-0.4V
		-	15.5	-		R_L≧10kΩ, VCC=16V, VEE=0V V_{RL}=8V, V_{OH}=VCC-0.5V
Maximum Output Voltage(Low)	V_{OL}	0.5	0.2	-	V	R_L≧2.5kΩ, V_{OLmin}=VEE+0.5V
		-	0.4	-		R_L≧10kΩ, VCC=12V, VEE=0V V_{RL}=6V, V_{OL}=VEE+0.4V
		-	0.5	-		R_L≧10kΩ, VCC=16V, VEE=0V V_{RL}=8V, V_{OL}=VEE+0.5V
Output Source Current	I_{SOURCE}	-	1.4	-	mA	-
Output Sink Current	I_{SINK}	-	90	-	mA	-
Large Signal Voltage Gain	A_V	60	80	-	dB	R_L≧10kΩ, VOUT=±2V V_{ICM}=0V
Input Common-mode Voltage Range	V_{ICM}	±1.5	-	-	V	(VEE+1.0V) - (VCC-1.0V)
Common-mode Rejection Ratio	CMRR	60	74	-	dB	V_{ICM}=-1.5V to +1.5V
Power Supply Rejection Ratio	PSRR	60	80	-	dB	VEE=0V, VCC=2V to 14V
Slew Rate	SR	-	4	-	V/μs	Av=0dB, +IN=2V_{PP}
Gain Bandwidth Product	GBW	-	12	-	MHz	f=10kHz
Unity Gain Frequency	f_T	-	3.4	-	MHz	0dB cross frequency
Input Referred Noise Voltage	V_N	-	7	-	nV/$\sqrt{Hz}$	R_S=600Ω, DIN-AUDIO
		-	0.9	-	μVrms	R_S=600Ω, DIN-AUDIO
Total Harmonic Distortion	THD+N	-	0.008	-	%	Av=20dB, f=1kHz, DIN-AUDIO
Channel Separation	CS	-	100	-	dB	Av=40dB

(Note 9) Absolute value
(Note 10) Current direction: Since first input stage is composed with PNP transistor, input bias current flows out from IC.

Description of Electrical Characteristics

Described below are descriptions of the relevant electrical terms used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacturer's document or general document.

1. Absolute maximum ratings

Absolute maximum rating items indicate the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

(1) Supply Voltage (VCC / VEE)
Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal without deterioration or destruction of characteristics of internal circuit.

(2) Differential Input Voltage (V_{ID})
Indicates the maximum voltage that can be applied between non-inverting and inverting terminals without damaging the IC.

(3) Input Common-mode Voltage Range (V_{ICM})
Indicates the maximum voltage that can be applied to the non-inverting and inverting terminals without deterioration or destruction of electrical characteristics. Input common-mode voltage range of the maximum ratings does not assure normal operation of IC. For normal operation, use the IC within the input common-mode voltage range characteristics.

(4) Power dissipation (P_D)
Indicates the power that can be consumed by the IC when mounted on a specific board at the ambient temperature 25°C (normal temperature). As for package product, Pd is determined by the temperature that can be permitted by the IC in the package (maximum junction temperature) and the thermal resistance of the package.

2. Electrical characteristics

(1) Input Offset Voltage (V_{IO})
Indicates the voltage difference between non-inverting terminal and inverting terminals. It can be translated into the input voltage difference required for setting the output voltage at 0 V.

(2) Input Offset Current (I_{IO})
Indicates the difference of input bias current between the non-inverting and inverting terminals.

(3) Input Bias Current (I_B)
Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias currents at the non-inverting and inverting terminals.

(4) Supply Current (I_{CC})
Indicates the current that flows within the IC under specified no-load conditions.

(5) Maximum Output Voltage(High) / Maximum Output Voltage(Low) (VOH/VOL)
Indicates the voltage range of the output under specified load condition. It is typically divided into maximum output voltage High and low. Maximum output voltage high indicates the upper limit of output voltage. Maximum output voltage low indicates the lower limit.

(6) Output Source Current/ Output Sink Current (I_{source} / I_{sink})
The maximum current that can be output from the IC under specific output conditions. The output source current indicates the current flowing out from the IC, and the output sink current indicates the current flowing into the IC.
indicates the current flowing out from the IC, and the output sink current indicates the current flowing into the IC.

(7) Large Signal Voltage Gain (Av)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
Av = (Output voltage) / (Differential Input voltage)

(8) Input Common-mode Voltage Range (V_{ICM})
Indicates the input voltage range where IC normally operates.

(9) Common-mode Rejection Ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when the input common mode voltage is changed. It is normally the fluctuation of DC.
CMRR = (Change of Input common-mode voltage)/(Input offset fluctuation)

(10) Power Supply Rejection Ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed.
It is normally the fluctuation of DC.
PSRR= (Change of power supply voltage)/(Input offset fluctuation)

(11) Slew Rate (SR)
Indicates the ratio of the change in output voltage with time when a step input signal is applied.

(12) Gain Bandwidth (GBW)
The product of the open-loop voltage gain and the frequency at which the voltage gain decreases 6dB/octave.

(13) Unity gain frequency (f_T)
Indicates a frequency where the voltage gain of operational amplifier is 1.

(14) Input Referred Noise Voltage (V_N)
Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.

(15) Total harmonic distortion + Noise (THD+N)
Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

(16) Channel Separation (CS)
Indicates the fluctuation in the output voltage of the driven channel with reference to the change of output voltage of the channel which is not driven.

Typical Performance Curves

○BA2107

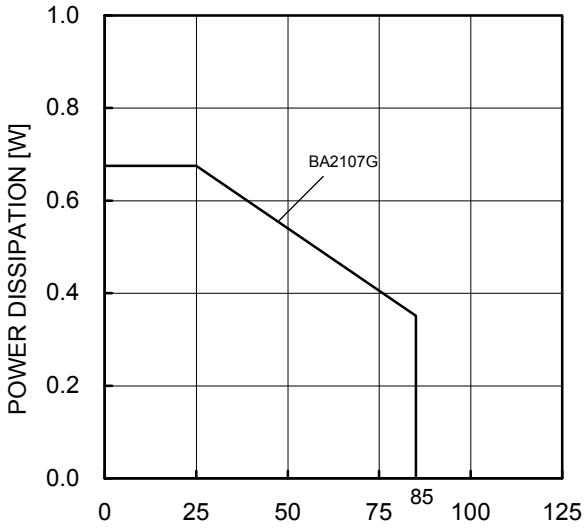


Figure 2.
Derating Curve

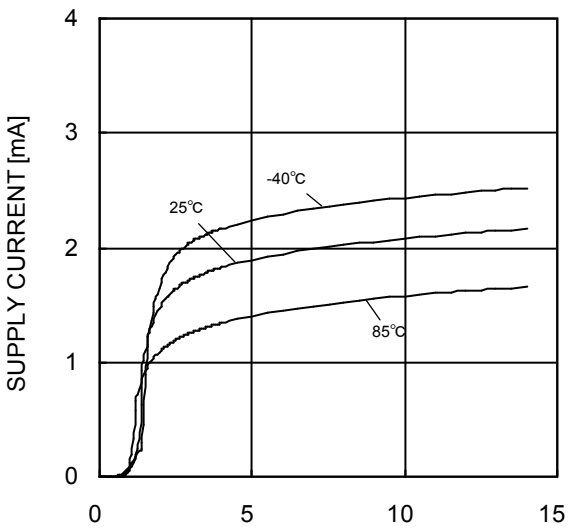


Figure 3.
Supply Current - Supply Voltage

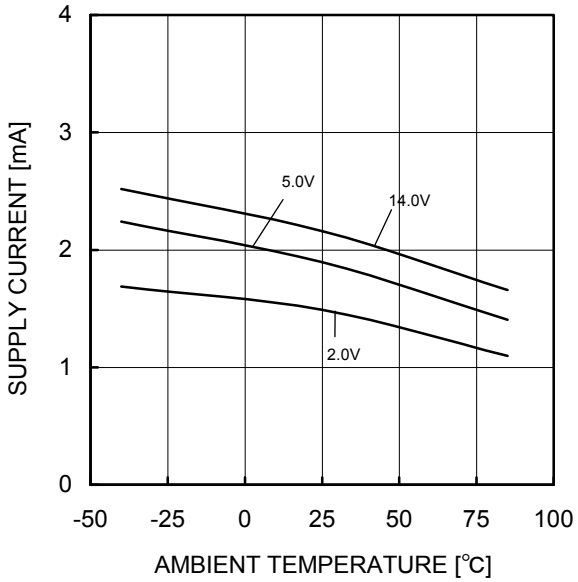


Figure 4.
Supply Current - Ambient Temperature

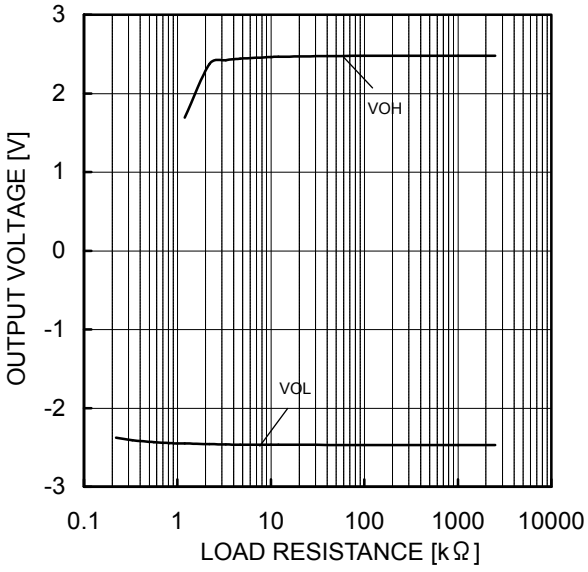


Figure 5.
Output Voltage - Load Resistance
(VCC/VEE=+2.5V/-2.5V)

(*)The above data is measurement value of typical sample, it is not guaranteed.

○BA2107

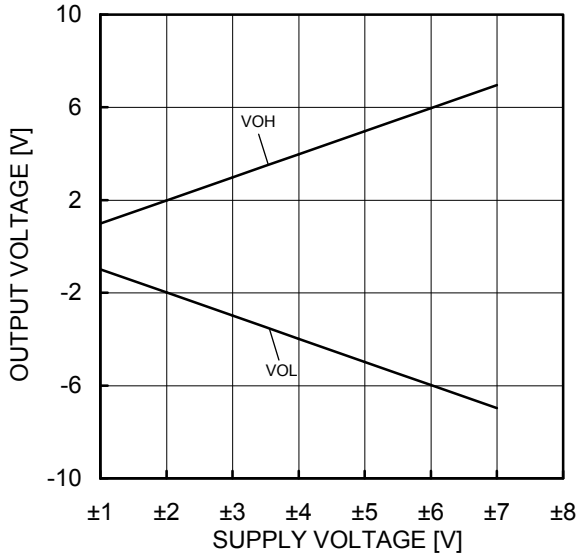


Figure 6.
Output Voltage - Supply Voltage
(R_L=10kΩ)

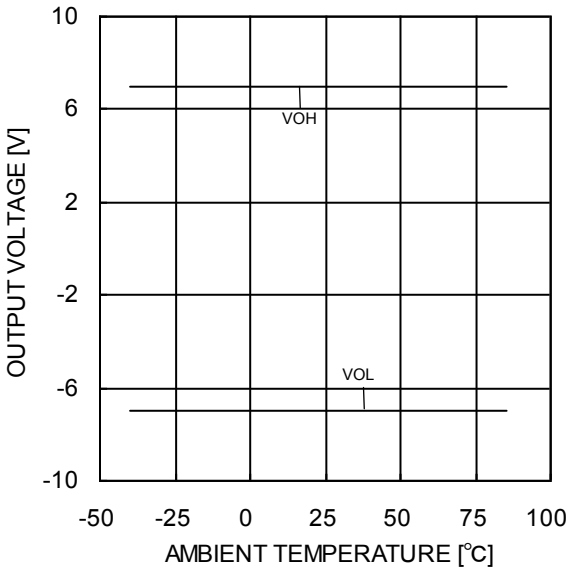


Figure 7.
Output Voltage - Ambient Temperature
(VCC/VEE=+7.0V/-7.0V, R_L=10kΩ)

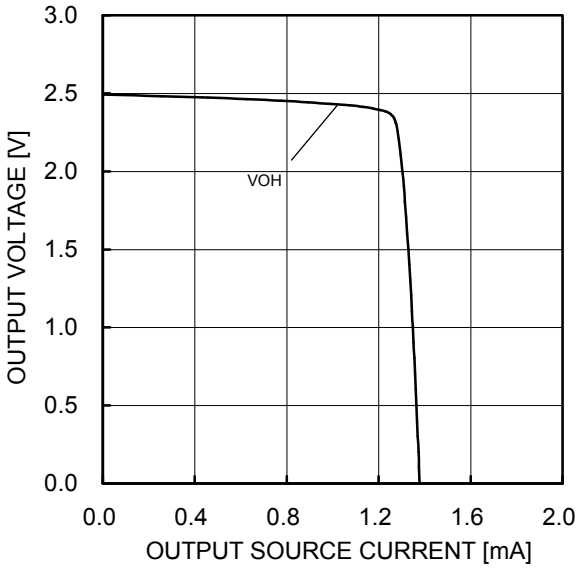


Figure 8.
Output Voltage - Output Source Current
(VCC/VEE=+2.5V/-2.5V)

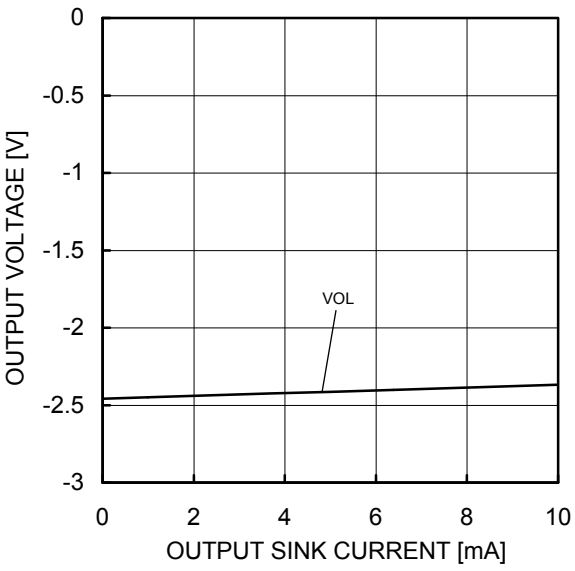


Figure 9.
Output Voltage - Output Sink Current
(VCC/VEE=+2.5V/-2.5V)

(*)The above data is measurement value of typical sample, it is not guaranteed.

○BA2107

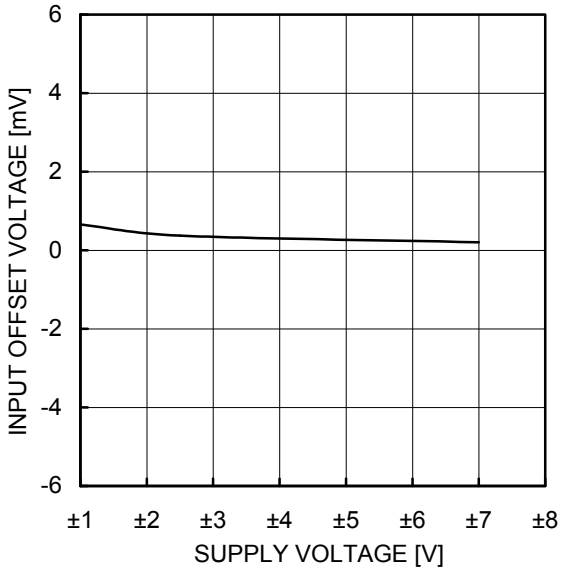


Figure 10.
Input Offset Voltage - Supply Voltage
(V_{ICM}=0V, VOUT=0V)

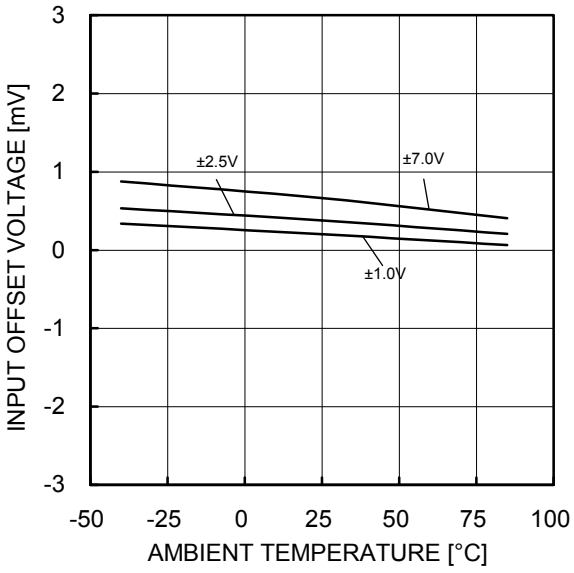


Figure 11.
Input Offset Voltage - Ambient Temperature
(V_{ICM}=0V, VOUT=0V)

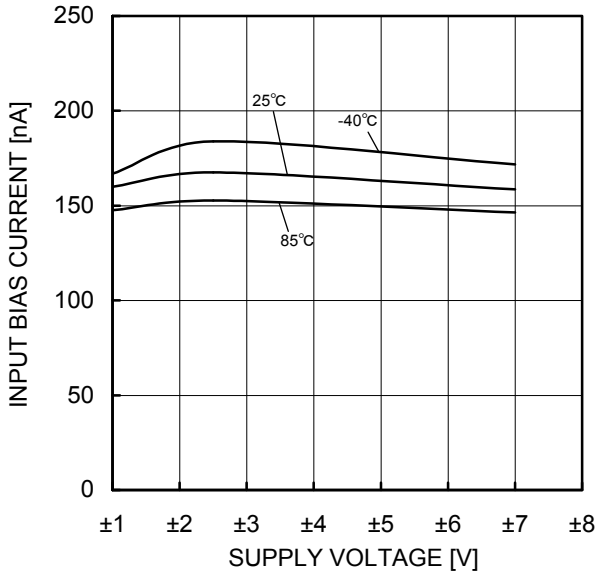


Figure 12.
Input Bias Current - Supply Voltage
(V_{ICM}=0V, VOUT=0V)

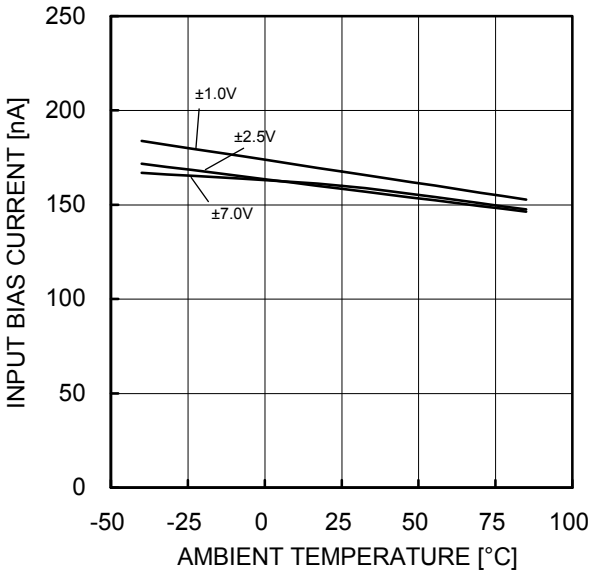


Figure 13.
Input Bias Current - Ambient Temperature
(V_{ICM}=0V, VOUT=0V)

(*)The above data is measurement value of typical sample, it is not guaranteed.

○BA2107

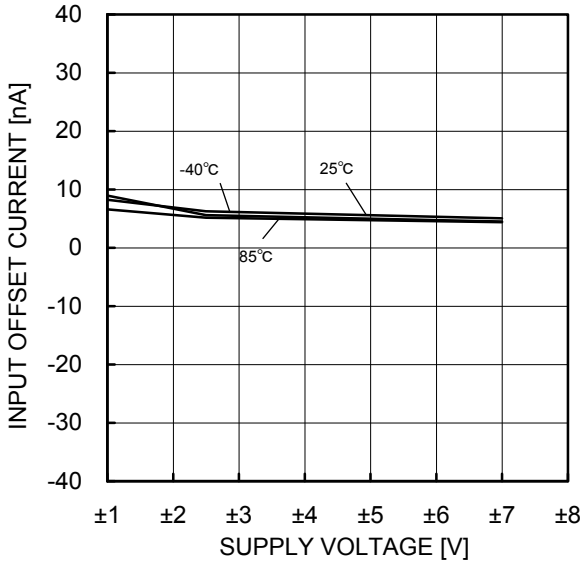


Figure 14.
Input Offset Current - Supply Voltage
(V_{ICM}=0V, VOUT=0V)

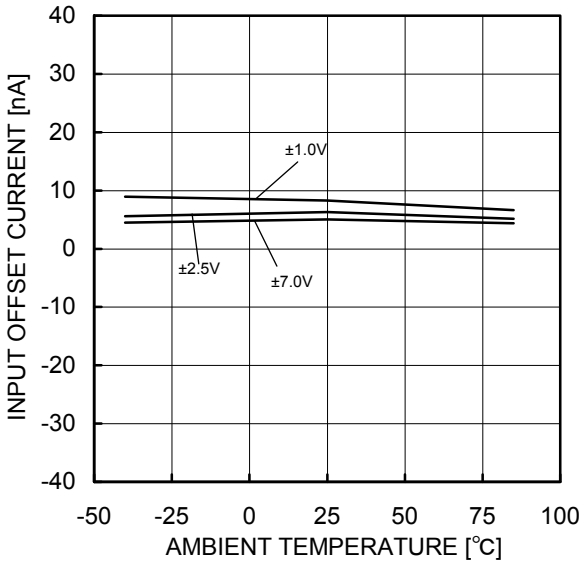


Figure 15.
Input Offset Current - Ambient Temperature
(V_{ICM}=0V, VOUT=0V)

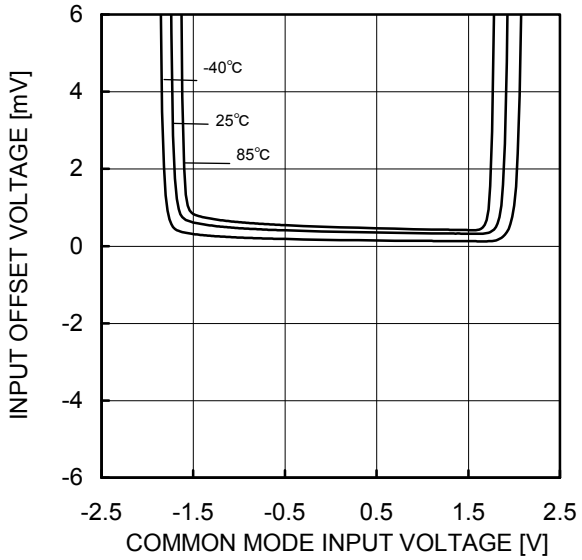


Figure 16.
Input Offset Voltage
- Common Mode Input Voltage
(VCC/VEE=+2.5V/-2.5V, VOUT=0V)

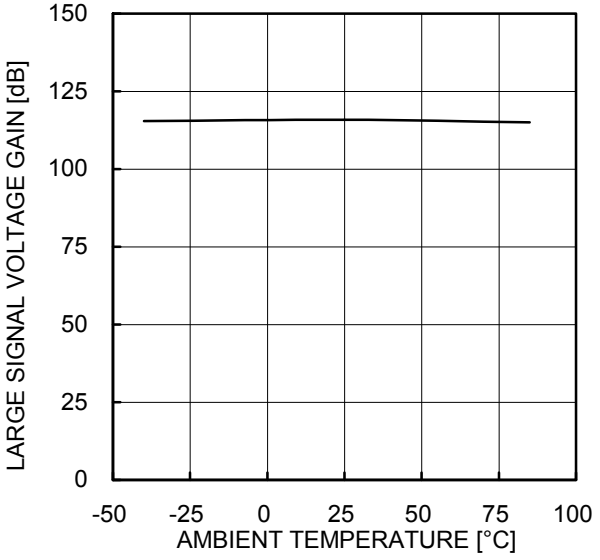


Figure 17.
Large Signal Voltage Gain
- Ambient Temperature
(VCC/VEE=+2.5V/-2.5V)

(*)The above data is measurement value of typical sample, it is not guaranteed.

○BA2107

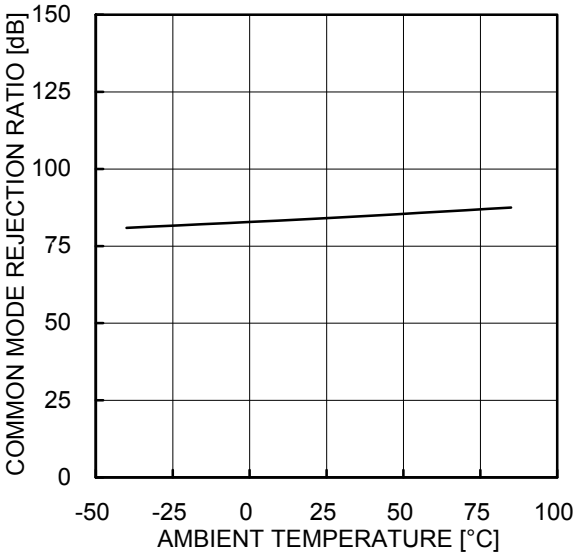


Figure 18.
Common Mode Rejection Ratio
- Ambient Temperature
(VCC/VEE=+2.5V/-2.5V)

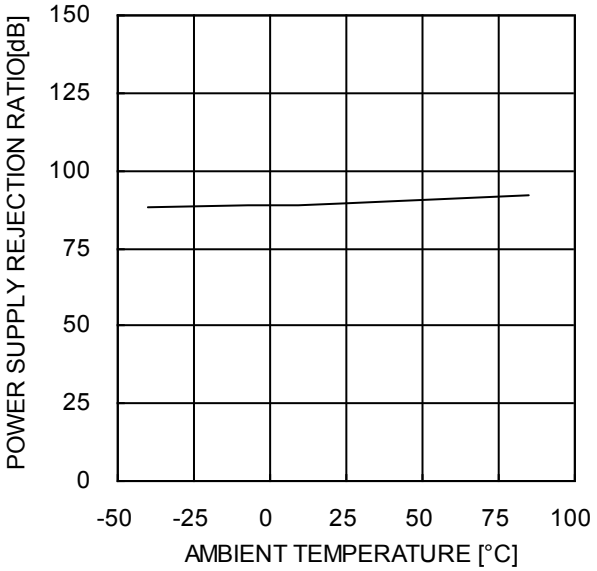


Figure 19.
Power Supply Rejection Ratio
- Ambient Temperature
(VCC/VEE=+2.5V/-2.5V)

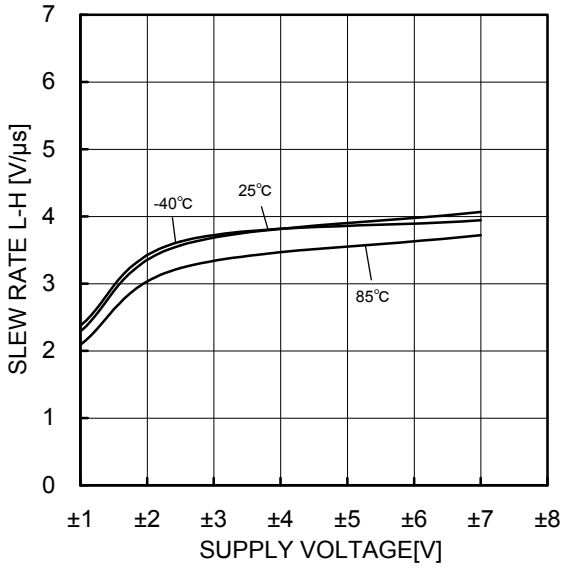


Figure 20.
Slew Rate L-H - Supply Voltage

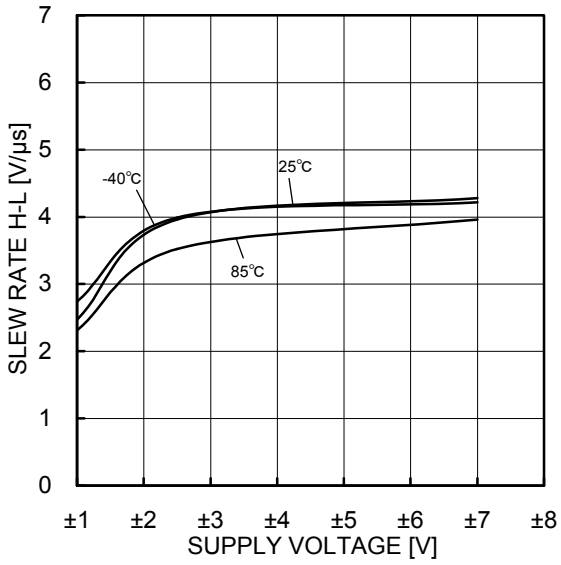


Figure 21.
Slew Rate H-L - Supply Voltage

(*)The above data is measurement value of typical sample, it is not guaranteed.

○BA2107

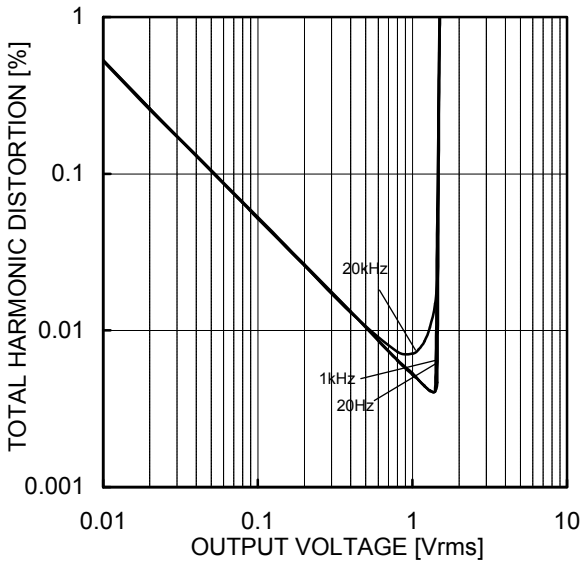


Figure 22.
Total Harmonic Distortion - Output Voltage
(VCC/VEE=2.5V/-2.5V, R_L=2kΩ
80kHz-LPF, T_A=25℃)

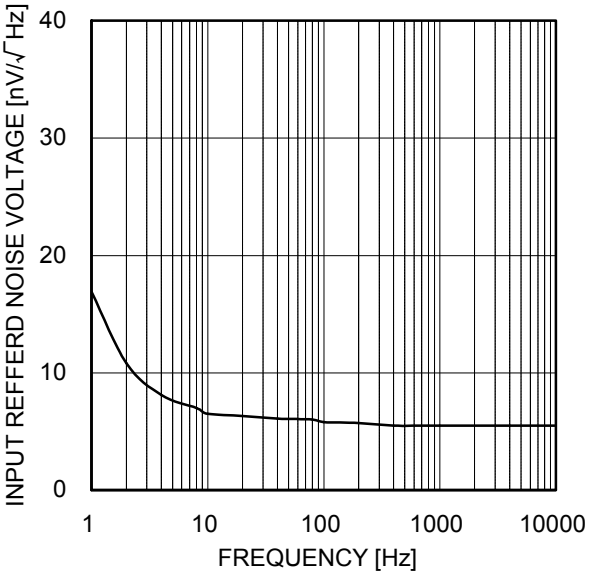


Figure 23.
Equivalent Input Noise Voltage - Frequency
(VCC/VEE=2.5V/-2.5V)

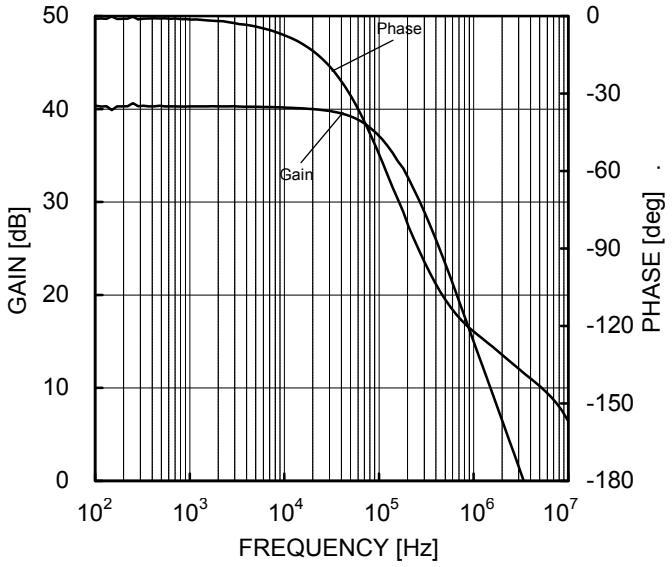


Figure 24.
Voltage Gain - Frequency
(VCC/VEE=2.5V/-2.5V, Av=40dB, R_L=10kΩ)

(*)The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves

○BA2115

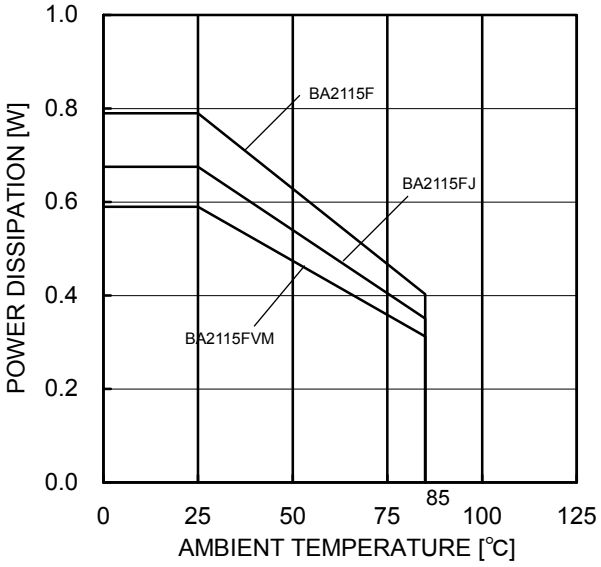


Figure 25.
Derating Curve

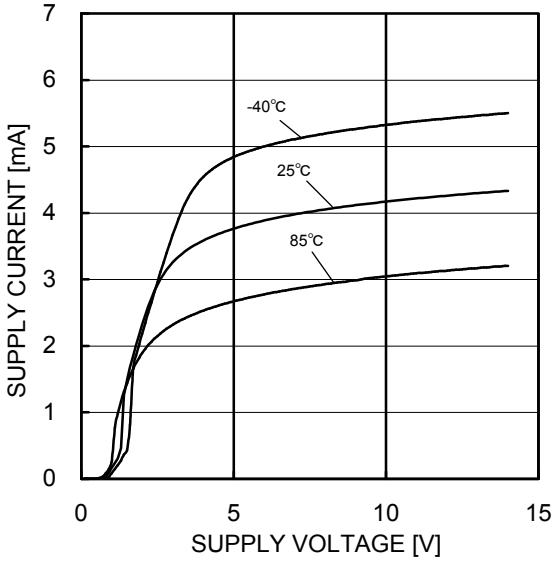


Figure 26.
Supply Current - Supply Voltage

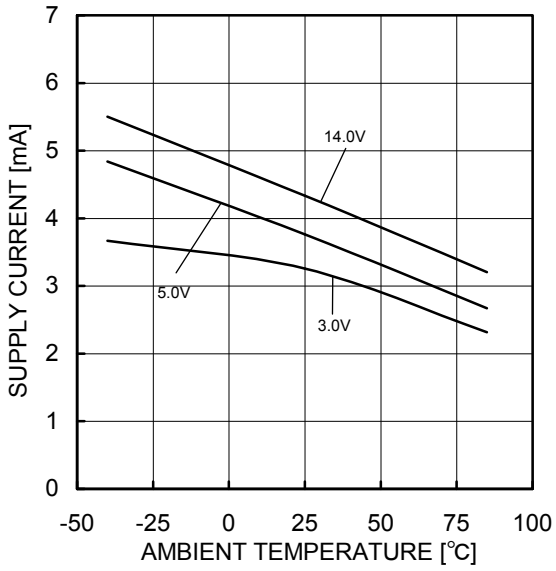


Figure 27.
Supply Current - Ambient Temperature

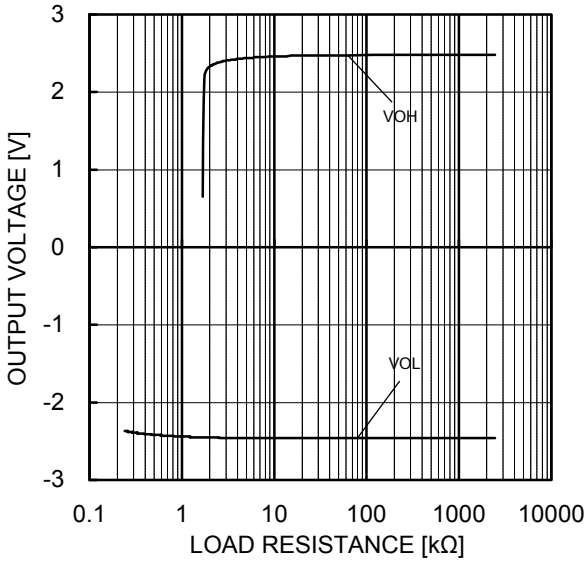


Figure 28.
Output Voltage - Load Resistance
(VCC/VEE=+2.5V/-2.5V)

(*)The above data is measurement value of typical sample, it is not guaranteed.

○BA2115

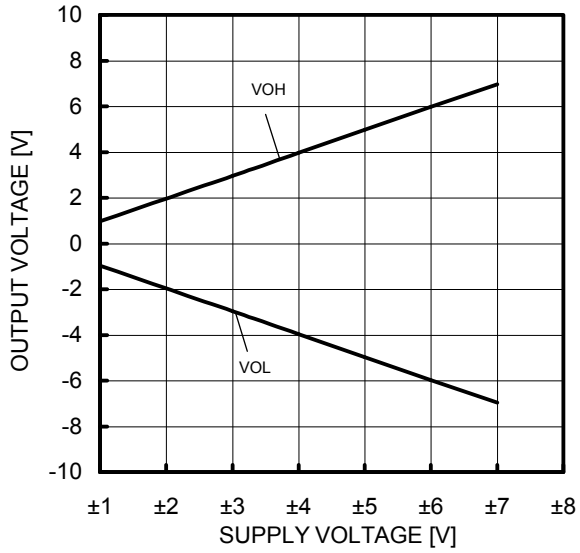


Figure 29.
Maximum Output Voltage
- Supply Voltage
(R_L=10kΩ)

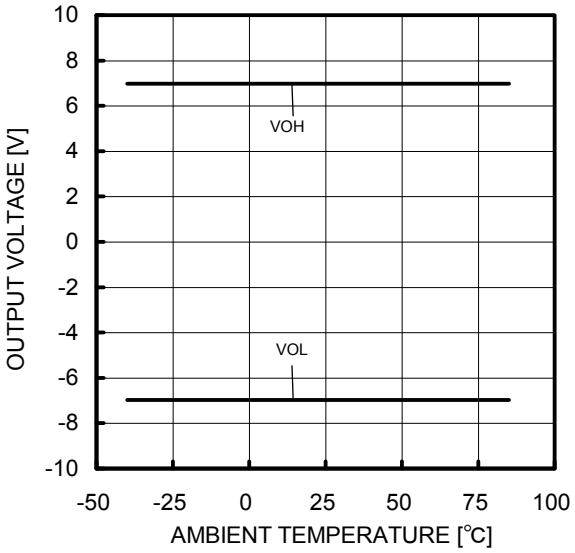


Figure 30.
Maximum Output Voltage
- Ambient Temperature
(VCC/VEE=+7V/-7V, R_L=10kΩ)

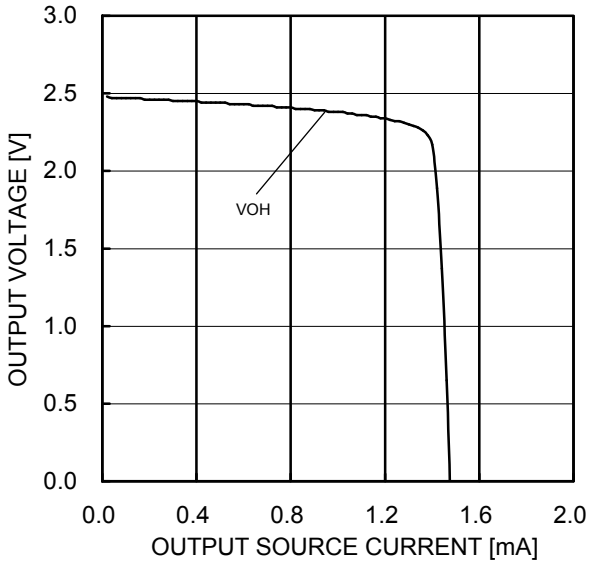


Figure 31.
Maximum Output Voltage
- Output Source Current
(VCC/VEE=+2.5V/-2.5V)

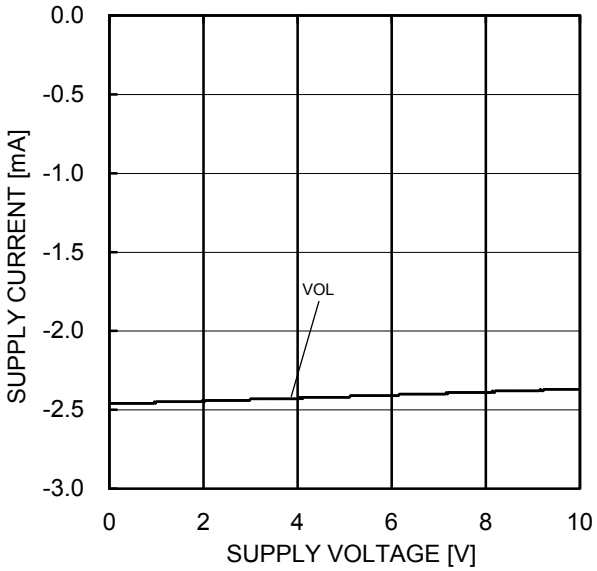


Figure 32.
Maximum Output Voltage
- Output Sink Current
(VCC/VEE=+2.5V/-2.5V)

(*)The above data is measurement value of typical sample, it is not guaranteed.

○BA2115

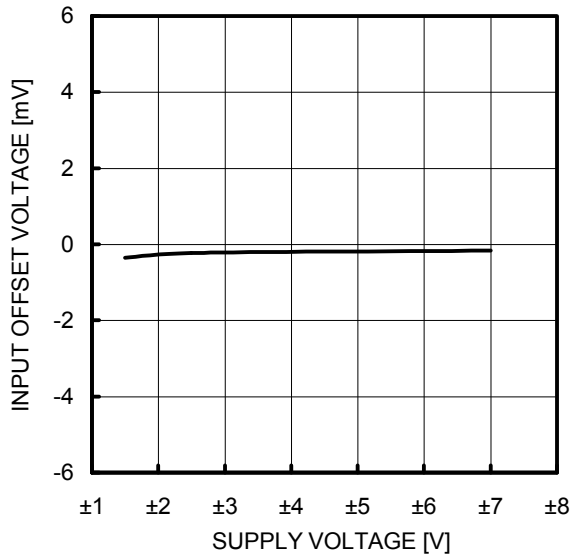


Figure 33.
Input Offset Voltage - Supply Voltage
(V_{ICM}=0V, VOUT=0V)

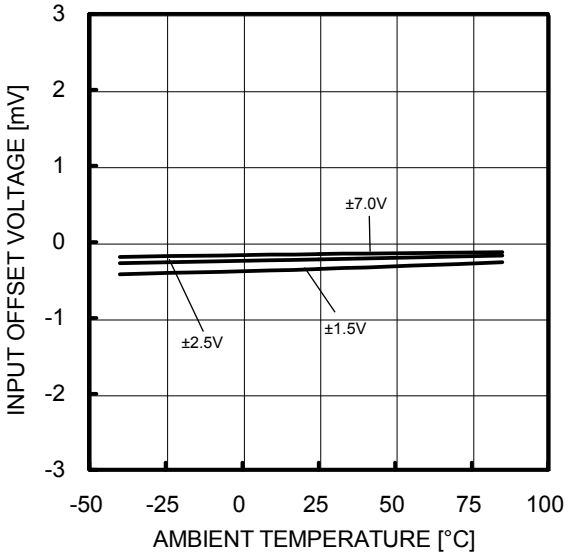


Figure 34.
Input Offset Voltage - Ambient Temperature
(V_{ICM}=0V, VOUT=0V)

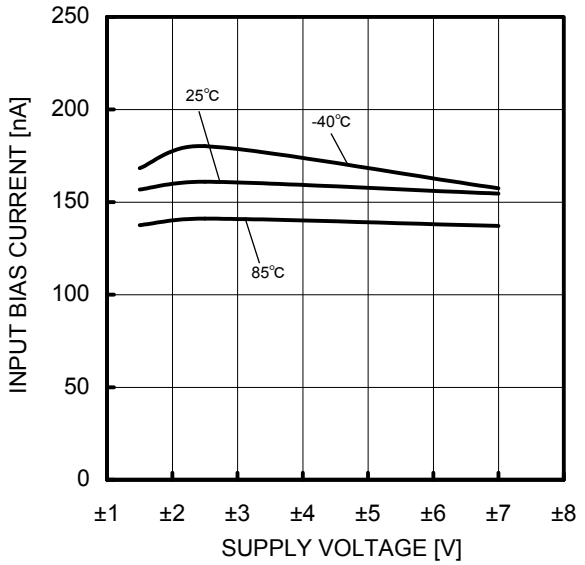


Figure 35.
Input Bias Current - Supply Voltage
(V_{ICM}=0V, VOUT=0V)

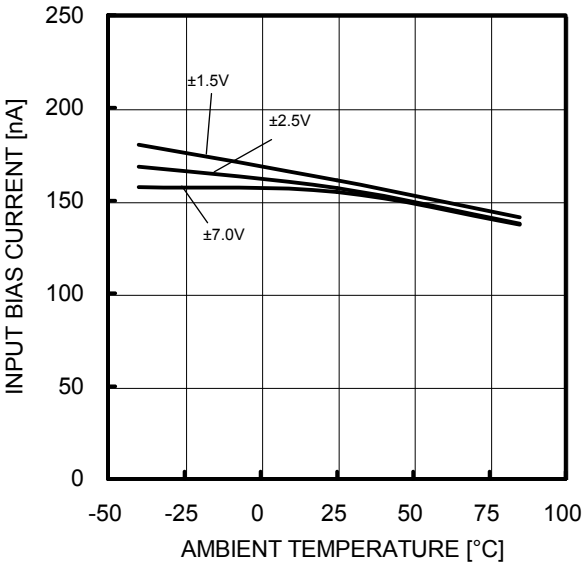


Figure 36.
Input Bias Current - Ambient Temperature
(V_{ICM}=0V, VOUT=0V)

(*)The above data is measurement value of typical sample, it is not guaranteed.

○BA2115

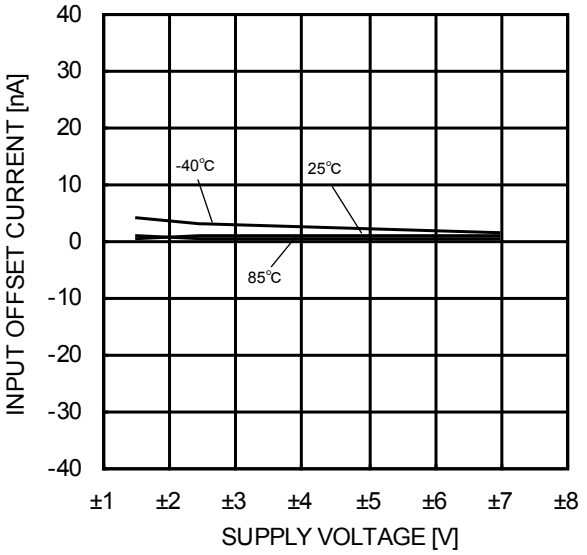


Figure 37.
Input Offset Current - Supply Voltage
(V_{ICM}=0V, VOUT=0V)

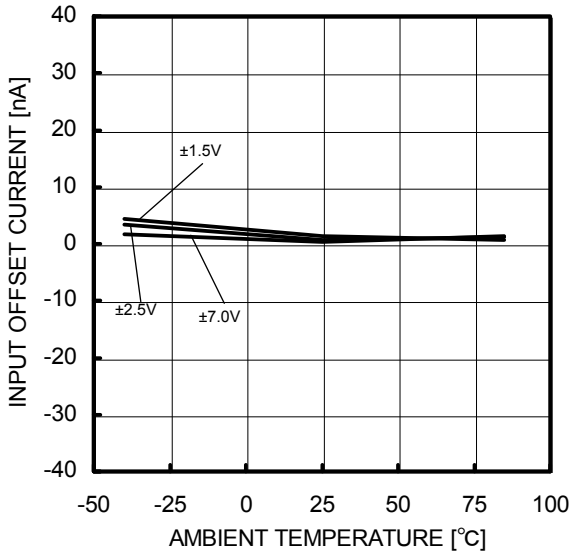


Figure 38.
Input Offset Current - Ambient Temperature
(V_{ICM}=0V, VOUT=0V)

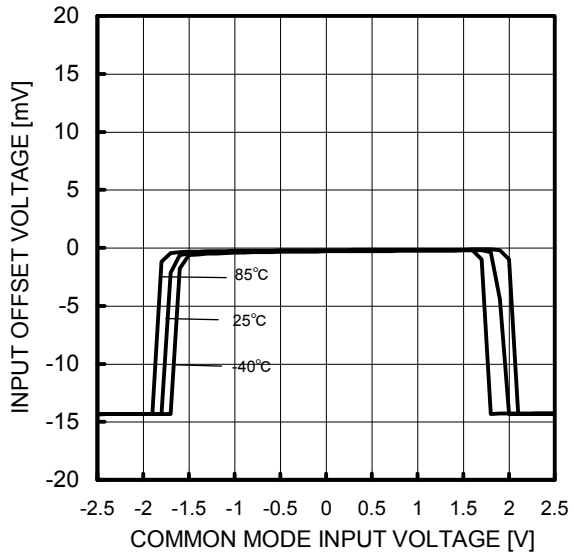


Figure 39.
Input Offset Voltage
- Common Mode Input Voltage
(VCC/VEE=+2.5V/-2.5V, VOUT=0V)

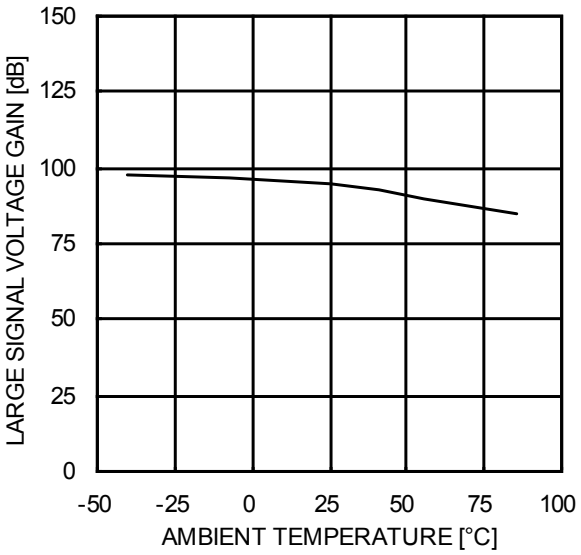


Figure 40.
Large Signal Voltage Gain
- Ambient Temperature
(VCC/VEE=+2.5V/-2.5V)

(*)The above data is measurement value of typical sample, it is not guaranteed.

○BA2115

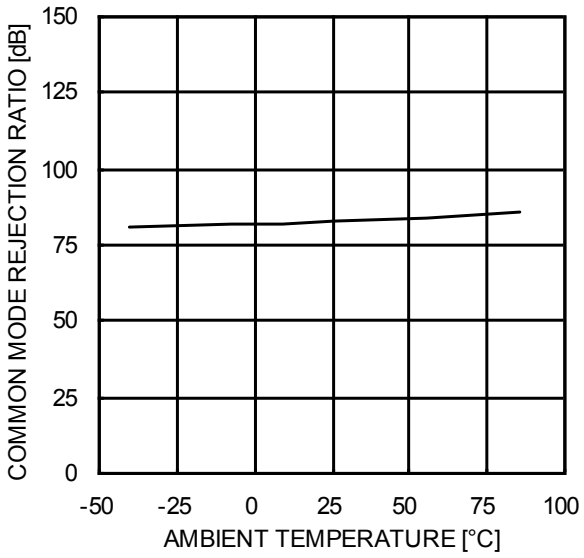


Figure 41.
Common Mode Rejection Ratio
- Ambient Temperature
(VCC/VEE=+2.5V/-2.5V)

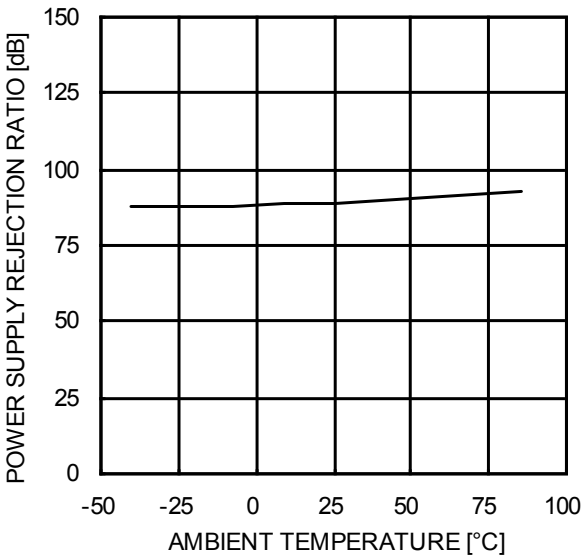


Figure 42.
Power Supply Rejection Ratio
- Ambient Temperature
(VCC/VEE=+2.5V/-2.5V)

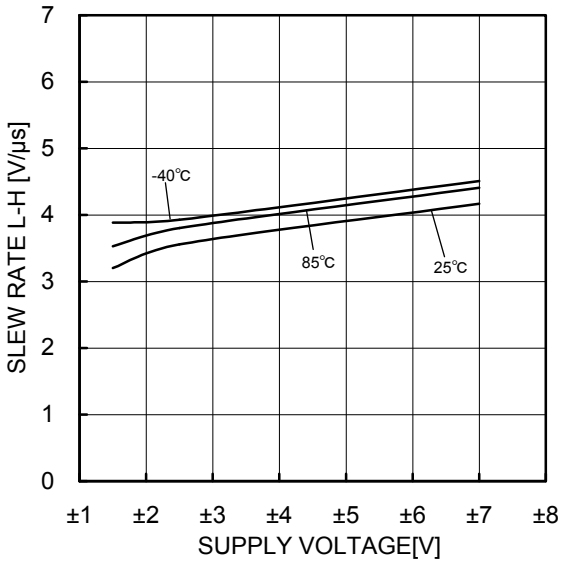


Figure 43.
Slew Rate L-H - Supply Voltage

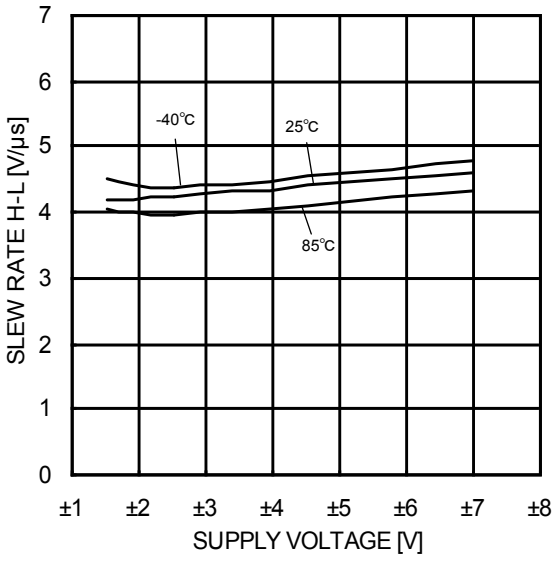


Figure 44.
Slew Rate H-L - Supply Voltage

(*)The above data is measurement value of typical sample, it is not guaranteed.

○BA2115

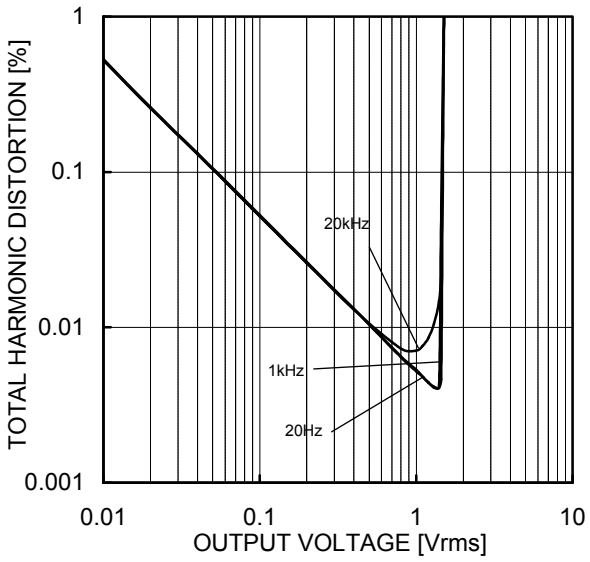


Figure 45.
Total Harmonic Distortion - Output Voltage
(VCC/VEE=2.5V/-2.5V, R_L=3kΩ
80kHz-LPF, T_A=25℃)

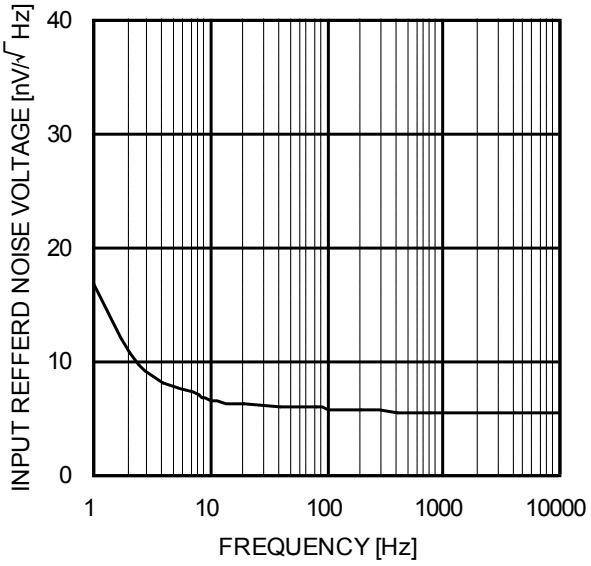


Figure 46.
Equivalent Input Noise Voltage - Frequency
(VCC/VEE=2.5V/-2.5V)

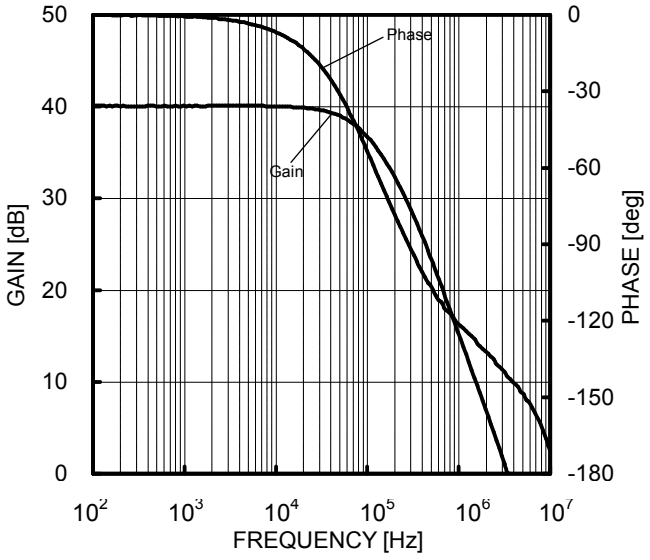


Figure 47.
Voltage Gain - Frequency
(VCC/VEE=2.5V/-2.5V, Av=40dB, R_L=10kΩ)

(*)The above data is measurement value of typical sample, it is not guaranteed.

Application Information

NULL method condition for Test Circuit 1

VCC, VEE, E_K, V_{ICM} Unit: V

Parameter	V_F	S1	S2	S3	VCC	VEE	E_K	V_{ICM}	calculation
Input Offset Voltage	V_{F1}	ON	ON	OFF	2.5	-2.5	0	0	1
Input Offset Current	V_{F2}	OFF	OFF	OFF	2.5	-2.5	0	0	2
Input Bias Current	V_{F3}	OFF	ON	OFF	2.5	-2.5	0	0	3
	V_{F4}	ON	OFF						
Large Signal Voltage Gain	V_{F5}	ON	ON	ON	2.5	-2.5	-1.0	0	4
	V_{F6}				1.5	-2.5	1.0	0	
Common-mode Rejection Ratio (Input common-mode Voltage Range)	V_{F7}	ON	ON	OFF	1.5	-3.5	-1.0	0	5
	V_{F8}				3.5	-1.5	1.0	0	
Power Supply Rejection Ratio	V_{F9}	ON	ON	OFF	0.75	-1.25	0	0	6
	V_{F10}				7.0	-7.0	0	0	

-Calculation-

1. Input Offset Voltage (Vio) $$V_{IO} = \frac{|V_{F1}|}{1+R_F/R_S} \ [V]$$

2. Input Offset Current (Iio) $$I_{IO} = \frac{|V_{F2}-V_{F1}|}{R_I \times (1+R_F/R_S)} \ [A]$$

3. Input Bias Current (Ib) $$I_B = \frac{|V_{F4}-V_{F3}|}{2 \times R_I \times (1+R_F/R_S)} \ [A]$$

4. Large Signal Voltage Gain (Av) $$A_V = 20\mathrm{Log} \frac{\Delta E_K \times (1+R_F/R_S)}{|V_{F5}-V_{F6}|} \ [dB]$$

5. Common-mode Rejection Ration (CMRR) $$CMRR = 20\mathrm{Log} \frac{\Delta V_{ICM} \times (1+R_F/R_S)}{|V_{F8}-V_{F7}|} \ [dB]$$

6. Power Supply Rejection Ratio (PSRR) $$PSRR = 20\mathrm{Log} \frac{\Delta V_{CC} \times (1+R_F/R_S)}{|V_{F10}-V_{F9}|} \ [dB]$$

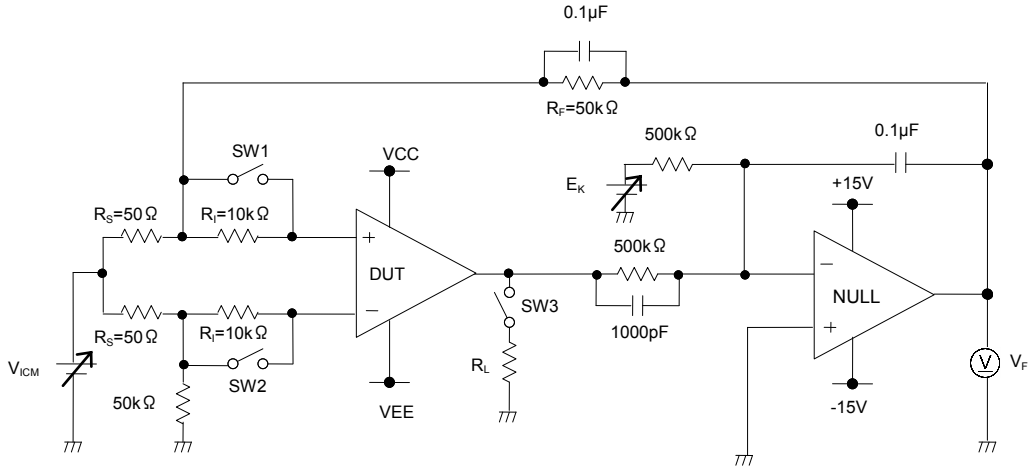


Figure 48. Test circuit1 (one channel only)

Switch Condition for Test Circuit 2

SW No.	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12	SW13	SW14
Supply Current	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage(High)	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
Maximum Output Voltage(Low)	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
Output Source Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Output Sink Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Slew Rate	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
Gain Bandwidth Product	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Equivalent Input Noise Voltage	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF

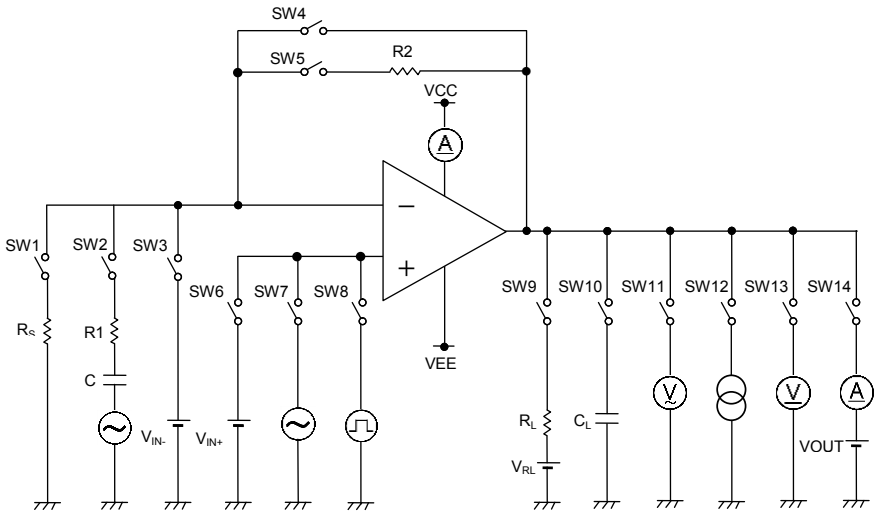


Figure 49. Test Circuit 2 (each Op-Amp)

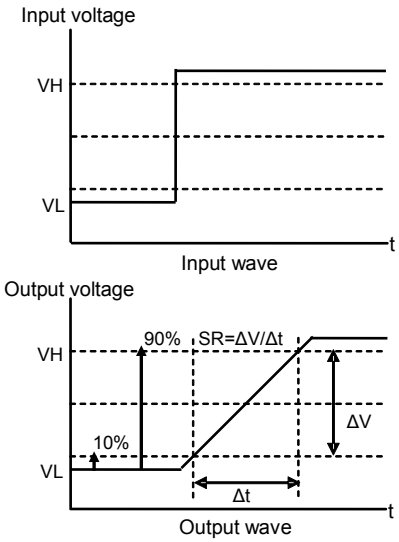
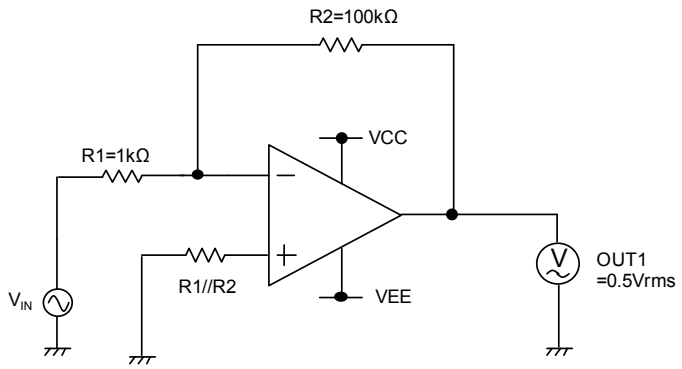
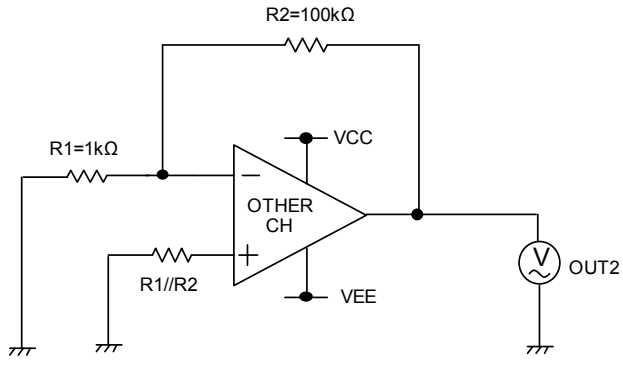


Figure 50. Slew Rate Input Waveform





$$CS=20\times\log\frac{100\times OUT1}{OUT2}$$

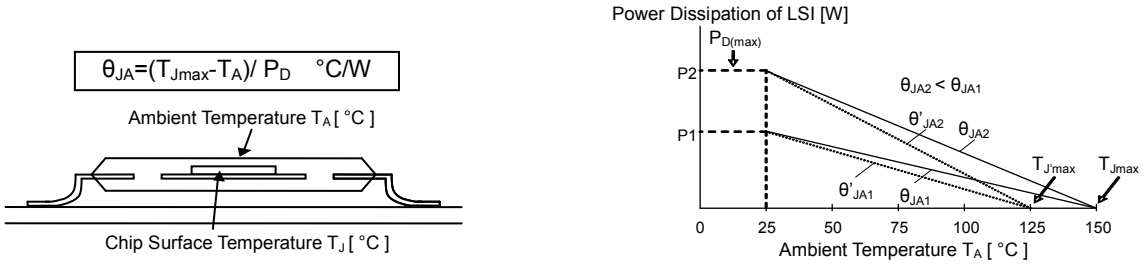
Figure 51. Test circuit 3(Channel Separation)
(VCC=+2.5V, VEE=-2.5V)

Power Dissipation

Power dissipation(total loss) indicates the power that can be consumed by IC at T_A=25℃(normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip(maximum junction temperature) and thermal resistance of package(heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability(hardness of heat release)is called thermal resistance, represented by the symbol θ_{JA}℃/W.The temperature of IC inside the package can be estimated by this thermal resistance. Figure 52. (a) shows the model of thermal resistance of the package. Thermal resistance θ_{JA}, ambient temperature T_A, maximum junction temperature T_{JMAX}, and power dissipation Pd can be calculated by the equation below:

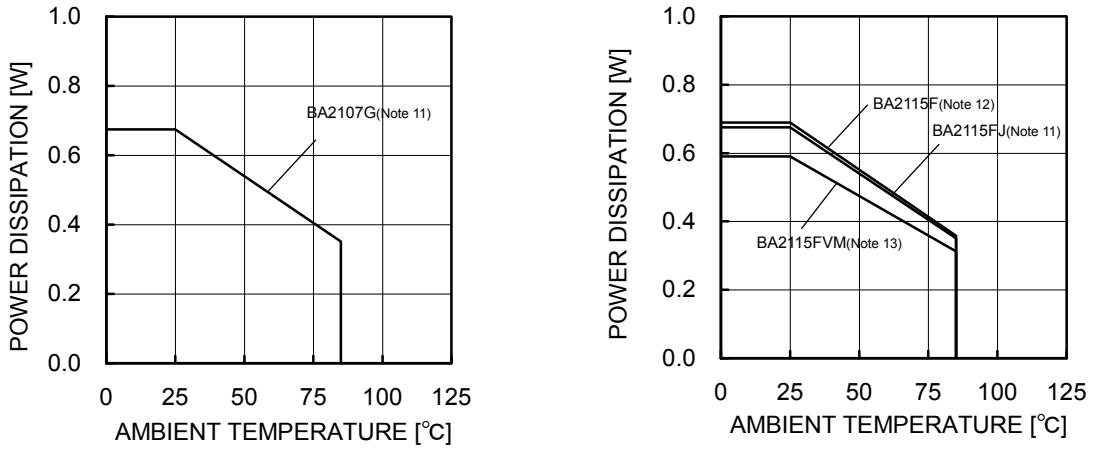
$$\theta_{JA} = (T_{JMAX}-T_A) / P_D \quad ℃/W \quad \cdots\cdots (I)$$

Derating curve in Figure 52. (b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θja. Thermal resistance θ_{JA} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 53. (c),(d) show a derating curve for an example of BA2107,BA2115.



(a) Thermal Resistance (b) Derating Curve

Figure 52. Thermal Resistance and Derating Curve



(c)BA2107 (d)BA2115

(Note 11)	(Note 12)	(Note 13)	Unit
5.4	6.2	4.8	mW/℃

When using the unit above T_A=25℃, subtract the value above per ℃. Permissible dissipation is the value.
Permissible dissipation is the value when FR4 glass epoxy board 70mm ×70mm ×1.6mm (cooper foil area below 3%) is mounted.

Figure 53. Derating Curve

Application Example

○Voltage Follower

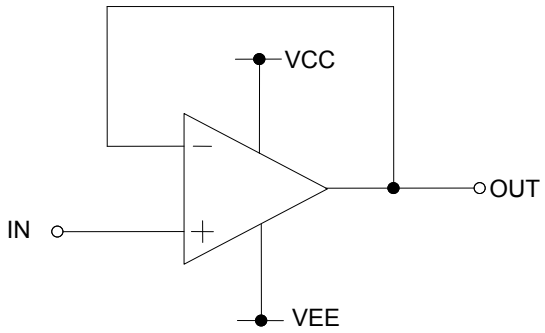


Figure 54. Voltage Follower Circuit

Voltage gain is 0 dB.
This circuit controls output voltage (OUT) equal input voltage (IN), and keeps OUT with stable because of high input impedance and low output impedance.
OUT is shown next expression.
OUT=IN

○Inverting Amplifier

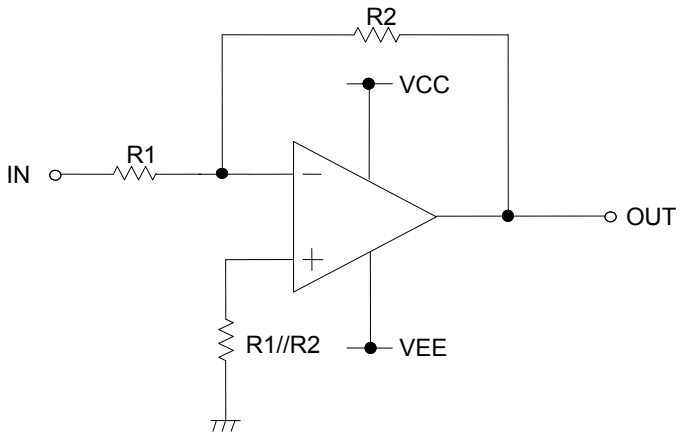


Figure 55. Inverting Amplifier Circuit

For inverting amplifier, Vi(b) Derating curve voltage gain decided R1 and R2, and phase reversed voltage is output.
OUT is shown next expression.
OUT=-(R2/R1)・IN
Input impedance is R1.

○Non-inverting Amplifier

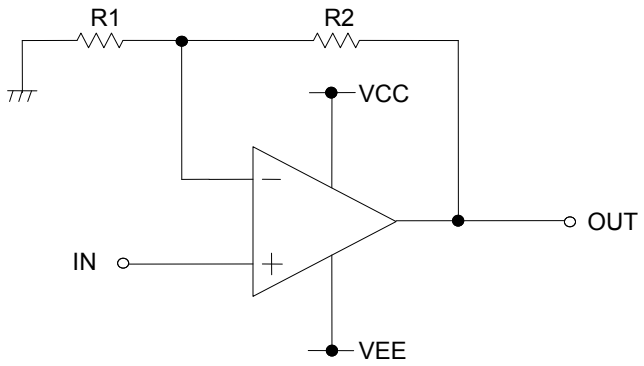


Figure 56. Non-inverting Amplifier Circuit

For non-inverting amplifier, IN is amplified by voltage gain decided R1 and R2, and phase is same with IN.
OUT is shown next expression.
OUT=(1 + R2/R1)・IN
This circuit performs high input impedance because Input impedance is operational amplifier's input Impedance.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the P_D stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the P_D rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

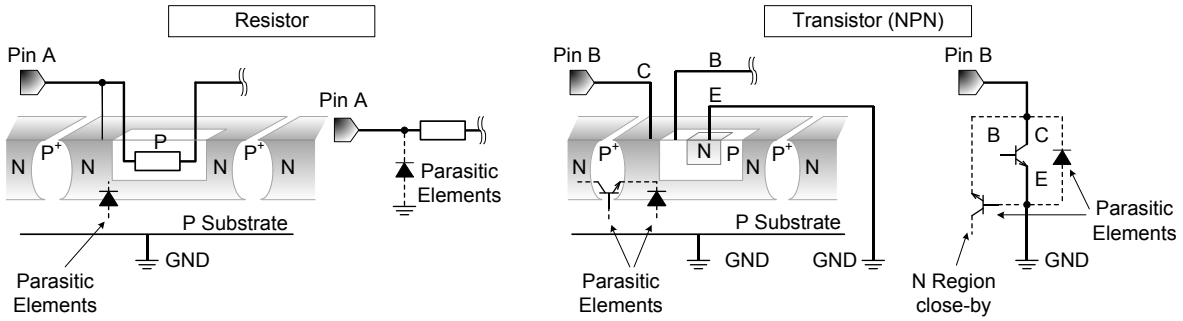


Figure 57. Example of monolithic IC structure

12. Unused Circuits

It is recommended to apply the connection (see Figure 58.) and set the non-inverting input terminal at a potential within the Input Common-mode Voltage Range (V_{ICM}) for any unused circuit.

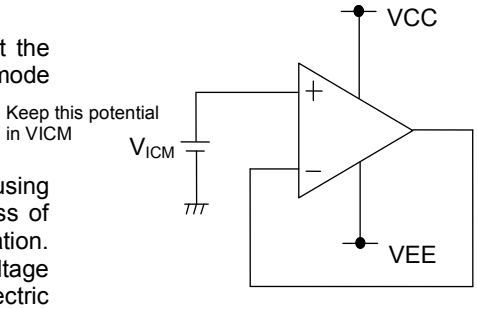


Figure 58. Example of Application Circuit for Unused Op-amp

13. Input Voltage

Applying VEE +36V to the input terminal is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

14. Power Supply(single/dual)

The operational amplifier operates when the voltage supplied is between VCC and VEE. Therefore, the single supply operational amplifier can be used as dual supply operational amplifier as well.

15. IC Handling

When pressure is applied to the IC through warp on the printed circuit board, the characteristics may fluctuate due to the piezo effect. Be careful with the warp on the printed circuit board.

16. The IC Destruction Caused by Capacitive Load

The IC may be damaged when VCC terminal and VEE terminal is shorted with the charged output terminal capacitor. When IC is used as an operational amplifier or as an application circuit where oscillation is not activated by an output capacitor, output capacitor must be kept below 0.1μF in order to prevent the damage mentioned above.