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STRUCTURE : Silicon Monolithic Integrated Circuit
PRODUCT SERIES : Power driver for compact disc player
TYPE : BA5830FM

Features
- 4CH BTL Driver.
- Employs the HSOP-M28PIN power package for compaction.
- Has a wide dynamic range. (PreVcc=PowVcc=8V,RL=8Ω、6.0V(typ.))
- Incorporates the thermal shutdown circuit.
- Separating Vcc into Pre and Power (Power divides into CH1/2 and CH3/4), can make better Power efficiency.
- Switches CH4 input by CNT.
- Incorporates mute function by CNT terminal and mute terminal.
- A variable regulator is built in.

○ Absolute Maximum Rating (Ta=25℃)

Item	Symbol	Rating	Unit
Supply voltage	PreVcc,PowVcc	18	V
Input terminal voltage	VIN*1	18	V
Power dissipation	Pd	2.2*2	W
Maximum output current	Iomax	1*3	A
Operating temperature range	Topr	-40 ~ +85	℃
Storage temperature range	Tstg	-55 ~ +150	℃

*1 It shows each terminal of OPIN1(-),OPIN2(-),OPIN3(-),OPINSL(-),OPOUT1,OPOUT2,OPOUT3, OPOUTSL,LDIN,BIAS,CNT,MUTE,REG(+)

*2 Rating for 70mm×70mm(size), 1.6mm(thickness), copper foil occupation ratio less than 3%, And use of glass-epoxy substrate.
When this IC is used above Ta=25℃, note that this rating decreases 17.6mW each time the temperature increases 1℃.

*3 This rating of permissible dissipation must not exceed ASO.

○ Operating Supply Range (To determine a power supply voltage, the power dissipation must be taken into consideration.)

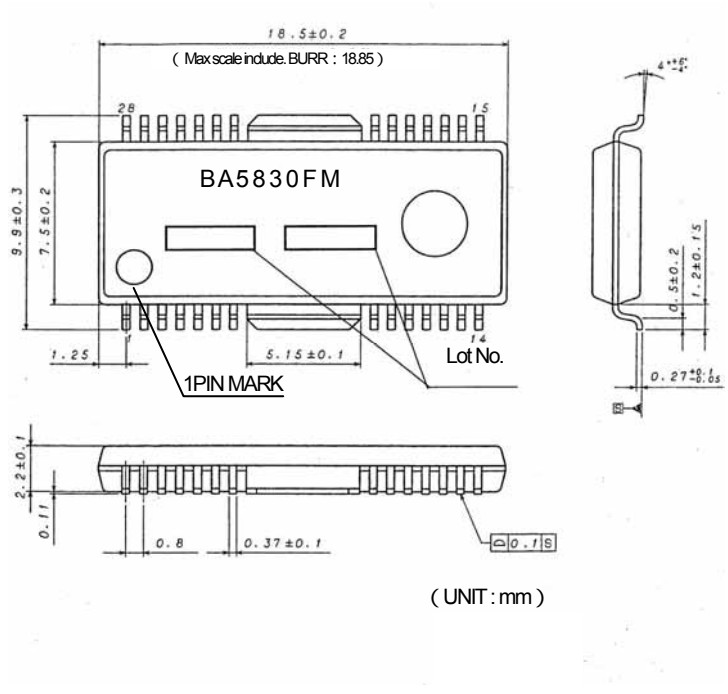
PreVcc	5.5 ~ 14 (V)*4
PowVcc	4.5 ~ PreVcc (V)

*4 When regulator isn't used, 4.5 ~ 14(V)

○ Electrical characteristics (Unless otherwise noted, Ta=25℃, PreVcc=PowVcc=8V, BIAS=2.5V, RL=8Ω)

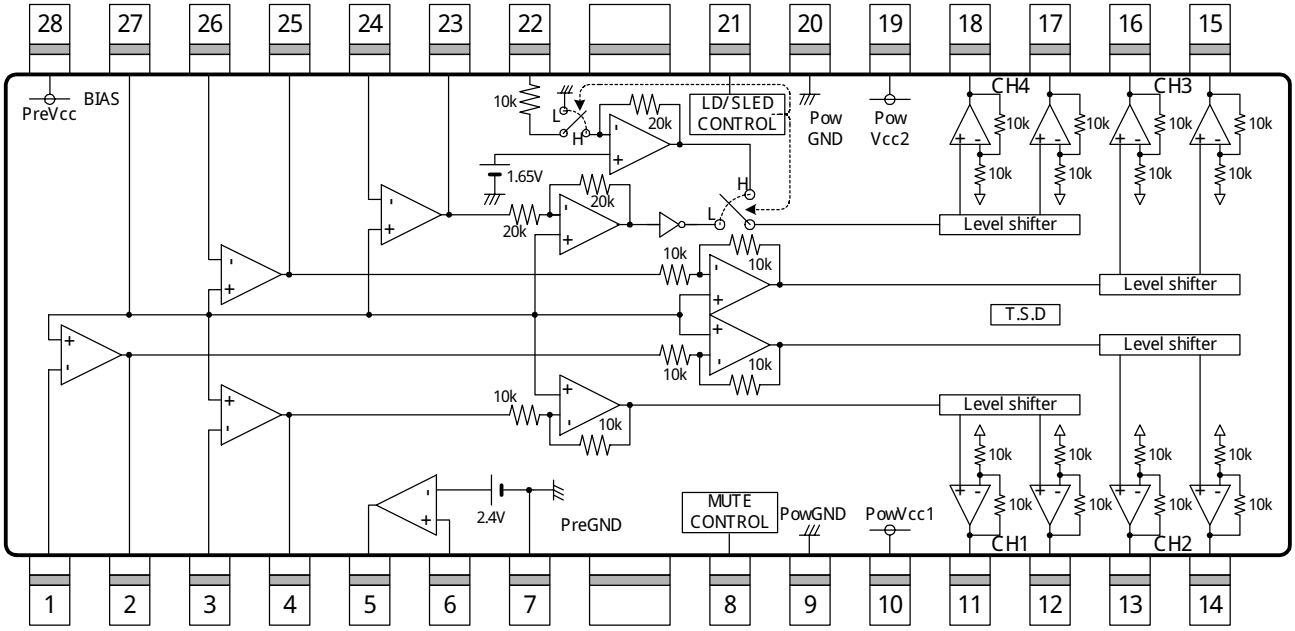
Parameter	Symbol	MIN	TYP	MAX	Unit	Condition
Quiescent dissipation current	IQ	-	22	32	mA	RL=∞
<Driver>						
Output offset voltage	Voof	-50	0	50	mV	
Maximum output amplitude	VOM	5.4	6.0	-	V	
Closed circuit voltage gain (CH1,2,3,SLED)	Gvc	10.0	11.7	13.4	dB	VIN=± 0.5V
Closed circuit voltage gain (LOADING)	GvcLD	16.0	17.7	19.4	dB	VIN=± 0.5V
MUTE terminal low-level input voltage	VML	-	-	0.5	V	
MUTE terminal high-level input voltage	VMH	2.0	-	-	V	
CNT terminal low-level input voltage	VCNTL	-	-	0.5	V	
CNT terminal high-level input voltage	VCNTH	2.0	-	-	V	
LDIN terminal voltage (SLED input)	VLDIN	-	0.1	0.3	V	CNT='L'
<Pre OP amp>						
Internal bias voltage	VBIN	1.53	1.65	1.77	V	CNT='H'
Input offset voltage	VOFOP	-6	0	6	mV	
Input bias current	IBOP	-	-	300	nA	
High-level output voltage	VOHOP	7.5	7.9	-	V	
low-level output voltage	VOLOP	-	0.2	0.5	V	
Output driving current sink	ISI	0.5	-	-	mA	
Output driving current source	ISO	0.5	-	-	mA	
Slew rate	SROP	-	1	-	V/μ s	100KHz square wave, 2Vp-p input
<Regulator>						
Output voltage	Vreg	4.79	5.04	5.29	V	IREG=150mA
Load regulation	Δ VRL	-40	0	20	mV	IREG=0~500mA、5Vsetup
Supply voltage regulation	Δ VVCC	-20	10	40	mV	VCC=5.5~14V、5Vsetup
REG.P terminal voltage	VREGP	2.28	2.4	2.52	V	

○ Package outlines : HSOP-M28



(UNIT : mm)

○ APPLICATION CIRCUIT DIAGRAM



T.S.D : Thermal shutdown
Resistance unit : [Ω]

○ Pin Description

No.	Pin name	Pin description	No.	Pin name	Pin description
1	OPIN2(-)	CH2 Pre OP amplifier invert input	15	VO3(+)	Driver CH3 positive output
2	OPOUT2	CH2 Pre OP amplifier output	16	VO3(-)	Driver CH3 negative output
3	OPIN1(-)	CH1 Pre OP amplifier invert input	17	VO4(+)	Driver CH4 positive output
4	OPOUT1	CH1 Pre OP amplifier output	18	VO4(-)	Driver CH4 negative output
5	REG-B	Connect to external Tr. Base	19	PowVcc2	CH3,4 Power Block VCC
6	REG(+)	Regulator terminal of output feedback	20	PowGND	Power Block GND
7	PreGND	Pre Block and Regulator GND	21	CNT	Control terminal
8	MUTE	Mute terminal	22	LDIN	Loading input
9	PowGND	Power Block GND	23	OPOUTSL	SLED Pre OP amplifier output
10	PowVcc1	CH1,2 Power Block VCC	24	OPINSL(-)	SLED Pre OP amplifier invert input
11	VO1(-)	Driver CH1 negative output	25	OPOUT3	CH3 Pre OP amplifier output
12	VO1(+)	Driver CH1 positive output	26	OPIN3(-)	CH3 Pre OP amplifier invert input
13	VO2(-)	Driver CH2 negative output	27	BIAS	BIAS input
14	VO2(+)	Driver CH2 positive output	28	PreVcc	Pre-Block VCC

Note) When PIN2,4,22,25 is high("H"), the positive output pin of the driver is high("H") and the negative output pin is low("L").
When PIN23 is high("H"), the positive output pin of CH4 is low("L") and negative output pin is high("H").

○ Notes on use

(1) Drivers can be switched mute ON/OFF by inputting combinations of H-level signal and L-level signal to MUTE and CNT terminal. There is the logic diagram in under table. (SL:Sled、 LD:Loading)

INPUT		OUTPUT	
MUTE	CNT	CH1~3	CH4
H	H	MUTE OFF	LD ON
H	L	MUTE OFF	SL ON
L	H	MUTE ON	LD ON
L	L	MUTE ON	MUTE ON

(2) When the BIAS terminal (27PIN) is lowered below 0.7V(typ.), the output is muted. In the normal state, this PIN must be pulled up above 1.3V. (When CNT is 'H', CH4 isn't muted.)

(3) When the supply voltage reaches 3.8V (typ.) or lower, the output current is muted. When it rises to 4.0V (typ.) again, the driver circuit is activated.

(4) The output is muted in the event of a thermal shut down, mute-on, or bias and Pre Vcc voltage drop. Only the driver is muted. When muted, output terminal becomes internal reference voltage (about (PowVcc-Vf)/2).

(5) When a capacitance load is connected to the OP amplifier output, the amplifier phase margin decreases, which causes the peak or oscillator..When connecting such load, insert a resistance in series between the output and the capacitance load and take a full consideration for frequency characteristics, to prevent problems during practical use.

(6) Connect a coupling capacitor (approx 0.1μF) between the power supplies at the root of this IC.

(7) Connect the radiation fin to the external GND.

(8) Avoid the short-circuits between: Output pin and Vcc、 Output pin and GND、 Output pins
If this caution is ignored, IC damage may cause smokes.

(9) About absolute maximum ratings
Exceeding the absolute maximum ratings, such as the applied voltage or the operating temperature range, may cause permanent device damage. As these cases cannot be limited to the broken short mode or the open mode, if a special mode where the absolute maximum ratings may be exceeded is assumed, it is recommended to take mechanical safety measures such as attaching fuses.

(10) About power supply lines
As a measure against the back current regenerated by a counter electromotive force of the motor, a capacitor to be used as a regenerated-current path can be installed between the power supply and GND and its capacitance value should be determined after careful check that any problems, for example, a leak capacitance of the electrolytic capacitor at low temperature, are not found in various characteristics.

(11) About GND potential
The electric potential of the GND terminal must be kept lowest in the circuitry at any operation states.

(12) About thermal design
With consideration of the power dissipation (Pd) under conditions of actual use, a thermal design provided with an enough margin should be done.

(13) About operations in a strong electric field. When used in a strong electric field, note that a malfunction may occur.

(14) ASO
When using this IC, the output Tr must be set not to exceed the values specified in the absolute maximum ratings and ASO.

(15) Thermal shutdown circuit
This IC incorporates a thermal shutdown circuit (TSD circuit). When the chip temperature reaches the value shown below, the coil output to the motor will be set to open.
The thermal shutdown circuit is designed only to shut off the IC from a thermal runaway and not intended to protect or guarantee the entire IC functions.Therefore, users cannot assume that the TSD circuit once activated can be used continuously in the subsequent operations.

TSD ON Temperature [°C] (typ.)	Hysteresis Temperature [°C] (typ.)
175	25

(16) About earth wiring patterns
When a small signal GND and a large current GND are provided, it is recommended that the large current GND pattern and the small signal GND pattern should be separated and grounded at a single point of the reference point of the set in order to prevent the voltage of the small signal GND from being affected by a voltage change caused by the resistance of the pattern wiring and the large current.
Make sure that the GND wiring patterns of the external components will not change, too.

(17) About each input terminal
This IC is a monolithic IC which has a P^+ isolations and P substrate to isolate elements each other.
This P layer and an N layer in each element form a PN junction to construct various parasitic elements.
Due to the IC structure, the parasitic elements are inevitably created by the potential relationship.
Activation of the parasitic elements can cause interference between circuits and may result in a malfunction or, consequently, a fatal damage.
Therefore, make sure that the IC must not be used under conditions that may activate the parasitic elements, for example, applying the lower voltage than the ground level(GND, P substrate) to the input terminals.
Note that, while not applying the power supply voltage to the IC, any voltage must not be applied to the input terminals. In addition, do not apply the voltage to input terminals without applying the power supply voltage to the IC. Also while applying the power supply voltage, each input terminal must be the power supply voltage or less; or within the guaranteed values in the electric characteristics.

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