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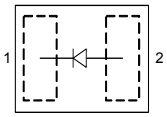
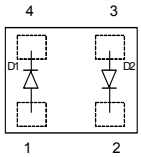
Silicon Deep Trench PIN Diodes

- Optimized for low bias current antenna switches in hand held applications
- Very low capacitance at zero volt reverse bias at frequencies above 1GHz (typ. 0.19 pF)
- Low forward resistance (typ. 1.3 Ω @ I_F = 3 mA)
- Improved ON / OFF mode harmonic distortion balance
- Pb-free (RoHS compliant) package

RoHS

BAR90-02EL **BAR90-098LRH**
BAR90-02ELS





Type	Package	Configuration	L_S(nH)	Marking
BAR90-02ELS	TSSLP-2-3	single, leadless	0.2	J*
BAR90-02EL	TSLP-2-19	single, leadless	0.4	X
BAR90-098LRH	TSLP-4-7	anti-parallel pair, leadless	0.4	T9

* Marking of TSSLP-2-3 with underline

Maximum Ratings at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	80	V
Forward current	I_F	100	mA
Total power dissipation	P_{tot}		mW
T_S ≤ 137 °C, BAR90-02ELS		150	
T_S ≤ 133°C, all others		250	
Junction temperature	T_j	150	°C
Operating temperature range	T_{op}	-55 ... 125	
Storage temperature	T_{stg}	-55 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point[1)]	R_{thJS}		K/W
BAR90-02ELS		≤ 90	
All others		≤ 65	

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Breakdown voltage $I_{(BR)}$ = 5 µA	$V_{(BR)}$	80	-	-	V
Reverse current V_R = 60 V	I_R	-	-	50	nA
Forward voltage	V_F				V
I_F = 3 mA		0.75	0.81	0.87	
I_F = 100 mA		-	0.9	1	

[1]For calculation of R_{thJA} please refer to Application Note AN077 (Thermal Resistance Calculation)

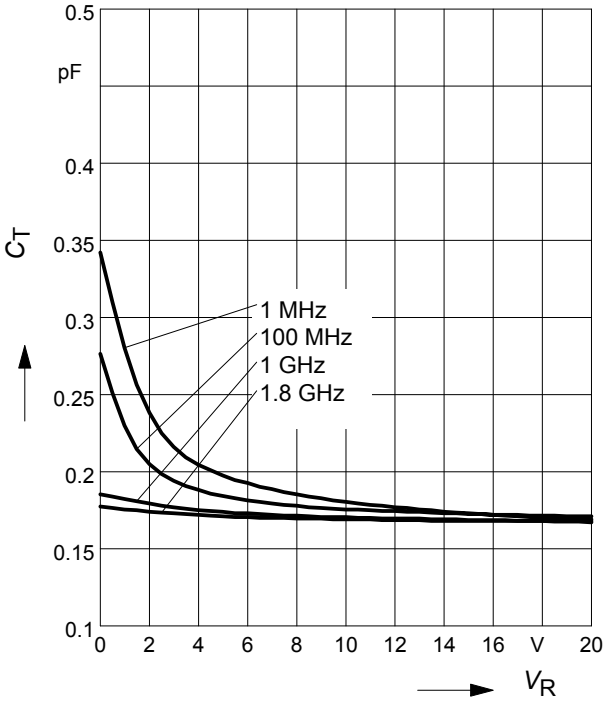
Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics					
Diode capacitance	C_T				pF
V_R = 1 V, f = 1 MHz		-	0.25	0.35	
V_R = 0 V, f = 100 MHz		-	0.3	-	
V_R = 0 V, f = 1 GHz		-	0.19	-	
V_R = 0 V, f = 1.8 GHz		-	0.18	-	
Reverse parallel resistance	R_P				kΩ
V_R = 0 V, f = 100 MHz		-	35	-	
V_R = 0 V, f = 1 GHz		-	5	-	
V_R = 0 V, f = 1.8 GHz		-	4	-	
Forward resistance	r_f				Ω
I_F = 1 mA, f = 100 MHz		-	2	-	
I_F = 3 mA, f = 100 MHz		-	1.3	2.3	
I_F = 10 mA, f = 100 MHz		-	0.8	-	
Charge carrier life time	τ_{rr}	-	750	-	ns
I_F = 10 mA, I_R = 6 mA, measured at I_R = 3 mA, R_L = 100 Ω					
I-region width	W_I	-	20	-	µm
Insertion loss[1)]	I_L				dB
I_F = 1 mA, f = 1.8 GHz		-	0.16	-	
I_F = 3 mA, f = 1.8 GHz		-	0.11	-	
I_F = 10 mA, f = 1.8 GHz		-	0.08	-	
Isolation[1)]	I_{SO}				
V_R = 0 V, f = 0.9 GHz		-	18.5	-	
V_R = 0 V, f = 1.8 GHz		-	13.5	-	
V_R = 0 V, f = 2.45 GHz		-	11.5	-	

[1]BAR90-02EL in series configuration, Z = 50 Ω

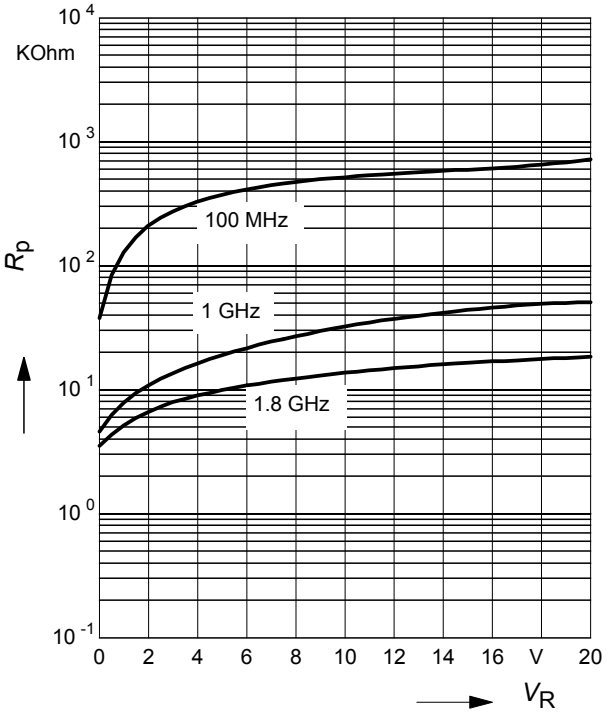
Diode capacitance $C_T = f(V_R)$

f = Parameter



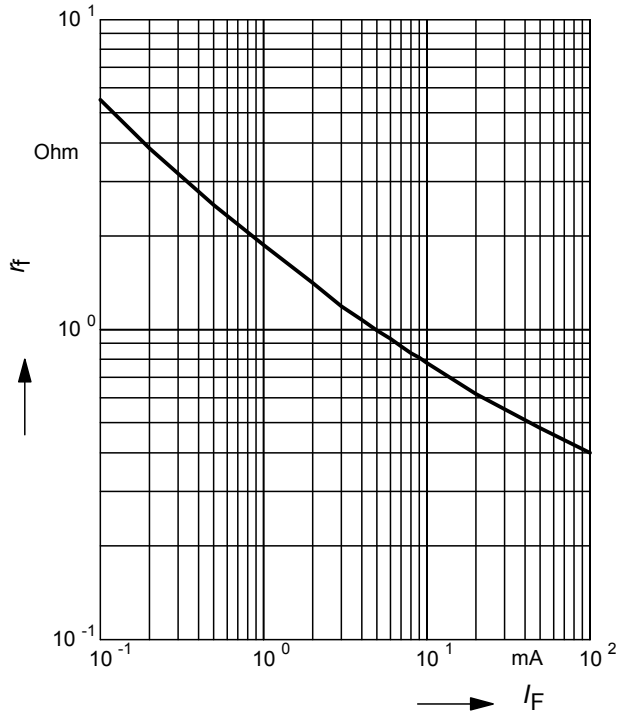
Reverse parallel resistance $R_P = f(V_R)$

f = Parameter



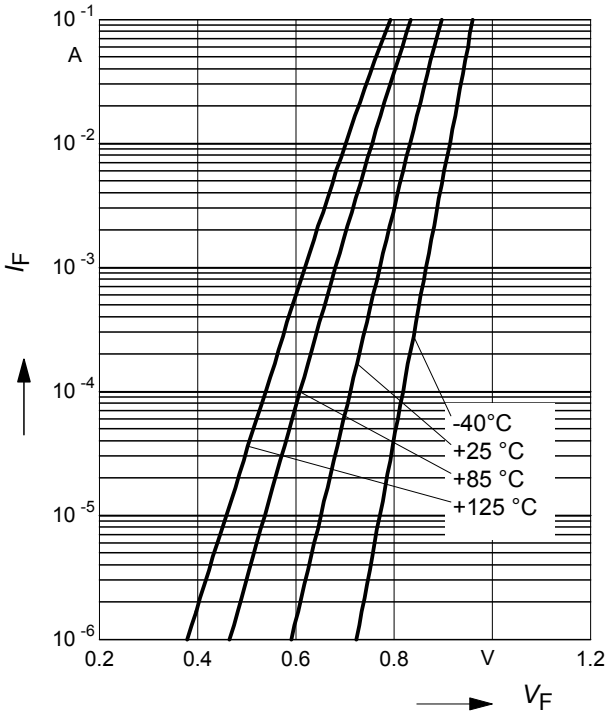
Forward resistance $r_f = f(I_F)$

f = 100 MHz



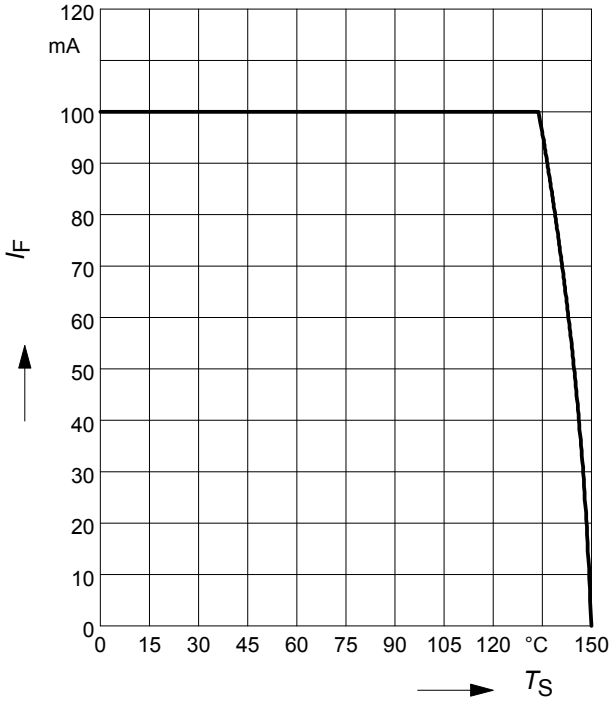
Forward current $I_F = f(V_F)$

T_A = Parameter



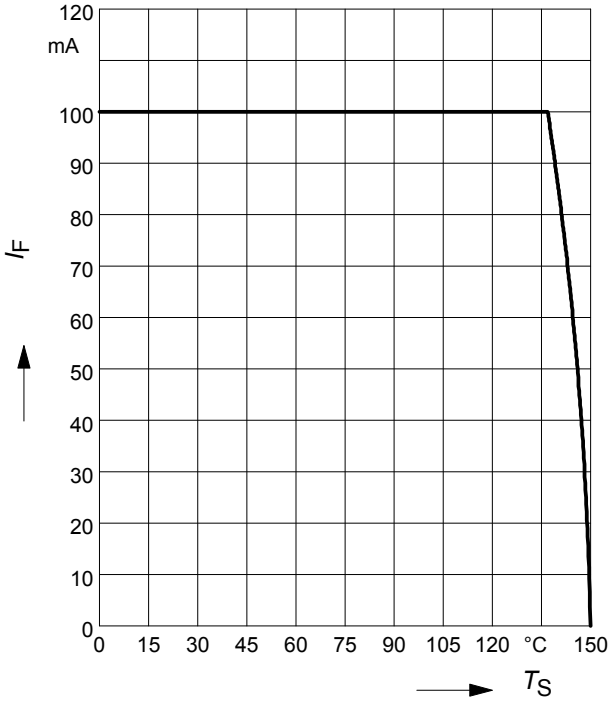
Forward current $I_F = f(T_S)$

BAR90-02EL / -098LRH



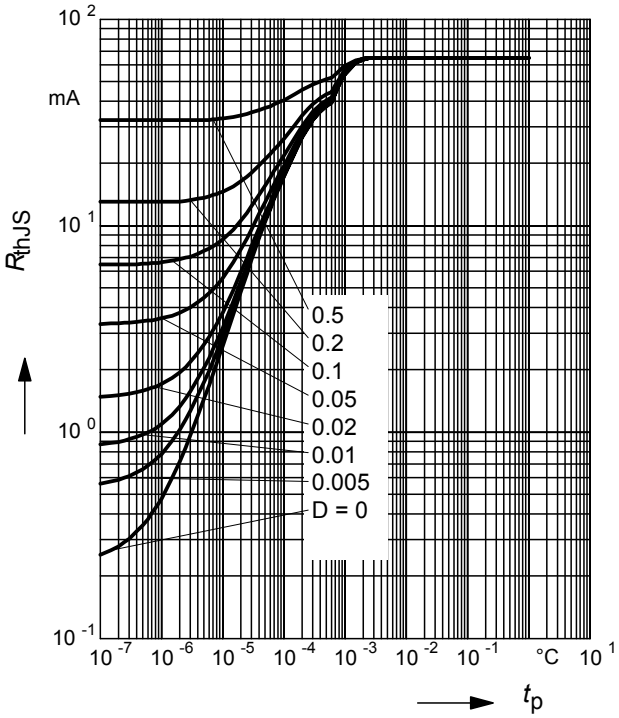
Forward current $I_F = f(T_S)$

BAR90-02ELS



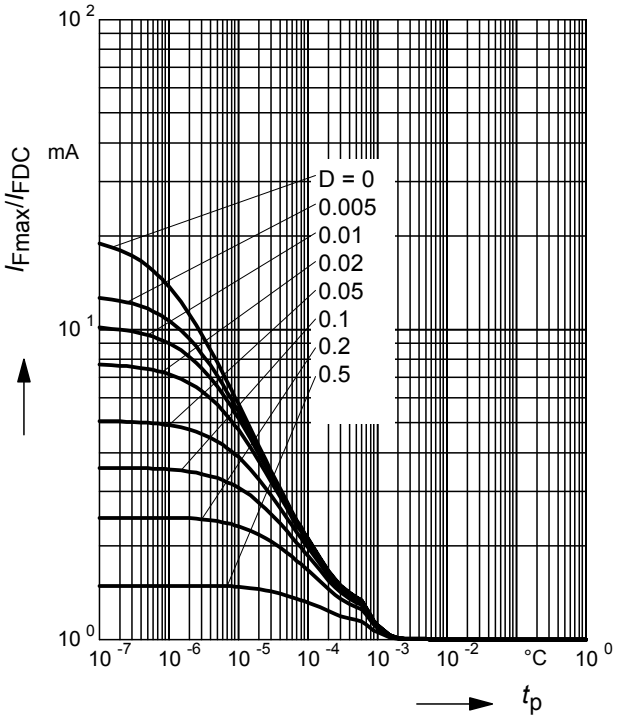
Permissible Puls Load $R_{thJS} = f(t_p)$

BAR90-02EL / -098LRH



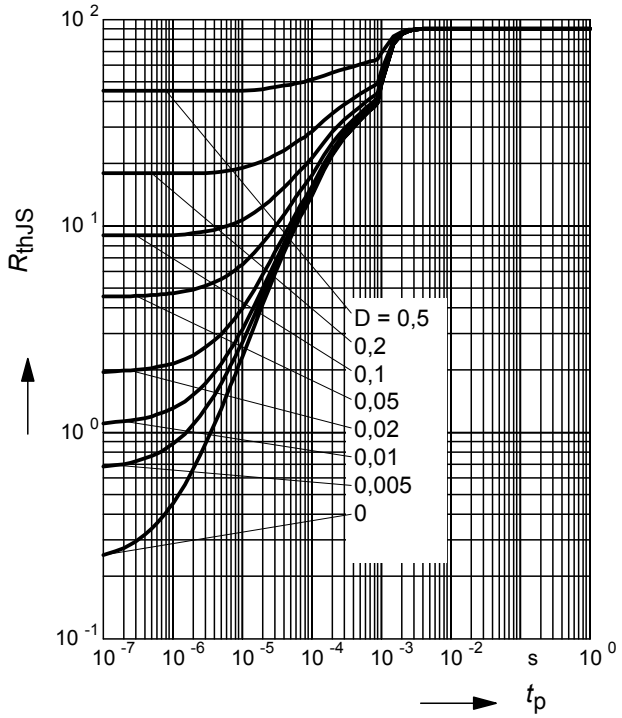
Permissible Pulse Load

$I_{Fmax}/ I_{FDC} = f(t_p)$ BAR90-02EL /-098LRH



Permissible Puls Load $R_{thJS} = f(t_p)$

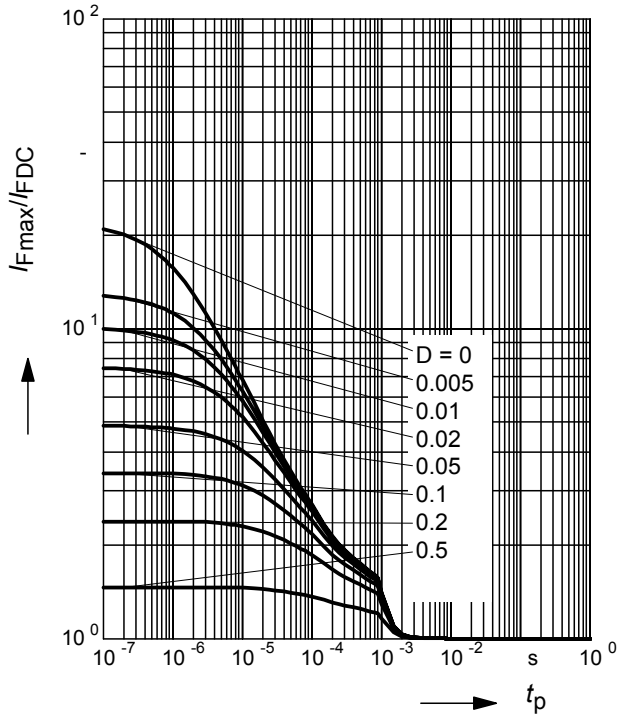
BAR90-02ELS



Permissible Pulse Load

$I_{Fmax}/ I_{FDC} = f(t_p)$

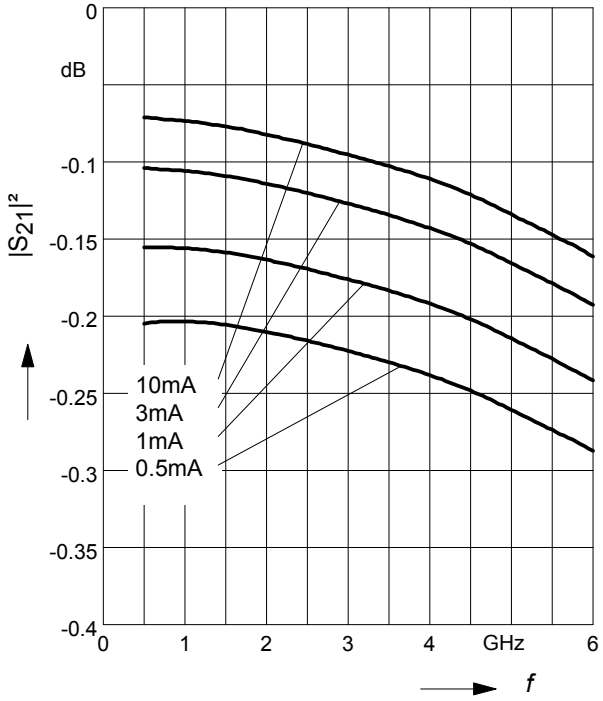
BAR90-02ELS



Insertion loss $I_L = -|S_{21}|^2 = f(f)$

I_F = Parameter

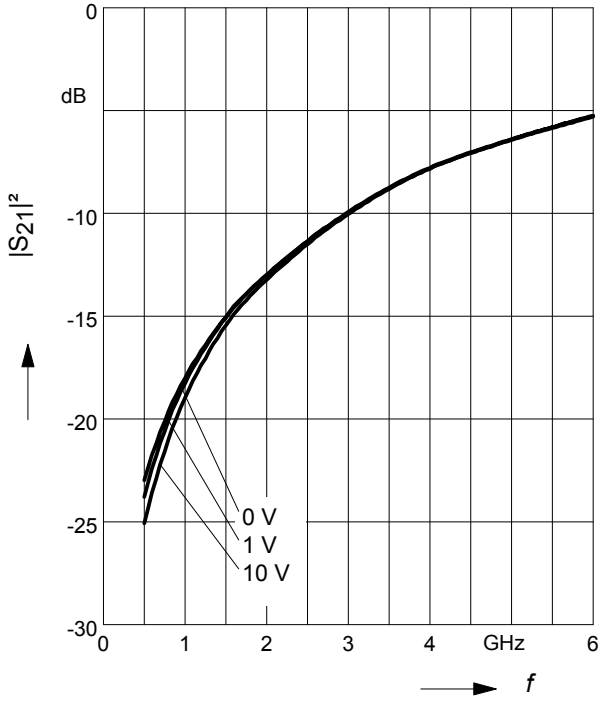
BAR90-02EL in series configuration, $Z = 50\Omega$



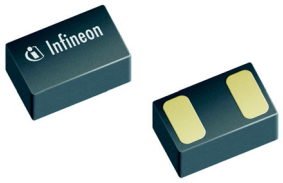
Isolation $I_{SO} = -|S_{21}|^2 = f(f)$

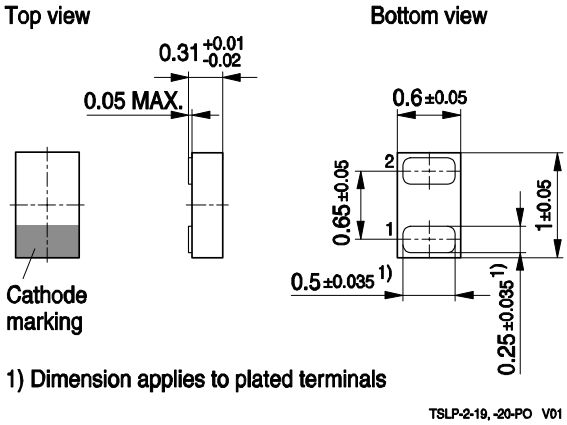
V_R = Parameter

BAR90-02EL in series configuration, $Z = 50\Omega$



Package Outline



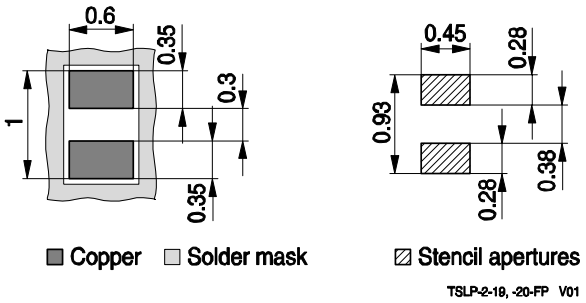


1) Dimension applies to plated terminals

TSLP-2-19, -20-PO V01

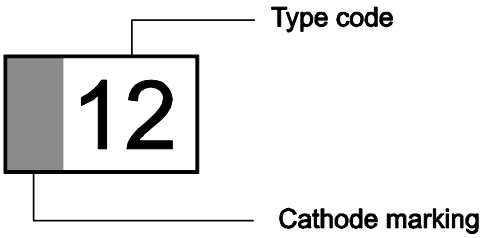
Foot Print

For board assembly information please refer to Infineon website „Packages“



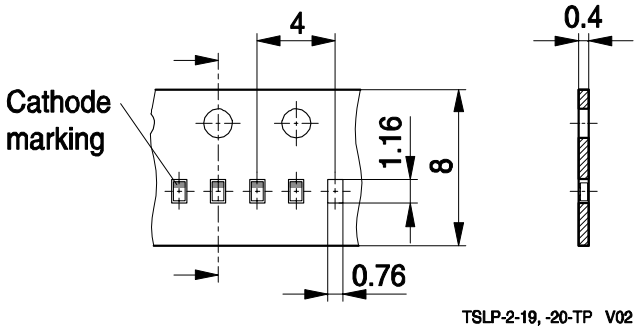
TSLP-2-19, -20-FP V01

Marking layout (Example)



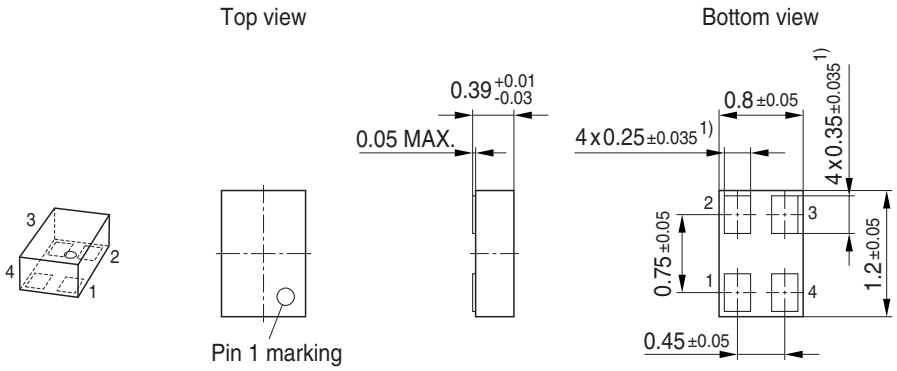
Standard Packing

Reel Ø 180 mm: 15.000 Pieces / Reel
Reel Ø 330 mm: 6.000 Pieces / Reel
Reel Ø 330 mm: 50.000 Pieces / Reel



TSLP-2-19, -20-TP V02

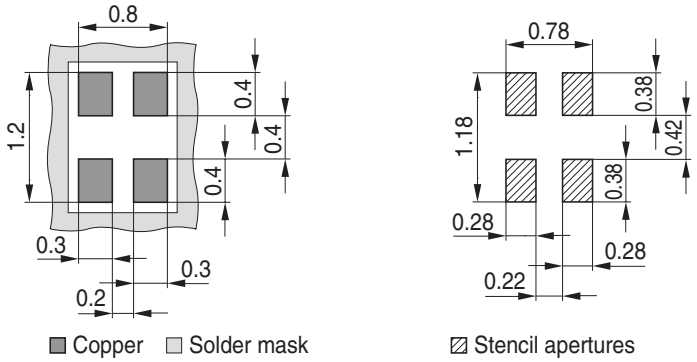
Package Outline



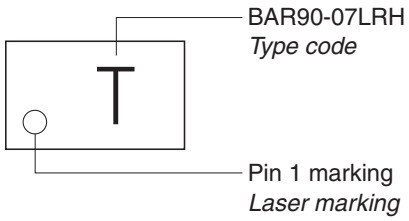
1) Dimension applies to plated terminal

Foot Print

For board assembly information please refer to Infineon website "Packages"

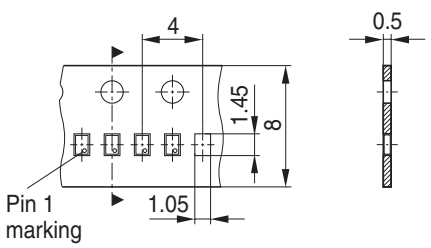


Marking Layout (Example)

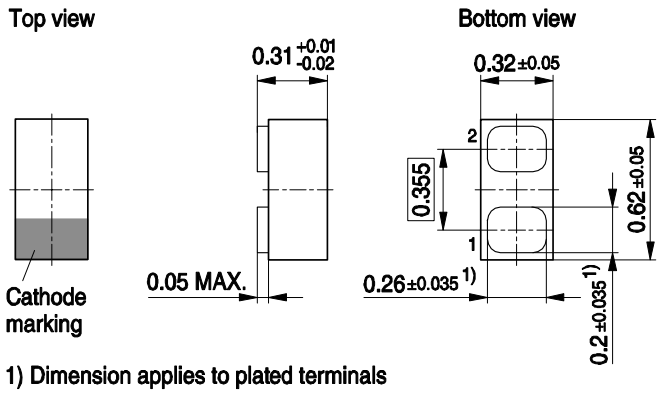


Standard Packing

Reel ø180 mm = 15.000 Pieces/Reel



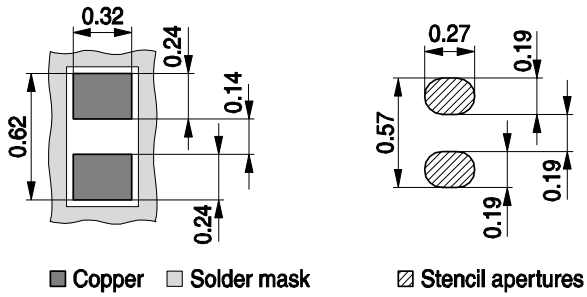
Package Outline



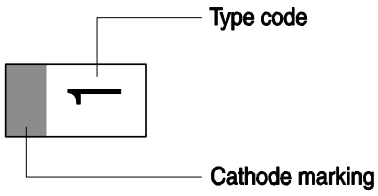
1) Dimension applies to plated terminals

Foot Print

For board assembly information please refer to Infineon website "Packages"

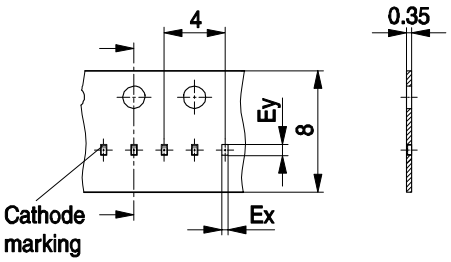


Marking Layout



Standard Packing

Reel ø330 mm = 15.000 Pieces/Reel



Tape type	Ex	Ey
Punched Tape	0.43	0.73
Embossed Tape	0.37	0.67

Deliveries can be both tape types (no selection possible).
Specification allows identical processing (pick & place) by users.

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