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Device Features

BlueCore™4-Audio Flash

- Fully Qualified Bluetooth v2.0+EDR
- Enhanced Data Rate (EDR) compliant with v2.0 of the specification for both 2Mbps and 3Mbps modulation modes
- Full Speed Bluetooth Operation with Piconet and Scatternet Support
- Embedded 6Mbit Flash
- Low Power 1.8V operation
- Integrated Switch-mode Regulator
- Integrated Battery Charger with Programmable Current
- 8 x 8mm 96-ball TFBGA Package
- UART Port
- 15-bit Linear Audio CODEC
- 4.2V Tolerant LED Drivers with Intensity Control

Single Chip Bluetooth® v2.0 + EDR System

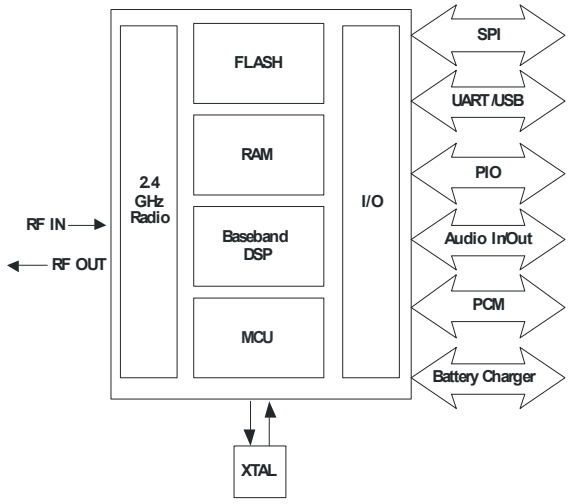
Production Information Data Sheet For BC41C671A

January 2007

General Description

BlueCore™4-Audio Flash is a single chip radio and baseband IC for Bluetooth 2.4GHz systems including enhanced data rates (EDR) to 3Mbps.

BlueCore4-Audio Flash contains 6Mbits of internal Flash memory. When used with the CSR Bluetooth software stack, it provides a fully compliant Bluetooth system to v2.0 + EDR of the specification for data and voice communications.



System Architecture

Applications

- Headsets
- Automotive Hands-Free Kits
- General purpose Bluetooth systems requiring an on-chip audio CODEC

BlueCore4-Audio Flash has been designed to reduce the number of external components required which ensures production costs are minimised. The device incorporates auto-calibration and built in self test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v2.0 + EDR specification (all mandatory and optional features).

BlueCore™4-Audio Flash Product Data Sheet

Contents

List of Figures

List of Tables

List of Equations

Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Life Support Policy and Use in Safety-Critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

RoHS Compliance

BlueCore4-Audio Flash devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

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CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

1 Key Features

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time. No external trimming is required in production
- Bluetooth v2.0 + EDR Specification compliant

Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch
- Class 1 support using external power amplifier with RF power controlled by an internal 8-bit DAC

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser; requires no external VCO, varactor diode, resonator or loop filter
- Compatible with an external crystal or with an external clock using sinusoidal or logic-level signals
- Accepts 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies typically used in GSM and CDMA devices with sinusoidal or logic level signals

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low Park/Sniff/Hold mode
- Clock request output to control external clock
- On-chip high efficiency switch-mode regulator output from 2.5V to 4.2V input.
- On-chip linear regulator; 1.8V output from a 2.2 to 4.2V input, can also be used to generate microphone bias
- Power-on-reset cell detects low supply voltage

Auxiliary Features (Continued)

- Arbitrary power supply sequencing permitted
- 8-bit ADC and DAC available to applications
- Battery charger with programmable current (25 -100mA) for Lithium Ion/Polymer battery
- LED intensity control for dedicated LED1 and LED0 outputs

Baseband and Software

- Internal 6Mbit Flash for complete sytem solution
- Internal 48KB RAM to support EDR. Allows full speed data transfer, mixed voice and data, and full piconet operation
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbits/s for system debugging
- UART interface with programmable baud rate up to 3Mbits/s with an optional bypass mode
- Full speed USB v1.1 interface supports OHCI and UHCI host interfaces. Compliant with USB v2.0
- Optional I²C™ compatible interface

Audio CODEC

- 15-bit resolution, 8kHz sampling frequency
- Digital enhancements to add bass cut, side tone and treble boost
- Analogue enhancements to support single-ended speaker drive capability and reference availability

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on-chip in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded to RFCOMM
- Customised builds with embedded application code

Package Options

- 96-ball TFBGA, 8 x 8 x 1.2mm, 0.65mm pitch

2 Package Information

2.1 BC41C671A Pinout Diagram

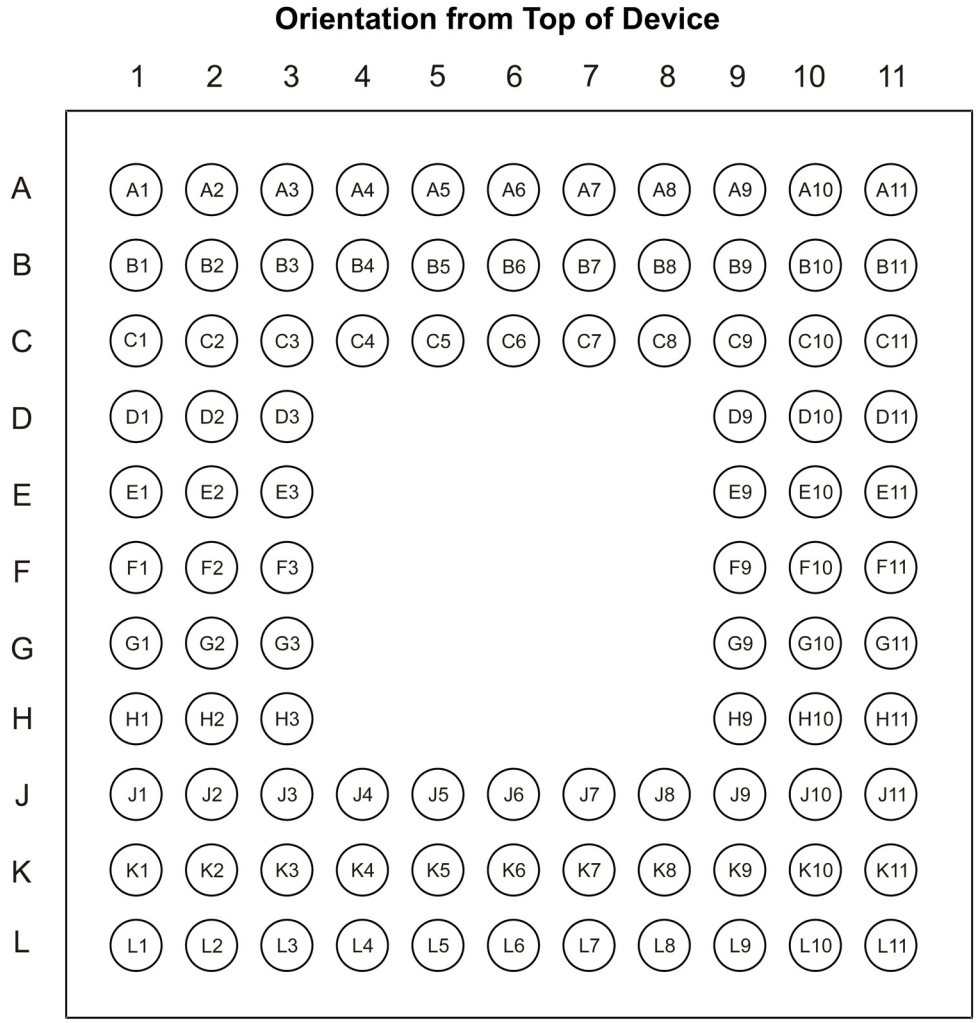

Figure 2.1: BlueCore4-Audio Flash Device Pinout

2.2 Device Terminal Functions

Radio	Ball	Pad Type	Supply Pad	Description
RX_IN	D1	Analogue	VDD_RADIO	Single ended receiver input
PIO[0]/RXEN	A1	Bi-directional with programmable strength internal pull-up/down	VDD_PIO	Control output for external TX/RX switch (if fitted)
PIO[1]/TXEN	B2	Bi-directional with programmable strength internal pull-up/down	VDD_PIO	Control output for external PA (If fitted)
RF_P	F1	Analogue	VDD_RADIO	Transmitter output/switched receiver input
RF_N	E1	Analogue	VDD_RADIO	Complement of RF_P
AUX_DAC	C3	Analogue	VDD_PIO	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Supply Pad	Description
XTAL_IN	L4	Analogue	VDD_ANA	For crystal or external clock input
XTAL_OUT	K4	Analogue	VDD_ANA	Drive for crystal

USB and UART	Ball	Pad Type	Supply Pad	Description
UART_TX	K9	CMOS output, tri-state, with weak internal pull-up	VDD_USB	UART data output
UART_RX	K10	CMOS input with weak internal pull-down	VDD_USB	UART data input
UART_RTS	L8	CMOS output, tri-state, with weak internal pull-up	VDD_USB	UART request to send active low
UART_CTS	K11	CMOS input with weak internal pull-down	VDD_USB	UART clear to send active low
USB_DP	L10	Bi-directional	VDD_USB	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	L9	Bi-directional	VDD_USB	USB data minus

PCM Interface	Ball	Pad Type	Supply Pad	Description
PCM_OUT	G11	CMOS output, tri-state, with weak internal pull-down	VDD_PADS	Synchronous data output
PCM_IN	J11	CMOS input, with weak internal pull-down	VDD_PADS	Synchronous data input
PCM_SYNC	H9	Bi-directional with weak internal pull-down	VDD_PADS	Synchronous data sync
PCM_CLK	H11	Bi-directional with weak internal pull-down	VDD_PADS	Synchronous data clock

PIO Port	Ball	Pad Type	Supply Pad	Description
PIO[2]/CLK_REQ	A2	Bi-directional with programmable strength internal pull-up/down	VDD_PIO	PIO or external clock request
PIO[3]/USB_WAKE_UP/ HOST_CLK_REQ	B3	Bi-directional with programmable strength internal pull-up/down	VDD_PIO	PIO or output goes high to wake up PC when in USB mode or clock request input from host controller
PIO[4]/USB_ON	F9	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	PIO or USB on (input senses when VBUS is high, wakes BlueCore4-Audio Flash)
PIO[5]/USB_DETACH	F10	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	PIO line or chip detaches from USB when this input is high
PIO[6]/CLK_REQ	F11	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	PIO line or clock request output to enable external clock for external clock line
PIO[7]/CLK_OUT	G9	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line or programmable frequency clock output
PIO[8]	A5	Bi-directional with programmable strength internal pull-up/down	VDD_PIO	Programmable input/output line
PIO[9]	A4	Bi-directional with programmable strength internal pull-up/down	VDD_PIO	Programmable input/output line
PIO[10]	B4	Bi-directional with programmable strength internal pull-up/down	VDD_PIO	Programmable input/output line
PIO[11]	A3	Bi-directional with programmable strength internal pull-up/down	VDD_PIO	Programmable input/output line
AIO[0]	J6	Bi-directional	VDD_USB	Programmable input/output line
AIO[1]	L6	Bi-directional	VDD_USB	Programmable input/output line
AIO[2]	L7	Bi-directional	VDD_USB	Programmable input/output line
LED[0]	A9	Open drain output	VDD_BAT	Current sink to drive LED
LED[1]	A10	Open drain output	VDD_BAT	Current sink to drive LED

Test and Debug	Ball	Pad Type	Supply Pad	Description
MIC_P	L2	Analogue	VDD_ANA	Microphone differential, Input P
MIC_N	L3	Analogue	VDD_ANA	Microphone differential, Input N
SPKR_P	J2	Analogue	VDD_ANA	Speaker differential output P or single ended output
SPKR_N	J1	Analogue	VDD_ANA	Speaker differential output N

Test and Debug	Ball	Pad Type	Supply Pad	Description
RESETB	D10	CMOS input with weak internal pull-up	VDD_PADS	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	B9	CMOS input with weak internal pull-up	VDD_PADS	Chip select for Synchronous Serial Interface active low
SPI_CLK	C11	CMOS input with weak internal pull-down	VDD_PADS	Serial Peripheral Interface clock
SPI_MOSI	C9	CMOS input with weak internal pull-down	VDD_PADS	Serial Peripheral Interface data input
SPI_MISO	B11	CMOS output, tri-state, with weak internal pull-down	VDD_PADS	Serial Peripheral Interface data output
TEST_EN	C10	CMOS input with strong internal pull-down	VDD_PADS	For test purposes only(leave unconnected)

Power Supplies and Control	Ball	Pad Type	Description
VREG_ENABLE	H3	CMOS input	Regulator control input
VREG_IN	H1	Regulator input	Linear regulator input
VREG_OUT	K1	Regulator output	Linear regulator output
V_CHG	A11	Charger input	Lithium Ion battery charger input
BAT_P	A8	Battery terminal +	Lithium Ion battery positive terminal/Ground connection for switch-mode regulator
BAT_N	A7	Battery terminal -	Lithium Ion battery negative terminal/Ground connection for switch-mode regulator
LX	A6	Switch-mode regulator output	Switch-mode power regulator output
VDD_USB	L11	VDD	Positive supply for UART/USB ports and AIOs
VDD_PIO	B1	VDD	Positive supply for PIO and AUX DAC[a]
VDD_MEM	B6,B8,J7, K8	VDD	Positive supply for memory. Connect to VDD_CORE to provide pin compatibility with previous devices
VDD_PADS	D11	VDD	Positive supply for all digital Input/Output ports[b]
VDD_CORE	E11	VDD	Positive supply for internal digital circuitry
VDD_RADIO	C1	VDD/Regulator sense	Positive supply for RF circuitry
VDD_VCO	H2	VDD	Positive supply for local oscillator circuitry
VDD_ANA	L1,L5	VDD	Positive supply for analogue circuitry and 1.8V regulated output
VSS_MEM	C5,C7	VSS	Ground connection for memory. Connect to provide pin compatibility with future devices
VSS_PADS	C4, C8, D9,J9	VSS	Ground connection for input/output ports
VSS_CORE	E9	VSS	Ground connection for internal digital circuitry
VSS_RADIO	C2,D2,E2, F2	VSS	Ground connections for RF circuitry
VSS_VCO	G1,G2	VSS	Ground connections for local oscillator
VSS_ANA	J3,J4,J5,K 2,K3	VSS	Ground connections for analogue circuitry
VSS	E3	VSS	Ground connection

(a) Positive supply for PIO[3:0] and PIO[11:6].
(b) Positive supply for SPI/PCM ports and PIO[7:4]

Unconnected Terminals	Ball	Description
N/C	B5, B7, B10, C6, D3, E10, F3, G3, G10, H10, J8, J10, K5, K6, K7	Leave unconnected

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Rating	Min	Max
Storage temperature	-40°C	+150°C
Supply voltage: VDD_RADIO, VDD_VCO, VDD_ANA and VDD_CORE	-0.4V	2.2V
Supply voltage: VDD_PADS, VDD_PIO, VDD_MEM and VDD_USB	-0.4V	3.7V
Supply Voltage: VREG_IN	-0.4V	5.6V
Supply Voltage: BAT_P, VREG_ENABLE and LED [1:0]	-0.4V	4.25V
Supply Voltage: V_CHG	-0.4V	6.5V
Other terminal voltages	VSS-0.4V	VDD+0.4V

3.2 Recommended Operating Conditions

Operating Condition	Min	Max
Operating temperature range	-40°C	+105°C
Guaranteed RF performance range[a]	-25°C	+85°C
Supply voltage: VDD_RADIO, VDD_VCO, VDD_ANA and VDD_CORE	1.7V	1.9V
Supply voltage: VDD_PADS, VDD_PIO, VDD_MEM and VDD_USB	1.7V	3.6V
Supply voltage: VREG_IN	2.2V	4.2V[b]
Supply voltage: BAT_P, VREG_ENABLE and LED [1:0]	2.5V	4.2V
Supply voltage: V_CHG	4.35V	6.5V

(a) Typical figures are given for RF performance between -40°C and +105°C.

(b) The device will operate without damage with VREG_IN as high as 5.6V. However the RF performance is not guaranteed above 4.2V.

3.3 Linear Regulator

Linear Regulator	Min	Typ	Max	Unit
Normal Operation				
Input voltage	2.2	-	4.2[a]	V
Dropout voltage (I_{load} = 70 mA)	-	-	350	mV
Output Voltage[b] (I_{load} = 70 mA)	1.70	1.78	1.85	V
Temperature Coefficient	-250	-	+250	ppm/°C
Output Noise[c] [d]	-	-	1	mV rms
Load Regulation (I_{load} < 100 mA)	-	-	50	mV/A
Settling Time[c] [e]	-	-	50	µs
Maximum Output Current	100	-	-	mA
Minimum Load Current	5	-	-	µA
Input Voltage	-	-	4.2	V
Quiescent Current (excluding load, I_{load} < 1mA)	25	35	50	µA
Low Power Mode[f]				
Quiescent Current (excluding load, I_{load} < 100µA)	4	7	10	µA
Disabled Mode[g]				
Quiescent Current	1.5	2.5	3.5	µA

(a) Operation up to 5.6V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore4-Audio Flash, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.2V.

(b) If the Linear Regulator is used as the power supply, the VDD_ANA ball adjacent to VREG_IN should be used for regulator output to optimise performance.

(c) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

(d) Frequency range is 100Hz to 100kHz.

(e) 1mA to 70mA pulsed load.

(f) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode.

(g) The linear regulator is disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA. If the firmware does not latch the regulator internally, the regulator is also disabled when VREG_ENABLE is pulled low.

3.4 Switch-mode Regulator

Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.5	-	4.2	V
Output voltage (I_{load} = 70 mA)	1.70	1.78	1.9	V
Temperature coefficient	-250	-	+250	ppm/°C
Normal Operation				
Output ripple	-	-	1	mV rms
Transient settling time[a]	-	-	50	µs
Maximum load current	100	-	-	mA
Conversion effeciency (I_{load} 70 mA)	-	90	-	%
Switching frequency[b]	-	1.333	-	MHz
Start-up current limit[c]	-	60	-	mA
Low Power Mode[d]				
Output ripple	-	-	1	mV rms
Transient settling time [e]	-	-	700	µs
Maximum load current	20	-	-	mA
Minimum load current	0	-	-	µA
Conversion efficiency (I_{load} 1mA)	-	80	-	%
Switching frequency[f]	50	-	150	kHz
Disabled Mode				
Quiescent Current	-	-	1	µA

(a) 1mA to 70mA pulsed load
(b) Locked to crystal frequency
(c) Current is limited on start-up to prevent excessive stored energy in the filter inductor. The regulator will operate with reduced efficiency until the current limiter is disabled during the firmware boot-up sequence
(d) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode
(e) 100µA to 1mA pulsed load
(f) Defines minimum period between pulses. Pulses are skipped at low current loads

3.5 Battery Charger

Battery Charger	Min	Typ	Max	Unit
Input voltage	4.5	-	6.5	V
Charging Mode (BAT_P rising to 4.2V)				
Supply current [a]	-	2	-	mA
Flat battery charge current[b]	-	4	-	mA
Battery trickle charge current[c] [d]				
Maximum setting (I-CTRL=15):	-	10	-	mA
Minimum setting (I-CTRL=0):	-	2.5	-	mA
Maximum battery fast charge current (I-CTRL =15)[e] [d]				
Headroom[f] > 0.7V:	-	100	-	mA
Headroom[f] = 0.3V:	-	50	-	mA
Minimum battery fast charge current (I-CTRL=0)[e] [d]				
Headroom[f] > 0.7V:	-	25	-	mA
Headroom[f] = 0.3V:	-	15	-	mA
Trickle charge voltage threshold	-	2.9	-	V
Float voltage (with correct trim value set)[g]	4.17	4.2	4.23	V
Float voltage trim step size[g]	-	50	-	mV
Battery charge termination current[h]	-	10	-	%
Standby Mode (BAT_P falling from 4.2V)				
Supply current[a]	-	80	-	µA
Battery current	-	-40	-	µA
Battery recharge hysteresis[i]	100	-	200	mV
Shutdown Mode (V_CHG too low)				
V_CHG under-voltage threshold				
(V_CHG rising):	-	3.9	-	V
(V_CHG falling):	-	3.7	-	V
V_CHG - BAT_P lockout threshold				
(V_CHG rising):	-	0.22	-	V
(V_CHG falling):	-	0.17	-	V
Supply current	-	-	100	µA
Battery current	-1	-	0	µA

(a) Current into V_CHG - does not include current delivered to battery (I (V_CHG) - I (BAT_P))
(b) BAT_P < 1.8V approx.
(c) 1.8V < BAT_P < Float voltage
(d) Charge current can be set in 16 equally spaced steps, under the control of a register setting I-CTRL
(e) Trickle charge threshold < BAT_P < Float voltage
(f) Headroom is defined as the difference between the V_CHG and BAT_P voltages
(g) Float voltage can be adjusted in 15 steps. Trim setting is determined in production test and must be loaded into the battery charger by firmware during boot-up sequence
(h) Specified as a percentage of the Fast charge current

(i) Hysteresis of (V_{FLOAT} - BAT_P) for charging to restart

3.6 Digital Terminals

Digital Terminals		Min	Typ	Max	Unit
Input Voltage Levels					
V_{IL} input logic level low	2.7V ≤ VDD ≤ 3.6V	-0.4	-	+0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	+0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, (I_o = 4.0mA), 2.7V ≤ VDD ≤ 3.6V		-	-	0.2	V
V_{OL} output logic level low, (I_o = 4.0mA), 1.7V ≤ VDD ≤ 1.9V		-	-	0.4	V
V_{OH} output logic level high, (I_o = -4.0mA), 2.7V ≤VDD ≤ 3.6V		VDD-0.2	-	-	V
V_{OH} output logic level high, (I_o = -4.0mA), 1.7V ≤VDD ≤1.9V		VDD-0.4	-	-	V
Input and Tri-state Current with:					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		+10	+40	+100	µA
Weak pull-up		-5.0	-1.0	-0.2	µA
Weak pull-down		+0.2	+1.0	+5.0	µA
I/O pad leakage current		-1	0	+1	µA
C_I Input Capacitance		1.0	-	5.0	pF

3.7 USB Terminals

USB Terminals	Min	Typ	Max	Unit
VDD_USB for correct USB operation	3.1		3.6	V
Input Threshold				
V_{IL} input logic level low	-	-	0.3VDD_USB	V
V_{IH} input logic level high	0.7VDD_USB	-	-	V
Input Leakage Current				
VSS_PADS < VIN < VDD_USB[a]	-1	1	5	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

(a) Internal USB pull-up disabled

3.8 Power on Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

3.9 Auxilliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	8	Bits
Input voltage range (LSB size = VDD_ANA/255)		0	-	VDD_ANA	V
Accuracy	INL	-1	-	1	LSB
(Guaranteed monotonic)	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain Error		-0.8	-	0.8	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate[a]		-	-	700	Samples/s

[a] ADC is accessed through the VM function. The sample rate given is achieved as part of this function.

3.10 Auxilliary DAC

Auxiliary DAC	Min	Typ	Max	Unit
Resolution	-	-	8	Bits
Average output step size[a]	12.5	14.5	17.0	mV
Output Voltage		monotonic[a]		
Voltage range (I_O=0mA)	VSS_PADS	-	VDD_PIO	V
Current range	-10.0	-	0.1	mA
Minimum output voltage (I_O=100µA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	1	µA
Offset	-220	-	120	mV
Integral non-linearity[a]	-2	-	2	LSB
Settling time (50pF load)	-	-	10	µs

(a) Specified for an output voltage between 0.2V and VDD_PIO -0.2V. Output is high impedance when chip is in Deep Sleep mode

3.11 Clocks

Crystal Oscillator	Min	Typ	Max	Unit
Crystal frequency[a]	8.0	-	32.0	MHz
Digital trim range[b]	5.0	6.2	8.0	pF
Trim step size[b]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance[c]	870	1500	2400	Ω
External Clock				
Input frequency[d]	7.5	-	40.0	MHz
Clock input level[e]	0.2	-	VDD_ANA	V pk-pk
Allowable Jitter	-	-	15	ps rms
XTAL_IN input impedance	-	-	-	kΩ
XTAL_IN input capacitance	-	7	-	pF

(a) Integer multiple of 250kHz
(b) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim
(c) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF
(d) Clock input can be any frequency between 8MHz and 40MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz
(e) Clock input can be either sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA. A DC blocking capacitor is required between the signal and XTAL_IN

3.12 Audio CODEC

Audio CODEC, 15Bit Resolution	Min	Typ	Max	Unit
Microphone Amplifier				
Input full scale at maximum gain	-	3	-	mV rms
Input full scale at minimum gain	-	350	-	mV rms
Gain resolution(a)	2.8	3	3.2	dB
Distortion at 1kHz	-	-	-78	dB
Input referenced rms noise(b)	-	5	-	μV rms
Bandwidth	-	20	-	kHz
Mic mode input impedance	-	20	-	kΩ
Input mode input impedance	-	130	-	Ω
Analogue to Digital Converter				
Input sample rate(c)	-	1	-	MSamples/s
Output sample rate(d)	-	8	-	KSamples/s
Distortion and noise at 1kHz (relative to full scale)	-	-78	-75	dB
Digital to Analogue Converter				
Gain resolution	2.8	3	3.2	dB
Min gain(e)	-	-18	-	dB
Max gain(e)	-	3	-	dB
Loudspeaker Driver				
Output voltage full scale swing (differential)	-	2.0	-	V Pk-Pk
Output current drive (at full scale swing)(f)	10	20	40	mA
Output full scale current (at reduced swing)(g)	-	75	-	mA
Output -3dB bandwidth	-	18.5	-	kHz
Distortion and noise (relative to full scale) (32Ω load) differential	-	-75	-	dB
Allowed load: resistive	8(h)	-	Open Circuit	Ω
Allowed load: capacitive	-	-	500	pF

(a) 42dB range of gain control (under software control)
(b) Noise in bandwidth from 100Hz to 4kHz gain setting >17dB
(c) Single bit, second order T - Δ ADC clocked at 1MHz
(d) This is the decimated and filtered output at 15-bit resolution
(e) 21dB gain range (under software control)
(f) Output for 0.1%THD, signal level of 2V Pk-Pk differential
(g) Output for 1%THD, signal level of 1V Pk-Pk differential
(h) Output swing reduced to 1.2V Pk-Pk differential with 1%THD or 0.1V Pk-Pk differential with 0.1%THD

3.13 Power Consumption

3.13.1 Typical Average Current

Operation Mode	Connection Type	UART Rate (kbps)	Average	Unit[a]
Page scan	-	115.2	0.49	mA
Inquiry and page scan	-	115.2	0.83	mA
ACL No traffic	Master	115.2	4.1	mA
ACL With file transfer	Master	115.2	12	mA
ACL No traffic	Slave	115.2	17	mA
ACL With file transfer	Slave	115.2	21	mA
ACL 40ms sniff	Master	38.4	2.4	mA
ACL 1.28s sniff	Master	38.4	0.37	mA
SCO HV1	Master	38.4	41	mA
SCO HV3	Master	38.4	21	mA
SCO HV3 30ms sniff	Master	38.4	20	mA
ACL 40ms sniff	Slave	38.4	2.1	mA
ACL 1.28s sniff	Slave	38.4	0.42	mA
Parked 1.28s beacon	Slave	38.4	0.20	mA
SCO HV1	Slave	38.4	41	mA
SCO HV3	Slave	38.4	26	mA
SCO HV3 30ms sniff	Slave	38.4	20	mA
Standby Host connection[b]	-	38.4	76	µA
Reset (RESETB low)[b]	-	-	58	µA

[a] Current measured into the 1V8 supply pins.

[b] Low power mode on the linear regulator is entered and exited automatically when the chip enters/leaves Deep Sleep mode. For more information about the electrical characteristics of the linear regulator, see section 3.3 in this document.

3.13.2 Typical Measurement Conditions

Firmware	HCI 19.2
VREG_IN, VDD_PIO, VDD_PADS	3.15V
Clock source	26MHz crystal
Output power	0dBm

4 Radio Characteristics - Basic Data Rate

Important Note:

BlueCore4-Audio Flash meets the Bluetooth v2.0+EDR specification when used in a suitable application circuit between -40°C and +105°C. TX output is guaranteed unconditionally stable over guaranteed temperature range (between -25°C and +85°C).

4.1 Temperature +20°C

4.1.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = +20°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power(a) (b)	-	6.0	-	-6 to +4(c)	dBm
RF power variation over temperature range with compensation enabled(±)(d)	-	1.5	-	-	dB
RF power variation over temperature range with compensation disabled(±)(d)	-	2.7	-	-	dB
RF power control range	-	35	-	≥16	dB
RF power range control resolution(e)	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	940	-	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$(f) (g)	-	-45	-	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$(f) (g)	-	-45	-	≤-40	dBm
Adjacent channel transmit power $F = F_0 \pm > 3MHz$(f) (g)	-	-50	-	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	-	164	-	$140<f1_{avg}<175$	kHz
$\Delta f2_{max}$ Minimum Modulation	-	150	-	≥115	kHz
$\Delta f1_{avg}/\Delta f2_{avg}$	-	0.97	-	≥0.80	-
Initial carrier frequency tolerance	-	5	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	10	-	≤25	kHz
Drift (five slot packet)	-	12	-	≤40	kHz
2nd Harmonic Content	-	-50	-	≤-30	dBm
3rd Harmonic Content	-	-45	-	≤-30	dBm

(a) The BlueCore4-Audio Flash firmware maintains the transmit power within Bluetooth v2.0+EDR specification limits

(b) Measurement using PSKEY_LC_MAX_TX_POWER setting corresponding to a PSKEY_LC_POWER_TABLE power table entry = 63

(c) Class 2 RF transmit power range, Bluetooth specification v2.0+EDR

(d) These parameters are dependent on matching circuit used, and its behaviour over temperature, therefore these parameters are not under CSR's direct control

(e) Resolution guaranteed over the range -5dB to -25dB relative to maximum power for Tx Level > 20

(f) Measured at F_0 = 2441MHz

(g) BlueCore4-Audio Flash guaranteed to meet ACP performance in Bluetooth v2.0+EDR specification, three exceptions allowed