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CYPRESS
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CYW20735

Single-Chip Bluetooth Transceiver for Wireless Input Devices

The Cypress CYW20735 is a Bluetooth 4.2-compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver. Manufactured using the industry's advanced 40 nm CMOS low-power process, the CYW20735 employs high levels of integration to minimize external components, reducing the device footprint and the costs associated with implementing Bluetooth solutions.

The CYW20735 is the optimal solution for applications in wireless input devices including game controllers, remote controls, keyboards, and joysticks.

Built-in firmware adheres to the Bluetooth Low Energy (BLE) profile and the BLE Human Interface Device (HID) profile.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Cypress to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM20735	CYW20735
BCM20735PKML1G	CYW20735PKML1G
BCM20735KFBG	CYW20735KFBG

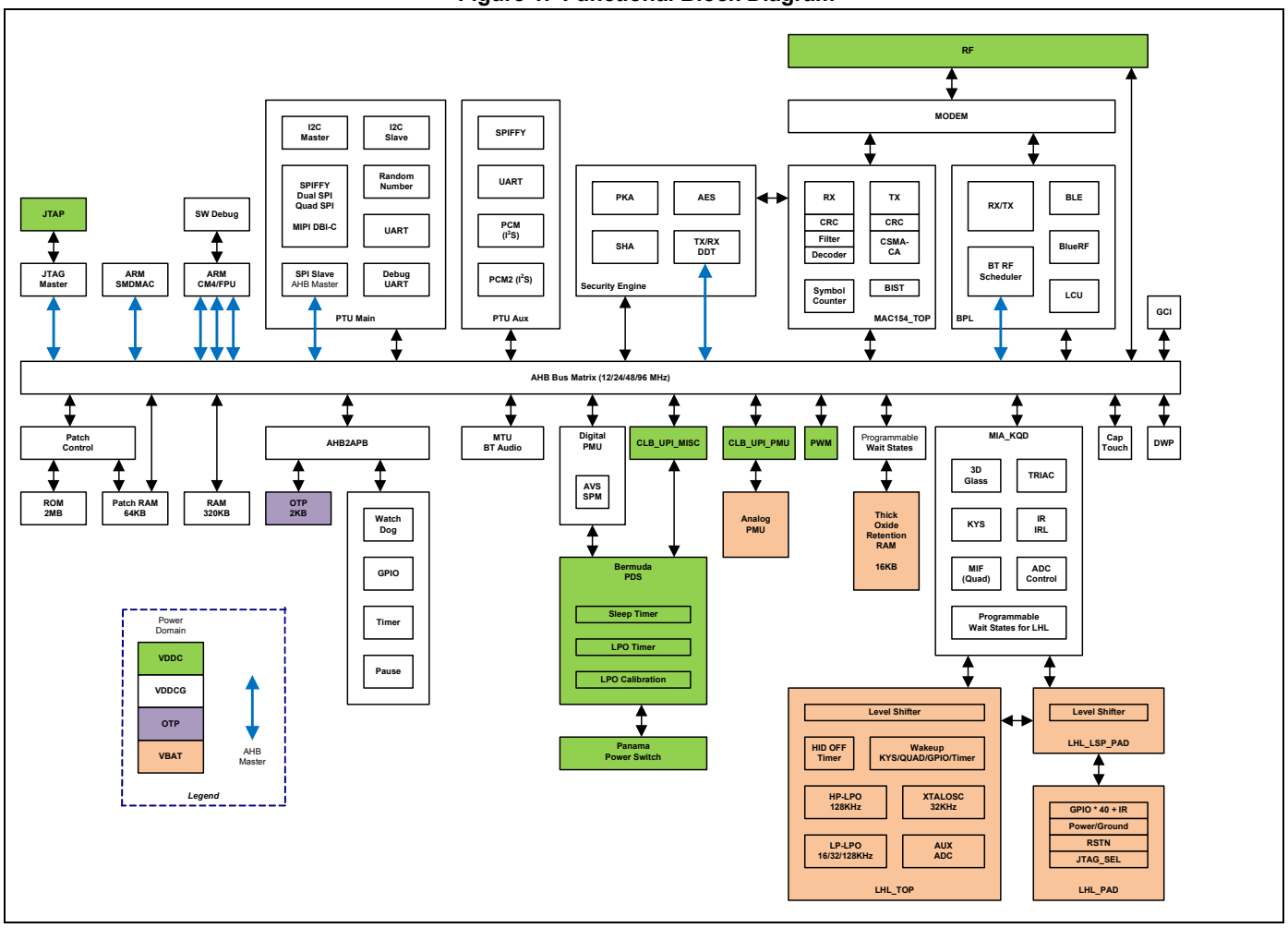
Applications

- Game controllers
- Wireless pointing devices (mice)
- Remote controls
- Wireless keyboards
- Joysticks
- Home automation
- Point-of-sale input devices
- 3D glasses
- Blood pressure monitors
- Find-me devices
- Heart-rate monitors
- Proximity sensors
- Thermometers

Features

- Complies with Bluetooth Core Specification version 4.2 including Basic Rate (BR) BR/BLE
- Supports Cypress proprietary data rate up to 2 Mbps
- BLE HID profile version 1.00 compliant
- Bluetooth Device ID profile version 1.3 compliant
- Supports Generic Access Profile (GAP)
- Supports Adaptive Frequency Hopping (AFH)
- Excellent receiver sensitivity
- Programmable output power control
- Integrated ARM Cortex-M4 microprocessor core floating point unit (FPU)
- On-chip power-on reset (POR)
- Support for serial flash devices
- Integrated buck and low dropout (LDO) regulators
- On-chip software controlled power management unit
- Programmable key scan matrix interface, up to 8 × 20 key-scanning matrix
- Three-axis quadrature signal decoder
- Infrared modulator
- IR learning
- Auxiliary ADC with up to 28 analog channels
- On-chip support for serial peripheral interface (SPI) (master and slave modes)
- Cypress Serial Communications (BSC) interface (compatible with NXP I^2C slaves)
- LE packet extension
- Timed wakeup
- Wireless charging interface
- Package types:
  - 60-pin quad flat no-lead (QFN)
  - 111-pin fine pitch ball grid array (FBGA)
  - RoHS compliant

Figure 1. Functional Block Diagram



IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

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1. Functional Description

1.1 Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL and TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

1.1.1 Bluetooth 4.2 Features

The CYW20735 supports the following Bluetooth v4.2 features:

- LE data packet length extension
- LE secure connections
- Link layer privacy

1.1.2 Bluetooth 4.1 Features

The CYW20735 supports the following Bluetooth v4.1 features:

- Secure connections for BR
- Fast advertising interval
- Piconet clock adjust
- Connectionless broadcast
- LE privacy v1.1
- Low duty cycle directed advertising
- LE dual-mode topology

1.1.3 Bluetooth 4.0 Features

The BBC supports all Bluetooth 4.0 features, with the following benefits:

- Dual-mode Bluetooth low energy (BT and BLE operation)
- Extended inquiry response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption pause resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure simple pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link supervision timeout (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link time-out supervision.
- Quality of service (QoS) enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

1.1.4 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task is performed in a different state or substate in the Bluetooth Link Controller.

- BLE states:
  - Advertising
  - Scanning
  - Connection
- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

1.1.5 Test Mode Support

The CYW20735 fully supports Bluetooth Test mode as described in Part I:1 of the Specification of the Bluetooth System Version 3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYW20735 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

1.1.6 Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number based on the link controller state, Bluetooth clock, and device address.

1.2 Microprocessor Unit

The CYW20735 microprocessor unit runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is a Cortex-M4 32-bit RISC processor with embedded ICE-RT debug and serial wire debug (SWD) interface units. The microprocessor also includes 2 MB of ROM memory for program storage and 384 KB of RAM for data scratch-pad.

The internal ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and feature additions. The device also supports the integration of user applications and profiles.

1.2.1 Floating Point Unit

CYW20735 includes the CM4 single precision IEEE-754 compliant floating point unit. For details see the Cortex-M4 manual.

1.2.2 OTP Memory

The CYW20735 includes 2 KB of one-time programmable memory that can be used by the factory to store product-specific information.

Note: Use of OTP requires that a 3V supply be present at all times.

1.2.3 NVRAM Configuration Data and Storage

NVRAM contains configuration information about the customer application, including the following:

- Fractional-N information
- BD_ADDR
- UART baud rate
- SDP service record
- File system information used for code, code patches, or data. The CYW20735 uses SPI flash for NVRAM storage.

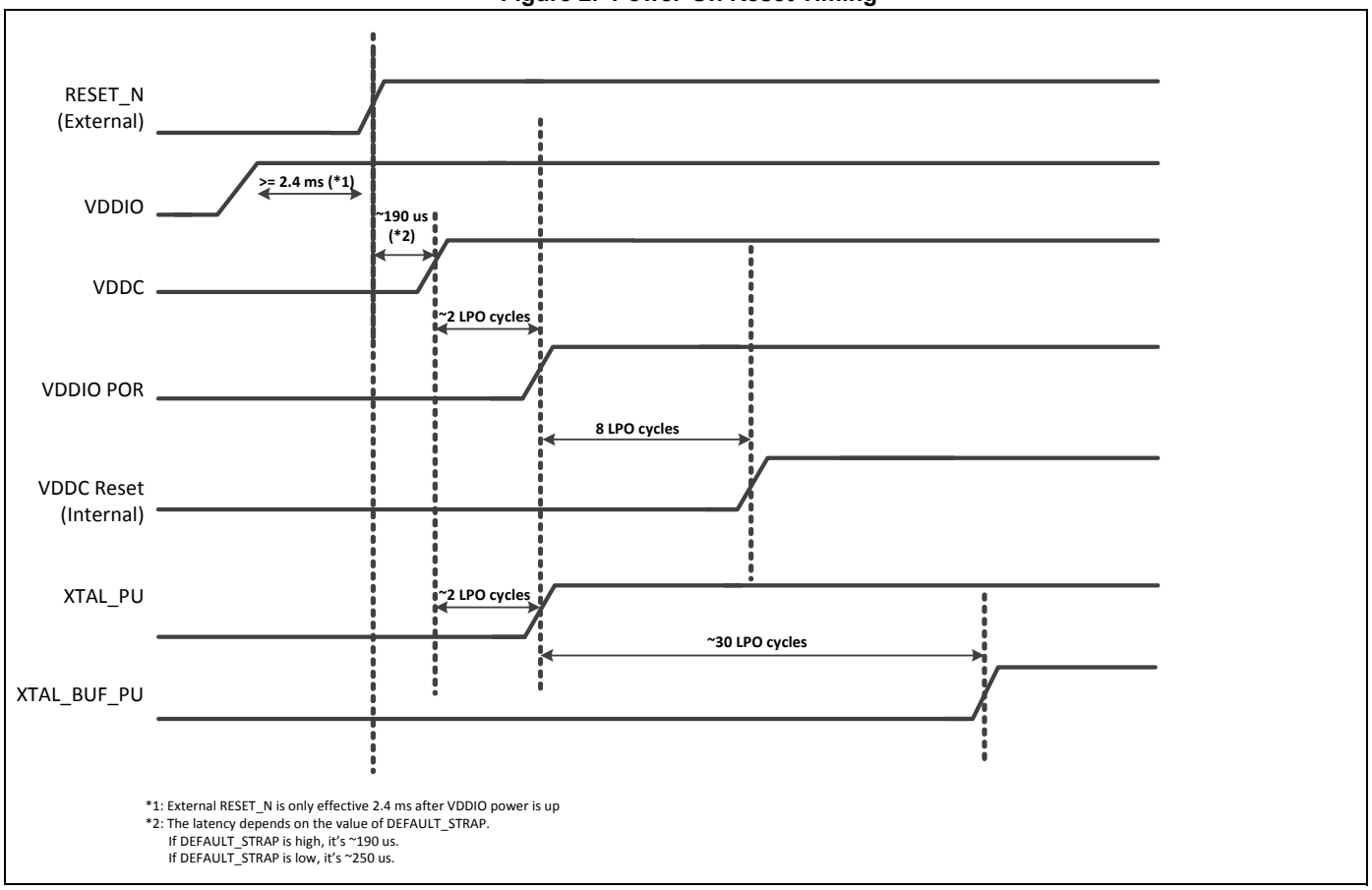
1.2.4 Power-On Reset

The CYW20735 includes POR logic to allow the part to initialize correctly when power is applied. Figure 2 shows the sequence used by the CYW20735 during initialization. An small external cap may be used on RESET_N to add delay as VDDIO ramps up.

1.2.5 External Reset

An external active-low reset signal, RESET_N, can be used to put the CYW20735 in the reset state.

Figure 2. Power-On Reset Timing



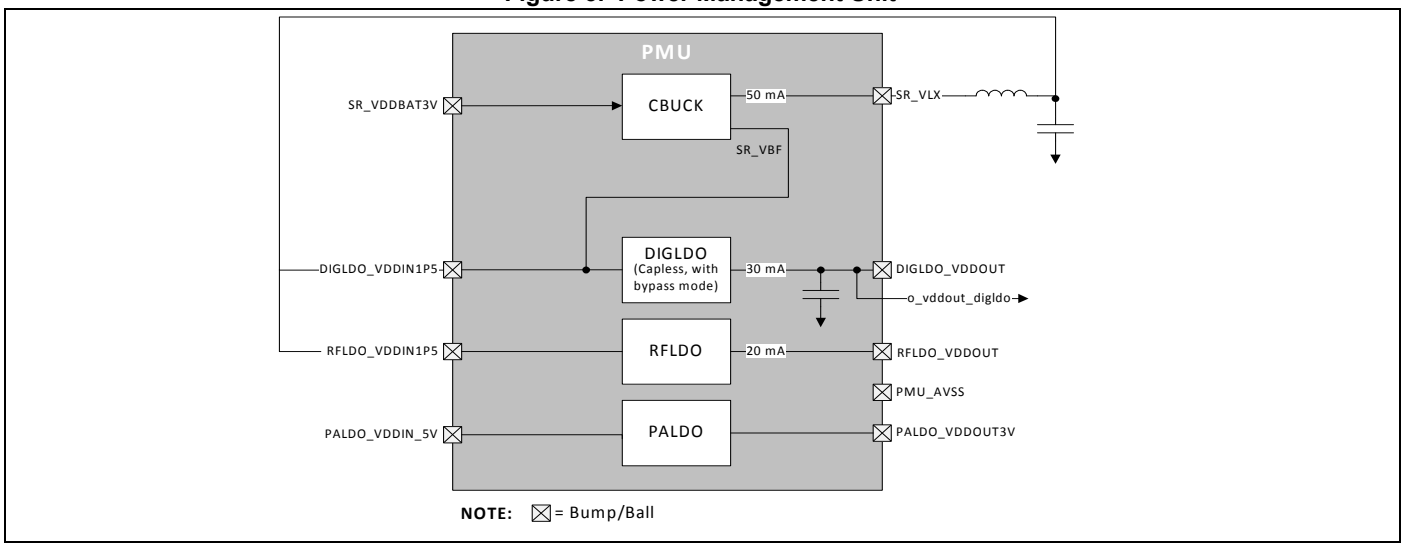
1.2.6 Brownout Detection

An external voltage detector reset IC may be used if brownout detection is required. The reset IC should release RESET_N only after the VDDO supply voltage level has been at or above a minimum operating voltage for 50 ms or longer.

1.3 Power Management Unit

Figure 3 shows the CYW20735 power management unit (PMU) block diagram. The CYW20735 includes an integrated buck regulator, a capless LDO, PALDO and an additional 1.2V LDO for RF.

Figure 3. Power Management Unit



1.4 Integrated Radio Transceiver

The CYW20735 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The CYW20735 is fully compliant with the Bluetooth Radio Specification and meets or exceeds the requirements to provide the highest communication link quality of service.

1.4.1 Transmit Path

The CYW20735 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

1.4.2 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

1.4.3 Power Amplifier

The CYW20735 has an integrated power amplifier (PA) that can transmit up to +10 dBm for class 1 operations.

1.4.4 Receiver Path

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the CYW20735 to be used in most applications with minimal off-chip filtering.

1.4.5 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer takes the low-IF received signal and performs an optimal frequency tracking and bit-synchronization algorithm.

1.4.6 Receiver Signal Strength Indicator

The radio portion of the CYW20735 provides a receiver signal strength indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

1.4.7 Local Oscillator

A local oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The CYW20735 uses an internal loop filter.

1.4.8 Calibration

The CYW20735 radio transceiver features a self-contained automated calibration scheme. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration compensates for filter, matching network, and amplifier gain and phase characteristics to yield radio performance within 2% of what is optimal. Calibration takes process and temperature variations into account, and it occurs transparently during normal operation and hop setting times.

1.5 Peripheral Transport Unit

1.5.1 Cypress Serial Communications Interface

The CYW20735 provides a 2-pin master BSC to communicate with peripherals such as trackball or touch-pad modules, and motion tracking ICs used in mouse devices. The BSC interface is compatible with I^2C slave devices. BSC does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by BSC:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I^2C-compatible speed.)
- 1 MHz (Compatibility with high-speed I^2C-compatible devices is not guaranteed.)

The following transfer types are supported by BSC:

- Read (Up to 8 bytes can be read.)
- Write (Up to 8 bytes can be written.)
- Read-then-Write (Up to 8 bytes can be read and up to 8 bytes can be written.)
- Write-then-Read (Up to 8 bytes can be written and up to 8 bytes can be read.)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins. Pull-up resistors external to the CYW20735 are required on both the SCL and SDA pins for proper operation.

1.6 UART Interface

The CYW20735 includes a UART interface for factory programming and when operating as a BT HCI device in a system with an external host. The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 57600 bps to 6 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The CYW20735 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz, and can be configured to run as high as 48 MHz to support up to 6 Mbps. The baud rate of the CYW20735 UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

Table 2 on page 11 contains example values to generate common baud rates with a 24 MHz UART clock.

Table 2. Common Baud Rate Examples, 24 MHz Clock

Baud Rate (bps)	Baud Rate Adjustment		Mode	Error (%)
	High Nibble	Low Nibble		
3M	0xFF	0xF8	High rate	0.00
2M	0XFF	0XF4	High rate	0.00
1M	0X44	0XFF	Normal	0.00
921600	0x05	0x05	Normal	0.16
460800	0x02	0x02	Normal	0.16
230400	0x04	0x04	Normal	0.16
115200	0x00	0x00	Normal	0.16
57600	0x00	0x00	Normal	0.16

Table 3 contains example values to generate common baud rates with a 48 MHz UART clock.

Table 3. Common Baud Rate Examples, 48 MHz Clock

Baud Rate (bps)	High Rate	Low Rate	Mode	Error (%)
6M	0xFF	0xF8	High rate	0
4M	0xFF	0xF4	High rate	0
3M	0x0	0xFF	Normal	0
2M	0x44	0xFF	Normal	0
1.5M	0x0	0xFE	Normal	0
1M	0x0	0xFD	Normal	0
921600	0x22	0xFD	Normal	0.16
230400	0x0	0xF3	Normal	0.16
115200	0x1	0xE6	Normal	–0.08
57600	0x1	0xCC	Normal	0.04

Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYW20735 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%.

1.7 Peripheral UART Interface

The CYW20735 has a second UART that may be used to interface to peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin. The CYW20735 can map the peripheral UART to any LHL GPIO. The peripheral UART clock is fixed at 24 MHz. Both TX and RX have a 256-byte FIFO (see Table 2: “Common Baud Rate Examples, 24 MHz Clock,” on page 11).

1.8 Clock Frequencies

The CYW20735 uses a 24 MHz crystal oscillator (XTAL).

1.8.1 Crystal Oscillator

The XTAL must have an accuracy of ±20 ppm as defined by the Bluetooth specification. Two external load capacitors in the range of 5 pF to 30 pF are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent (see Figure 4).

Figure 4. Recommended Oscillator Configuration—12 pF Load Crystal

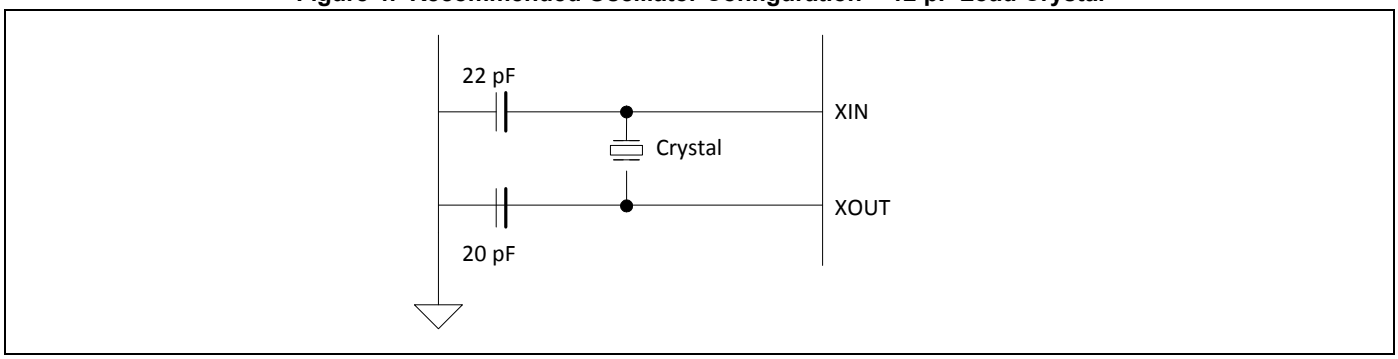


Table 4 shows the recommended crystal specifications.

Table 4. Reference Crystal Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Nominal frequency	–	–	24.000	–	MHz
Oscillation mode	–	Fundamental			–
Frequency tolerance	@25°C	–	±10	–	ppm
Tolerance stability over temp	@0°C to +70°C	–	±10	–	ppm
Equivalent series resistance	–	–	–	60	Ω
Load capacitance	–	–	10	–	pF
Operating temperature range	–	0	–	+70	°C
Storage temperature range	–	–40	–	+125	°C
Drive level	–	–	–	200	µW
Aging	–	–	±3	±10	ppm/year
Shunt capacitance	–	–	–	2	pF

1.8.2 HID Peripheral Block

The peripheral blocks of the CYW20735 all run from a single 128 kHz low-power RC oscillator. The oscillator can be turned on at the request of any of the peripherals. If the peripheral is not enabled, it shall not assert its clock request line.

The keyboard scanner is a special case, in that it may drop its clock request line even when enabled, and then reassert the clock request line if a keypress is detected.

1.8.3 32 kHz Crystal Oscillator

Figure 5 shows the 32 kHz XTAL oscillator with external components and Table 5 on page 13 lists the oscillator's characteristics. It is a standard Pierce oscillator using a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis was added to eliminate any chatter when the input is around the threshold of the comparator and is ~100 mV. This circuit can be operated with a 32 kHz or 32.768 kHz crystal oscillator or be driven with a clock input at a similar frequency. The default component values are: R1 = 10 MΩ and C1 = C2 = ~10 pF. The values of C1 and C2 are used to fine-tune the oscillator.

Figure 5. 32 kHz Oscillator Block Diagram

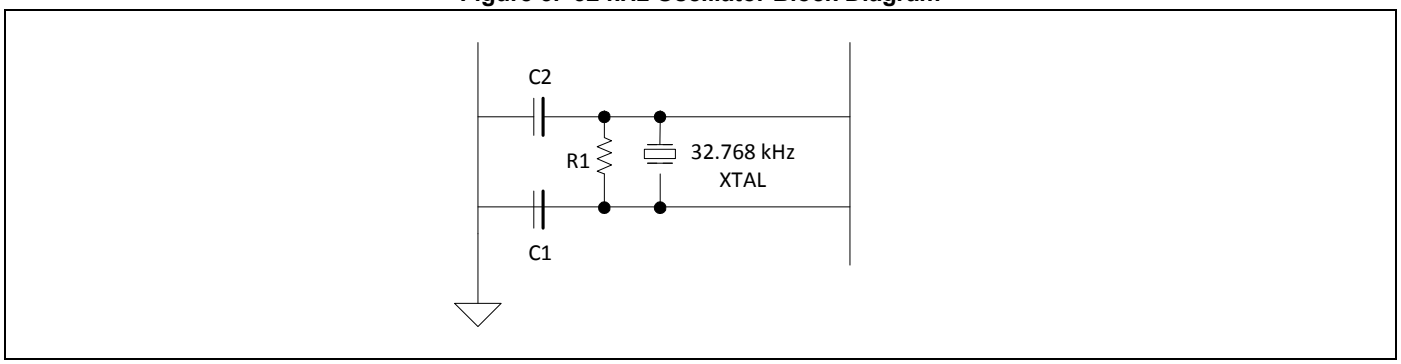


Table 5. XTAL Oscillator Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	–	Crystal-dependent	–	100	–	ppm
Start-up time	$T_{startup}$	–	–	–	500	ms
XTAL drive level	P_{drv}	For crystal selection	0.5	–	–	µW
XTAL series resistance	R_{series}	For crystal selection	–	–	70	kΩ
XTAL shunt capacitance	C_{shunt}	For crystal selection	–	–	1.3	pF

1.9 GPIO Ports

1.9.1 60-Pin QFN Package

The 60-pin QFN package GPIO ports are shown in Table 7 on page 22.

1.9.2 111-Pin FBGA Package

The 111-pin FBGA package GPIO ports are also shown in Table 7 on page 22.

The CYW20735 uses 40 general-purpose I/Os (GPIOs) in the 111-pin FBGA package. All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3V or 4 mA at 1.8V, except P26, P27, P28, and P29, which are capable of driving up to 16 mA at 3.3V or 8 mA at 1.8V.

P0, P1, P8-P19, P21-23, P28-P38: all of these pins can be programmed as ADC inputs.

Port 26–Port 29: all four of these pins are capable of sinking up to 16 mA for LEDs. These pins also have the PWM function, which can be used for LED dimming.

1.10 Keyboard Scanner

The keyboard scanner is designed to autonomously sample keys and store them into buffer registers without the need for the host microcontroller to intervene. The scanner has the following features:

- Ability to turn off its clock if no keys are pressed.
- Sequential scanning of up to 160 keys in an 8 × 20 matrix.
- Programmable number of columns from 1 to 20.
- Programmable number of rows from 1 to 8.
- 16-byte key code buffer (can be augmented by firmware).
- 128 kHz clock that allows scanning of full 160-key matrix in about 1.2 ms.
- N-key rollover with selective 2-key lockout if ghost is detected.
- Keys are buffered until host microcontroller has a chance to read it, or until overflow occurs.
- Hardware debouncing and noise/glitch filtering.
- Low-power consumption. Single-digit µA-level sleep current.

1.10.1 Theory of Operation

The key scan block is controlled by a state machine with the following states:

1.10.2 Idle

The state machine begins in the idle state. In this state, all column outputs are driven high. If any key is pressed, a transition occurs on one of the row inputs. This transition causes the 128 kHz clock to be enabled (if it is not already enabled by another peripheral) and the state machine to enter the scan state. Also in this state, an
8-bit row-hit register and an 8-bit key-index counter is reset to 0.

1.10.3 Scan

In the scan state, a row counter counts from 0 up to a programmable number of rows minus 1. After the last row is reached, the row counter is reset and the column counter is incremented. This cycle repeats until the row and column counters are both at their respective terminal count values. At that point, the state machine moves into the Scan-End state.

As the keys are being scanned, the key-index counter is incremented. This counter value is compared to the modifier key codes stored in RAM, or in the key code buffer if the key is not a modifier key. It can be used by the microprocessor as an index into a lookup table of usage codes.

Also, as the *n*th row is scanned, the row-hit register is ORed with the current 8-bit row input values if the current column contains two or more row hits. During the scan of any column, if a key is detected at the current row, and the row-hit register indicates that a hit was detected in that same row on a previous column, then a ghost condition may have occurred, and a bit in the status register is set to indicate this.

1.10.4 Scan End

This state determines whether any keys were detected while in the scan state. If yes, the state machine returns to the scan state. If no, the state machine returns to the idle state, and the 128 kHz clock request signal is made inactive.

Note: The microcontroller can poll the key status register.

1.11 Mouse Quadrature Signal Decoder

The mouse signal decoder is designed to autonomously sample two quadrature signals commonly generated by an optomechanical mouse. The decoder has the following features:

- Three pairs of inputs for X, Y, and Z (typical scroll wheel) axis signals. Each axis has two options:
  - For the X axis, choose P2 or P32 as X0 and P3 or P33 as X1.
  - For the Y axis, choose P4 or P34 as Y0 and P5 or P35 as Y1.
  - For the Z axis, choose P6 or P36 as Z0 and P7 or P37 as Z1.
- Control of up to four external high-current GPIOs to power external optoelectronics:
  - Turn-on and turn-off time can be staggered for each HC-GPIO to avoid simultaneous switching of high currents and having multiple high-current devices on at the same time.
  - Sample time can be staggered for each axis.
  - Sense of the control signal can be active high or active low.
  - Control signal can be tristated for off condition or driven high or low, as appropriate.

1.11.1 Theory of Operation

The mouse decoder block has four 10-bit PWMs for controlling external quadrature devices and sampling the quadrature inputs at its core.

The GPIO signals may be used to control such items as LEDs, external ICs that may emulate quadrature signals, photodiodes, and photodetectors.

1.12 ADC Port

The ADC block is a single switched-cap Σ-Δ ADC core for audio and DC measurement. It operates at the 12 MHz clock rate and has 32 DC input channels, including 28 GPIO inputs. The internal bandgap reference has ±5% accuracy without calibration. Different calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC mode.

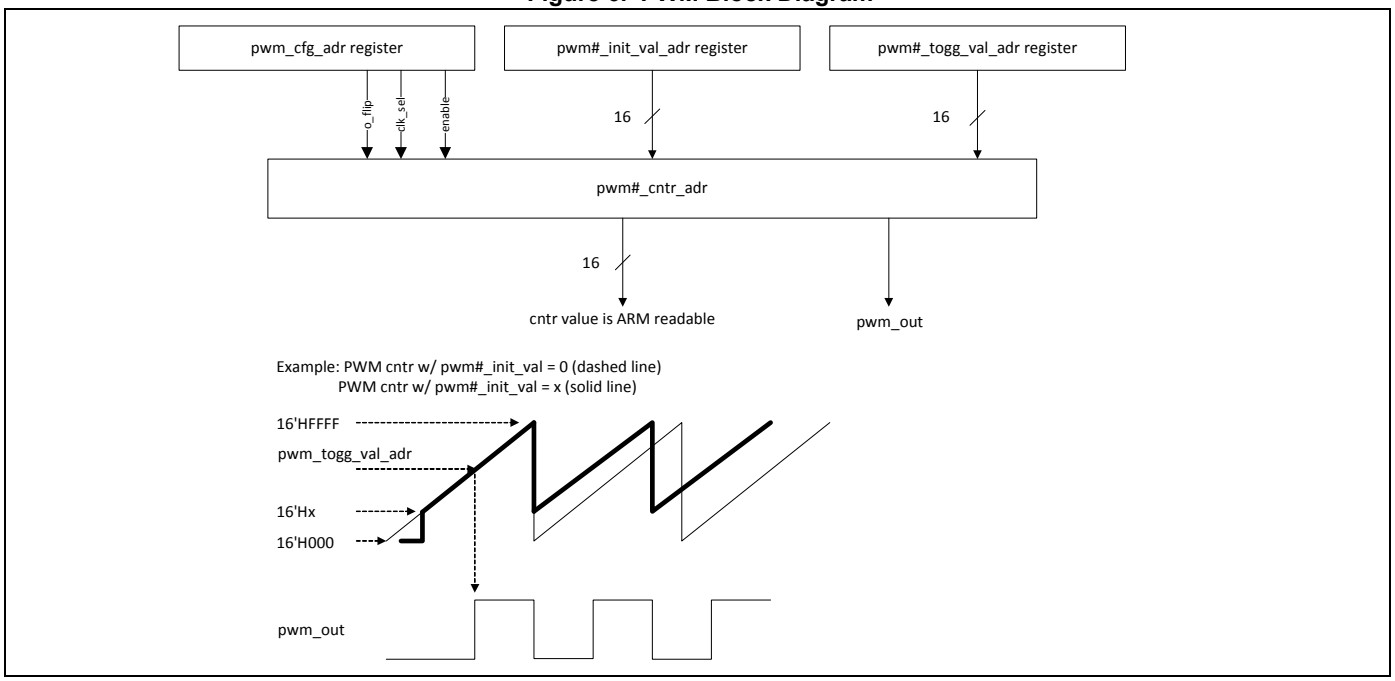
1.13 PWM

The CYW20735 has six internal PWMs. The PWM module consists of the following:

- PWM0–5. Each of the six PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register shared among PWM0–5 (read/write). This 18-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 6 shows the structure of one PWM.

Figure 6. PWM Block Diagram



1.14 Triac Control

The CYW20735 includes hardware support for zero-crossing detection and trigger control for up to four triacs. The CYW20735 detects zero-crossing on the AC zero detection line and uses that to provide a pulse that is offset from the zero crossing. This allows the CYW20735 to be used in dimmer applications, as well as any other applications that require a control signal that is offset from an input event.

The zero-crossing hardware includes an option to suppress glitches.

1.15 Serial Peripheral Interface

The CYW20735 has two independent SPI interfaces, both of which support single, dual, and quad mode SPI operations.

Either interface can be a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYW20735 has optional I/O ports that can be configured individually and separately for each functional pin. The CYW20735 acts as an SPI master device that supports 1.8V or 3.3V SPI slaves. The CYW20735 can also act as an SPI slave device that supports a 1.8V or 3.3V SPI master.

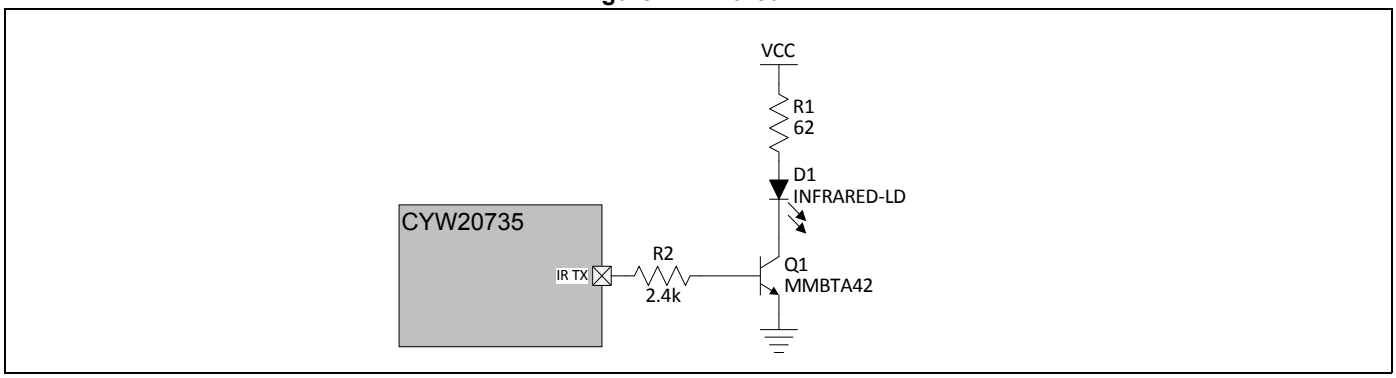
Note: SPI voltage depends on VDDO/VDDM; therefore, it defines the type of devices that can be supported.

1.16 Infrared Modulator

The CYW20735 includes hardware support for infrared TX. The hardware can transmit both modulated and unmodulated waveforms. For modulated waveforms, hardware inserts the desired carrier frequency into all IR transmissions. IR TX can be sourced from firmware-supplied descriptors, a programmable bit, or the peripheral UART transmitter.

If descriptors are used, they include IR on/off state and the duration between 1–32767 µsec. The CYW20735 IR TX firmware driver inserts this information in a hardware FIFO and makes sure that all descriptors are played out without a glitch due to underrun (see Figure 7).

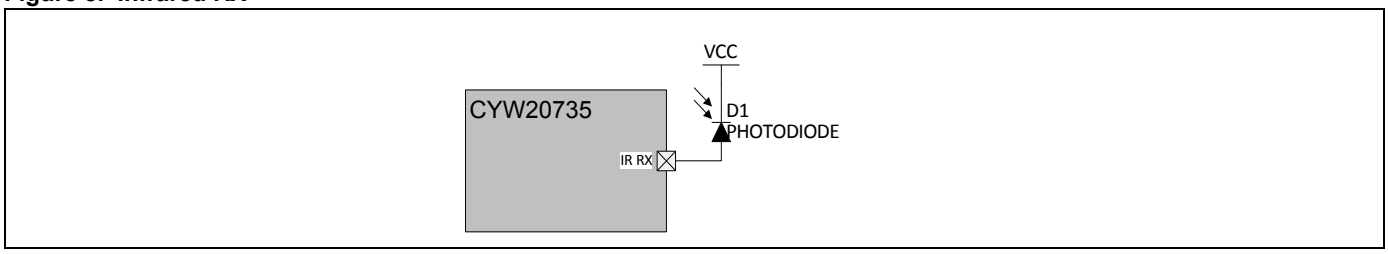
Figure 7. Infrared TX



1.17 Infrared Learning

The CYW20735 includes hardware support for infrared learning. The hardware can detect both modulated and unmodulated signals. For modulated signals, the CYW20735 can detect carrier frequencies between 10 kHz and 500 kHz, and the duration that the signal is present or absent. The CYW20735 firmware driver supports further analysis and compression of the learned signal. The learned signal can then be played back through the CYW20735 IR TX subsystem (see Figure 8).

Figure 8. Infrared RX



1.18 PDM Microphone

The CYW20735 accepts a ΣΔ-based one-bit pulse density modulation (PDM) input stream and outputs filtered samples at either 8 kHz or 16 kHz sampling rates. The PDM signal derives from an external kit that can process analog microphone signals and generate digital signals. The digital signal passes through the chip IO and MUX inputs using an auxADC signal. The PDM shares the filter path with the auxADC. Two types of data rates can be supported:

- 8 kHz
- 16 kHz

The external digital microphone accepts a 2.4 MHz clock generated by the CYW20735 and outputs a PDM signal which is registered by the PDM interface with either the rising or falling edge of the 2.4 MHz clock selectable through a programmable control bit. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible.

1.19 Security Engine

The CYW20735 includes a hardware security accelerator that greatly decreases the time required to perform typical security operations. These functions include:

- Public key acceleration (PKA) cryptography
- AES-CTR/CBC-MAC/CCM acceleration
- SHA2 message hash and HMAC acceleration
- RSA encryption and decryption of modulus sizes up to 2048 bits
- Elliptic curve Diffie-Hellman in prime field GF(p)
- Generic modular math functions

1.20 Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

1.20.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver, which then processes the power-down functions accordingly.

1.20.2 Host Controller Power Management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in HIDOFF (deep sleep) mode.

1.20.3 BBC Power Management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection mode. While in these low-power connection modes, the CYW20735 runs on the Low Power Oscillator and wakes up after a predefined time period.

The CYW20735 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDOFF (deep sleep) mode

The CYW20735 transitions to the next lower state after a programmable period of user inactivity. When user activity resumes, the CYW20735 immediately enters Active mode.

In HIDOFF mode, the CYW20735 baseband and core are powered off by disabling power to VDDC_OUT and PAVDD. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is used for longer periods of inactivity.

2. Pin Assignments and GPIOs

2.1 Pin Assignments

Table 6. Pin Assignments

Pin Name	QFN Pin	FBGA Pin	I/O	Power Domain	Description
Microphone					
ADC_AVDDBAT	–	A4	I	ADC_AVDD	ADC supply
ADC_AVDDC	–	B8	I	ADC_AVDDC	ADC supply
MIC_AVDD	48	A5	I	MIC_AVDD	Microphone supply
MICBIAS	45	A8	I	MIC_AVDD	Microphone bias supply
MICN	47	A6	I	MIC_AVDD	Microphone negative input
MICP	46	A7	I	MIC_AVDD	Microphone positive input
ADC_AVSS	–	C7	I	AVSS	Analog ground
ADC_AVSSC	–	B7	I	AVSS	Analog ground
ADC_REFGND	–	C8	I	AVSS	Analog reference ground
MIC_AVSS	–	B6	I	AVSS	Microphone analog ground
Baseband Supply					
BT_VDDO	36	D11	I	VDDO	I/O pad power supply
BT_VDDC	37	A10, L4	I	VDDC	Baseband core power supply
BT_VSSC	–	D4, D6, D8, G7	I	VSSC	Digital ground
LHL_VDDO	60	E11	I	VDDO	LHL PAD power supply: can be tied to BT_VDDO
OTP_3P3V	–	G6	I	BT_OTP_3P3V	Power supply to the OTP: Leave floating.
OTP_3P3V_ON	–	F7	I	VDDO	This pin should be connected to ground
RF Power Supply					
BT_PAVDD2P5	26	L8	I	PAVDD2P5	PA supply
BT_PLLVDD1P2	31	J9	I	PLLVDD1P2	RFPLL and crystal oscillator supply
BT_VCOVDD1P2	29	L11	I	VCOVDD1P2	VCO supply
BT_IFVDD1P2	28	J8	I	IFVDD1P2	IFPLL power supply
Onboard LDOs					
DIGLDO_VDDIN1P5	25	K7	I	–	Internal digital LDO input and feedback pin of switching regulator (CBUCK).
DIGLDO_VDDOUT	–	H6	O	–	Internal digital LDO output
RFLDO_VDDIN1P5	24	H7	I	–	RF LDO input
RFLDO_VDDOUT	23	J7	O	–	RF LDO output
PALDO_VDDIN_5V	19	K5	I	–	PA LDO input
PALDO_VDDOUT3V	20	J5	O	–	PA LDO output
SR_VDDBAT3V	22	K6	I	–	Core buck input
VDDBAT3V	–	J6	I	–	Core buck input
SR_VLX	21	L6	O	–	Core buck output
Ground Pins					
SR_PVSS	–	L5	I	VSS	Ground
PMU_AVSS	–	H5	I	PMU_AVSS	PMU ground

Table 6. Pin Assignments (Cont.)

Pin Name	QFN Pin	FBGA Pin	I/O	Power Domain	Description
HS-VSS	H	–	I	VSS	Digital ground
PALDO_AVSS	–	H4			PALDO ground
IF_VSS	–	K8			IFPLL ground
PAVSS	–	K9			PA ground
PLLVSS	–	J10			RFPLL ground
VCOVSS	–	K10			VCO ground
NC_PCB_VSS	–	K11			PCB ground
NC_PCB_VSS1	–	L10			PCB ground
NC_PCB_VSS2	–	L7			PCB ground
UART					
UART_CTS_N	44	F10	I, PU	VDDO	CTS for HCI UART interface: NC if unused.
UART_RTS_N	43	E10	O, PU	VDDO	RTS for HCI UART interface. NC if unused.
UART_RXD	41	F11	I	VDDO	UART serial input. Serial data input for the HCI UART interface.
UART_TXD	42	E9	O, PU	VDDO	UART serial input. Serial data input for the HCI UART interface.
Serial Peripheral Interface					
SPI_MISO	40	A11	I	VDDO	SPI Master In Slave Out
SPI_MOSI	39	B11	O	VDDO	SPI Master Out Slave In
SPI_CSN	38	C10	O	VDDO	SPI Chip Select
SPI_CLK	35	C11	O	VDDO	SPI Clock
Crystal					
BT_XTALI	32	J11	I	PLLVDD1P2	Crystal oscillator input: see “Crystal Oscillator” on page 12 for options
BT_XTALO	33	H11	O	PLLVDD1P2	Crystal oscillator output
XTALI_32K	50	B1	I	VDDO	Low-power oscillator input
XTALO_32K	49	A1	O	VDDO	Low-power oscillator output
Others					
Bond 0	–	E7	N/A	N/A	Reserved: Connect to ground for all applications.
Bond 1		E8			
Bond 2		F6			
Bond 3		E6			
DEFAULT_STRAP	18	K4	I	VDDO	Connect to VDDO
BT_HOST_WAKE	34	H8	O	VDDO	Host wake-up. This is a signal from the Bluetooth device to the host indicating that the Bluetooth device requires attention. ■ Asserted: Host device must wake up or remain awake. ■ Deasserted: Host device may sleep when sleep criteria is met. The polarity of this signal is software configurable and can be asserted high or low.

Table 6. Pin Assignments (Cont.)

Pin Name	QFN Pin	FBGA Pin	I/O	Power Domain	Description
BT_DEV_WAKE	–	H9	O	VDDO	Bluetooth device wake-up: This is a signal from the host to the Bluetooth device that the host requires attention. ■Asserted: Bluetooth device must wake up or remain awake. ■Deasserted: Bluetooth device may sleep when sleep criteria is met. The polarity of this signal is software configurable and can be asserted high or low. By default, BT_DEV_WAKE is active-low (if BT-WAKE is low it requires the device to wake up or remain awake). For USB applications, this pin can be used to disable the BT radio, which puts the device in Airport mode.
BT_RF	27	L9	I/O	PAVDD2P5	RF antenna port
CLK_REQ	–	E5	O	VDDO	Used for shared-clock application.
JTAG_SEL	17	F4	–	–	ARM JTAG debug mode control: connect to GND for all applications
RST_N	16	G4	I	VDDO	Active-low system reset with open-drain output and internal pull-up resistor
BT_TM1	–	G5			Reserved: Connect to GND for all applications.
BT_VDDC_ISO_2	–	G9			Leave floating
VDDC_ISO_1	–	G8			Leave floating
VDDC_ISO_1_2	–	D5			Leave floating
ANATEST	–	E4			Leave floating
NC	30	–			Leave floating

2.2 GPIO Pin Descriptions

Table 7. GPIO Pin Descriptions[ab]

QFN Pin Number	FBGA Pin Number	Pin Name	Default Direction	POR State	Power Domain	Default Alternate Function Description
8	F1	P0	Input	Floating	VDDO	■GPIO: P0 ■Keyboard scan input (row): KSI0 ■A/D converter input 29 ■Peripheral UART: puart_tx ■SPI_1: MOSI (master and slave) ■IR_RX ■60Hz_main **Note:** Not available during TM1 = 1.
9	J1	P1	Input	Floating	VDDO	■GPIO: P1 ■Keyboard scan input (row): KSI1 ■A/D converter input 28 ■Peripheral UART: puart_rts ■SPI_1: MISO (master and slave) ■IR_TX
52	A3	P2	Input	Floating	VDDO	■GPIO: P2 ■Keyboard scan input (row): KSI2 ■Quadrature: QDX0 ■Peripheral UART: puart_rx ■SPI_1: SPI_CS (slave only) ■SPI_1: MOSI (master only)
53	A2	P3	Input	Floating	VDDO	■GPIO: P3 ■Keyboard scan input (row): KSI3 ■Quadrature: QDX1 ■Peripheral UART: puart_cts ■SPI_1: SPI_CLK (master and slave)

Table 7. GPIO Pin Descriptions[ab] (Cont.)

QFN Pin Number	FBGA Pin Number	Pin Name	Default Direction	POR State	Power Domain	Default Alternate Function Description
54	B2	P4	Input	Floating	VDDO	■ GPIO: P4 ■ Keyboard scan input (row): KSI4 ■ Quadrature: QDY0 ■ Peripheral UART: puart_rx ■ SPI_1: MOSI (master and slave) ■ IR_TX
55	C4	P5	Input	Floating	VDDO	■ GPIO: P5 ■ Keyboard scan input (row): KSI5 ■ Quadrature: QDY1 ■ Peripheral UART: puart_tx ■ SPI_1: MISO (master and slave) ■ BSC: SDA
56	C3	P6	Input	Floating	VDDO	■ GPIO: P6 ■ Keyboard scan input (row): KSI6 ■ Quadrature: QDZ0 ■ Peripheral UART: puart_rts ■ SPI_1: SPI_CS (slave only) ■ 60Hz_main
57	C2	P7	Input	Floating	VDDO	■ GPIO: P7 ■ Keyboard scan input (row): KSI7 ■ Quadrature: QDZ1 ■ Peripheral UART: puart_cts ■ SPI_1: SPI_CLK (master and slave) ■ BSC: SCL

Table 7. GPIO Pin Descriptions[ab] (Cont.)

QFN Pin Number	FBGA Pin Number	Pin Name	Default Direction	POR State	Power Domain	Default Alternate Function Description
58	C1	P8	Input	Floating	VDDO	■GPIO: P8 ■Keyboard scan output (column): KSO0 ■A/D converter input 27 ■External T/R switch control: ~tx_pd
1	B4	P9	Input	Floating	VDDO	■GPIO: P9 ■Keyboard scan output (column): KSO1 ■A/D converter input 26 ■External T/R switch control: tx_pd
2	B3	P10	Input	Floating	VDDO	■GPIO: P10 ■Keyboard scan output (column): KSO2 ■A/D converter input 25 ■External PA ramp control: ~PA_Ramp
3	G11	P11	Input	Floating	VDDO	■GPIO: P11 ■Keyboard scan output (column): KSO3 ■A/D converter input 24
4	L2	P12	Input	Floating	VDDO	■GPIO: P12 ■Keyboard scan output (column): KSO4 ■A/D converter input 23
5	E3	P13	Input	Floating	VDDO	■GPIO: P13 ■Keyboard scan output (column): KSO5 ■A/D converter input 22 ■PWM3 ■Triac control 3

Table 7. GPIO Pin Descriptions[ab] (Cont.)

QFN Pin Number	FBGA Pin Number	Pin Name	Default Direction	POR State	Power Domain	Default Alternate Function Description
59	B10	P14	Input	Floating	VDDO	■GPIO: P14 ■Keyboard scan output (column): KSO6 ■A/D converter input 21 ■PWM2 ■Triac control 4
50	B5	P15	Input	Floating	VDDO	■GPIO: P15 ■Keyboard scan output (column): KSO7 ■A/D converter input 20 ■IR_RX ■60Hz_main
51	E1	P16	Input	Floating	VDDO	■GPIO: P16 ■Keyboard scan output (column): KSO8 ■A/D converter input 19
–	E2	P17	Input	Floating	VDDO	■GPIO: P17 ■Keyboard scan output (column): KSO9 ■A/D converter input 18
–	D3	P18	Input	Floating	VDDO	■GPIO: P18 ■Keyboard scan output (column): KSO10 ■A/D converter input 17
–	D2	P19	Input	Floating	VDDO	■GPIO: P19 ■Keyboard scan output (column): KSO11 ■A/D converter input 16
–	D1	P20	Input	Floating	VDDO	■GPIO: P20 ■Keyboard scan output (column): KSO12