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BCM® in a VIA Package Bus Converter

BCM3814x60E10A5yzz

Isolated Fixed-Ratio DC-DC Converter

Features & Benefits

- Up to 150A continuous low voltage side current
- Fixed transformation ratio (K) of 1/6
- Up to 769W/in^3 power density
- 97.2% peak efficiency
- Integrated ceramic capacitance filtering
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 3814 package
- High MTBF
- Thermally enhanced VIA package
- PMBus™ management interface

Typical Applications

- DC Power Distribution
- Information and Communication Technology (ICT) Equipment
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Energy Systems
- Transportation

Product Ratings	
V_{HI} = 54V (36 – 60V)	I_{LO} = up to 150A
V_{LO} = 9V (6 – 10V) (NO LOAD)	K = 1/6

Product Description

The BCM3814x60E10A5yzz in a VIA package is a high efficiency Bus Converter, operating from a 36 to 60V_{DC} high voltage bus to deliver an isolated 6 to 10V_{DC} unregulated, low voltage.

This unique ultra-low profile module incorporates DC-DC conversion, integrated filtering and PMBus™ commands and controls in a chassis or PCB mount form factor.

The BCM offers low noise, fast transient response and industry leading efficiency and power density. A low voltage side referenced PMBus™ compatible telemetry and control interface provides access to the BCM's configuration, fault monitoring and other telemetry functions.

Leveraging the thermal and density benefits of Vicor's VIA packaging technology, the BCM module offers flexible thermal management options with very low top and bottom side thermal impedances.

When combined with downstream Vicor DC-DC conversion components and regulators, the BCM allows the Power Design Engineer to employ a simple, low-profile design, which will differentiate the end system without compromising on cost or performance metrics.

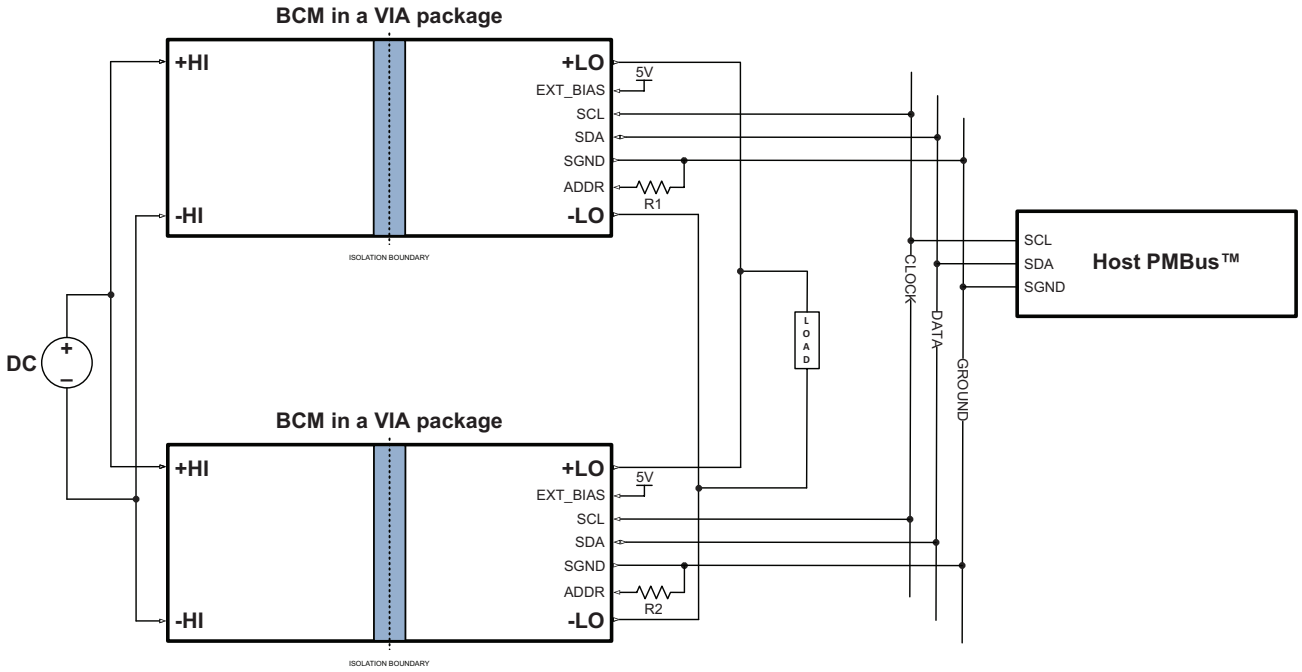
Size:
3.76 x 1.40 x 0.37in
95.59 x 35.54 x 9.40mm

Part Ordering Information

Product Function	Package Length	Package Width	Package Type	Max High Side Voltage	High Side Voltage Range Ratio	Max Low Side Voltage	Max Low Side Current	Product Grade (Case Temperature)	Option Field
BCM	38	14	x	60	E	10	A5	y	zz
BCM = Bus Converter Module	Length in Inches x 10	Width in Inches x 10	B = Board VIA V = Chassis VIA	Internal Reference				C = -20 to 100°C [1] T = -40 to 100°C [1]	02 = Chassis/PMBus 06 = Short Pin/PMBus 10 = Long Pin/PMBus

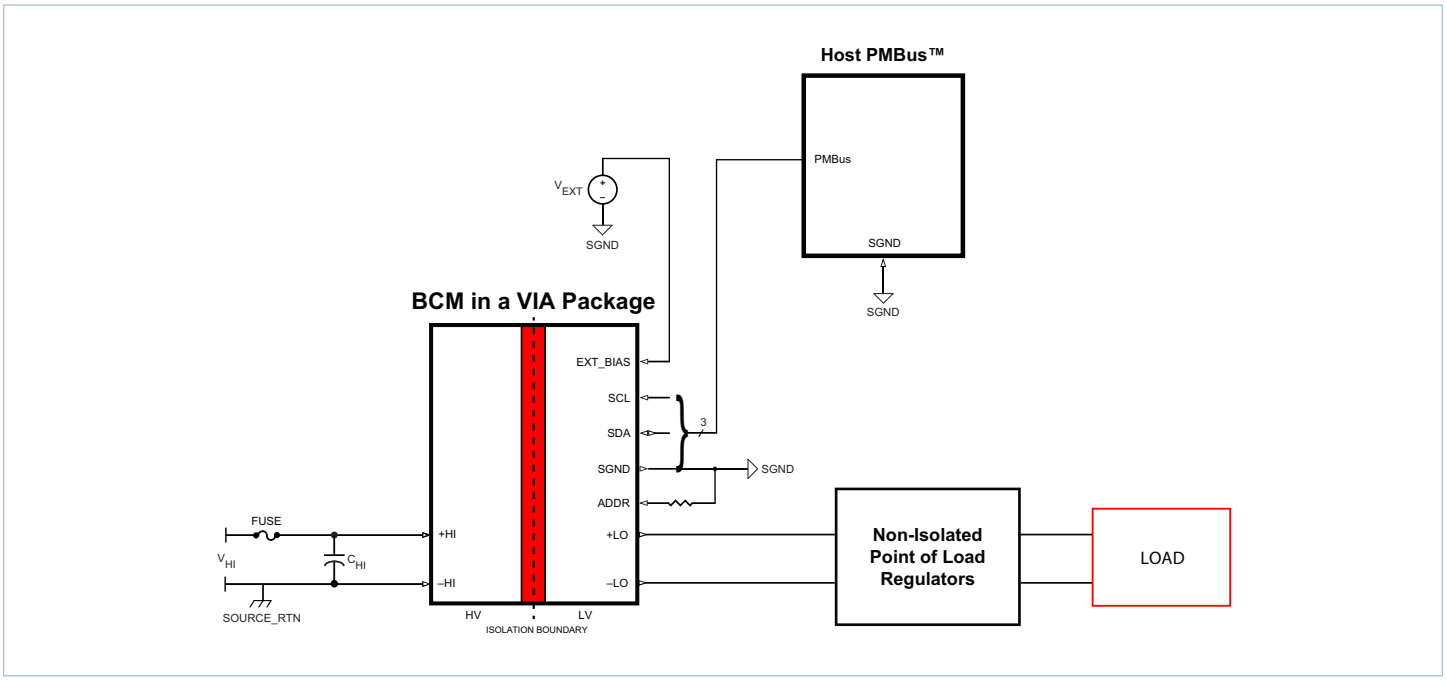
[1] The PMBus name, SMIF, Inc. and logo are trademarks of SMIF, Inc.
[2] High temperature current derating may apply; See Figure 1, specified thermal operating area.

Typical Applications

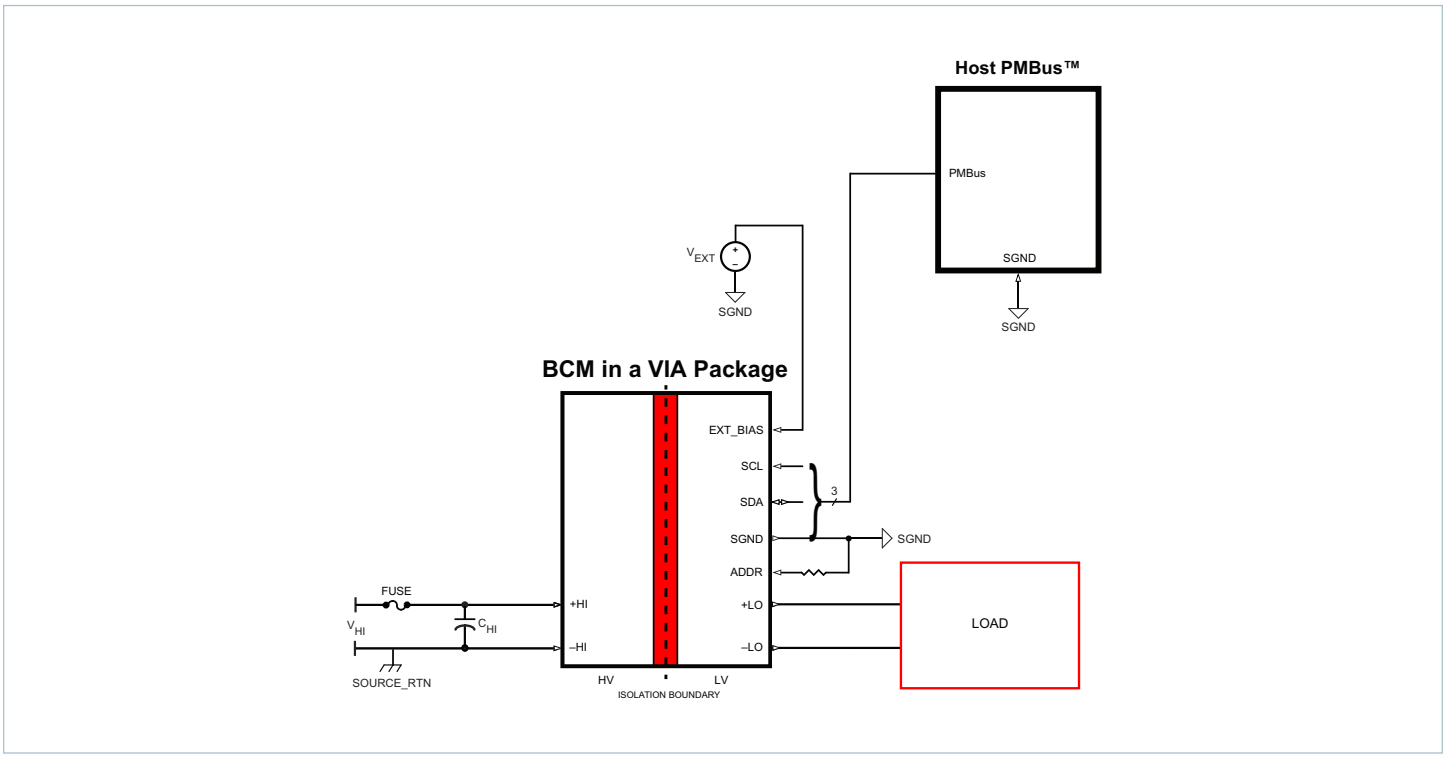


Paralleling PMBus BCM in a VIA package – connection to Host PMBus

Typical Applications (Cont.)

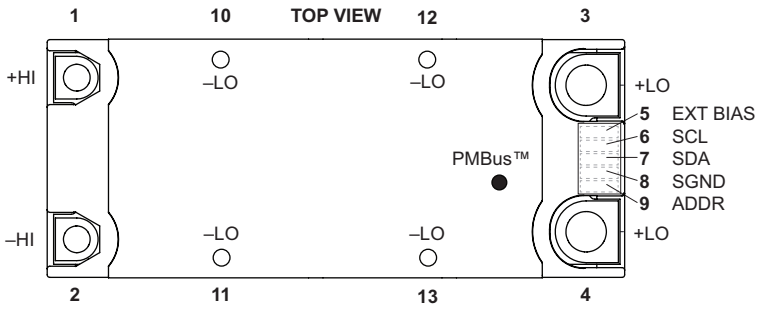


BCM3814x60E10A5yzz at point of load – connection to Host PMBus – connection to Host PMBus

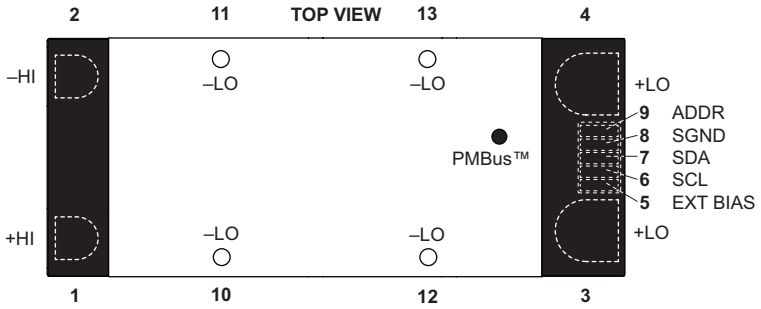


BCM3814x60E10A5yzz direct to load – connection to Host PMBus

Pin Configuration



BCM in a 3814 VIA Package - Chassis (Lug) Mount



BCM in a 3814 VIA Package - Board (PCB) Mount

Note: The dot on the VIA housing indicates the location of the signal pin 9.

Pin Descriptions

Pin Number	Signal Name	Type	Function
1	+HI	HIGH SIDE POWER	High voltage side positive power terminal
2	–HI	HIGH SIDE POWER RETURN	High voltage side negative power terminal
3, 4	+LO	LOW SIDE POWER	Low voltage side positive power terminal
5	EXT BIAS	INPUT	5V supply input
6	SCL	INPUT	I²C™ [1] Clock, PMBus™ Compatible
7	SDA	INPUT/OUTPUT	I²C Data, PMBus Compatible
8	SGND	LOW SIDE SIGNAL RETURN	Signal Ground
9	ADDR	INPUT	Address assignment - Resistor based
10, 11, 12, 13	–LO	LOW SIDE POWER RETURN	Low voltage side negative power terminal

Notes: All signal pins (5, 6, 7, 8, 9) are referenced to the low voltage side and isolated from the high voltage side.
Keep SGND signal separated from the low voltage side power return terminal (–LO) in electrical design.

[1] I²C™ is a trademark of NXP Semiconductor

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+HI to –HI		-1	80	V
HI_DC or LO_DC Slew Rate			1	V/µs
+LO to –LO		-1	15	V
EXT BIAS to SGND		-0.3	10	V
			0.15	A
SCL to SGND		-0.3	5.5	V
SDA to SGND		-0.3	5.5	V
ADDR to SGND		-0.3	3.6	V
Isolation Voltage / Dielectric Withstand	Basic insulation (high voltage side to case)	1500		V_{DC}
	Basic insulation (high voltage side to low voltage side) [1]	1500		V_{DC}
	Functional insulation (low voltage side to case)	N/A		V_{DC}

[1] The absolute maximum rating listed above for the dielectric withstand (high voltage side to the low voltage side) refers to the VIA package. The internal safety approved isolating component (ChiP) provides basic insulation (2250V) from the high voltage side to the low voltage side. However, the VIA package itself can only be tested at a basic insulation value (1500V).

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side)						
HI Side Voltage Range (Continuous)	V_{HI_DC}		**36**		**60**	V
HI Side Voltage Initialization Threshold	$V_{\mu C\_ACTIVE}$	HI side voltage where internal controller is initialized, (powertrain inactive)			14	V
HI Side Quiescent Current	I_{HI_Q}	Disabled, V_{HI_DC} = 54V		5		mA
		T_{CASE} ≤ 100°C			10	
No Load Power Dissipation	P_{HI_NL}	V_{HI_DC} = 54V, T_{CASE} = 25°C		7.2	9	W
		V_{HI_DC} = 54V	**5**		**14**	
		V_{HI_DC} = 36V to 60V, T_{CASE} = 25°C			12	
		V_{HI_DC} = 36V to 60V			**17**	
HI Side Inrush Current Peak	$I_{HI\_INR\_PK}$	V_{HI_DC} = 60V, C_{LO_EXT} = 4000µF, R_{LOAD_LO} = 20% of full load current		30		A
		T_{CASE} ≤ 100°C			35	
DC HI Side Current	$I_{HI\_IN\_DC}$	At $I_{LO\_OUT\_DC}$ = 150A, T_{CASE} ≤ 85°C			25.5	A
Transformation Ratio	K	High voltage to low voltage, K = V_{LO_DC} / V_{HI_DC}, at no load		1/6		V/V
LO Side Current (Continuous)	$I_{LO\_OUT\_DC}$	T_{CASE} ≤ 85°C			150	A
LO Side Current (Pulsed)	$I_{LO\_OUT\_PULSE}$	10ms pulse, 25% duty cycle, $I_{LO\_OUT\_AVG}$ ≤ 50% rated $I_{LO\_OUT\_DC}$			180	A
Efficiency (Ambient)	η_{AMB}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A	95.2	95.8		%
		V_{HI_DC} = 36V to 60V, $I_{LO\_OUT\_DC}$ = 150A	93.6			
		V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 75A	96.7	97.2		
Efficiency (Hot)	η_{HOT}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A T_{CASE} = 85°C	95.4	95.6		%
Efficiency (Over Load Range)	$\eta_{20\%}$	30A < $I_{LO\_OUT\_DC}$ < 150A	93			%
LO Side Output Resistance	R_{LO_COLD}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A, T_{CASE} = -40°C	0.9	1.7	2.1	mΩ
	R_{LO_AMB}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A	2	2.1	2.4	
	R_{LO_HOT}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A, T_{CASE} = 85°C	1.6	2.3	2.6	
Switching Frequency	F_{SW}	Low side voltage ripple frequency = 2x F_{SW}	**0.85**	0.90	**0.95**	MHz
LO Side Voltage Ripple	$V_{LO\_OUT\_PP}$	C_{LO_EXT} = 0µF, $I_{LO\_OUT\_DC}$ = 150A, V_{HI_DC} = 54V, 20MHz BW		120		mV
		T_{CASE} ≤ 100°C			200	

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side), Cont.						
Effective HI Side Capacitance (Internal)	C_{HI_INT}	Effective value at 54V_{HI_DC}		11.2		µF
Effective LO Side Capacitance (Internal)	C_{LO_INT}	Effective value at 9V_{LO_DC}		202		µF
Rated LO Side Capacitance (External)	$C_{LO\_OUT\_EXT}$	Excessive capacitance may drive module into short circuit protection			**6000**	µF
Rated LO Side Capacitance (External), Parallel Array Operation	$C_{LO\_OUT\_AEXT}$	$C_{LO\_OUT\_AEXT}$ Max = N * 0.5 * $C_{LO\_OUT\_EXT\ MAX}$, where N = the number of units in parallel				
Powertrain Hardware Protection Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side)						
• These built-in powertrain protections are fixed in hardware and cannot be configured through PMBus™. • When duplicated in supervisory limits, hardware protections serve a secondary role and become active when supervisory limits are disabled through PMBus.						
Auto Restart Time	$t_{AUTO\_RESTART}$	Startup into a persistent fault condition. Non-latching fault detection given V_{HI_DC} > V_{HI_UVLO+}	**490**		**560**	ms
HI Side Overvoltage Lockout Threshold	V_{HI_OVLO+}		**63**	67	**71**	V
HI Side Overvoltage Recovery Threshold	V_{HI_OVLO-}		**61**	65	**69**	V
HI Side Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			2		V
HI Side Overvoltage Lockout Response Time	t_{HI_OVLO}			100		µs
HI Side Soft-Start Time	$t_{HI\_SOFT-START}$	From powertrain active. Fast current limit protection disabled during soft-start		1		ms
LO Side Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		**180**	204	**240**	A
LO Side Overcurrent Response Time Constant	$t_{LO\_OUT\_OCP}$	Effective internal RC filter		3		ms
LO Side Short Circuit Protection Trip Threshold	$I_{LO\_OUT\_SCP}$		**195**			A
LO Side Short Circuit Protection Response Time	$t_{LO\_OUT\_SCP}$			1		µs
Overtemperature Shutdown Threshold	t_{OTP+}	Internal	**125**			°C

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Supervisory Limits Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side)						
• These supervisory limits are set in the internal controller and can be reconfigured or disabled through PMBus™. • When disabled, the powertrain protections presented in the previous table will intervene during fault events.						
HI Side Overvoltage Lockout Threshold	V_{HI_OVLO+}		**64**	66	**68**	V
HI Side Overvoltage Recovery Threshold	V_{HI_OVLO-}		**60**	64	**66**	V
HI Side Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			2		V
HI Side Overvoltage Lockout Response Time	t_{HI_OVLO}			100		µs
HI Side Undervoltage Lockout Threshold	V_{HI_UVLO-}		**26**	28	**30**	V
HI Side Undervoltage Recovery Threshold	V_{HI_UVLO+}		**28**	30	**32**	V
HI Side Undervoltage Lockout Hysteresis	$V_{HI\_UVLO\_HYST}$			2		V
HI Side Undervoltage Lockout Response Time	t_{HI_UVLO}			100		µs
HI Side Undervoltage Startup Delay	$t_{HI\_UVLO+\_DELAY}$	From V_{HI_DC} = V_{HI_UVLO+} to powertrain active (i.e., one time startup delay from application of V_{HI_DC} to V_{LO_DC})		20		ms
LO Side Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		**193**	204	**215**	A
LO Side Overcurrent Response Time Constant	$t_{LO\_OUT\_OCP}$	Effective internal RC filter		3		ms
Overtemperature Shutdown Threshold	t_{OTP+}	Internal	**125**			°C
Overtemperature Recovery Threshold	$t_{OTP–}$	Internal	105	110	115	°C
Undertemperature Shutdown Threshold (Internal)	t_{UTP}	C-Grade			-25	°C
		T-Grade			-45	
Undertemperature Restart Time	$t_{UTP\_RESTART}$	Startup into a persistent fault condition. Non-latching fault detection given V_{HI_DC} > V_{HI_UVLO+}		3		s

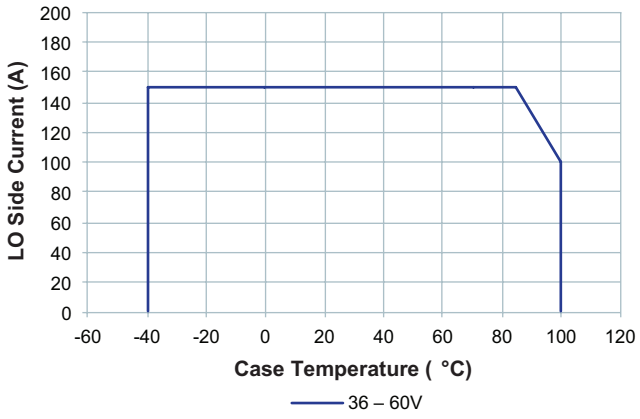


Figure 1 *— Specified thermal operating area*

1.The BCM in a VIA package is cooled through the bottom case (bottom housing).
2. The thermal rating is based on typical measured device efficiency.
3. The case temperature in the graph is the measured temperature of the bottom housing, such that the internal operating temperature does not exceed 125°C.

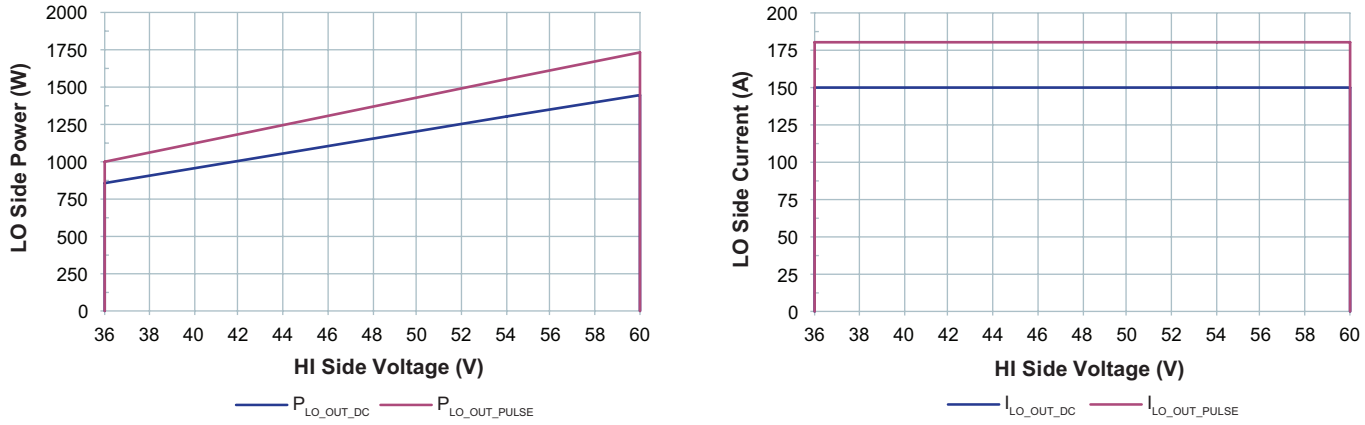


Figure 2 *— Specified electrical operating area using rated R_{LO_HOT}*

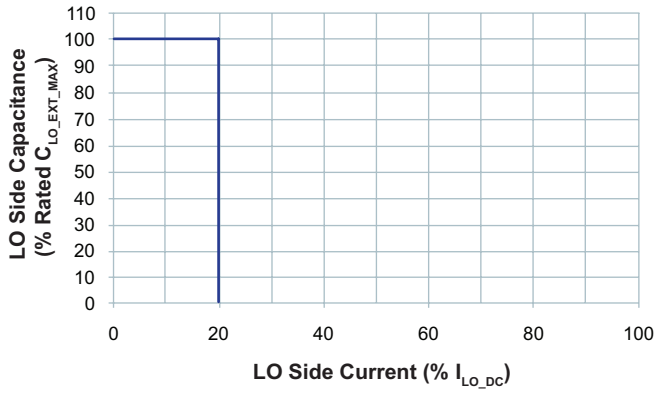


Figure 3 *— Specified HI side startup into load current and external capacitance*

PMBus™ Reported Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Monitored Telemetry					
ATTRIBUTE	**PMBus™ READ COMMAND**	**ACCURACY (RATED RANGE)**	**FUNCTIONAL REPORTING RANGE**	**UPDATE RATE**	**REPORTED UNITS**
HI Side Voltage	(88h) READ_VIN	± 5% (LL - HL)	28V to 66V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
HI Side Current	(89h) READ_IIN	± 20% (10 - 20% of FL) ± 5% (20 - 133% of FL)	-1A to 34A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
LO Side Voltage [1]	(8Bh) READ_VOUT	± 5% (LL - HL)	4.7V to 11V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
LO Side Current	(8Ch) READ_IOUT	± 20% (10 - 20% of FL) ± 5% (20 - 133% of FL)	-6A to 204A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
LO Side Resistance	(D4h) READ_ROUT	± 5% (50 - 100% of FL) at NL ± 10% (50 - 100% of FL) (LL - HL)	500µΩ to 3000µΩ	100ms	$R_{ACTUAL} = R_{REPORTED} \times 10^{-5}$
Temperature [2]	(8Dh) READ_TEMPERATURE_1	± 7°C (Full Range)	- 55°C to 130°C	100ms	$T_{ACTUAL} = T_{REPORTED}$

[1] Default READ LO Side Voltage returned when unit is disabled = -300V.
[2] Default READ Temperature returned when unit is disabled = -273°C.

Variable Parameters					
• Factory setting of all Thresholds and Warning limits listed below are 100% of specified protection values. • Variables can be written only when module is disabled with $V_{HI} < V_{HI\_UVLO-}$ and external bias (VDDB) applied. • Module must remain in a disabled mode for 3ms after any changes to the variables below to allow sufficient time to commit changes to EEPROM.					
ATTRIBUTE	**PMBus™ COMMAND**	**CONDITIONS / NOTES**	**ACCURACY (RATED RANGE)**	**FUNCTIONAL REPORTING RANGE**	**DEFAULT VALUE**
HI Side Overvoltage Protection Limit	(55h) VIN_OV_FAULT_LIMIT	V_{HI_OVLO-} is automatically 3% lower than this setpoint	± 5% (LL - HL)	28V to 66V	100%
HI Side Overvoltage Warning Limit	(57h) VIN_OV_WARN_LIMIT		± 5% (LL - HL)	28V to 66V	100%
HI Side Undervoltage Protection Limit	(D7h) DISABLE_FAULTS	Can only be disabled to a preset default value	± 5% (LL - HL)	28V or 66V	100%
HI Side Overcurrent Protection Limit	(5Bh) IIN_OC_FAULT_LIMIT		± 20% (10 - 20% of FL) ± 5% (20 - 133% of FL)	0 to 34A	100%
HI Side Overcurrent Warning Limit	(5Dh) IIN_OC_WARN_LIMIT		± 20% (10 - 20% of FL) ± 5% (20 - 133% of FL)	0 to 34A	100%
Overtemperature Protection Limit	(4Fh) OT_FAULT_LIMIT	Internal temperature	± 7°C (Full Range)	0 to 125°C	100%
Overtemperature Warning Limit	(51h) OT_WARN_LIMIT	Internal temperature	± 7°C (Full Range)	0 to 125°C	100%
Turn On Delay	(60h) TON_DELAY	Additional time delay to the undervoltage startup delay	± 50µs	0 to 100ms	0ms

Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted. **Please note:** For chassis mount model, Vicor part number 42550 will be needed for applications requiring the use of the signal pins. Signal cable 42550 is rated up to five insertions and extractions. To avoid unnecessary stress on the connector, the cable should be appropriately strain relieved.

EXT. BIAS (VDDB) Pin

- VDDB powers the internal controller.
- VDDB needs to be applied to enable and disable the BCM through PMBus™ control (using OPERATION COMMAND), and to adjust warning and protection thresholds.
- VDDB voltage not required for telemetry; however, if VDDB is not applied, telemetry information will be lost when V_{IN} is removed.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
INPUT	Regular Operation	VDDB Voltage	V_{VDDB}		4.5	5	9	V
		VDDB Current Consumption	I_{VDDB}				50	mA
	Startup	Inrush Current Peak	I_{VDDB_INR}	V_{VDDB} slew rate = 1V/µs		3.5		A
		Turn On Time	t_{VDDB_ON}	From V_{VDDB_MIN} to PMBus active		1.5		ms

SGND Pin

- All PMBus interface signals (SCL, SDA, ADDR) are referenced to SGND pin.
- SGND pin also serves as return pin (ground pin) for VDDB.
- Keep SGND signal separated from the low voltage side power return terminal (–LO) in electrical design.

Address (ADDR) Pin

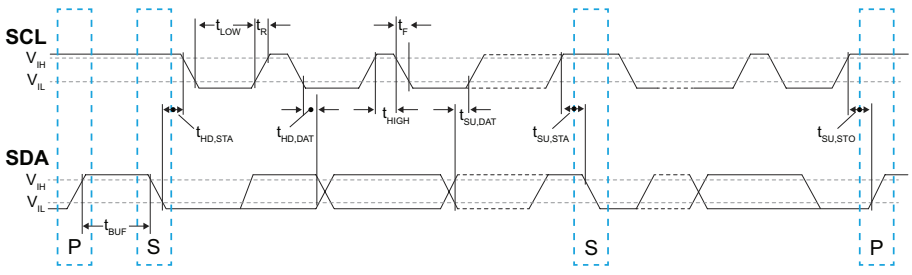
- This pin programs the address using a resistor between ADDR pin and signal ground.
- The address is sampled during startup and is stored until power is reset. This pin programs only a Fixed and Persistent address.
- This pin has an internal 10kΩ pullup resistor to 3.3V.
- 16 addresses are available. The range of each address is 206.25mV (total range for all 16 addresses is 0V to 3.3V).

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
MULTI–LEVEL INPUT	Regular Operation	ADDR Input Voltage	V_{SADDR}	See address section	0		3.3	V
		ADDR Leakage Current	I_{SADDR}	Leakage current			1	µA
	Startup	ADDR Registration Time	t_{SADDR}	From V_{VDDB_MIN}		1		ms

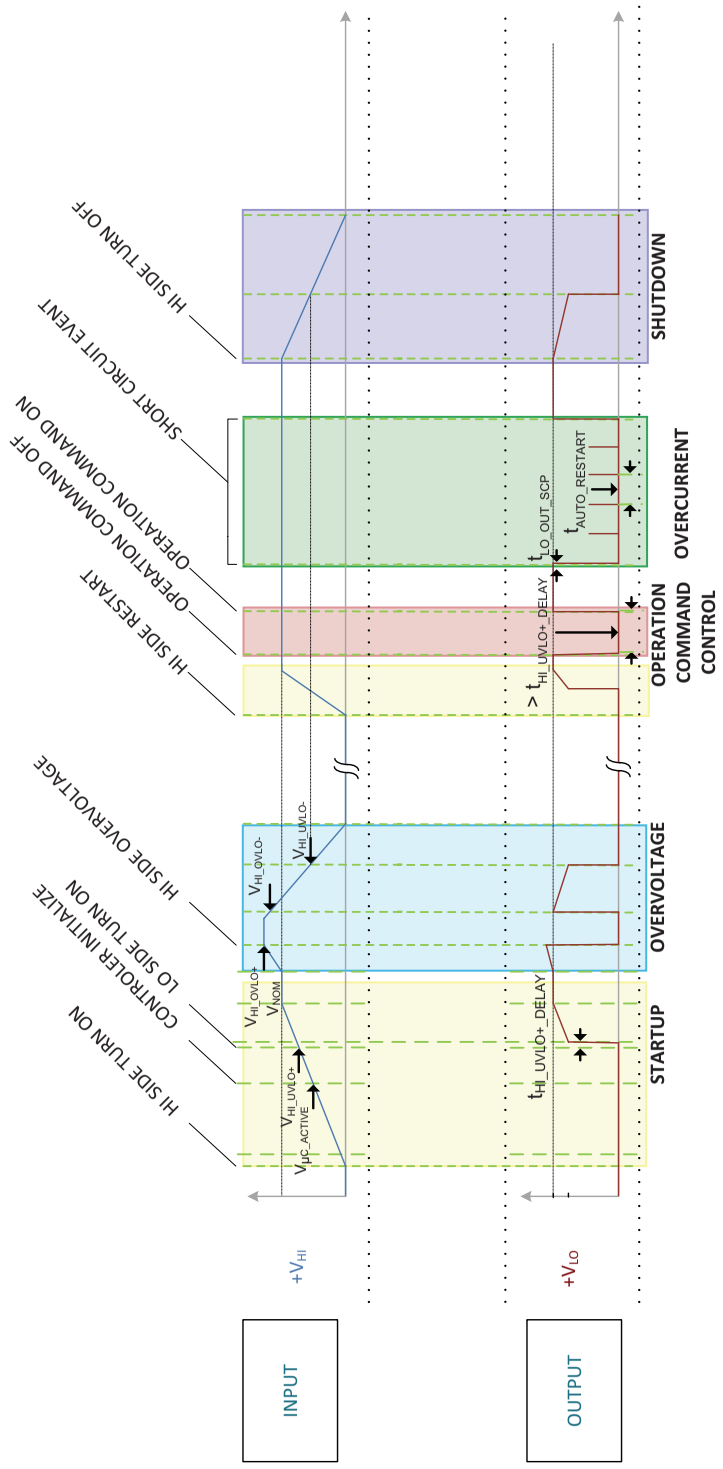
Serial Clock input (SCL) AND Serial Data (SDA) Pins

- High power SMBus specification and SMBus physical layer compatible. Note that optional SMBALERT# is not supported.
- PMBus™ command compatible.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT	Regular Operation	**Electrical Parameters**						
		Input Voltage Threshold	V_{IH}		2.1			V
			V_{IL}				0.8	V
		Output Voltage Threshold	V_{OH}		3			V
			V_{OL}				0.4	V
		Leakage Current	I_{LEAK_PIN}	Unpowered device			10	µA
		Signal Sink Current	I_{LOAD}	V_{OL} = 0.4V	4			mA
		Signal Capacitive Load	C_I	Total capacitive load of one device pin			10	pF
		Signal Noise Immunity	V_{NOISE_PP}	10MHz to 100MHz	300			mV
		Timing Parameters						
		Operating Frequency	F_{SMB}	Idle state = 0Hz	10		400	kHz
		Free Time Between Stop and Start Condition	t_{BUF}		1.3			µs
		Hold Time After Start or Repeated Start Condition	$t_{HD:STA}$	First clock is generated after this hold time	0.6			µs
		Repeat Start Condition Setup Time	$t_{SU:STA}$		0.6			µs
		Stop Condition Setup Time	$t_{SU:STO}$		0.6			µs
		Data Hold Time	$t_{HD:DAT}$		300			ns
		Data Setup Time	$t_{SU:DAT}$		100			ns
		Clock Low Time Out	$t_{TIMEOUT}$		25		35	ms
		Clock Low Period	t_{LOW}		1.3			µs
		Clock High Period	t_{HIGH}		0.6		50	µs
		Cumulative Clock Low Extend Time	$t_{LOW:SEXT}$				25	ms
		Clock or Data Fall Time	t_F		20		300	ns
		Clock or Data Rise Time	t_R		20		300	ns



Timing Diagram (Forward Direction)



Application Characteristics

Temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (high voltage side to low voltage side). See associated figures for general trend data.

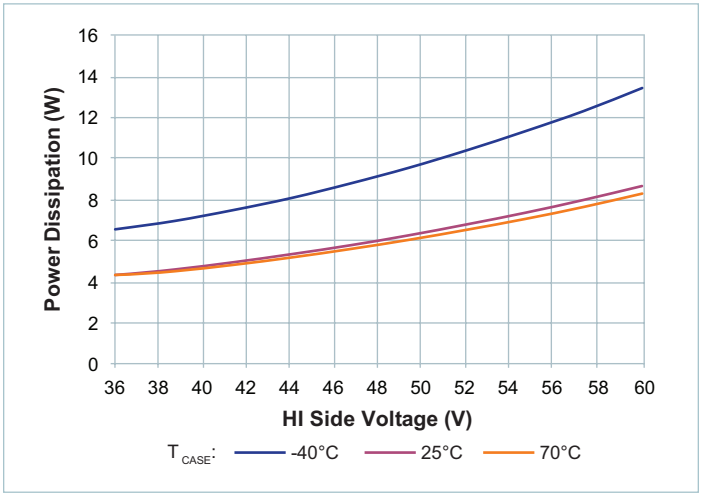


Figure 4 — *No load power dissipation vs. V_{HI_DC}*

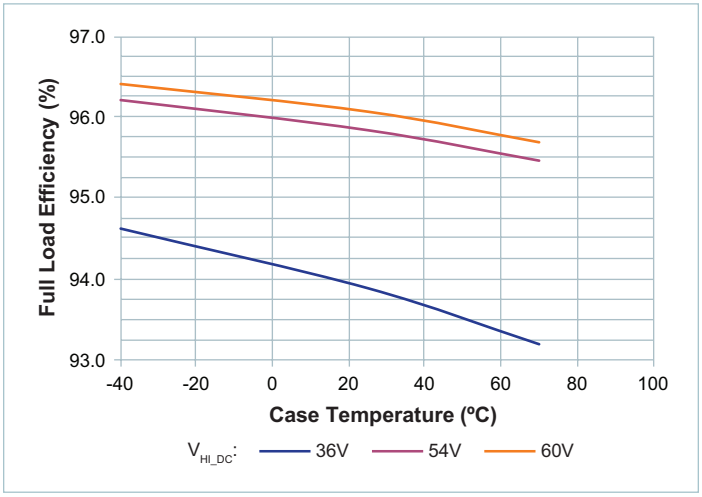


Figure 5 — *Full load efficiency vs. temperature*

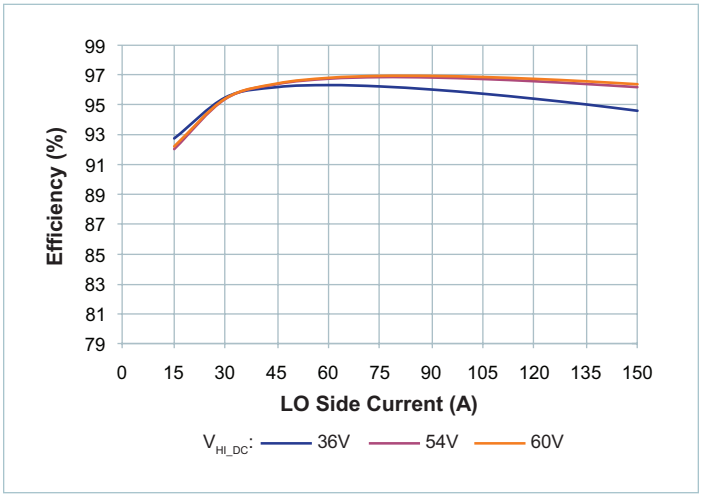


Figure 6 — *Efficiency at T_{CASE} = -40°C*

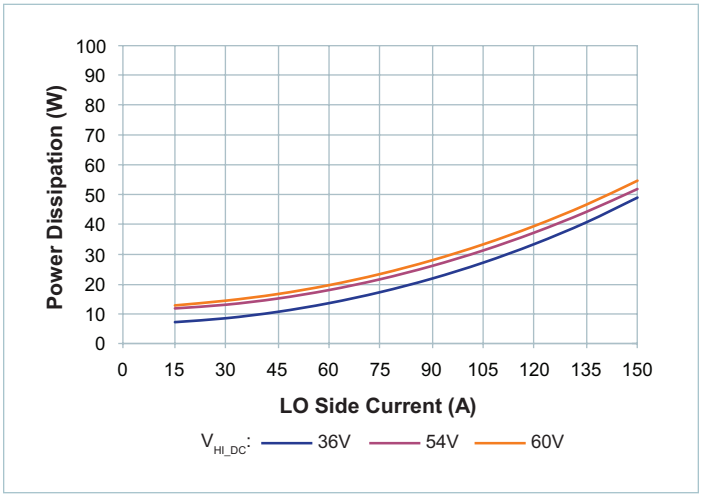


Figure 7 — *Power dissipation at T_{CASE} = -40°C*

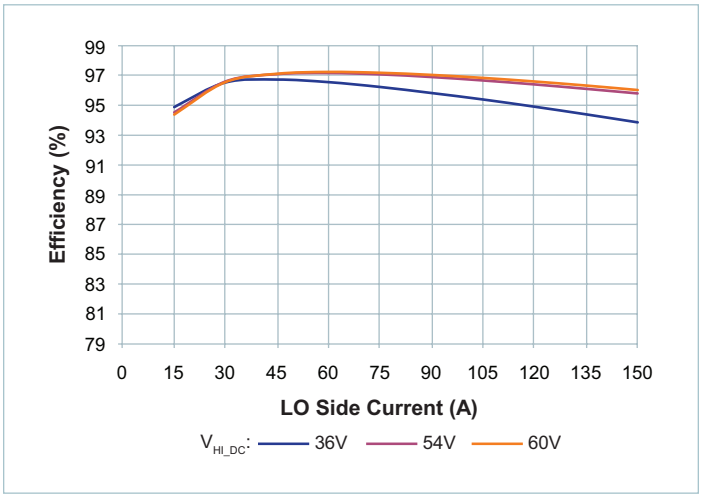


Figure 8 — *Efficiency at T_{CASE} = 25°C*

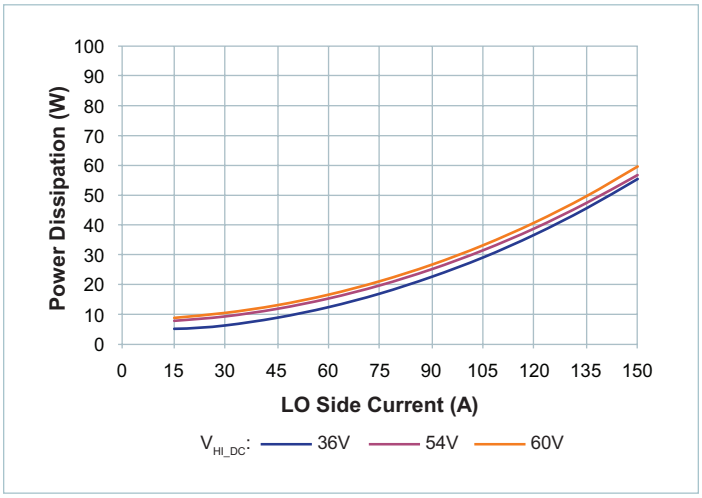


Figure 9 — *Power dissipation at T_{CASE} = 25°C*

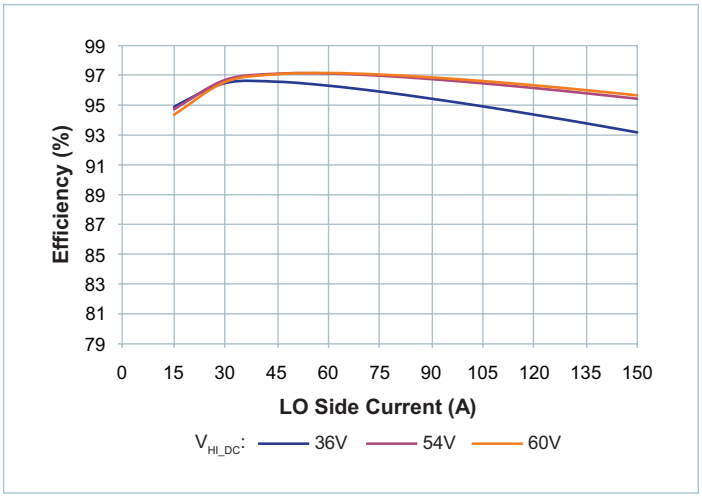


Figure 10 — *Efficiency at T_{CASE} = 0°C*

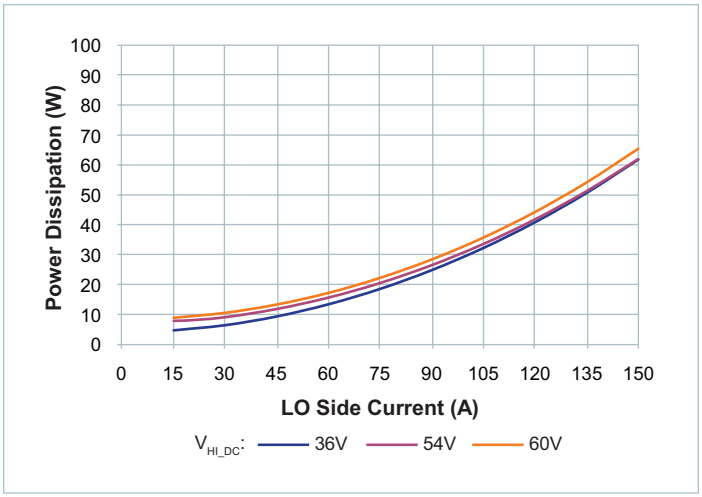


Figure 11 — *Power dissipation at T_{CASE} = 70°C*

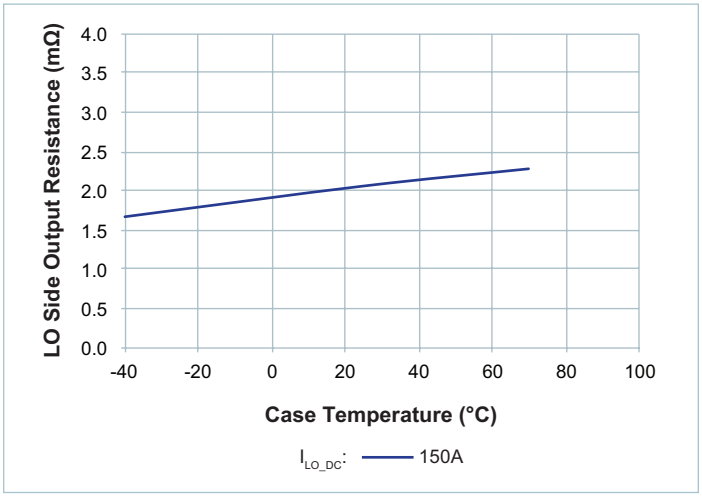


Figure 12 — *R_{LO} vs. temperature; Nominal V_{HI_DC} I_{LO_DC} = 150A at T_{CASE} = 70°C*

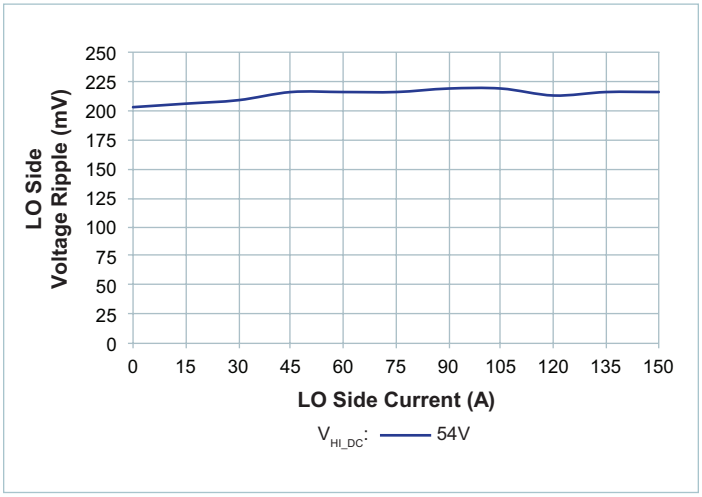


Figure 13 — *$V_{LO\_OUT\_PP}$ vs. I_{LO_DC} ; No external $C_{LO\_OUT\_EXT.}$ Board mounted module, scope setting: 20MHz analog BW*

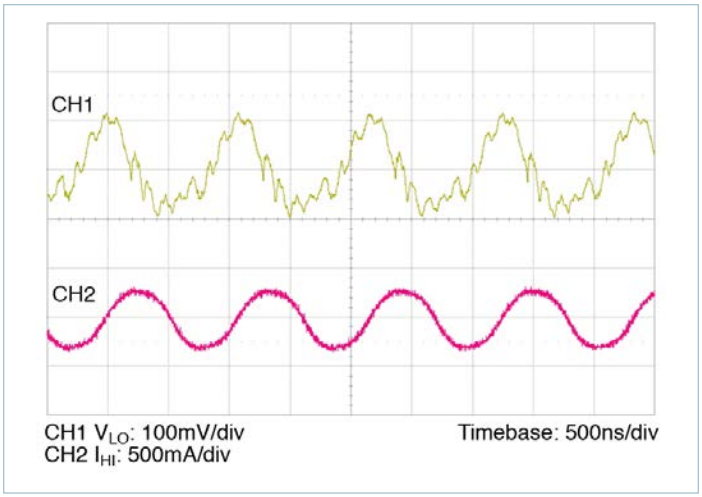


Figure 14 — *Full load LO side voltage ripple, 300µF $C_{HI\_IN\_EXT}$; no external $C_{LO\_OUT\_EXT}$. Board mounted module, scope setting: 20MHz analog BW*

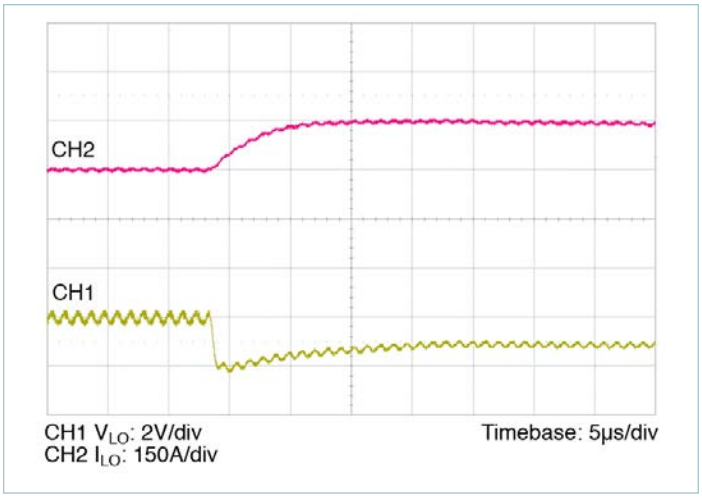


Figure 15 — *0A – 150A transient response: $C_{HI\_IN\_EXT}$ = 300µF, no external $C_{LO\_OUT\_EXT}$*

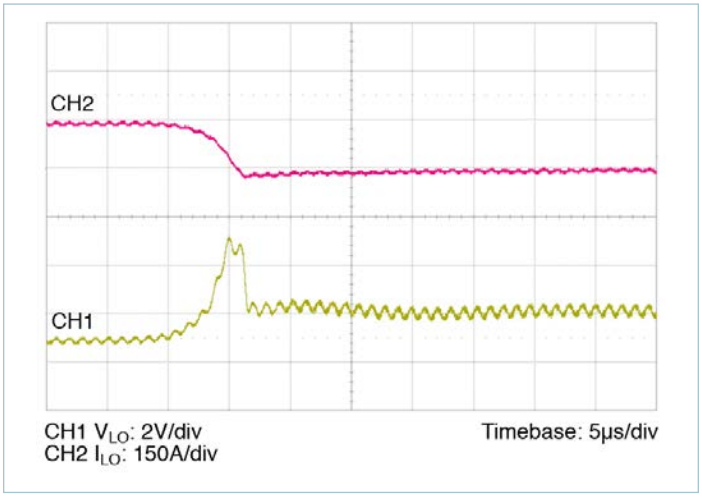


Figure 16 — *150A – 0A transient response: $C_{HI\_IN\_EXT}$ = 300µF, no external $C_{LO\_OUT\_EXT}$*

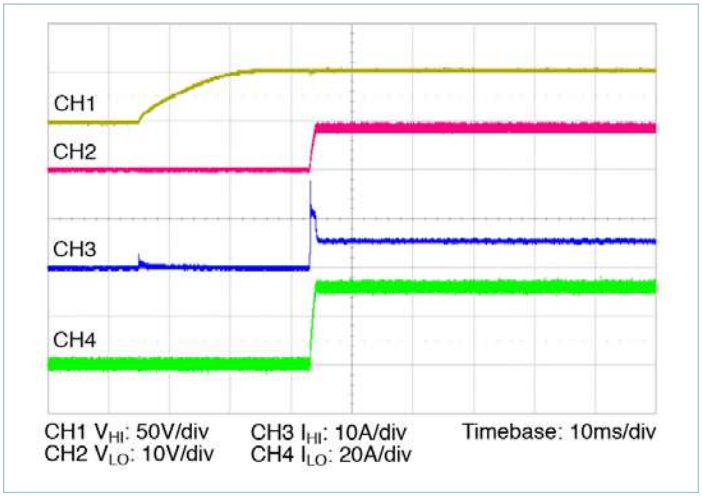


Figure 17 — *Startup from application of V_{HI_DC} = 54V, 20% I_{LO_DC} 100% $C_{LO\_OUT\_EXT}$*

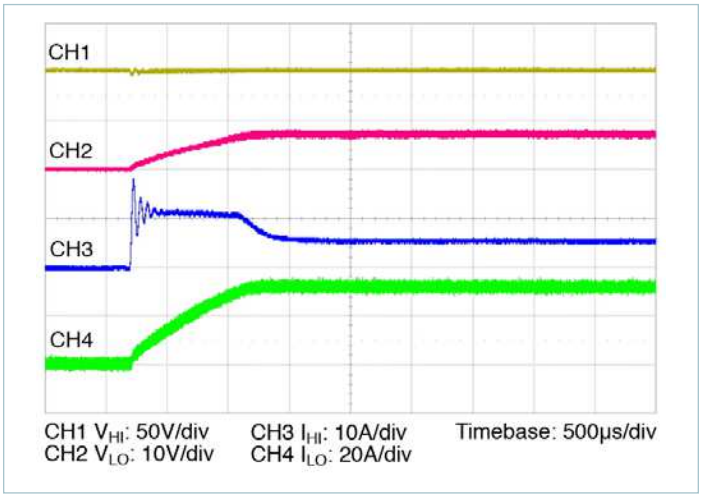


Figure 18 — *Startup from application of OPERATION COMMAND with pre-applied V_{HI_DC} = 54V, 20% I_{LO_DC}, 100% $C_{LO\_OUT\_EXT}$*

General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); All other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L	Lug (Chassis) Mount	95.34 / [3.75]	95.59 / [3.76]	95.84 / [3.77]	mm / [in]
Length	L	PCB (Board) Mount	97.55 / [3.84]	97.80 / [3.85]	98.05 / [3.86]	mm / [in]
Width	W		35.29 / [1.39]	35.54 / [1.40]	35.79 / [1.41]	mm / [in]
Height	H		9.019 / [0.355]	9.40 / [0.37]	9.781 / [0.385]	mm / [in]
Volume	Vol	Without heatsink		31.93 / [1.95]		cm^3/ [in^3]
Weight	W			130.4 / [4.6]		g / [oz]
Pin Material		C145 copper				
Underplate		Low stress ductile Nickel	50		100	µin
Pin Finish (Gold)		Palladium	0.8		6	µin
		Soft Gold	0.12		2	
Pin Finish (Tin)		Whisker resistant matte Tin	200		400	µin
Thermal						
Operating Internal Temperature	T_{INT}	BCM3814x60E10A5yzz (T-Grade)	-40		125	°C
		BCM3814x60E10A5yzz (C-Grade)	-20		125	
Operating Case Temperature	T_{CASE}	BCM3814x60E10A5yzz (T-Grade), derating applied, see safe thermal operating area	-40		100	
		BCM3814x60E10A5yzz (C-Grade), derating applied, see safe thermal operating area	-20		100	
Thermal Resistance Top Side	Φ_{INT_TOP}	Estimated thermal resistance to maximum temperature internal component from isothermal top		0.97		°C/W
Thermal Resistance Coupling Between Top Case and Bottom Case	Φ_{HOU}	Estimated thermal resistance of thermal coupling between the top and bottom case surfaces		0.58		°C/W
Thermal Resistance Bottom Side	Φ_{INT_BOT}	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		0.59		°C/W
Thermal Capacity				52		Ws/°C
Assembly						
Storage Temperature	T_{ST}	BCM3814x60E10A5yzz (T-Grade)	-40		125	°C
		BCM3814x60E10A5yzz (C-Grade)	-40		125	°C
ESD Withstand	ESD_{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2kV)	1000			
	ESD_{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V)	200			

General Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); All other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Safety						
Isolation Capacitance	C_{HI_LO}	Unpowered unit	**620**	**780**	**940**	pF
Isolation Resistance	R_{HI_LO}	At $500V_{DC}$	**10**			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		2.2		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		3.6		MHrs
Agency Approvals / Standards						
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

BCM in a VIA Package

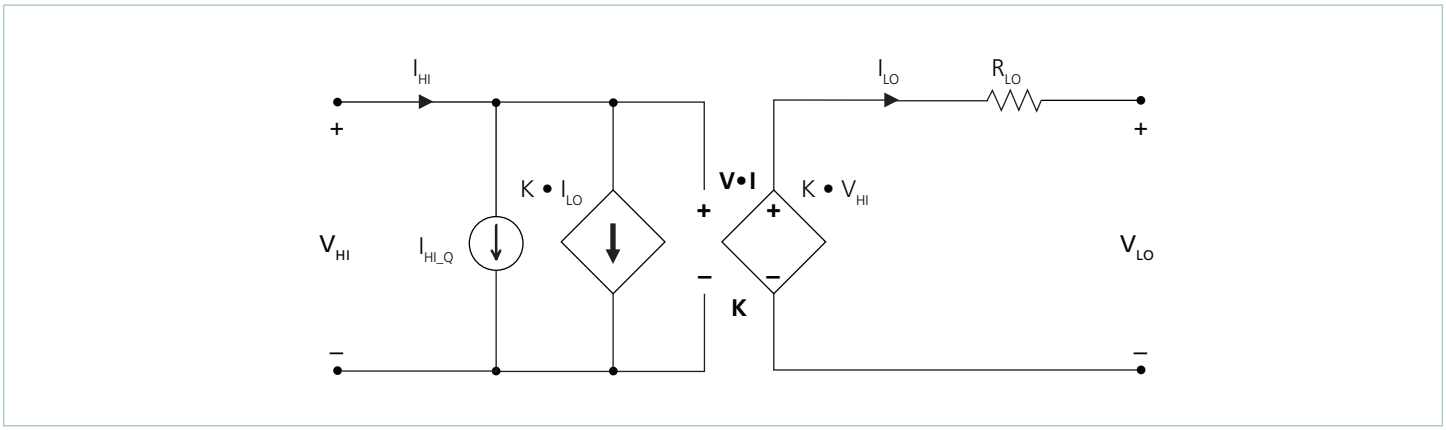


Figure 19 *— BCM DC model (Forward Direction)*

The BCM uses a high frequency resonant tank to move energy from the high voltage side to the low voltage side and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of the HI side voltage and the LO side current. A small amount of capacitance embedded in the high voltage side and low voltage side stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM3814x60E10A5yzz can be simplified into the model shown in Figure 19.

At no load:

$$V_{LO} = V_{HI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the BCM.
Rearranging Eq (1):

$$K = \frac{V_{LO}}{V_{HI}} \qquad (2)$$

In the presence of a load, V_{LO} is represented by:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R_{LO} \qquad (3)$$

and I_{LO} is represented by:

$$I_{LO} = \frac{I_{HI} - I_{HI\_Q}}{K} \qquad (4)$$

R_{LO} represents the impedance of the BCM and is a function of the R_{DS_ON} of the HI side and LO side MOSFETs, PC board resistance of HI side and LO side boards and the winding resistance of the power transformer. I_{HI_Q} represents the HI side quiescent current of the BCM controller, gate drive circuitry and core losses.

The effective DC voltage transformer action provides additional interesting attributes. Assuming that R_{LO} = 0Ω and I_{HI_Q} = 0A, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with V_{HI}.

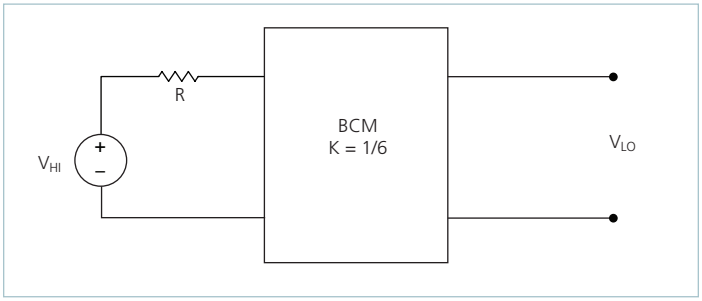


Figure 20 *— K = 1/6 BCM with series HI side resistor*

The relationship between V_{HI} and V_{LO} becomes:

$$V_{LO} = \left(V_{HI} - I_{HI} \bullet R\right) \bullet K \qquad (5)$$

Substituting the simplified version of Eq. (4) (I_{HI_Q} is assumed = 0A) into Eq. (5) yields:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Eq. (3), where R_{LO} is used to represent the characteristic impedance of the BCM. However, in this case a real resistor, R, on the high voltage side of the BCM is effectively scaled by K^2 with respect to the low voltage side.

Assuming that R = 1Ω, the effective R as seen from the low voltage side is 28mΩ, with K = 1/6.

A similar exercise can be performed with the addition of a capacitor or shunt impedance at the high voltage side of the BCM. A switch in series with V_{HI} is added to the circuit. This is depicted in Figure 21.

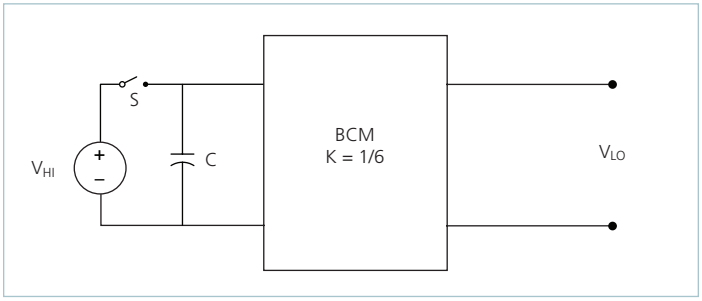


Figure 21 *— BCM with HI side capacitor*

A change in V_{HI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{HI}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{HI}, the switch is opened and the capacitor is discharged through the idealized BCM. In this case,

$$I_C = I_{LO} \bullet K \qquad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{LO}(t) = \frac{C}{K^2} \bullet \frac{dV_{LO}}{dt} \qquad (9)$$

The equation in terms of the LO side has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the low voltage side when expressed in terms of the high voltage side. With a K = 1/6 as shown in Figure 21, C = 1µF would appear as C = 36µF when viewed from the low voltage side.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a BCM between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, these benefits are not achieved if the series impedance of the BCM is too high. The impedance of the BCM must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the BCM low involves switching at a high frequency. This enables the use of small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM module are:

- No load power dissipation (P_{HI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{LO}}$): refers to the power loss across the BCM module modeled as pure resistive impedance.

Therefore,

$$P_{DISSIPATED} = P_{HI\_NL} + P_{R_{LO}} \qquad (10)$$

The above relations can be combined to calculate the overall module efficiency:

$$P_{LO\_OUT} = P_{HI\_IN} - P_{DISSIPATED} = P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}} \qquad (11)$$

$$\eta = \frac{P_{LO\_OUT}}{P_{HI\_IN}} = \frac{P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}}}{P_{HI\_IN}} \qquad (12)$$

$$= \frac{V_{HI} \bullet I_{HI} - P_{HI\_NL} - (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}$$

$$= 1 - \left(\frac{P_{HI\_NL} + (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}\right)$$

Filter Design

A major advantage of BCM systems versus conventional PWM converters is that the transformer based BCM does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of HI side voltage and LO side current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the high voltage side and low voltage side stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- ***Guarantee low source impedance:***

  To take full advantage of the BCM module's dynamic response, the impedance presented to its HI side terminals must be low from DC to approximately 5MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the HI side should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be as high as 1µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

- ***Further reduce HI side and/or LO side voltage ripple without sacrificing dynamic response:***

  Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the LO side of the module multiplied by its K factor.

- ***Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:***

  The module high side/low side voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating HI side range. Even when disabled, the powertrain is exposed to the applied voltage and the power MOSFETs must withstand it.

Total load capacitance at the LO side of the BCM module shall not exceed the specified maximum. Owing to the wide bandwidth and small LO side impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the HI side of the module. At frequencies <500kHz the module appears as an impedance of R_{LO} between the source and load.

Within this frequency range, capacitance at the HI side appears as effective capacitance on the LO side per the relationship defined in Eq. (13).

$$C_{LO\_EXT} = \frac{C_{HI\_EXT}}{K^2} \qquad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Thermal Considerations

The VIA package provides effective conduction cooling from either of the two module surfaces. Heat may be removed from the top surface, the bottom surface or both. The extent to which these two surfaces are cooled is a key component for determining the maximum power that can be processed by a VIA, as can be seen from the specified thermal operating area in Figure 1. Since the VIA has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. For this purpose, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 22 shows the "thermal circuit" for the VIA module.

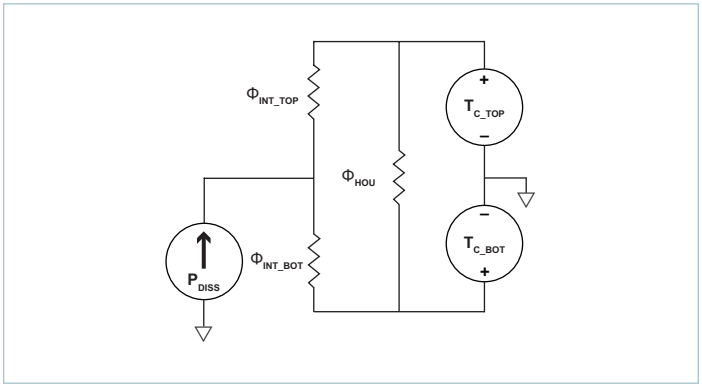


Figure 22 *— Double-sided cooling VIA thermal model*

In this case, the internal power dissipation is P_{DISS}, Φ_{INT_TOP} and Φ_{INT_BOT} are the thermal resistance characteristics of the VIA module and the top and bottom surface temperatures are represented as T_{C_TOP} and T_{C_BOT}. It is interesting to note that the package itself provides a high degree of thermal coupling between the top and bottom case surfaces (represented in the model by the resistor Φ_{HOU}). This feature enables two main options regarding thermal designs:

- Single side cooling: the model of Figure 22 can be simplified by calculating the parallel resistor network and using one simple thermal resistance number and the internal power dissipation curves; an example for bottom side cooling only is shown in Figure 23.

In this case, Φ_{INT} can be derived as follows:

$$\Phi_{INT} = \frac{(\Phi_{INT\_TOP} + \Phi_{HOU}) \bullet \Phi_{INT\_BOT}}{\Phi_{INT\_TOP} + \Phi_{HOU} + \Phi_{INT\_BOT}} \qquad (14)$$

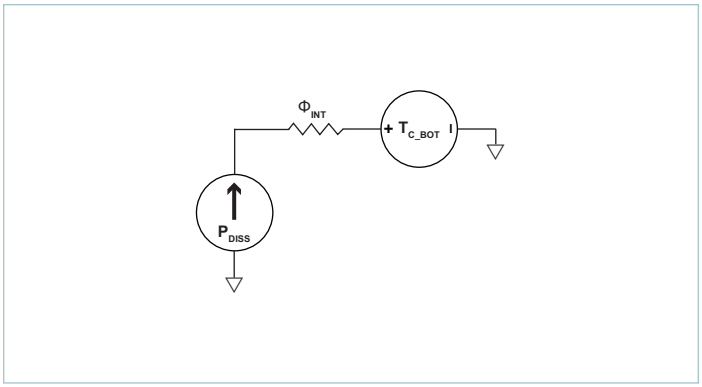


Figure 23 — *Single-sided cooling VIA thermal model*

- Double side cooling: while this option might bring limitedadvantage to the module internal components (given the surface-to-surface coupling provided), it might be appealing in cases where the external thermal system requires allocating power to two different elements, such as heatsinks with independent airflows or a combination of chassis/air cooling.

Current Sharing

The performance of the BCM is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load. Ensuring equal current sharing among modules requires that BCM array impedances be matched.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes/wires within the PCB/Chassis to deliver and return the current to the modules.
- Provide as symmetric a PCB/Wiring layout as possible among modules

For further details see AN:016 Using BCM Bus Converters in High Power Arrays.

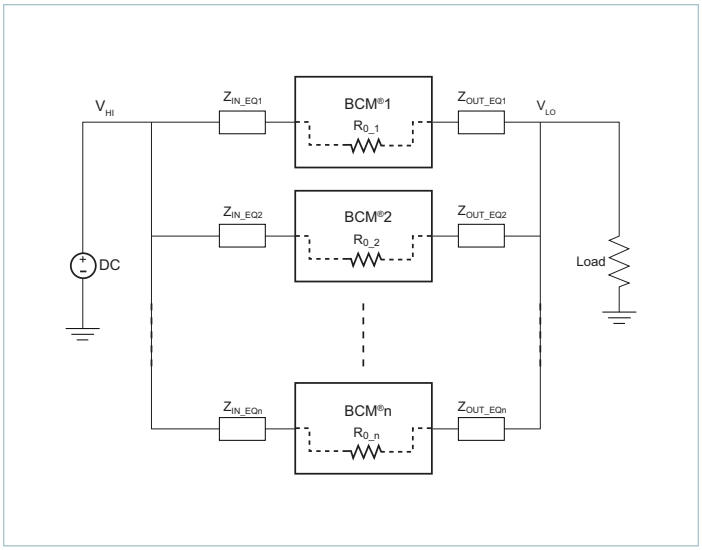


Figure 24 — *BCM module array*

Fuse Selection

In order to provide flexibility in configuring power systems, BCM in a VIA package modules are not internally fused. Input line fusing of BCM products is recommended at the system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of BCM module)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: ≤40A Littlefuse 456 Series (HI side)

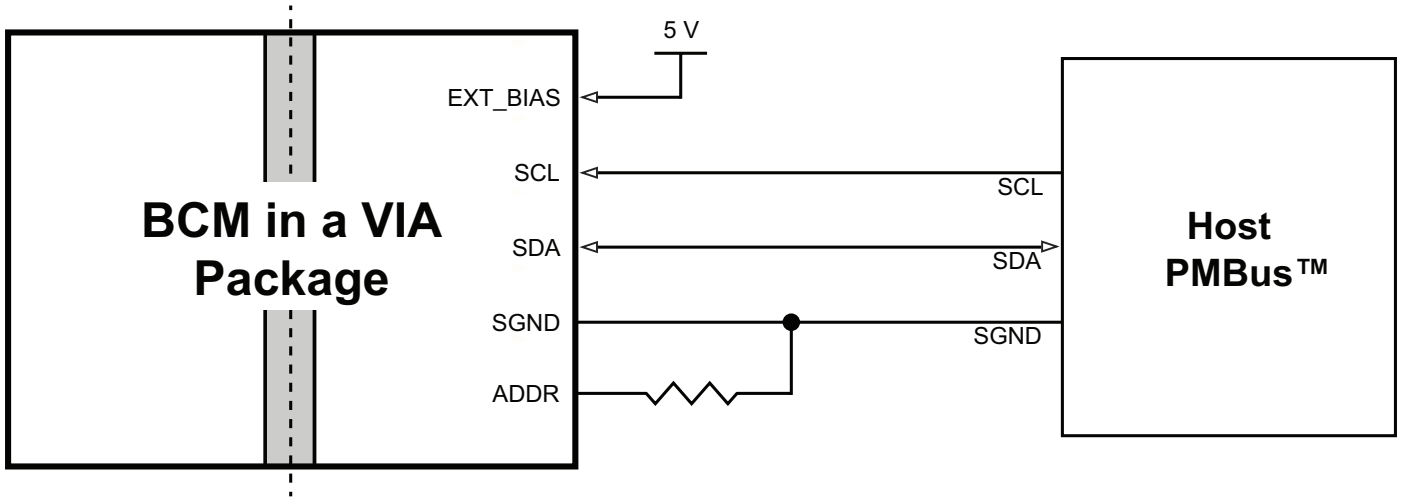
Reverse Operation

BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from the low voltage side back to the high voltage side whenever the low side voltage exceeds $V_{HI} \bullet K$. The module will continue operation in this fashion as long as no faults occur.

The BCM3814x60E10A5yzz has not been qualified for continuous operation in a reverse power condition. However, fault protections that help to protect the module in forward operation will also protect the module in reverse operation.

Transient operation in reverse is expected in cases where there is significant energy storage on the low voltage side and transient voltages appear on the high voltage side.

System Diagram for PMBus™ Interface



The controller of the BCM in a VIA package is referenced to the low voltage side signal ground (SGND).

The BCM in a VIA package provides the Host PMBus system with accurate telemetry monitoring and reporting, threshold and warning limits adjustment, in addition to corresponding status flags. The standalone BCM is periodically polled for status by the host PMBus. Direct communication to the BCM is enabled by a page command. For example, the page (0x00) prior to a telemetry inquiry points to the controller data and page (0x01) prior to a telemetry inquiry points to the BCM parameters.

The BCM enables the PMBus compatible host interface with an operating bus speed of up to 400kHz. The BCM follows the PMBus command structure and specification.

PMBus™ Interface

Refer to "PMBus Power System Management Protocol Specification Revision 1.2, Part I and II" for complete PMBus specifications details at http://pmbus.org.

Device Address

The PMBus address (ADDR Pin) should be set to one of the predetermined 16 possible addresses shown in the table below using a resistor between the ADDR pin and SGND pin.

The BCM accepts only a fixed and persistent address and does not support SMBus address resolution protocol. At initial power up, the BCM controller will sample the address pin voltage and will keep this address until device power is removed.

ID	Slave Address	HEX	Recommended Resistor R_{ADDR} (Ω)
1	1010 000b	50h	487
2	1010 001b	51h	1050
3	1010 010b	52h	1870
4	1010 011b	53h	2800
5	1010 100b	54h	3920
6	1010 101b	55h	5230
7	1010 110b	56h	6810
8	1010 111b	57h	8870
9	1011 000b	58h	11300
10	1011 001b	59h	14700
11	1011 010b	5Ah	19100
12	1011 011b	5Bh	25500
13	1011 100b	5Ch	35700
14	1011 101b	5Dh	53600
15	1011 110b	5Eh	97600
16	1011 111b	5Fh	316000

Reported DATA Formats

The BCM controller employs a direct data format where all reported measurements are in Volts, Amperes, Degrees Celsius, or Seconds. The host uses the following PMBus specification to interpret received values metric prefixes. Note that the COEFFICIENTS command is not supported:

$$X = \left(\frac{1}{m}\right) \bullet (Y \bullet 10^{-R} - b)$$

Where:

X, is a "real world" value in units (A, V, °C, s)

Y, is a two's complement integer received from the BCM controller

m, b and R are two's complement integers defined as follows:

Command	Code	m	R	b
TON_DELAY	60h	1	3	0
READ_VIN	88h	1	1	0
READ_IIN	89h	1	3	0
READ_VOUT [1]	8Bh	1	1	0
READ_IOUT	8Ch	1	2	0
READ_TEMPERATURE_1 [2]	8Dh	1	0	0
READ_POUT	96h	1	0	0
MFR_VIN_MIN	A0h	1	0	0
MFR_VIN_MAX	A1h	1	0	0
MFR_VOUT_MIN	A4h	1	0	0
MFR_VOUT_MAX	A5h	1	0	0
MFR_IOUT_MAX	A6h	1	0	0
MFR_POUT_MAX	A7h	1	0	0
READ_K_FACTOR	D1h	65536	0	0
READ_BCM_ROUT	D4h	1	5	0

[1] Default READ LO side voltage returned when BCM unit is disabled = –300V.
[2] Default READ Temperature returned when BCM unit is disabled = –273°C.

No special formatting is required when lowering the supervisory limits and warnings.

Supported Command List

Command	Code	Function	Default Data Content	Data Bytes
PAGE	00h	Access BCM stored information	00h	1
OPERATION	01h	Turn BCM on or off	80h	1
CLEAR_FAULTS	03h	Clear all faults	N/A	None
CAPABILITY	19h	Controller PMBus™ key capabilities set by factory	20h	1
OT_FAULT_LIMIT	4Fh [1]	Overtemperature protection	64h	2
OT_WARN_LIMIT	51h [1]	Overtemperature warning	64h	2
VIN_OV_FAULT_LIMIT	55h [1]	High voltage side overvoltage protection	64h	2
VIN_OV_WARN_LIMIT	57h [1]	High voltage side overvoltage warning	64h	2
IIN_OC_FAULT_LIMIT	5Bh [1]	High voltage side overcurrent protection	64h	2
IIN_OC_WARN_LIMIT	5Dh [1]	High voltage side overcurrent warning	64h	2
TON_DELAY	60h [1]	Startup delay in addition to fixed delay	00h	2
STATUS_BYTE	78h	Summary of faults	00h	1
STATUS_WORD	79h	Summary of fault conditions	00h	2
STATUS_IOUT	7Bh	Overcurrent fault status	00h	1
STATUS_INPUT	7Ch	Overvoltage and undervoltage fault status	00h	1
STATUS_TEMPERATURE	7Dh	Overtemperature and undertemperature fault status	00h	1
STATUS_CML	7Eh	PMBus communication fault	00h	1
STATUS_MFR_SPECIFIC	80h	Other BCM status indicator	00h	1
READ_VIN	88h	Reads HI side voltage	FFFFh	2
READ_IIN	89h	Reads HI side current	FFFFh	2
READ_VOUT	8Bh	Reads LO side voltage	FFFFh	2
READ_IOUT	8Ch	Reads LO side current	FFFFh	2
READ_TEMPERATURE_1	8Dh	Reads internal temperature	FFFFh	2
READ_POUT	96h	Reads LO side power	FFFFh	2
PMBUS_REVISION	98h	PMBus compatible revision	22h	1
MFR_ID	99h	BCM controller ID	"VI"	2
MFR_MODEL	9Ah	Internal controller or BCM model	Part Number	18
MFR_REVISION	9Bh	Internal controller or BCM revision	FW and HW revision	18
MFR_LOCATION	9Ch	Internal controller or BCM factory location	"AP"	2
MFR_DATE	9Dh	Internal controller or BCM manufacturing date	"YYWW"	4
MFR_SERIAL	9Eh	Internal controller or BCM serial number	Serial Number	16
MFR_VIN_MIN	A0h	Minimum rated high side voltage	Varies per BCM	2
MFR_VIN_MAX	A1h	Maximum rated high side voltage	Varies per BCM	2
MFR_VOUT_MIN	A4h	Minimum rated low side voltage	Varies per BCM	2
MFR_VOUT_MAX	A5h	Maximum rated low side voltage	Varies per BCM	2
MFR_IOUT_MAX	A6h	Maximum rated low side current	Varies per BCM	2
MFR_POUT_MAX	A7h	Maximum rated low side power	Varies per BCM	2
READ_K_FACTOR	D1h	Reads K factor	Varies per BCM	2
READ_BCM_ROUT	D4h	Reads low voltage side output resistance	Varies per BCM	2
SET_ALL_THRESHOLDS	D5h [1]	Set supervisory warning and protection thresholds	646464646464h	6
DISABLE_FAULT	D7h [1]	Disable overvoltage, overcurrent or undervoltage supervisory faults	00h	2

[1] The BCM must be in a disabled state with $V_{HI} < V_{HI\_UVLO-}$ and VDDB applied during a write message.