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BCM® in a VIA Package Bus Converter

BCM4414xD1E5135yzz

Isolated Fixed-Ratio DC-DC Converter

Features & Benefits

- Up to 35A continuous low voltage side current
- Fixed transformation ratio (K) of 1/8
- Up to 797W/in^3 power density
- 97.7% peak efficiency
- Built-in EMI filtering and inrush limiting circuit
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 4414 package
- High MTBF
- Thermally enhanced VIA package
- PMBus™ management interface
- Suitable for Hot-Swap applications

Typical Applications

- 380V_{DC} Power Distribution
- Information and Communication Technology (ICT) Equipment
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Energy Systems
- Transportation
- Green Buildings and Microgrids

Product Ratings	
V_{HI} = 400V (260 – 410V)	I_{LO} = up to 35A
V_{LO} = 50V (32.5 – 51.3V) (NO LOAD)	K = 1/8

Product Description

The BCM4414xD1E5135yzz in a VIA package is a high efficiency Bus Converter, operating from a 260 to 410V_{DC} high voltage bus to deliver an isolated 32.5 to 51.3V_{DC} unregulated, low voltage.

This unique ultra-low profile module incorporates DC-DC conversion, integrated filtering and PMBus™ [1] commands and controls in a chassis or PCB mount form factor.

The BCM offers low noise, fast transient response and industry leading efficiency and power density. A low voltage side referenced PMBus™ compatible telemetry and control interface provides access to the BCM's configuration, fault monitoring and other telemetry functions.

Leveraging the thermal and density benefits of Vicor's VIA packaging technology, the BCM module offers flexible thermal management options with very low top and bottom side thermal impedances.

When combined with downstream Vicor DC-DC conversion components and regulators, the BCM allows the Power Design Engineer to employ a simple, low-profile design, which will differentiate the end system without compromising on cost or performance metrics.

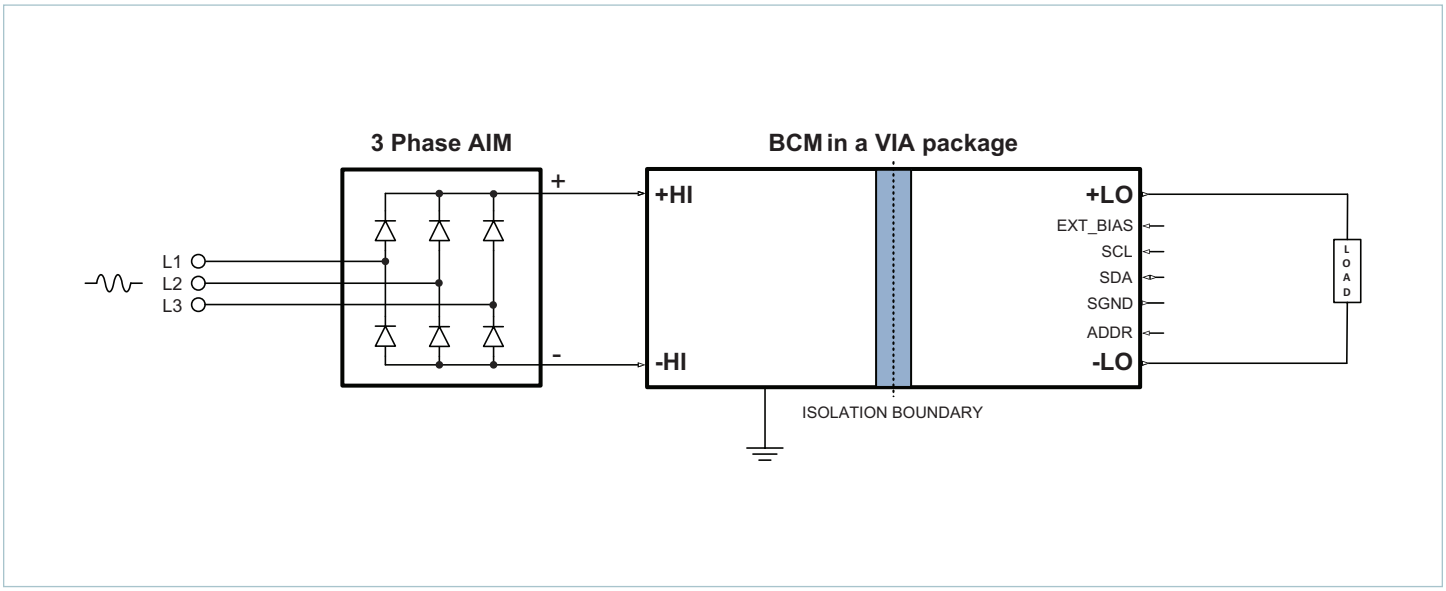
Size:
4.35 x 1.40 x 0.37 in
110.55 x 35.54 x 9.40mm

Part Ordering Information

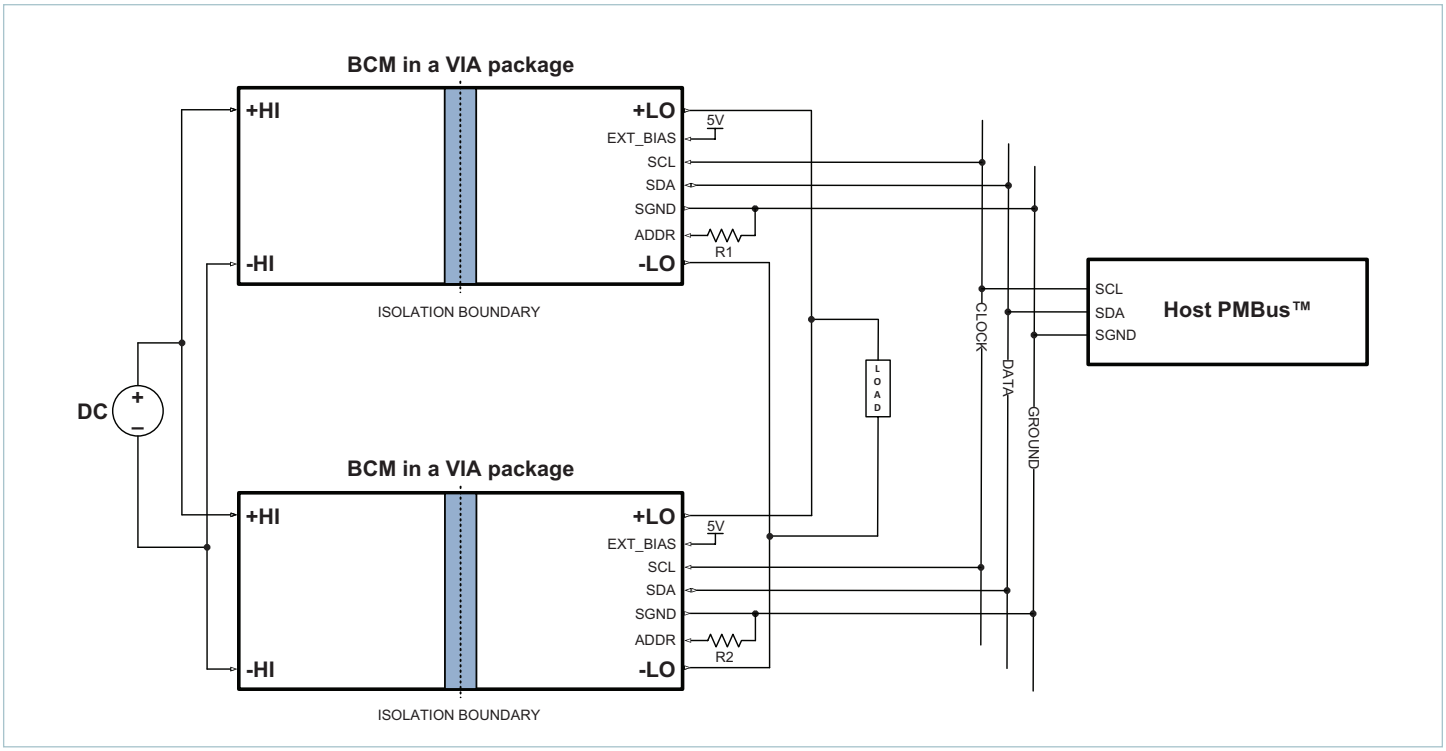
Product Function	Package Length	Package Width	Package Type	Max High Side Voltage	High Side Voltage Range Ratio	Max Low Side Voltage	Max Low Side Current	Product Grade (Case Temperature)	Option Field
BCM	44	14	x	D1	E	51	35	y	zz
BCM = Bus Converter Module	Length in Inches x 10	Width in Inches x 10	B = Board VIA V = Chassis VIA	Internal Reference				C = -20 to 100°C [2] T = -40 to 100°C [2]	02 = Chassis/PMBus 06 = Short Pin/PMBus 10 = Long Pin/PMBus

[1] The PMBus name, SMIF, Inc. and logo are trademarks of SMIF, Inc.
[2] High temperature current derating may apply; See Figure 1, specified thermal operating area.

Typical Applications

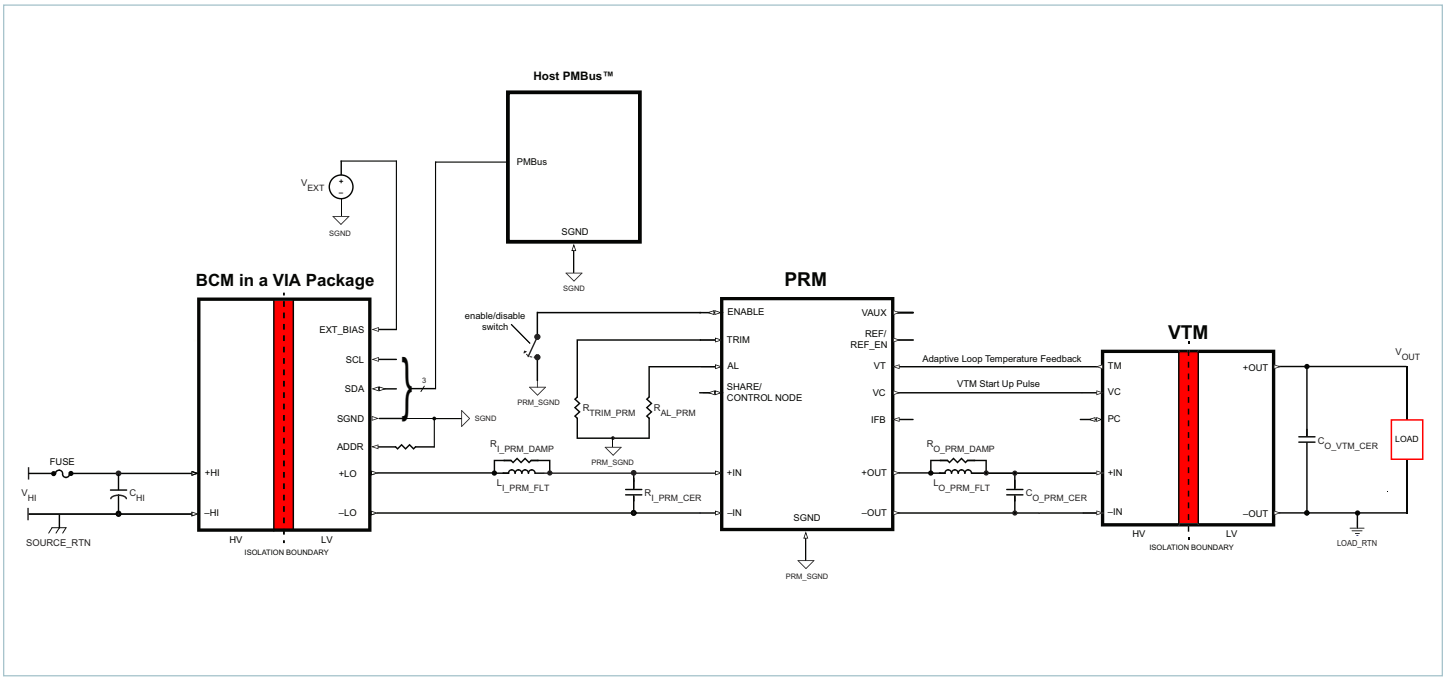


3 phase AC to point of load (3 phase AIM + BCM4414xD1E5135yzz)

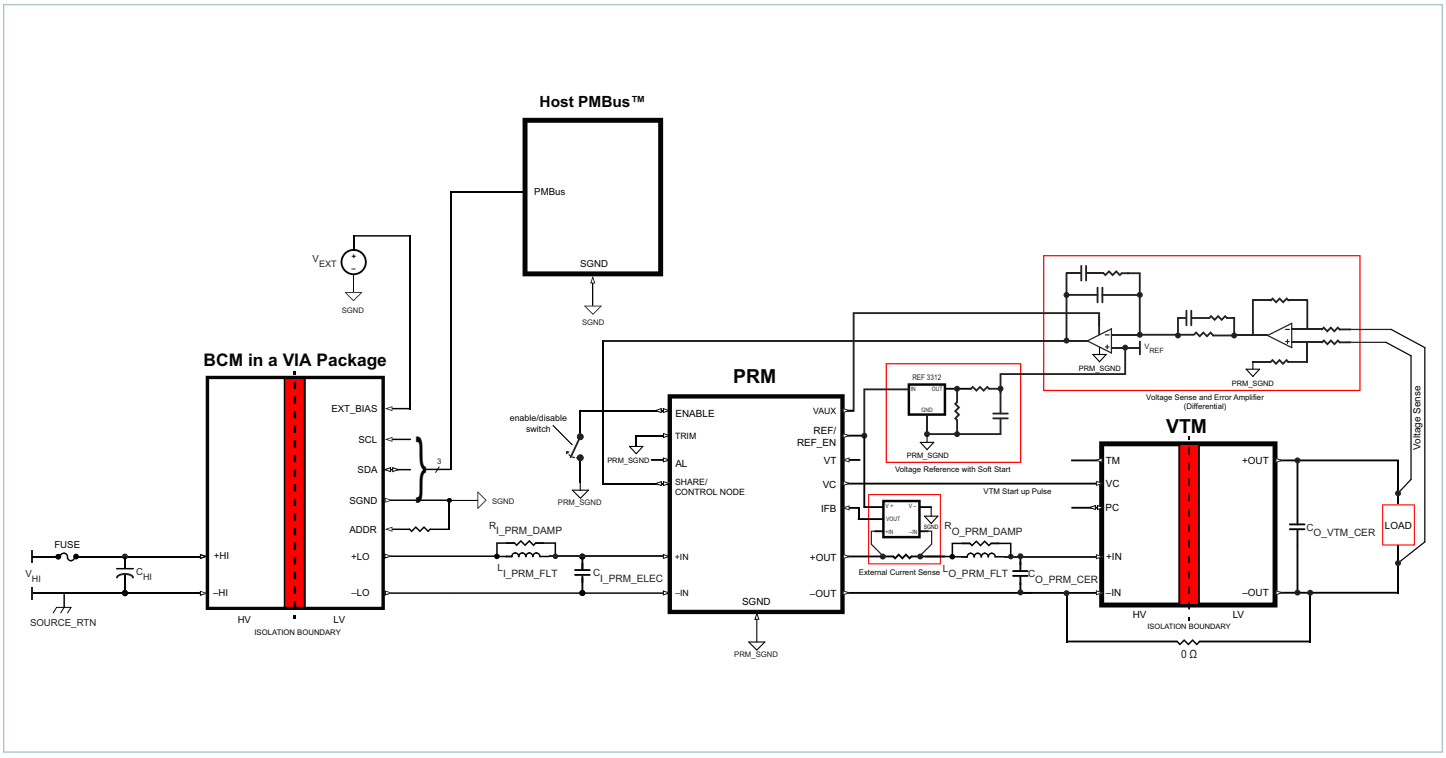


Paralleling PMBus BCM in a VIA package – connection to Host PMBus

Typical Applications (Cont.)

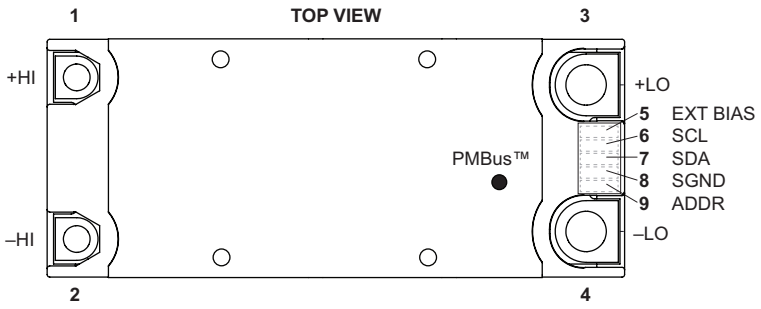


BCM4414xD1E5135yzz + PRM + VTM, Adaptive Loop Configuration – connection to Host PMBus

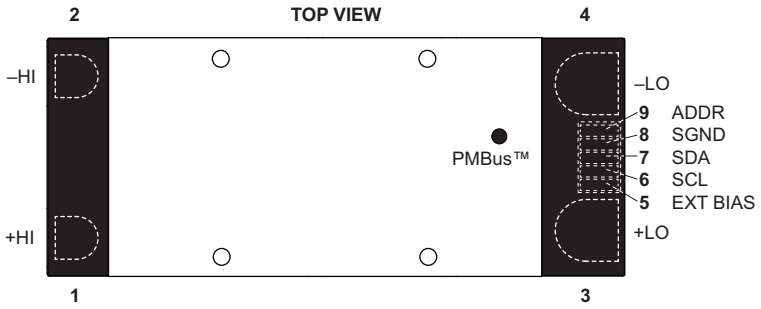


BCM4414xD1E5135yzz + PRM + VTM, Remote Sense Configuration – connection to Host PMBus

Pin Configuration



BCM in a 4414 VIA Package - Chassis (Lug) Mount



BCM in a 4414 VIA Package - Board (PCB) Mount

Note: The dot on the VIA housing indicates the location of the signal pin 9.

Pin Descriptions

Pin Number	Signal Name	Type	Function
1	+HI	HIGH SIDE POWER	High voltage side positive power terminal
2	–HI	HIGH SIDE POWER RETURN	High voltage side negative power terminal
3	+LO	LOW SIDE POWER	Low voltage side positive power terminal
4	–LO	LOW SIDE POWER RETURN	Low voltage side negative power terminal
5	EXT BIAS	INPUT	5V supply input
6	SCL	INPUT	I²C™ [1] Clock, PMBus™ Compatible
7	SDA	INPUT/OUTPUT	I²C Data, PMBus™ Compatible
8	SGND	LOW SIDE SIGNAL RETURN	Signal Ground
9	ADDR	INPUT	Address assignment - Resistor based

Notes: All signal pins (5, 6, 7, 8, 9) are referenced to the low voltage side and isolated from the high voltage side.
Keep SGND signal separated from the low voltage side power return terminal (–LO) in electrical design.

[1] I²C™ is a trademark of NXP Semiconductor

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+HI to –HI		-1	480	V
HI_DC or LO_DC Slew Rate	Internal hot-swap circuitry		N/A	V/µs
+LO to –LO		-1	60	V
EXT BIAS to SGND		-0.3	10	V
			0.15	A
SCL to SGND		-0.3	5.5	V
SDA to SGND		-0.3	5.5	V
ADDR to SGND		-0.3	3.6	V
Isolation Voltage / Dielectric Withstand	Basic insulation (high voltage side to case)	2121		V_{DC}
	Basic insulation (high voltage side to low voltage side) [1]	2121		V_{DC}
	Functional insulation (low voltage side to case)	707		V_{DC}

[1] The absolute maximum rating listed above for dielectric withstand (high voltage side to low voltage side) refers to the VIA package. The internal safety approved isolating component (ChiP) provides reinforced insulation (4242V) from high voltage side to low voltage side. However, the VIA package itself can only be tested at a basic insulation value (2121V).

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side)						
HI Side Voltage Range (Continuous)	V_{HI_DC}		**260**		**410**	V
HI Side Voltage Range (Transient)	V_{HI_TRANS}		**260**		**410**	V
HI Side Voltage Initialization Threshold	$V_{\mu C\_ACTIVE}$	HI side voltage where internal controller is initialized, (powertrain inactive)			120	V
HI Side Quiescent Current	I_{HI_Q}	Disabled, V_{HI_DC} = 400V		2		mA
		T_{CASE} ≤ 100°C			4	
No Load Power Dissipation	P_{HI_NL}	V_{HI_DC} = 400V, T_{CASE} = 25°C		10.5	17	W
		V_{HI_DC} = 400V	**6**		**21**	
		V_{HI_DC} = 260V to 410V, T_{CASE} = 25 °C			18	
		V_{HI_DC} = 260V to 410V			**22**	
HI Side Inrush Current Peak	$I_{HI\_INR\_PK}$	V_{HI_DC} = 410V, C_{LO_EXT} = 100µF, R_{LOAD_LO} = 25% of full load current		6		A
		T_{CASE} ≤ 100°C			12	
DC HI Side Current	$I_{HI\_IN\_DC}$	At $I_{LO\_OUT\_DC}$ = 35A, T_{CASE} ≤ 70°C			4.5	A
Transformation Ratio	K	High voltage to low voltage K = V_{LO_DC} / V_{HI_DC}, at no load		1/8		V/V
LO Side Current (Continuous)	$I_{LO\_OUT\_DC}$	T_{CASE} ≤ 70°C			35	A
LO Side Current (Pulsed)	$I_{LO\_OUT\_PULSE}$	2ms pulse, 25% duty cycle, $I_{LO\_OUT\_AVG}$ ≤ 50% rated $I_{LO\_OUT\_DC}$			40	A
Efficiency (Ambient)	η_{AMB}	V_{HI_DC} = 400V, $I_{LO\_OUT\_DC}$ = 35A	96.5	97.2		%
		V_{HI_DC} = 260V to 410V, $I_{LO\_OUT\_DC}$ = 35A	95.3			
		V_{HI_DC} = 400V, $I_{LO\_OUT\_DC}$ = 17.5A	96.8	97.6		
Efficiency (Hot)	η_{HOT}	V_{HI_DC} = 400V, $I_{LO\_OUT\_DC}$ = 35A, T_{CASE} = 70°C	95.7	96.5		%
Efficiency (Over Load Range)	$\eta_{20\%}$	7A < $I_{LO\_OUT\_DC}$ < 35A	94.5			%
LO Side Output Resistance	R_{LO_COLD}	V_{HI_DC} = 400V, $I_{LO\_OUT\_DC}$ = 35A, T_{CASE} = -40°C	18	22	25	mΩ
	R_{LO_AMB}	V_{HI_DC} = 400V, $I_{LO\_OUT\_DC}$ = 35A	27	29.5	33	
	R_{LO_HOT}	V_{HI_DC} = 400V, $I_{LO\_OUT\_DC}$ = 35A, T_{CASE} = 70°C	32	34.8	37	
Switching Frequency	F_{SW}	Low side voltage ripple frequency = 2x F_{SW}	**1.05**	1.10	**1.14**	MHz
LO Side Voltage Ripple	$V_{LO\_OUT\_PP}$	C_{LO_EXT} = 0µF, $I_{LO\_OUT\_DC}$ = 35A, V_{HI_DC} = 400V, 20MHz BW		250		mV
		T_{CASE} ≤ 100°C			550	

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side), Cont.						
Effective HI Side Capacitance (Internal)	C_{HI_INT}	Effective value at 400V_{HI_DC}		0.4		µF
Effective LO Side Capacitance (Internal)	C_{LO_INT}	Effective value at 50V_{LO_DC}		37.6		µF
Rated LO Side Capacitance (External)	$C_{LO\_OUT\_EXT}$	Excessive capacitance may drive module into short circuit protection			**100**	µF
Rated LO Side Capacitance (External), Parallel Array Operation	$C_{LO\_OUT\_AEXT}$	$C_{LO\_OUT\_AEXT}$ Max = N * 0.5 * $C_{LO\_OUT\_EXT\ MAX}$, where N = the number of units in parallel				
Powertrain Hardware Protection Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side)						
• These built-in powertrain protections are fixed in hardware and cannot be configured through PMBus™. • When duplicated in supervisory limits, hardware protections serve a secondary role and become active when supervisory limits are disabled through PMBus.						
Auto Restart Time	$t_{AUTO\_RESTART}$	Startup into a persistent fault condition. Non-latching fault detection given V_{HI_DC} > V_{HI_UVLO+}	**290**		**360**	ms
HI Side Overvoltage Lockout Threshold	V_{HI_OVLO+}		**430**	440	**450**	V
HI Side Overvoltage Recovery Threshold	V_{HI_OVLO-}		**420**	430	**440**	V
HI Side Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			10		V
HI Side Overvoltage Lockout Response Time	t_{HI_OVLO}			10		µs
HI Side Soft-Start Time	$t_{HI\_SOFT-START}$	From powertrain active. Fast current limit protection disabled during soft-start		1		ms
LO Side Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		**37.5**	47	**59**	A
LO Side Overcurrent Response Time Constant	$t_{LO\_OUT\_OCP}$	Effective internal RC filter		3.6		ms
LO Side Short Circuit Protection Trip Threshold	$I_{LO\_OUT\_SCP}$		**52**			A
LO Side Short Circuit Protection Response Time	$t_{LO\_OUT\_SCP}$			1		µs
Overtemperature Shutdown Threshold	t_{OTP+}	Internal	**125**			°C

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Supervisory Limits Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side)						
• These supervisory limits are set in the internal controller and can be reconfigured or disabled through PMBus™. • When disabled, the powertrain protections presented in the previous table will intervene during fault events.						
HI Side Overvoltage Lockout Threshold	V_{HI_OVLO+}		**420**	436	**450**	V
HI Side Overvoltage Recovery Threshold	V_{HI_OVLO-}		**405**	426	**440**	V
HI Side Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			10		V
HI Side Overvoltage Lockout Response Time	t_{HI_OVLO}			100		µs
HI Side Undervoltage Lockout Threshold	V_{HI_UVLO-}		**200**	226	**250**	V
HI Side Undervoltage Recovery Threshold	V_{HI_UVLO+}		**225**	244	**259**	V
HI Side Undervoltage Lockout Hysteresis	$V_{HI\_UVLO\_HYST}$			15		V
HI Side Undervoltage Lockout Response Time	t_{HI_UVLO}			100		µs
HI Side Undervoltage Startup Delay	$t_{HI\_UVLO+\_DELAY}$	From V_{HI_DC} = V_{HI_UVLO+} to powertrain active (i.e., one time startup delay from application of V_{HI_DC} to V_{LO_DC})		20		ms
LO Side Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		**42.5**	45	**47.5**	A
LO Side Overcurrent Response Time Constant	$t_{LO\_OUT\_OCP}$	Effective internal RC filter		2		ms
Overtemperature Shutdown Threshold	t_{OTP+}	Internal	**125**			°C
Overtemperature Recovery Threshold	t_{OTP-}	Internal	105	110	115	°C
Undertemperature Shutdown Threshold (Internal)	t_{UTP}	C-Grade			-25	°C
		T-Grade			-45	
Undertemperature Restart Time	$t_{UTP\_RESTART}$	Startup into a persistent fault condition. Non-latching fault detection given V_{HI_DC} > V_{HI_UVLO+}		3		s

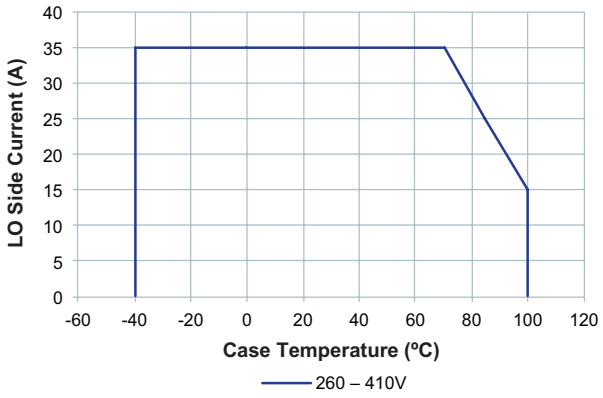


Figure 1 *— Specified thermal operating area*

1. The BCM in a VIA package is cooled through the bottom case (bottom housing).
2. The thermal rating is based on typical measured device efficiency.
3. The case temperature in the graph is the measured temperature of the bottom housing, such that the internal operating temperature does not exceed 125°C.

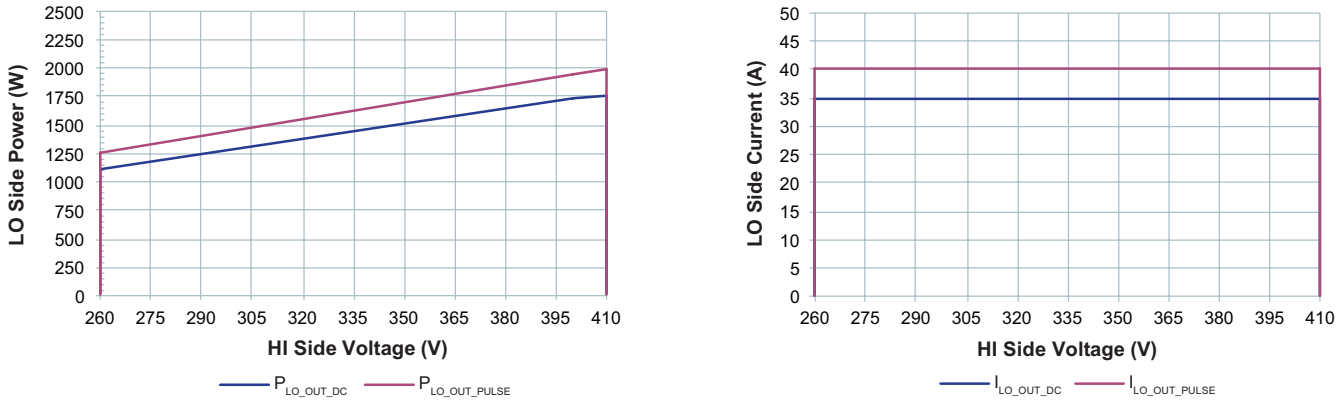


Figure 2 *— Specified electrical operating area using rated R_{LO_HOT}*

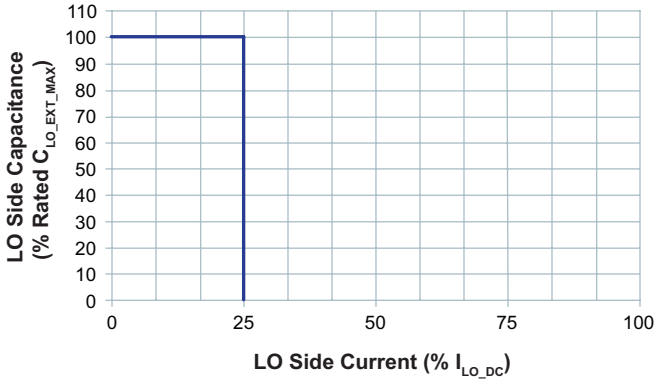


Figure 3 *— Specified HI side startup into load current and external capacitance*

PMBus™ Reported Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Monitored Telemetry					
ATTRIBUTE	**PMBus™ READ COMMAND**	**ACCURACY (RATED RANGE)**	**FUNCTIONAL REPORTING RANGE**	**UPDATE RATE**	**REPORTED UNITS**
HI Side Voltage	(88h) READ_VIN	± 5%(LL - HL)	130V to 450V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
HI Side Current	(89h) READ_IIN	± 20% (10 - 20% of FL) ± 5% (20 - 133% of FL)	-0.85A to 5.9A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-3}$
LO Side Voltage [1]	(8Bh) READ_VOUT	± 5% (LL - HL)	16.25V to 56.25V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
LO Side Current	(8Ch) READ_IOUT	± 20% (10 - 20% of FL) ± 5% (20 - 133% of FL)	-7A to 47.5A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
LO Side Resistance	(D4h) READ_ROUT	± 5% (50 - 100% of FL) at NL ± 10% (50 - 100% of FL) (LL - HL)	10mΩ to 40mΩ	100ms	$R_{ACTUAL} = R_{REPORTED} \times 10^{-5}$
Temperature [2]	(8Dh) READ_TEMPERATURE_1	± 7°C (Full Range)	- 55°C to 130°C	100ms	$T_{ACTUAL} = T_{REPORTED}$

[1] Default READ LO Side Voltage returned when unit is disabled = -300V.
[2] Default READ Temperature returned when unit is disabled = -273°C.

Variable Parameters					
• Factory setting of all Thresholds and Warning limits listed below are 100% of specified protection values. • Variables can be written only when module is disabled with $V_{HI} < V_{HI\_UVLO-}$ and external bias (VDDB) applied. • Module must remain in a disabled mode for 3ms after any changes to the variables below to allow sufficient time to commit changes to EEPROM.					
ATTRIBUTE	**PMBus™ COMMAND**	**CONDITIONS / NOTES**	**ACCURACY (RATED RANGE)**	**FUNCTIONAL REPORTING RANGE**	**DEFAULT VALUE**
HI Side Overvoltage Protection Limit	(55h) VIN_OV_FAULT_LIMIT	V_{HI_OVLO-} is automatically 3% lower than this setpoint	± 5% (LL - HL)	130V to 435V	100%
HI Side Overvoltage Warning Limit	(57h) VIN_OV_WARN_LIMIT		± 5% (LL - HL)	130V to 435V	100%
HI Side Undervoltage Protection Limit	(D7h) DISABLE_FAULTS	Can only be disabled to a preset default value	± 5% (LL - HL)	130V to 260V	100%
HI Side Overcurrent Protection Limit	(5Bh) IIN_OC_FAULT_LIMIT		± 20% (10 - 20% of FL) ± 5% (20 - 133% of FL)	0 to 5.625A	100%
HI Side Overcurrent Warning Limit	(5Dh) IIN_OC_WARN_LIMIT		± 20% (10 - 20% of FL) ± 5% (20 - 133% of FL)	0 to 5.625A	100%
Overtemperature Protection Limit	(4Fh) OT_FAULT_LIMIT	Internal temperature	± 7°C (Full Range)	0 to 125°C	100%
Overtemperature Warning Limit	(51h) OT_WARN_LIMIT	Internal temperature	± 7°C (Full Range)	0 to 125°C	100%
Turn On Delay	(60h) TON_DELAY	Additional time delay to the undervoltage startup delay	± 50µs	0 to 100ms	0ms

Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted. **Please note:** For chassis mount model, Vicor part number 42550 will be needed for applications requiring the use of the signal pins. Signal cable 42550 is rated up to five insertions and extractions. To avoid unnecessary stress on the connector, the cable should be appropriately strain relieved.

EXT. BIAS (VDDB) Pin

- VDDB powers the internal controller.
- VDDB needs to be applied to enable and disable the BCM through PMBus™ control (using OPERATION COMMAND), and to adjust warning and protection thresholds.
- VDDB voltage not required for telemetry; however, if VDDB is not applied, telemetry information will be lost when V_{IN} is removed.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
INPUT	Regular Operation	VDDB Voltage	V_{VDDB}		4.5	5	9	V
		VDDB Current Consumption	I_{VDDB}				50	mA
	Startup	Inrush Current Peak	I_{VDDB_INR}	V_{VDDB} slew rate = 1V/µs		3.5		A
		Turn On Time	t_{VDDB_ON}	From V_{VDDB_MIN} to PMBus active		1.5		ms

SGND Pin

- All PMBus interface signals (SCL, SDA, ADDR) are referenced to SGND pin.
- SGND pin also serves as return pin (ground pin) for VDDB.
- Keep SGND signal separated from the low voltage side power return terminal (–LO) in electrical design.

Address (ADDR) Pin

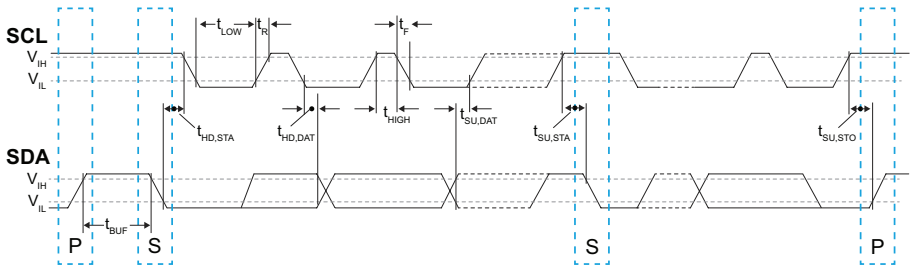
- This pin programs the address using a resistor between ADDR pin and signal ground.
- The address is sampled during startup and is stored until power is reset. This pin programs only a Fixed and Persistent address.
- This pin has an internal 10kΩ pullup resistor to 3.3V.
- 16 addresses are available. The range of each address is 206.25mV (total range for all 16 addresses is 0V to 3.3V).

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
MULTI–LEVEL INPUT	Regular Operation	ADDR Input Voltage	V_{SADDR}	See address section	0		3.3	V
		ADDR Leakage Current	I_{SADDR}	Leakage current			1	µA
	Startup	ADDR Registration Time	t_{SADDR}	From V_{VDDB_MIN}		1		ms

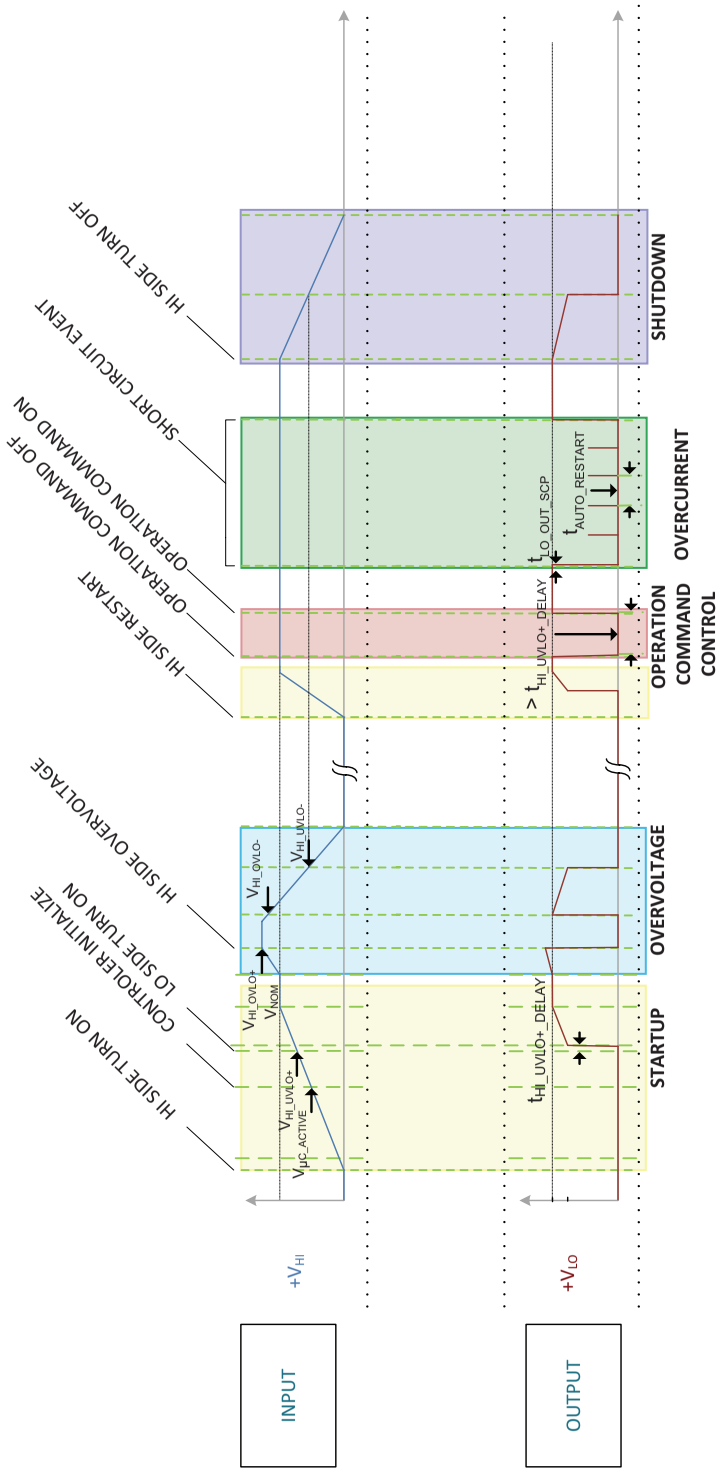
Serial Clock input (SCL) AND Serial Data (SDA) Pins

- High power SMBus specification and SMBus physical layer compatible. Note that optional SMBALERT# is not supported.
- PMBus™ command compatible.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT	Regular Operation	**Electrical Parameters**						
		Input Voltage Threshold	V_{IH}		2.1			V
			V_{IL}				0.8	V
		Output Voltage Threshold	V_{OH}		3			V
			V_{OL}				0.4	V
		Leakage Current	I_{LEAK_PIN}	Unpowered device			10	µA
		Signal Sink Current	I_{LOAD}	V_{OL} = 0.4V	4			mA
		Signal Capacitive Load	C_I	Total capacitive load of one device pin			10	pF
		Signal Noise Immunity	V_{NOISE_PP}	10MHz to 100MHz	300			mV
		Timing Parameters						
		Operating Frequency	F_{SMB}	Idle state = 0Hz	10		400	kHz
		Free Time Between Stop and Start Condition	t_{BUF}		1.3			µs
		Hold Time After Start or Repeated Start Condition	$t_{HD:STA}$	First clock is generated after this hold time	0.6			µs
		Repeat Start Condition Setup Time	$t_{SU:STA}$		0.6			µs
		Stop Condition Setup Time	$t_{SU:STO}$		0.6			µs
		Data Hold Time	$t_{HD:DAT}$		300			ns
		Data Setup Time	$t_{SU:DAT}$		100			ns
		Clock Low Time Out	$t_{TIMEOUT}$		25		35	ms
		Clock Low Period	t_{LOW}		1.3			µs
		Clock High Period	t_{HIGH}		0.6		50	µs
		Cumulative Clock Low Extend Time	$t_{LOW:SEXT}$				25	ms
		Clock or Data Fall Time	t_F		20		300	ns
		Clock or Data Rise Time	t_R		20		300	ns



Timing Diagram (Forward Direction)



Application Characteristics

Temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (high voltage side to low voltage side). See associated figures for general trend data.

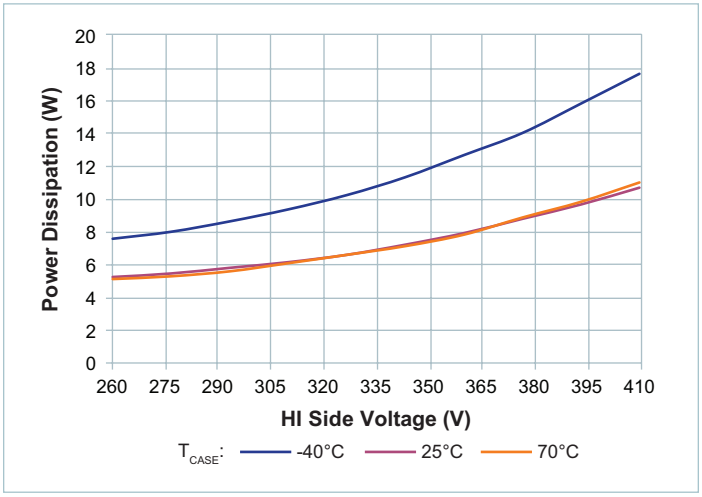


Figure 4 — *No load power dissipation vs. V_{HI_DC}*

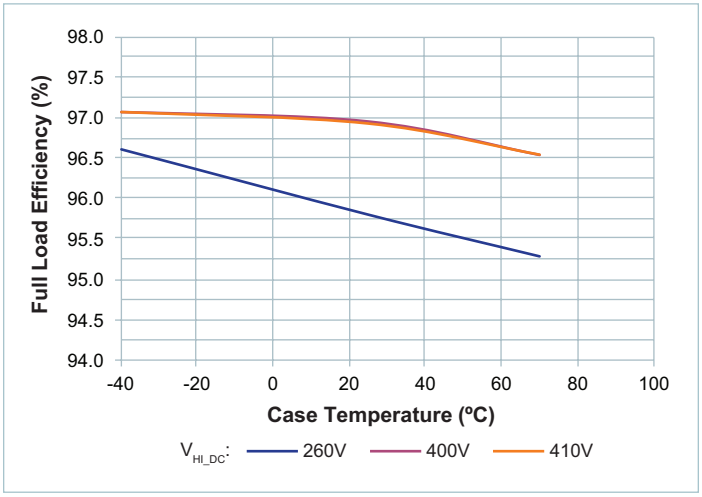


Figure 5 — *Full load efficiency vs. temperature*

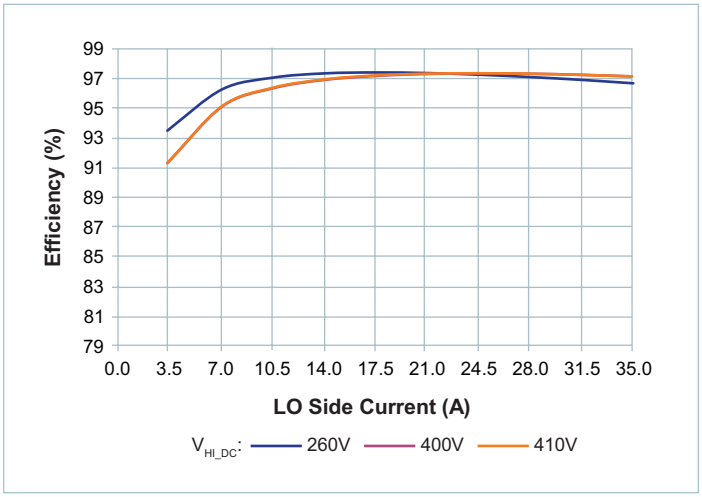


Figure 6 — *Efficiency at T_{CASE} = -40°C*

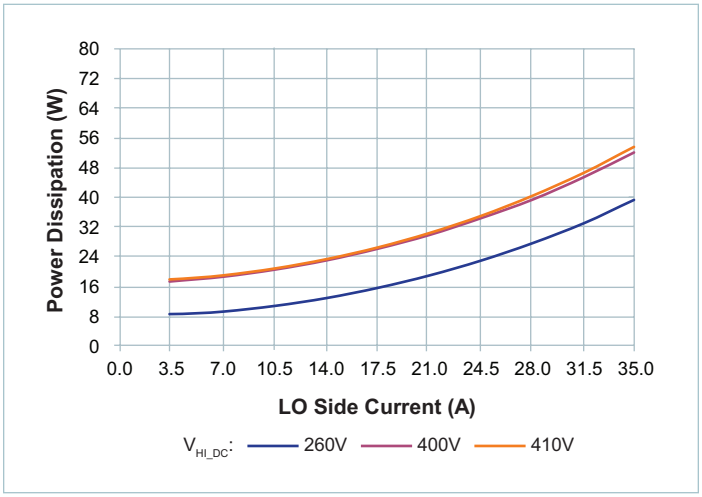


Figure 7 — *Power dissipation at T_{CASE} = -40°C*

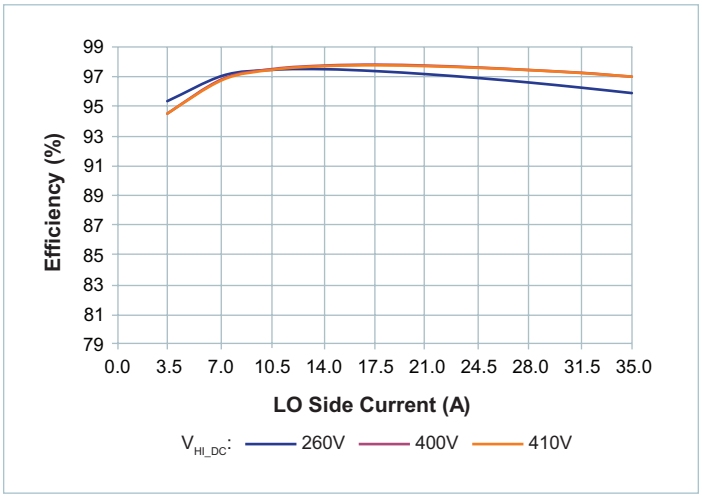


Figure 8 — *Efficiency at T_{CASE} = 25°C*

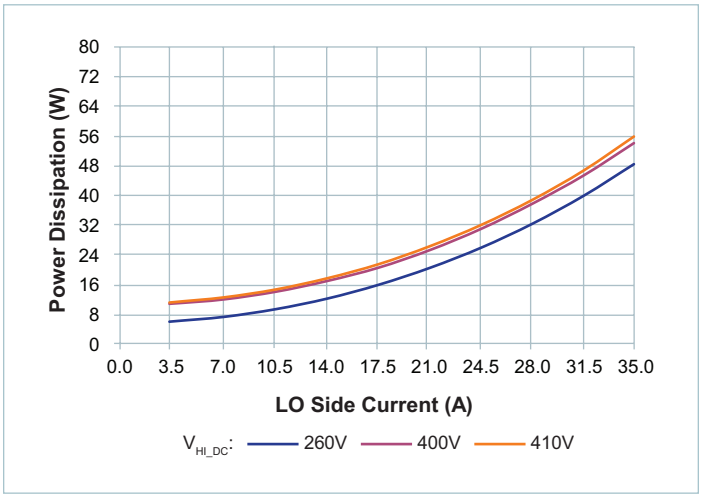


Figure 9 — *Power dissipation at T_{CASE} = 25°C*

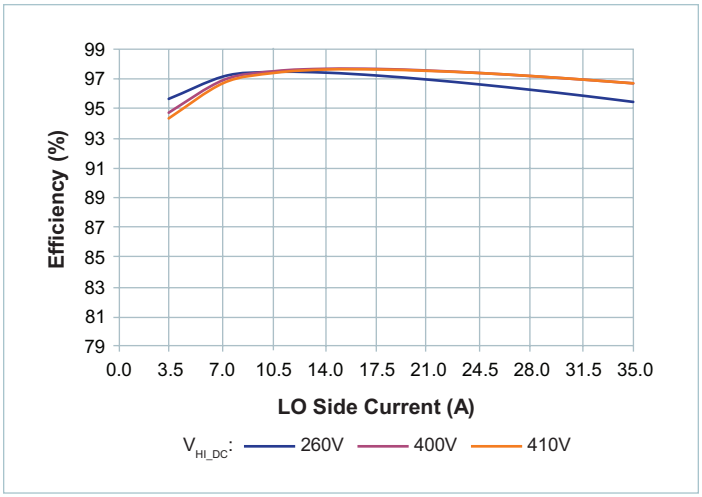


Figure 10 — *Efficiency at T_{CASE} = 70°C*

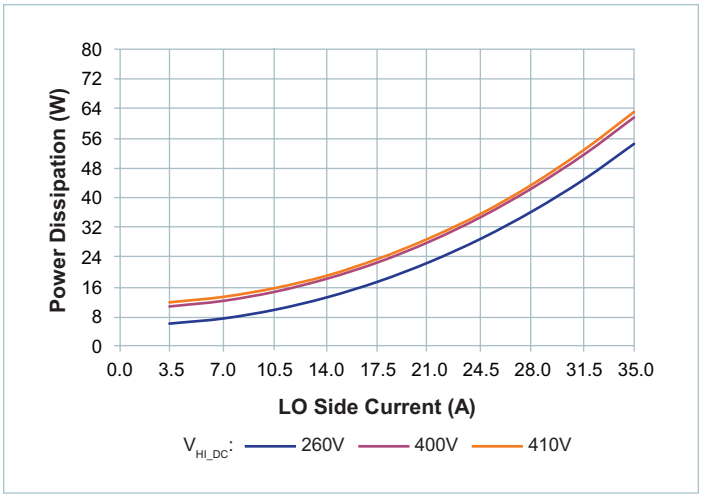


Figure 11 — *Power dissipation at T_{CASE} = 70°C*

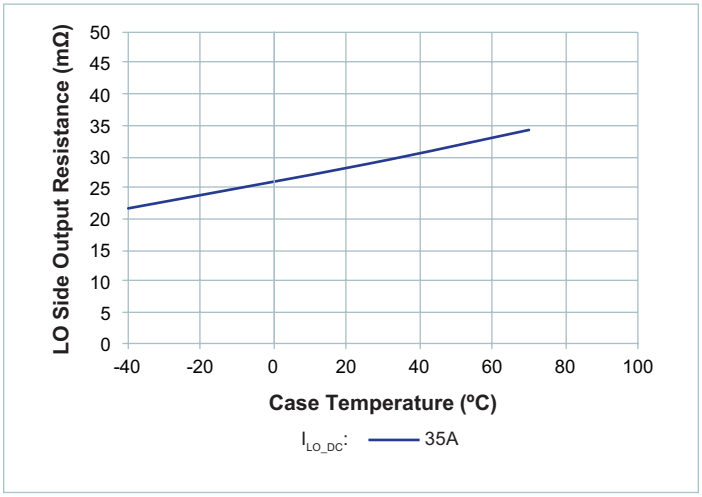


Figure 12 — *R_{LO} vs. temperature; Nominal V_{HI_DC} I_{LO_DC} = 35A at T_{CASE} = 70°C*

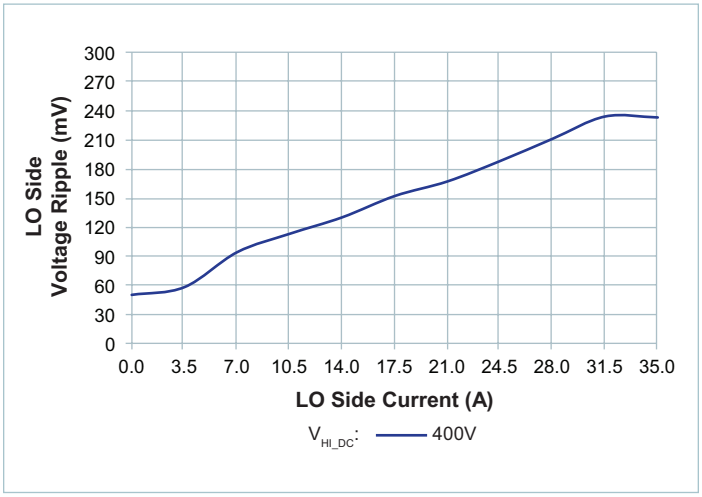


Figure 13 — *$V_{LO\_OUT\_PP}$ vs. I_{LO_DC} ; No external $C_{LO\_OUT\_EXT.}$ Board mounted module, scope setting: 20MHz analog BW*

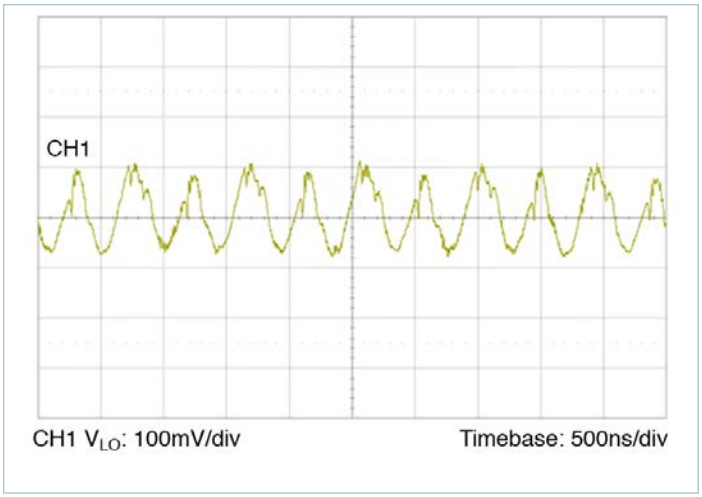


Figure 14 — *Full load LO side voltage ripple, 10µF $C_{HI\_IN\_EXT}$; no external $C_{LO\_OUT\_EXT}$. Board mounted module, scope setting: 20MHz analog BW*

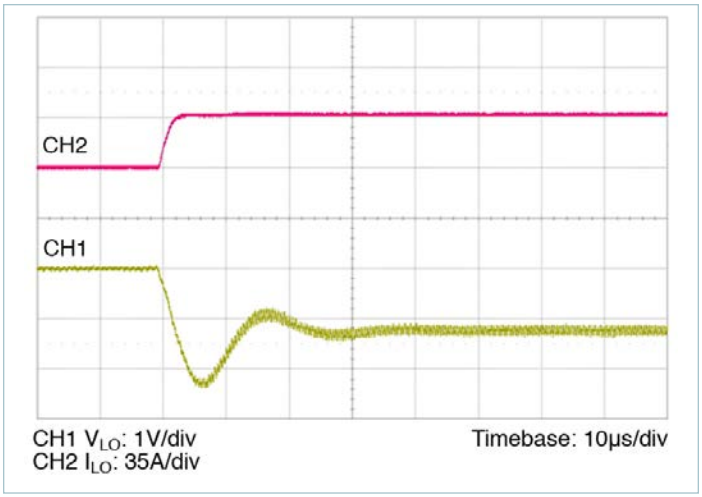


Figure 15 — *0A – 35A transient response: $C_{HI\_IN\_EXT}$ = 10µF, no external $C_{LO\_OUT\_EXT}$*

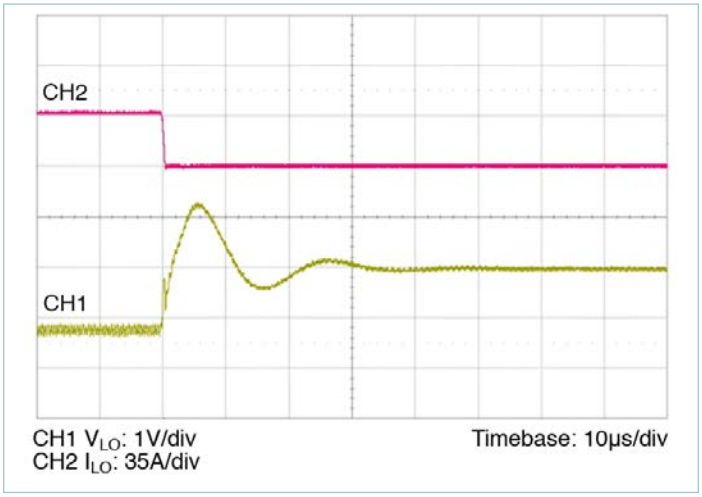


Figure 16 — *35A – 0A transient response: $C_{HI\_IN\_EXT}$ = 10µF, no external $C_{LO\_OUT\_EXT}$*

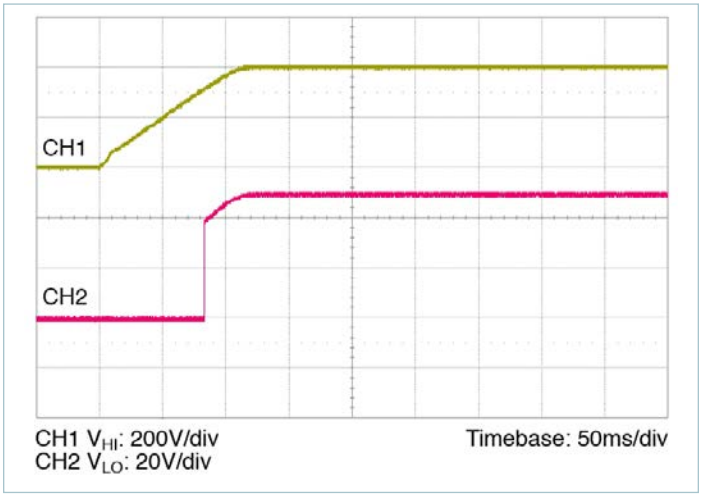


Figure 17 — *Startup from application of V_{HI_DC} = 400V, 25% I_{LO_DC}, 100% $C_{LO\_OUT\_EXT}$*

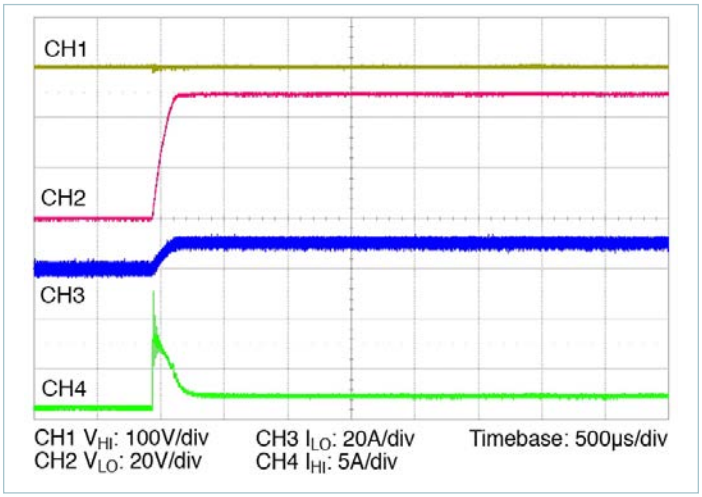


Figure 18 — *Startup from application of OPERATION COMMAND with pre-applied V_{HI_DC} = 400V, 25% I_{LO_DC}, 100% $C_{LO\_OUT\_EXT}$*

General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L	Lug (Chassis) Mount	110.30 / [4.34]	110.55 / [4.35]	110.80 / [4.36]	mm / [in]
Length	L	PCB (Board) Mount	112.51 / [4.43]	112.76 / [4.44]	113.01 / [4.45]	mm / [in]
Width	W		35.29 / [1.39]	35.54 / [1.40]	35.79 / [1.41]	mm / [in]
Height	H		9.019 / [0.355]	9.40 / [0.37]	9.781 / [0.385]	mm / [in]
Volume	Vol	Without heatsink		36.93 / [2.25]		cm^3/ [in^3]
Weight	W			140.5 / [4.96]		g / [oz]
Pin Material		C145 copper				
Underplate		Low stress ductile Nickel	50		100	µin
Pin Finish (Gold)		Palladium	0.8		6	µin
		Soft Gold	0.12		2	
Pin Finish (Tin)		Whisker resistant matte Tin	200		400	µin
Thermal						
Operating Internal Temperature	T_{INT}	BCM4414xD1E5135yzz (T-Grade)	-40		125	°C
		BCM4414xD1E5135yzz (C-Grade)	-20		125	
Operating Case Temperature	T_{CASE}	BCM4414xD1E5135yzz (T-Grade), derating applied, see safe thermal operating area	-40		100	
		BCM4414xD1E5135yzz (C-Grade), derating applied, see safe thermal operating area	-20		100	
Thermal Resistance Top Side	Φ_{INT_TOP}	Estimated thermal resistance to maximum temperature internal component from isothermal top		1.24		°C/W
Thermal Resistance Coupling Between Top Case and Bottom Case	Φ_{HOU}	Estimated thermal resistance of thermal coupling between the top and bottom case surfaces		0.63		°C/W
Thermal Resistance Bottom Side	Φ_{INT_BOT}	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		1.41		°C/W
Thermal Capacity				54		Ws/°C
Assembly						
Storage Temperature	T_{ST}	BCM4414xD1E5135yzz (T-Grade)	-40		125	°C
		BCM4414xD1E5135yzz (C-Grade)	-40		125	°C
ESD Withstand	ESD_{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2kV)	1000			
	ESD_{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V)	200			

General Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Safety						
Isolation Capacitance	C_{HI_LO}	Unpowered unit	620	780	940	pF
Isolation Resistance	R_{HI_LO}	At 500V_{DC}	10			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		3.53		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		3.90		MHrs
Agency Approvals / Standards		cTÜVus EN 60950-1				
		cURus UL 60950-1				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

BCM in a VIA Package

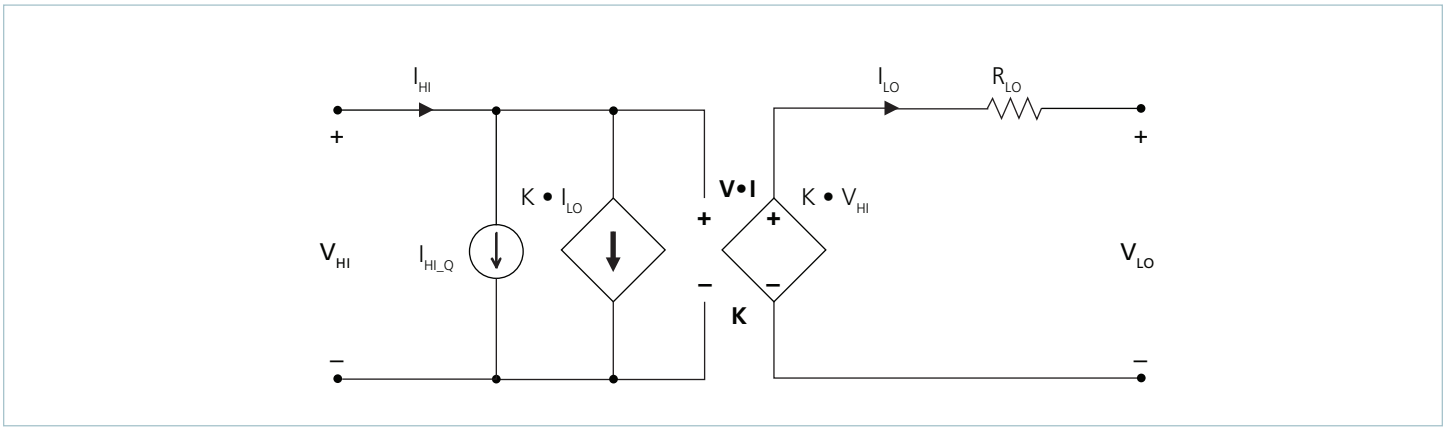


Figure 19 *— BCM DC model (Forward Direction)*

The BCM uses a high frequency resonant tank to move energy from the high voltage side to the low voltage side and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of the HI side voltage and the LO side current. A small amount of capacitance embedded in the high voltage side and low voltage side stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM4414xD1E5135yzz can be simplified into the model shown in Figure 19.

At no load:

$$V_{LO} = V_{HI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the BCM.
Rearranging Eq (1):

$$K = \frac{V_{LO}}{V_{HI}} \qquad (2)$$

In the presence of a load, V_{LO} is represented by:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R_{LO} \qquad (3)$$

and I_{LO} is represented by:

$$I_{LO} = \frac{I_{HI} - I_{HI\_Q}}{K} \qquad (4)$$

R_{LO} represents the impedance of the BCM and is a function of the R_{DS_ON} of the HI side and LO side MOSFETs, PC board resistance of HI side and LO side boards and the winding resistance of the power transformer. I_{HI_Q} represents the HI side quiescent current of the BCM controller, gate drive circuitry and core losses.

The effective DC voltage transformer action provides additional interesting attributes. Assuming that R_{LO} = 0Ω and I_{HI_Q} = 0A, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with V_{HI}.

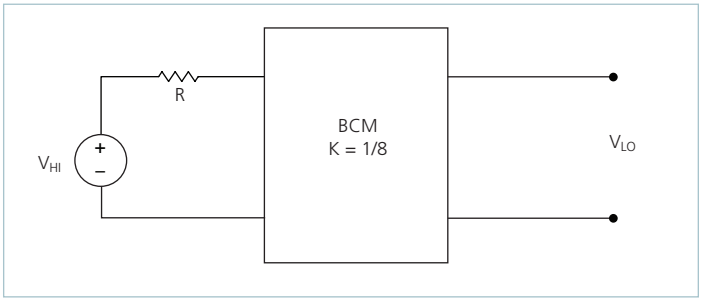


Figure 20 *— K = 1/8 BCM with series HI side resistor*

The relationship between V_{HI} and V_{LO} becomes:

$$V_{LO} = \left(V_{HI} - I_{HI} \bullet R\right) \bullet K \qquad (5)$$

Substituting the simplified version of Eq. (4) (I_{HI_Q} is assumed = 0A) into Eq. (5) yields:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Eq. (3), where R_{LO} is used to represent the characteristic impedance of the BCM. However, in this case a real resistor, R, on the high voltage side of the BCM is effectively scaled by K^2 with respect to the low voltage side.

Assuming that R = 1Ω, the effective R as seen from the low voltage side is 15.6mΩ, with K = 1/8.

A similar exercise can be performed with the addition of a capacitor or shunt impedance at the high voltage side of the BCM. A switch in series with V_{HI} is added to the circuit. This is depicted in Figure 21.

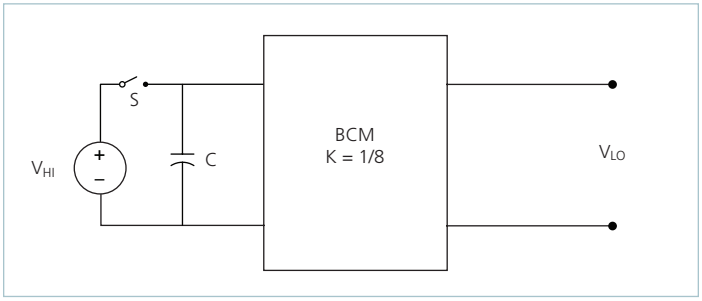


Figure 21 *— BCM with HI side capacitor*

A change in V_{HI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{HI}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{HI}, the switch is opened and the capacitor is discharged through the idealized BCM. In this case,

$$I_C = I_{LO} \bullet K \qquad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{LO}(t) = \frac{C}{K^2} \bullet \frac{dV_{LO}}{dt} \qquad (9)$$

The equation in terms of the LO side has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the low voltage side when expressed in terms of the high voltage side. With a K = 1/8 as shown in Figure 21, C = 1µF would appear as C = 64µF when viewed from the low voltage side.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a BCM between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, these benefits are not achieved if the series impedance of the BCM is too high. The impedance of the BCM must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the BCM low involves switching at a high frequency. This enables the use of small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM module are:

- No load power dissipation (P_{HI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{LO}}$): refers to the power loss across the BCM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{HI\_NL} + P_{R_{LO}} \qquad (10)$$

Therefore,

$$P_{LO\_OUT} = P_{HI\_IN} - P_{DISSIPATED} = P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{LO\_OUT}}{P_{HI\_IN}} = \frac{P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}}}{P_{HI\_IN}} \qquad (12)$$

$$= \frac{V_{HI} \bullet I_{HI} - P_{HI\_NL} - (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}$$

$$= 1 - \left(\frac{P_{HI\_NL} + (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}\right)$$

Thermal Considerations

The VIA package provides effective conduction cooling from either of the two module surfaces. Heat may be removed from the top surface, the bottom surface or both. The extent to which these two surfaces are cooled is a key component for determining the maximum power that can be processed by a VIA, as can be seen from the specified thermal operating area in Figure 1. Since the VIA has a maximum internal temperature rating, it is necessary to estimate this temperature based on a system-level thermal solution. For this purpose, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 22 shows the "thermal circuit" for the VIA module.

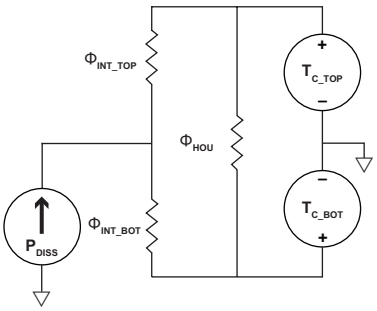


Figure 22 — *Double-sided cooling VIA thermal model*

In this case, the internal power dissipation is P_{DISS}, Φ_{INT_TOP} and Φ_{INT_BOT} are the thermal resistance characteristics of the VIA module and the top and bottom surface temperatures are represented as T_{C_TOP} and T_{C_BOT}. It is interesting to note that the package itself provides a high degree of thermal coupling between the top and bottom case surfaces (represented in the model by the resistor Φ_{HOU}). This feature enables two main options regarding thermal designs:

- Single side cooling: the model of Figure 22 can be simplified by calculating the parallel resistor network and using one simple thermal resistance number and the internal power dissipation curves; an example for bottom side cooling only is shown in Figure 23.

In this case, Φ_{INT} can be derived as follows:

$$\Phi_{INT} = \frac{(\Phi_{INT\_TOP} + \Phi_{HOU}) \bullet \Phi_{INT\_BOT}}{\Phi_{INT\_TOP} + \Phi_{HOU} + \Phi_{INT\_BOT}} \qquad (13)$$

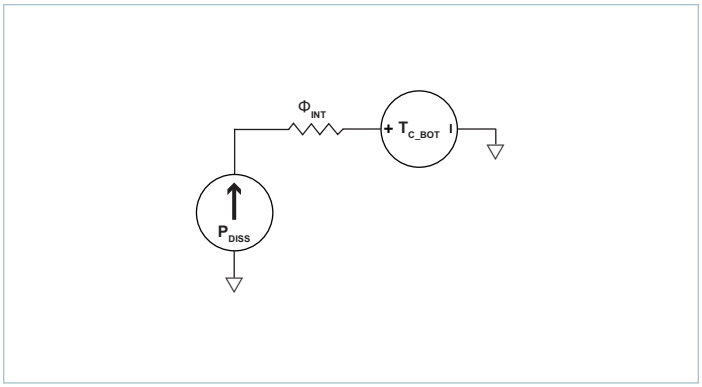


Figure 23 — *Single-sided cooling VIA thermal model*

- Double side cooling: while this option might bring limited advantage to the module internal components (given the surface-to-surface coupling provided), it might be appealing in cases where the external thermal system requires allocating power to two different elements, such as heatsinks with independent airflows or a combination of chassis/air cooling.

Current Sharing

The performance of the BCM is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load. Ensuring equal current sharing among modules requires that BCM array impedances be matched.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes/wires within the PCB/Chassis to deliver and return the current to the modules.
- Provide as symmetric a PCB/Wiring layout as possible among modules

For further details see AN:016 Using BCM Bus Converters in High Power Arrays.

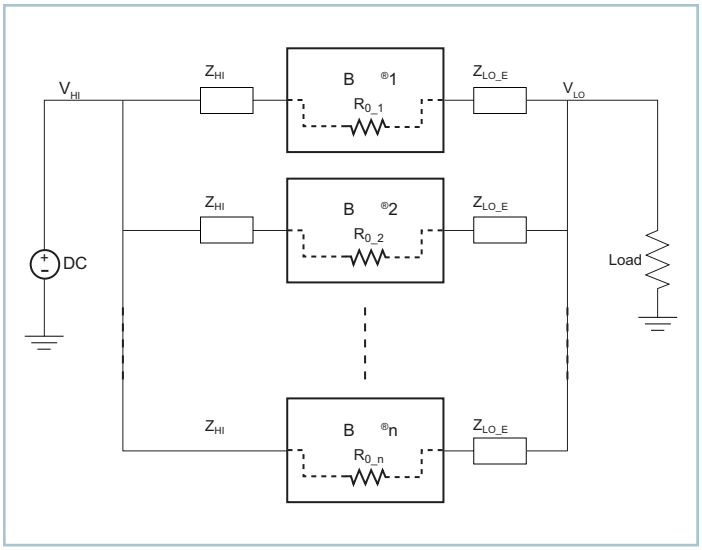


Figure 24 *— BCM module array*

Fuse Selection

In order to provide flexibility in configuring power systems, BCM in a VIA package modules are not internally fused. Input line fusing of BCM products is recommended at the system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of BCM module)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: 10A Littlefuse 505 Series or
  10A Littlefuse 487 Series (HI side)

Reverse Operation

BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from the low voltage side back to the high voltage side whenever the low side voltage exceeds $V_{HI} \bullet K$. The module will continue operation in this fashion as long as no faults occur.

The BCM4414xD1E5135yzz has not been qualified for continuous operation in a reverse power condition. However, fault protections that help to protect the module in forward operation will also protect the module in reverse operation.

Transient operation in reverse is expected in cases where there is significant energy storage on the low voltage side and transient voltages appear on the high voltage side.

Dielectric Withstand

The chassis of the BCM in a VIA package is required to be connected to Protective Earth when installed in the end application and must satisfy the requirements of IEC 60950-1 for Class I products.

The BCM in a VIA package contains an internal safety approved isolating component (ChiP) that provides Reinforced Insulation from high voltage side to low voltage side. The isolating component is individually tested for Reinforced Insulation from the high voltage side to the low voltage side at $4242V_{DC}$ prior to final assembly of the VIA. The Reinforced Insulation can only be tested on the completed VIA assembly at Basic Insulation values, as specified in the electric strength Test Procedure noted in clause 5.2.2 of IEC 60950-1.

Test Procedure Note from IEC 60950-1

"For equipment incorporating both REINFORCED INSULATION and lower grades of insulation, care is taken that the voltage applied to the REINFORCED INSULATION does not overstress BASIC INSULATION or SUPPLEMENTARY INSULATION."

Summary

The final VIA assembly provides basic insulation from the high voltage side to case, reinforced insulation from the high voltage side to the low voltage side, and functional insulation from the low voltage side to case. The case is required to be connected to protective earth in the final installation. The protective earth connection can be accomplished through a dedicated wiring harness (example: ring terminal clamped by mounting screw) or surface contact (example: pressure contact on bare conductive chassis or PCB copper layer with no solder mask).

The construction of the VIA can be summarized by describing it as a "Class II" component installed in a "Class I" subassembly. The insulation from the high voltage side to low voltage side can only be tested at basic insulation values on the fully assembled VIA product.

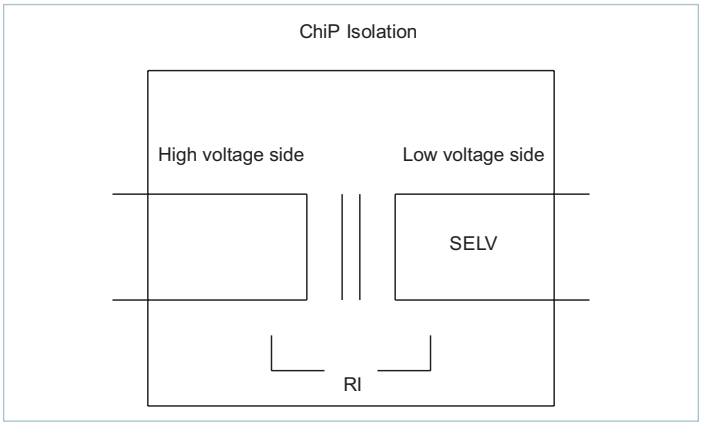


Figure 25 *— ChiP before final assembly in the VIA*

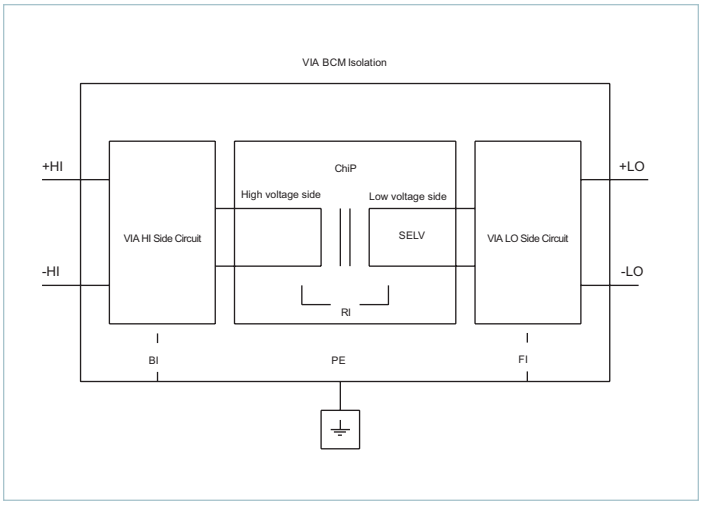


Figure 26 *— BCM in a VIA package after final assembly*

Filtering

The BCM in a VIA package has built-in single stage EMI filtering with Hot-Swap circuitry located on the high voltage side. The integrated EMI filtering consists of a common mode choke, differential mode capacitors, and Y2 common mode capacitors. A typical test set-up block diagram for conducted emissions is shown in Figure 27.

The built-in EMI filtering reduces the HI side voltage ripple. External LO side filtering can be added as needed, with ceramic capacitance used as a LO side bypass for this purpose. The filtering, along with Hot-Swap circuitry, protects the BCM in a VIA package from overvoltage transients imposed by a system that would exceed maximum ratings. VIA HI side and LO side voltage ranges shall not be exceeded. An internal overvoltage function prevents operation outside of the normal operating HI side range. However, the VIA is exposed to the applied voltage even when disabled and must withstand it.

The source response is generally the limiting factor in the overall system response, given the wide bandwidth of the BCM. Anomalies in the response of the source will appear at the LO side of the module multiplied by its K factor.

Total load capacitance at the LO side of the BCM shall not exceed the specified maximum to ensure correct operation in startup. Due to the wide bandwidth and small LO side impedance of the BCM, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the HI side of the BCM.

At frequencies less than 500kHz, the BCM appears as an impedance of R_{LO} between the source and load. Within this frequency range, capacitance connected at the HI side appears as an effective scaled capacitance on the LO side per the relationship defined in Eq. (14).

This enables a reduction in the size and number of capacitors used in a typical system.

$$C_{LO} = \frac{C_{HI}}{K^2} \qquad (14)$$

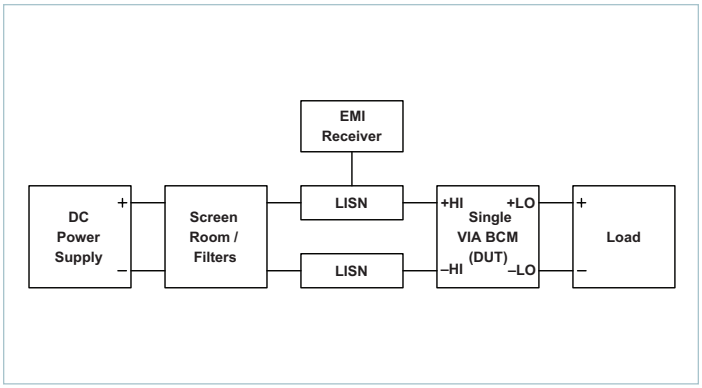


Figure 27 *— Typical test setup block diagram for conducted emissions*

Hot-Swap

Many applications use a power architecture based on a $380V_{DC}$ distribution bus. This supply level is emerging as a new standard for efficient distribution of power through board, rack and chassis mounted telecom and datacom systems. The interconnection between the different modules is accomplished with a backplane and motherboard. Power is commonly provided to the various module slots via a $380V_{DC}$ distribution bus.

In the event of a fault, removal of the faulty module from the rack is relatively easy, provided that the remaining power modules can support the step increase in load. Plugging in the replacement module has more potential for problems, as it presents an uncharged capacitor load and will draw a large inrush current. This could cause a momentary, but unacceptable interruption or sag in the backplane power bus if not limited. Additional problems may arise if ordinary power module connectors are used, since the connector pins will engage and disengage in a random and unpredictable sequence during insertion and removal.

Hot-Swap or hot-plug is a highly desirable feature in many applications, but also results in several issues that must be addressed in the system design. A number of related phenomena occur with a live insertion and removal event, including contact bouncing, arcing between HI side connector pins, and large voltage and current transients. Hot-Swap circuitry in the converter modules protects the module itself and the rest of the system from the problems associated with live insertion.

This module provides a high level of integration for DC-DC converters in $380V_{DC}$ distribution systems, saving design time and board space. To allow for maintenance, reconfiguration, redundancy and system upgrades, the BCM in a VIA package is designed to address the function of Hot-Swapping at the $380V_{DC}$ distribution bus. Hot-Swap circuitry, as shown in Figure 28, uses an active MOSFET switching device in series with the HI side line. During module insertion, the MOSFET is driven into a resistive state to limit the inrush current as the input capacitance of the inserted unit is charged. The MOSFET is fully enhanced once the module's HI side capacitor has sufficiently charged to minimize losses during normal operation. Verification of the Hot-Swap circuitry performance is illustrated through plots of the module's response to a live insertion event in Figures 30 and 31.

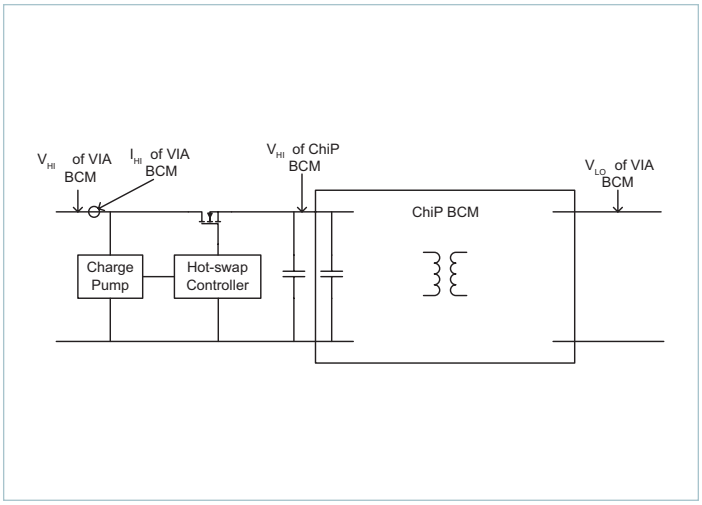


Figure 28 *— High level diagram for 384V_{DC} BCM in a VIA package showing internal Hot-Swap circuitry and ChiP BCM*

The BCM in a VIA package provides the opportunity to incorporate Hot-Swap capabilities into redundant power module arrays. This allows telecoms and other mission critical applications to continue operating without interruption even through failure and replacement of one or more power modules.

Hot-Swap Test – Test circuit and Procedure

- Two parallel BCMs in a VIA package with mercury relay#1 open
- Close mercury relay#1 and measure inrush current going into BCM#2

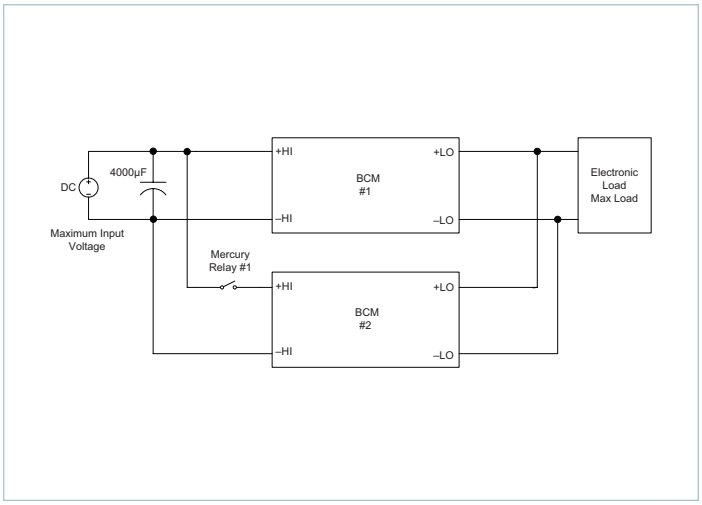


Figure 29 *— Hot-Swap test circuit*

Hot-Swap Test – Scope Pictures

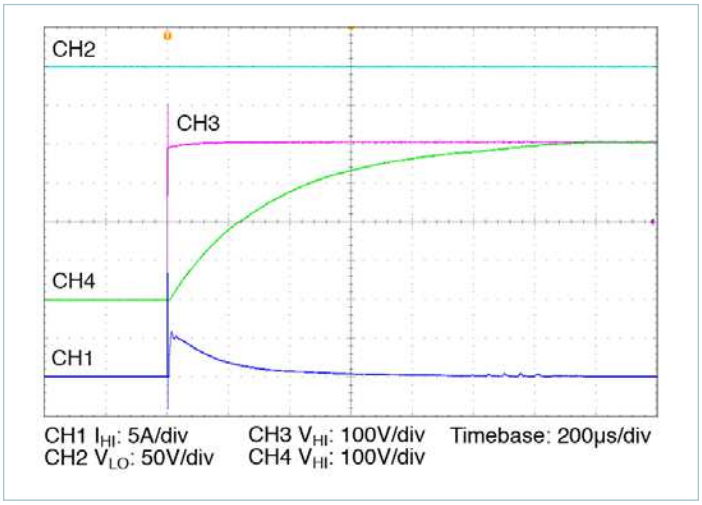


Figure 30 *— Hot-Swap startup*

Ch1: I_{HI} of BCM#2

Ch2: V_{LO} of BCM#2

Ch3: V_{HI} of BCM#2 shows the fast voltage transient at the high side terminal of BCM#2

Ch4: V_{HI} of internal ChiP BCM#2 shows the soft start charging the high side capacitor.

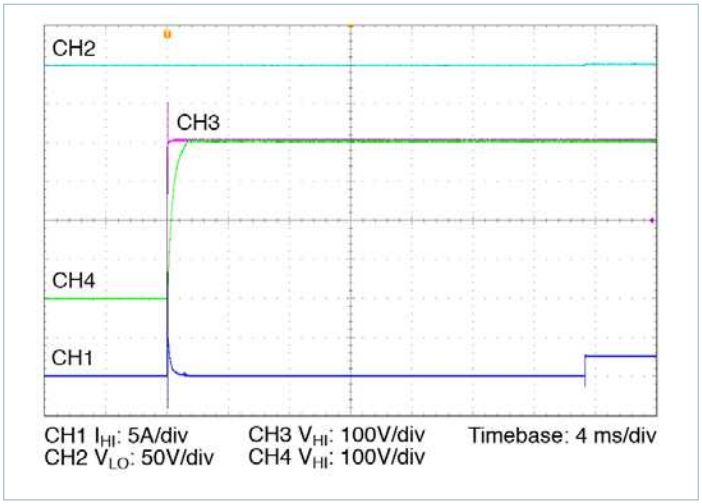
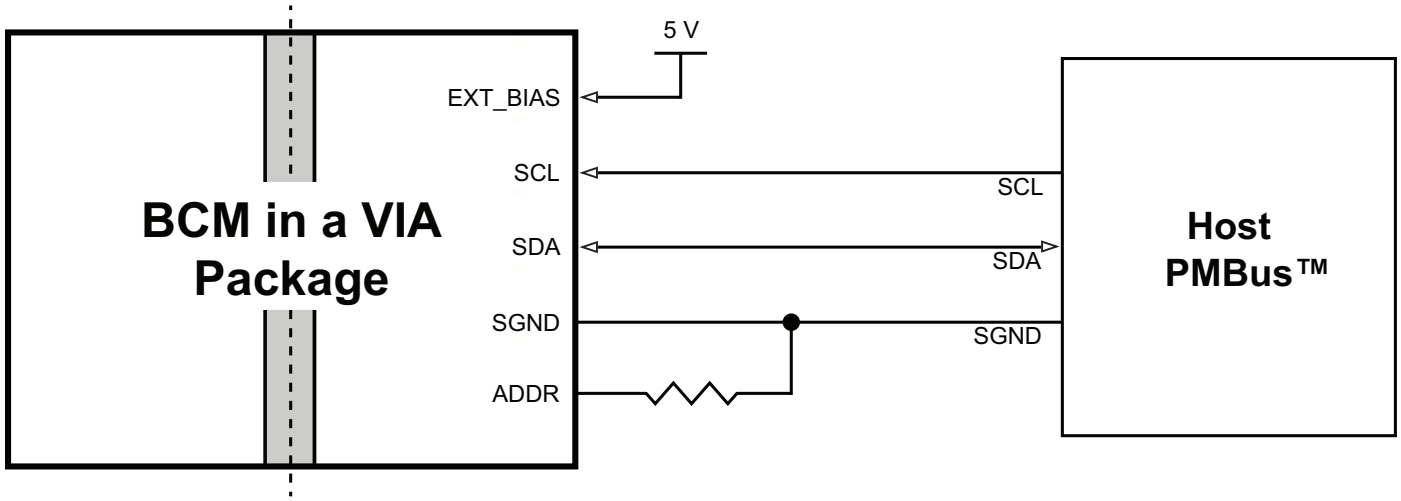


Figure 31 *— Expanded time scale version of Figure 30 showing startup of BCM#2*

System Diagram for PMBus™ Interface



The controller of the BCM in a VIA package is referenced to the low voltage side signal ground (SGND).

The BCM in a VIA package provides the Host PMBus system with accurate telemetry monitoring and reporting, threshold and warning limits adjustment, in addition to corresponding status flags. The standalone BCM is periodically polled for status by the host PMBus. Direct communication to the BCM is enabled by a page command. For example, the page (0x00) prior to a telemetry inquiry points to the controller data and page (0x01) prior to a telemetry inquiry points to the BCM parameters.

The BCM enables the PMBus compatible host interface with an operating bus speed of up to 400kHz. The BCM follows the PMBus command structure and specification.