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BCM® in a VIA™ Package Bus Converter

BCM4414xG0F4440yzz

Isolated Fixed-Ratio DC-DC Converter

Features & Benefits

- Up to 40A continuous low-voltage-side current
- Fixed transformation ratio (K) of 1/16
- Up to 776W/in^3 power density
- 97.5% peak efficiency
- Integrated filtering
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 4414 package
- High MTBF
- Thermally enhanced VIA package
- PMBus™ management interface
- Bidirectional operation (start up in forward direction only)

Typical Applications

- High-Voltage DC Power Distribution
- 3-Phase AC-DC Converters
- Information and Communication Technology (ICT) Equipment
- High-End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High-Density Energy Systems
- Transportation
- Green Buildings and Microgrids

Product Ratings	
V_{HI} = 544V (400 – 700V)	I_{LO} = up to 40A
V_{LO} = 34V (25 – 43.8V) (NO LOAD)	K = 1/16

Product Description

The BCM4414xG0F4440yzz in a VIA package is a high-efficiency Bus Converter, operating from a 400 to 700V_{DC} high-voltage bus to deliver an isolated 25 to 43.8V_{DC} unregulated, low voltage.

This unique ultra-low-profile module incorporates DC-DC conversion, integrated filtering and PMBus™ commands and controls in a chassis or PCB mount form factor.

The BCM offers low noise, fast transient response and industry-leading efficiency and power density. A low-voltage-side referenced PMBus-compatible telemetry and control interface provides access to the BCM's configuration, fault monitoring and other telemetry functions.

Leveraging the thermal and density benefits of Vicor VIA packaging technology, the BCM module offers flexible thermal management options with very low top and bottom side thermal impedances.

When combined with downstream Vicor DC-DC conversion components and regulators, the BCM allows the Power Design Engineer to employ a simple, low-profile design, which will differentiate the end system without compromising on cost or performance metrics.

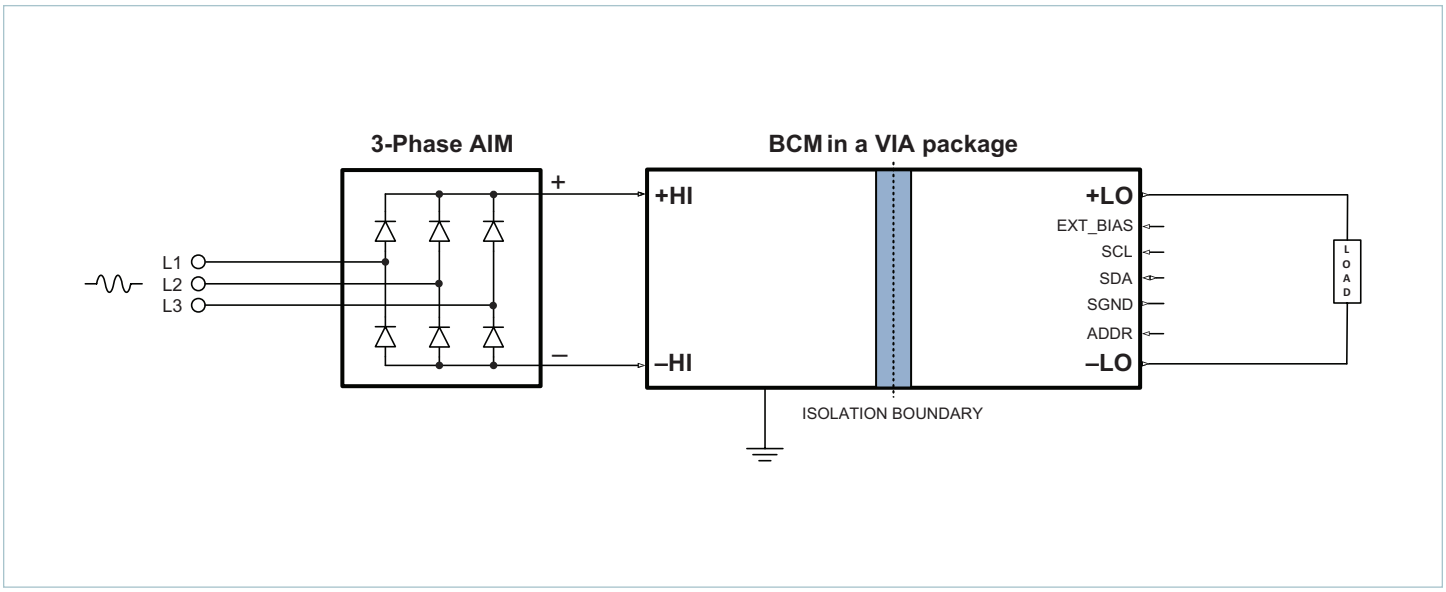
Size:
4.35 x 1.40 x 0.37in
[110.55 x 35.54 x 9.40mm]

Part Ordering Information

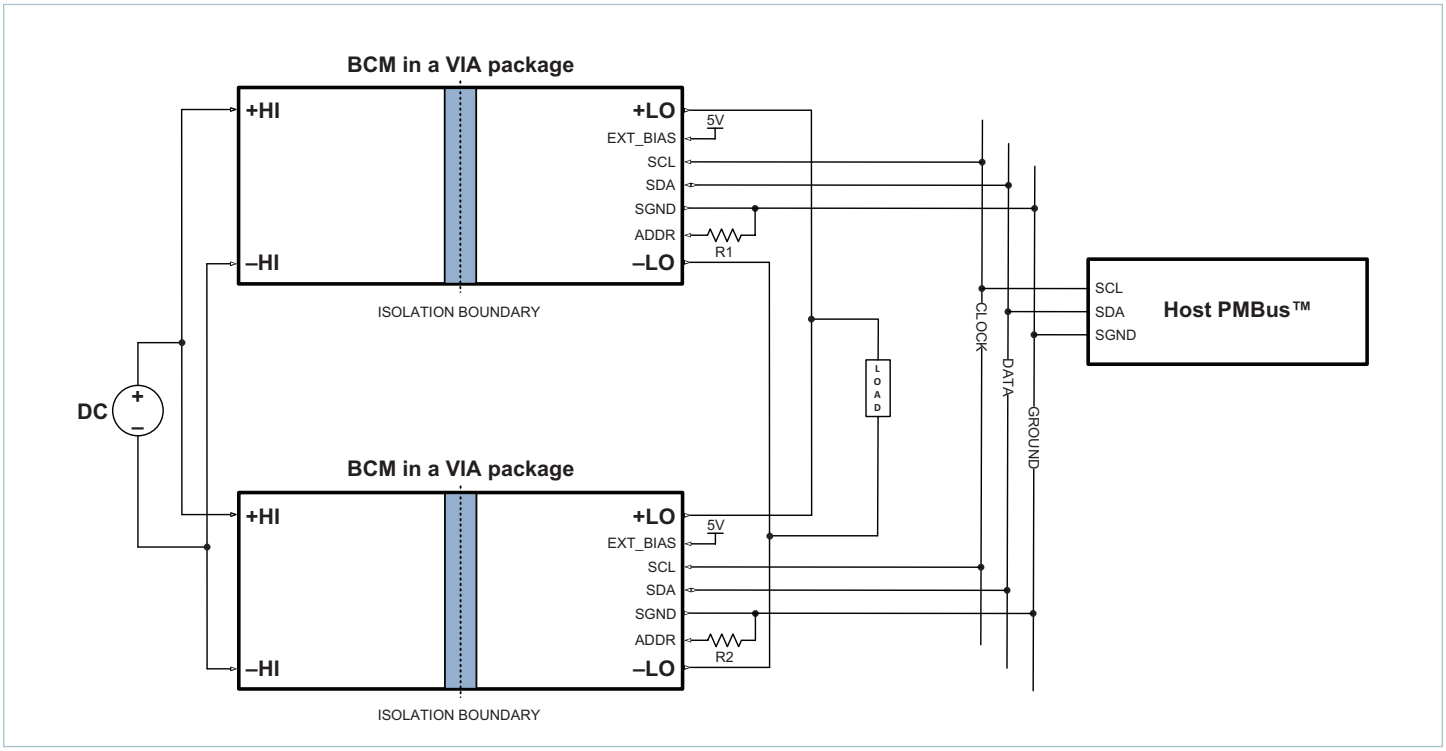
Product Function	Package Length	Package Width	Package Type	Max High-Side Voltage	High-Side Voltage Range Ratio	Max Low-Side Voltage	Max Low-Side Current	Product Grade (Case Temperature)	Option Field
BCM	44	14	x	G0	F	44	40	y	zz
BCM = Bus Converter Module	Length in Inches x 10	Width in Inches x 10	**B** = Board VIA **V** = Chassis VIA	Internal Reference				**C** = –20 to 100°C [a] **T** = –40 to 100°C [a]	**02** = Chassis/PMBus **06** = Short Pin/PMBus **10** = Long Pin/PMBus

[a] High-temperature current derating may apply; see Figure 1, specified thermal operating area.

Typical Applications

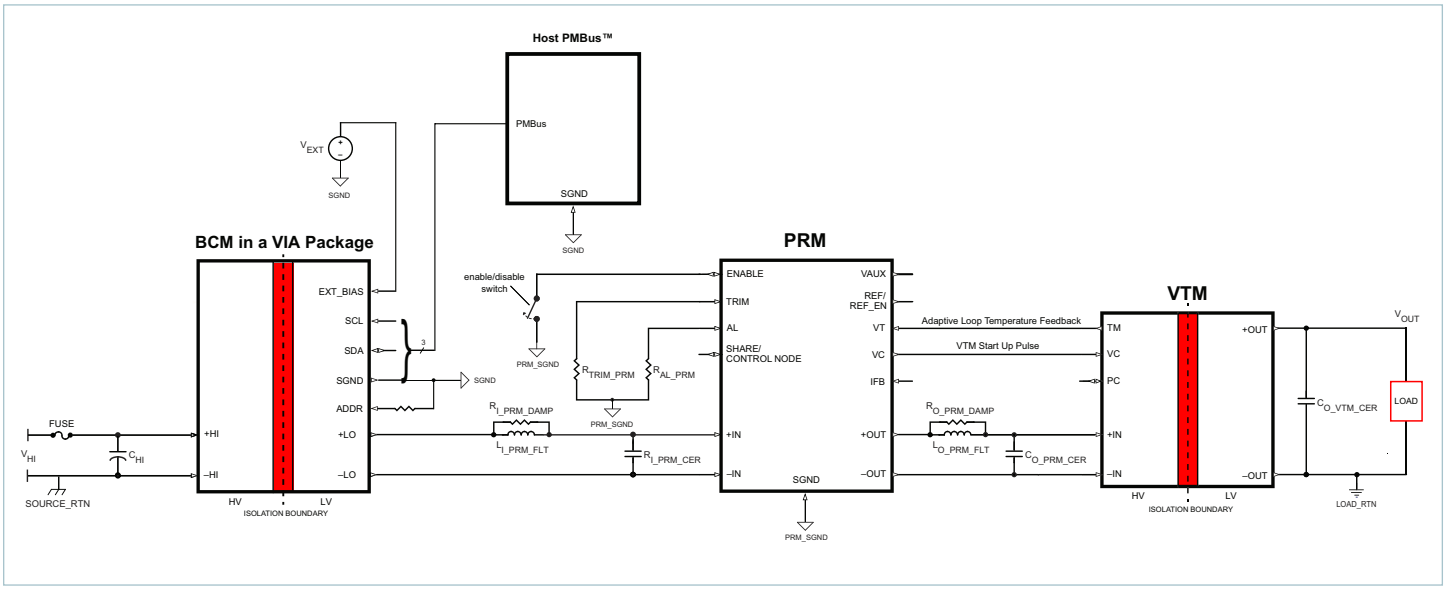


3-phase AC to point-of-load (3-phase AIM + BCM4414xG0F4440yzz)

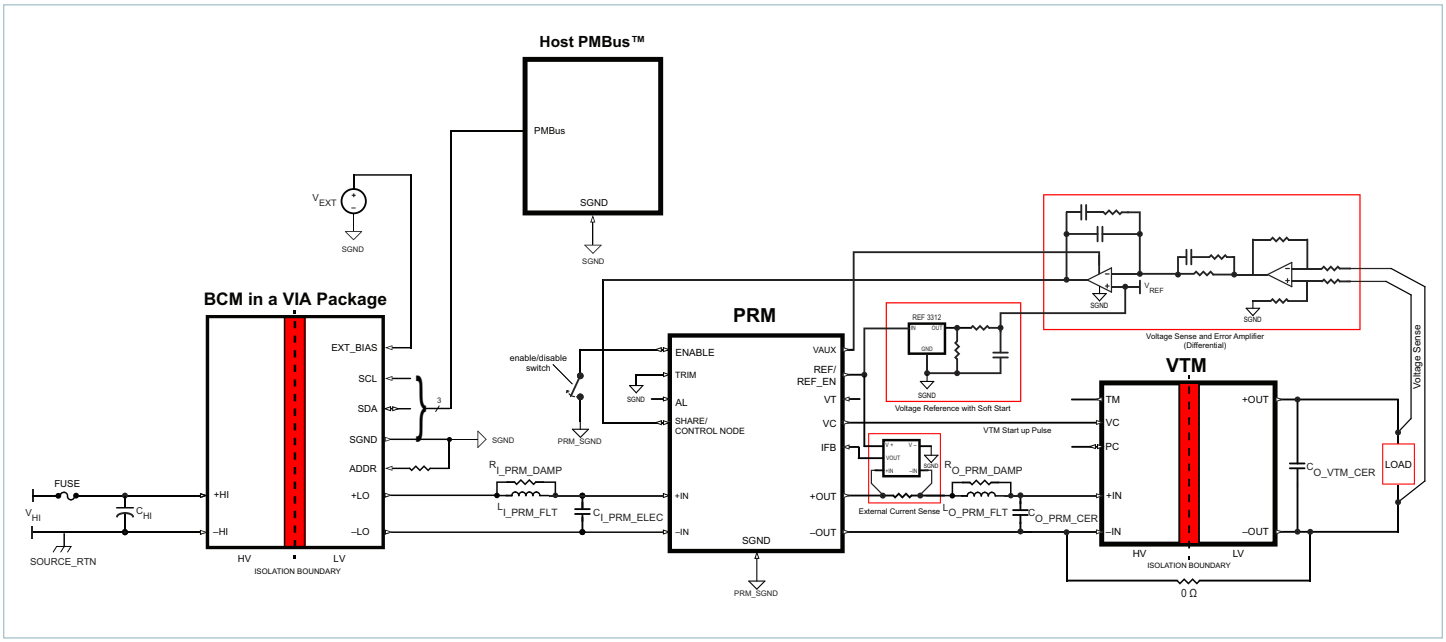


Paralleling BCM in a VIA package – connection to common Host PMBus

Typical Applications (Cont.)

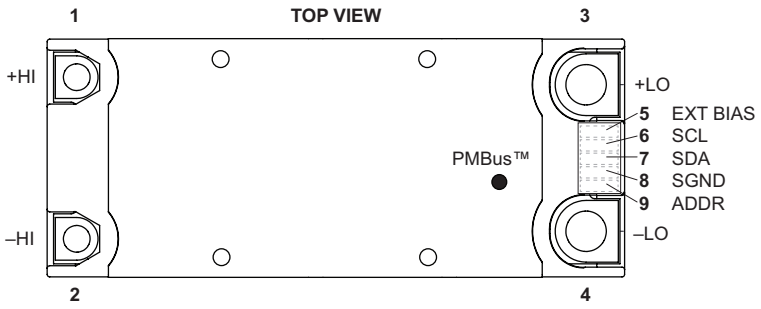


BCM4414xG0F4440yzz + PRM™ + VTM™, Adaptive-Loop Configuration – connection to common Host PMBus

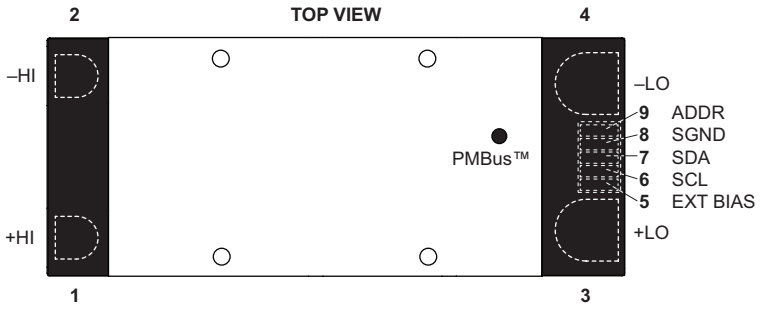


BCM4414xG0F4440yzz + PRM + VTM, Remote-Sense Configuration – connection to common Host PMBus

Pin Configuration



BCM4414 in a VIA Package - Chassis (Lug) Mount



BCM4414 in a VIA Package - Board (PCB) Mount

Note: The dot on the VIA housing indicates the location of the signal pin 9.

Pin Descriptions

Pin Number	Signal Name	Type	Function
1	+HI	HIGH SIDE POWER	High-voltage-side positive power terminal
2	–HI	HIGH SIDE POWER RETURN	High-voltage-side negative power terminal
3	+LO	LOW SIDE POWER	Low-voltage-side positive power terminal
4	–LO	LOW SIDE POWER RETURN	Low-voltage-side negative power terminal
5	EXT BIAS	INPUT	5V supply input
6	SCL	INPUT	I^2C™ Clock, PMBus™ Compatible
7	SDA	INPUT/OUTPUT	I^2C Data, PMBus Compatible
8	SGND	LOW SIDE SIGNAL RETURN	Signal Ground
9	ADDR	INPUT	Address assignment – Resistor based

Notes: All signal pins (5, 6, 7, 8, 9) are referenced to the low-voltage side and isolated from the high-voltage side.
Keep SGND signal separated from the low-voltage side power return terminal (–LO) in electrical design.

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+HI to –HI		–1	800	V
HI_DC or LO_DC Slew Rate			1	V/µs
+LO to –LO		–1	60	V
EXT BIAS to SGND		–0.3	10	V
			0.15	A
SCL to SGND		–0.3	5.5	V
SDA to SGND		–0.3	5.5	V
ADDR to SGND		–0.3	3.6	V
Isolation Voltage / Dielectric Withstand	High-voltage side to case	3100		V_{DC}
	High-voltage side to low-voltage side	4300		V_{DC}
	Low-voltage side to case	1200		V_{DC}

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Forward Direction Operation (High-Voltage Side to Low-Voltage Side)						
HI-Side Voltage Range, (Continuous)	V_{HI_DC}		**400**		**700**	V
HI-Side Voltage Range, (Transient)	V_{HI_TRANS}		**400**		**700**	V
HI-Side Voltage Initialization Threshold	$V_{\mu C\_ACTIVE}$	HI-side voltage where internal controller is initialized, (powertrain inactive)	130		350	V
HI-Side Quiescent Current	I_{HI_Q}	Disabled, V_{HI_DC} = 544V		6.3		mA
		T_{CASE} ≤ 100°C			10.2	
No-Load Power Dissipation	P_{HI_NL}	V_{HI_DC} = 544V, T_{CASE} = 25°C		9	15	W
		V_{HI_DC} = 544V	**3**		**30**	
		V_{HI_DC} = 400 – 700V, T_{CASE} = 25°C			18	
		V_{HI_DC} = 400 – 700V			**32**	
HI-Side Inrush Current Peak	$I_{HI\_INR\_PK}$	V_{HI_DC} = 700V, C_{LO_EXT} = 470µF, R_{LOAD_LO} = 20% of full-load current		4		A
		T_{CASE} ≤ 100°C			8	
DC HI-Side Current	$I_{HI\_IN\_DC}$	At $I_{LO\_OUT\_DC}$ = 40A, T_{CASE} ≤ 70°C			2.6	A
Transformation Ratio	K	High voltage to low voltage K = V_{LO_DC} / V_{HI_DC},at no load		1/16		V/V
LO-Side Current (Continuous)	$I_{LO\_OUT\_DC}$	T_{CASE} ≤ 70°C			40	A
LO-Side Current (Pulsed)	$I_{LO\_OUT\_PULSE}$	2ms pulse, 25% duty cycle, $I_{LO\_OUT\_AVG}$ ≤ 50% rated $I_{LO\_OUT\_DC}$			44	A
Efficiency (Ambient)	η_{AMB}	V_{HI_DC} = 544V, $I_{LO\_OUT\_DC}$ = 40A	95	96.9		%
		V_{HI_DC} = 400 – 700V, $I_{LO\_OUT\_DC}$ = 40A	94			
		V_{HI_DC} = 544V, $I_{LO\_OUT\_DC}$ = 20A	96	97.5		
Efficiency (Hot)	η_{HOT}	V_{HI_DC} = 544V, $I_{LO\_OUT\_DC}$ = 40A, T_{CASE} = 70°C	95	96.1		%
Efficiency (Over Load Range)	$\eta_{20\%}$	8A < $I_{LO\_OUT\_DC}$ < 40A	**92**			%
LO-Side Output Resistance	R_{LO_COLD}	V_{HI_DC} = 544V, $I_{LO\_OUT\_DC}$ = 40A, T_{CASE} = –40°C	7	10.8	20	mΩ
	R_{LO_AMB}	V_{HI_DC} = 544V, $I_{LO\_OUT\_DC}$ = 40A	8	14.4	22	
	R_{LO_HOT}	V_{HI_DC} = 544V, $I_{LO\_OUT\_DC}$ = 40A, T_{CASE} = 70°C	18	21.9	30	
Switching Frequency	F_{SW}	LO-side voltage ripple frequency = 2x F_{SW}	**0.7**	0.75	**0.8**	MHz
LO-Side Voltage Ripple	$V_{LO\_OUT\_PP}$	C_{LO_EXT} = 0µF, $I_{LO\_OUT\_DC}$ = 40A, V_{HI_DC} = 544V, 20MHz BW		300		mV
		T_{CASE} ≤ 100°C			800	

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Forward Direction Operation (High-Voltage Side to Low-Voltage Side) Cont.						
Effective HI-Side Capacitance (Internal)	C_{HI_INT}	Effective value at 544V_{HI_DC}		0.2		µF
Effective LO-Side Capacitance (Internal)	C_{LO_INT}	Effective value at 34V_{LO_DC}		36		µF
Rated LO-Side Capacitance (External)	$C_{LO\_OUT\_EXT}$	Excessive capacitance may drive module into short circuit protection			**470**	µF
Rated LO-Side Capacitance (External), Parallel Array Operation	$C_{LO\_OUT\_AEXT}$	$C_{LO\_OUT\_AEXT}$ Max = N • 0.5 • $C_{LO\_OUT\_EXT\ MAX}$, where N = the number of units in parallel				
Powertrain Hardware Protection Specification – Forward Direction Operation (High-Voltage Side to Low-Voltage Side)						
• These built-in powertrain protections are fixed in hardware and cannot be configured through PMBus™. • When duplicated in supervisory limits, hardware protections serve a secondary role and become active when supervisory limits are disabled through PMBus.						
Auto Restart Time	$t_{AUTO\_RESTART}$	Start up into a persistent fault condition. Non-latching fault detection given V_{HI_DC} > V_{HI_UVLO+}	**900**	1000	**1100**	ms
HI-Side Overvoltage Lockout Threshold	V_{HI_OVLO+}		**730**	750	**780**	V
HI-Side Overvoltage Recovery Threshold	$V_{HI\_OVLO–}$		**700**	730	**740**	V
HI-Side Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			20		V
HI-Side Overvoltage Lockout Response Time	t_{HI_OVLO}			10		µs
HI-Side Soft Start Time	$t_{HI\_SOFT\_START}$	From powertrain active. Fast current limit protection disabled during soft start		1		ms
LO-Side Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		**42**	50	**70**	A
LO-Side Overcurrent Response Time Constant	$t_{LO\_OUT\_OCP}$	Effective internal RC filter		3.6		ms
LO-Side Short Circuit Protection Trip Threshold	$I_{LO\_OUT\_SCP}$		**55**			A
LO-Side Short Circuit Protection Response Time	$t_{LO\_OUT\_SCP}$			1		µs
Overtemperature Shutdown Threshold	t_{OTP+}	Internal	**125**			°C

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Supervisory Limits Specification – Forward Direction Operation (High-Voltage Side to Low-Voltage Side)						
• These supervisory limits are set in the internal controller and can be reconfigured or disabled through PMBus™. • When disabled, the powertrain protections presented in the previous table will intervene during fault events.						
HI-Side Overvoltage Lockout Threshold	V_{HI_OVLO+}		**730**	750	**780**	V
HI-Side Overvoltage Recovery Threshold	$V_{HI\_OVLO–}$		**700**	730	**740**	V
HI-Side Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			20		V
HI-Side Overvoltage Lockout Response Time	t_{HI_OVLO}			100		µs
HI-Side Undervoltage Lockout Threshold	$V_{HI\_UVLO–}$		**350**	360	**370**	V
HI-Side Undervoltage Recovery Threshold	V_{HI_UVLO+}		**370**	380	**399**	V
HI-Side Undervoltage Lockout Hysteresis	$V_{HI\_UVLO\_HYST}$			20		V
HI-Side Undervoltage Lockout Response Time	t_{HI_UVLO}			100		µs
HI-Side Undervoltage Start Up Delay	$t_{HI\_UVLO+\_DELAY}$	From V_{HI_DC} = V_{HI_UVLO+} to powertrain active (i.e., one-time start up delay from application of V_{HI_DC} to V_{LO_DC})		50		ms
LO-Side Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		**42**	50	**70**	A
LO-Side Overcurrent Response Time Constant	$t_{LO\_OUT\_OCP}$	Effective internal RC filter		2		ms
Overtemperature Shutdown Threshold	t_{OTP+}	Internal	**125**			°C
Overtemperature Recovery Threshold	$t_{OTP–}$	Internal	105	110	115	°C
Undertemperature Shutdown Threshold (Internal)	t_{UTP}	C-Grade			–25	°C
		T-Grade			–45	
Undertemperature Restart Time	$t_{UTP\_RESTART}$	Start up into a persistent fault condition. Non-latching fault detection given V_{HI_DC} > V_{HI_UVLO+}		3		s

Operating Area

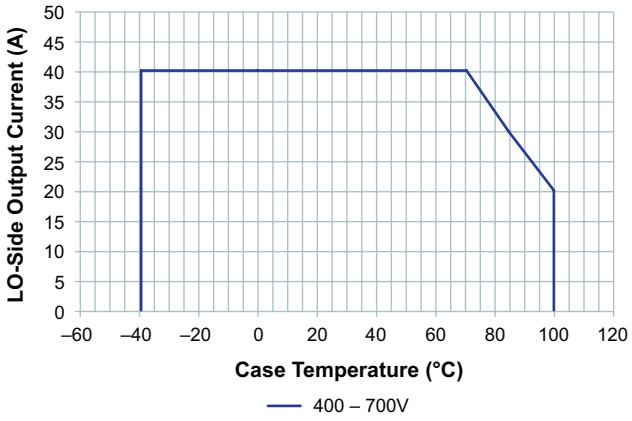


Figure 1 — *Specified thermal operating area*

1. The BCM in a VIA package is cooled through the non-pin-side case.
2. The thermal rating is based on typical measured device efficiency.
3. The case temperature in the graph is the measured temperature of the non-pin-side housing, such that the internal operating temperature does not exceed 125°C.

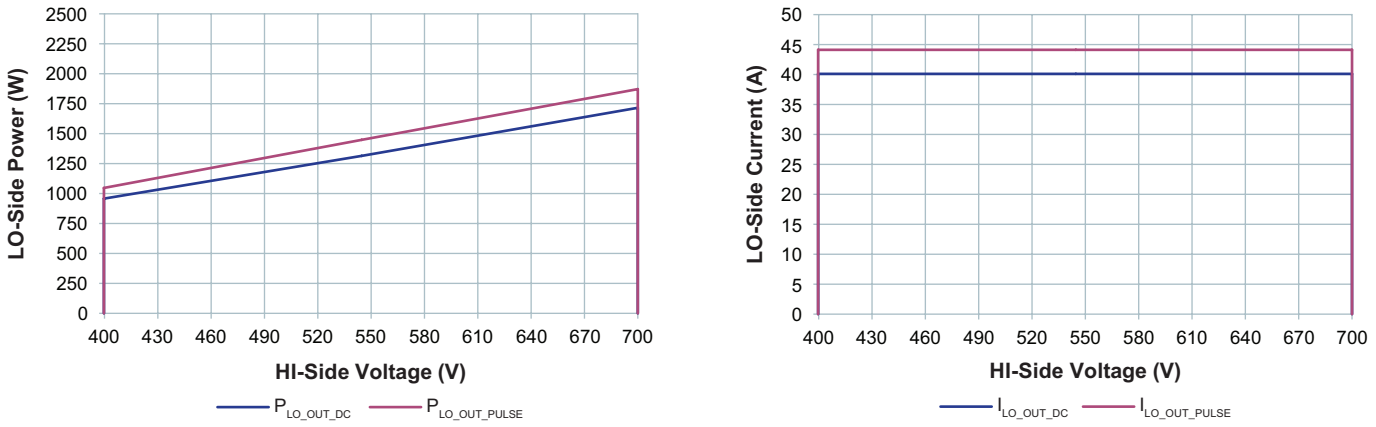


Figure 2 — *Specified electrical operating area using rated R_{LO_HOT}*

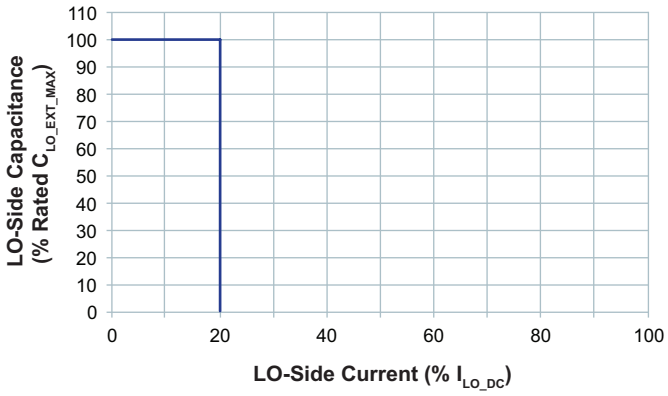


Figure 3 — *Specified HI-side start up into load current and external capacitance*

PMBus™ Reported Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Monitored Telemetry					
• The current telemetry is only available in forward operation. The input and output current reported value is not supported in reverse operation.					
Attribute	**PMBus™ Read Command**	**Accuracy (Rated Range)**	**Functional Reporting Range**	**Update Rate**	**Reported Units**
HI-Side Voltage	(88h) READ_VIN	±5% (LL – HL)	130 to 780V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
HI-Side Current	(89h) READ_IIN	±20% (10 – 20% of FL) ±5% (20 – 133% of FL)	–0.85 to 4.4A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-3}$
LO-Side Voltage [b]	(8Bh) READ_VOUT	±5% (LL – HL)	8.125 to 48.75V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
LO-Side Current	(8Ch) READ_IOUT	±20% (10 – 20% of FL) ±5% (20 – 133% of FL)	–13.6 to 70A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
LO-Side Resistance	(D4h) READ_ROUT	±5% (50 – 100% of FL) at NL ±10% (50 – 100% of FL)(LL – HL)	5 to 40mΩ	100ms	$R_{ACTUAL} = R_{REPORTED} \times 10^{-5}$
Temperature [c]	(8Dh) READ_TEMPERATURE_1	±7°C (Full Range)	–55 to 130°C	100ms	$T_{ACTUAL} = T_{REPORTED}$

[b] Default READ LO Side Voltage returned when unit is disabled = –300V.
[c] Default READ Temperature returned when unit is disabled = –273°C.

Variable Parameters					
• Factory setting of all Thresholds and Warning limits listed below are 100% of specified protection values. • Variables can be written only when module is disabled with $V_{HI} < V_{HI\_UVLO-}$ and external bias (VDDB) applied. • Module must remain in a disabled mode for 3ms after any changes to the variables below to allow sufficient time to commit changes to EEPROM.					
Attribute	**PMBus™ Command**	**Conditions / Notes**	**Accuracy (Rated Range)**	**Functional Reporting Range**	**Default Value**
HI-Side Overvoltage Protection Limit	(55h) VIN_OV_FAULT_LIMIT	V_{HI_OVLO-} is automatically 3% lower than this set point	±5% (LL – HL)	130 – 750V	100%
HI-Side Overvoltage Warning Limit	(57h) VIN_OV_WARN_LIMIT		±5% (LL – HL)	130 – 750V	100%
HI-Side Undervoltage Protection Limit	(D7h) DISABLE_FAULTS	Can only be disabled to a preset default value	±5% (LL – HL)	130 – 400V	100%
HI-Side Overcurrent Protection Limit	(5Bh) IIN_OC_FAULT_LIMIT		±20% (10 – 20% of FL) ±5% (20 – 133% of FL)	0 – 4.4A	100%
HI-Side Overcurrent Warning Limit	(5Dh) IIN_OC_WARN_LIMIT		±20% (10 – 20% of FL) ±5% (20 – 133% of FL)	0 – 4.4A	100%
Overtemperature Protection Limit	(4Fh) OT_FAULT_LIMIT	Internal temperature	±7°C (Full Range)	0 – 125°C	100%
Overtemperature Warning Limit	(51h) OT_WARN_LIMIT	Internal temperature	±7°C (Full Range)	0 – 125°C	100%
Turn On Delay	(60h) TON_DELAY	Additional time delay to the undervoltage start up delay	±50µs	0 – 100ms	0ms

Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted. **Please note:** For chassis mount model, Vicor part number 42550 will be needed for applications requiring the use of the signal pins. Signal cable 42550 is rated up to five insertions and extractions. To avoid unnecessary stress on the connector, the cable should be appropriately strain relieved.

EXT. BIAS (VDDB) Pin

- VDDB powers the internal controller.
- VDDB needs to be applied to enable and disable the BCM through PMBus™ control (using OPERATION COMMAND), and to adjust warning and protection thresholds.
- VDDB voltage not required for telemetry; however, if VDDB is not applied, telemetry information will be lost when V_{IN} is removed.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
INPUT	Regular Operation	VDDB Voltage	V_{VDDB}		4.5	5	9	V
		VDDB Current Consumption	I_{VDDB}				50	mA
	Start Up	Inrush Current Peak	I_{VDDB_INR}	V_{VDDB} slew rate = 1V/µs		3.5		A
		Turn-On Time	t_{VDDB_ON}	From V_{VDDB_MIN} to PMBus active		1.5		ms

SGND Pin

- All PMBus interface signals (SCL, SDA, ADDR) are referenced to SGND pin.
- SGND pin also serves as return pin (ground pin) for VDDB.
- Keep SGND signal separated from the low-voltage side power return terminal (–LO) in electrical design.

Address (ADDR) Pin

- This pin programs the address using a resistor between ADDR pin and signal ground.
- The address is sampled during start up and is stored until power is reset. This pin programs only a Fixed and Persistent address.
- This pin has an internal 10kΩ pullup resistor to 3.3V.
- 16 addresses are available. The range of each address is 206.25mV (total range for all 16 addresses is 0 – 3.3V).

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
MULTI–LEVEL INPUT	Regular Operation	ADDR Input Voltage	V_{SADDR}	See address section	0		3.3	V
		ADDR Leakage Current	I_{SADDR}	Leakage current			1	µA
	Start Up	ADDR Registration Time	t_{SADDR}	From V_{VDDB_MIN}		1		ms

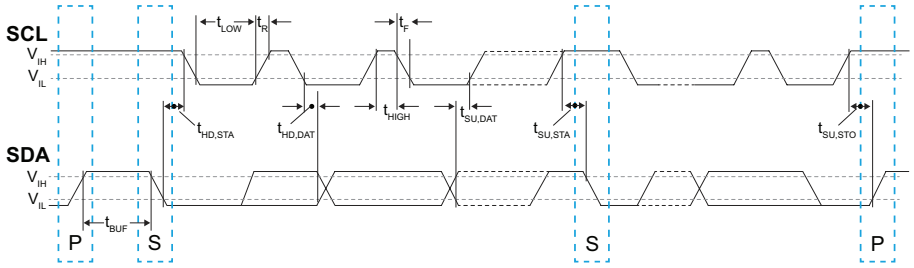
Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted. **Please note:** For chassis mount model, Vicor part number 42550 will be needed for applications requiring the use of the signal pins. Signal cable 42550 is rated up to five insertions and extractions. To avoid unnecessary stress on the connector, the cable should be appropriately strain relieved.

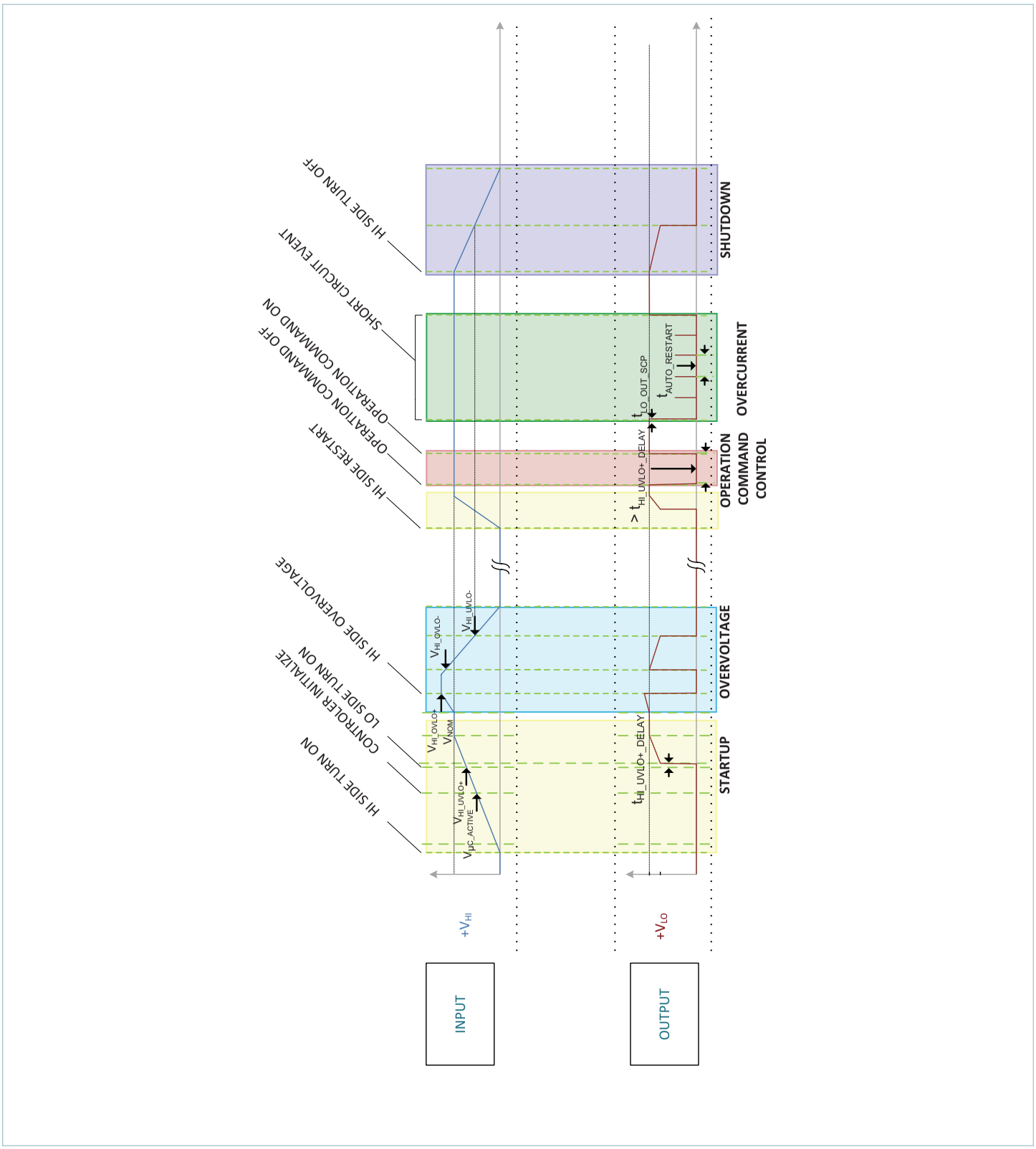
Serial Clock input (SCL) AND Serial Data (SDA) Pins

- High-power SMBus specification and SMBus physical layer compatible. Note that optional SMBALERT# is not supported.
- PMBus™ command compatible.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
DIGITAL INPUT/OUTPUT	Regular Operation	**Electrical Parameters**						
		Input Voltage Threshold	V_{IH}		2.1			V
			V_{IL}				0.8	V
		Output Voltage Threshold	V_{OH}		3			V
			V_{OL}				0.4	V
		Leakage Current	I_{LEAK_PIN}	Unpowered device			10	µA
		Signal Sink Current	I_{LOAD}	V_{OL} = 0.4V	4			mA
		Signal Capacitive Load	C_I	Total capacitive load of one device pin			10	pF
		Signal Noise Immunity	V_{NOISE_PP}	10 – 100MHz	300			mV
		Timing Parameters						
		Operating Frequency	F_{SMB}	Idle state = 0Hz	10		400	kHz
		Free Time Between Stop and Start Condition	t_{BUF}		1.3			µs
		Hold Time After Start or Repeated Start Condition	$t_{HD:STA}$	First clock is generated after this hold time	0.6			µs
		Repeat Start Condition Set-Up Time	$t_{SU:STA}$		0.6			µs
		Stop Condition Set-Up Time	$t_{SU:STO}$		0.6			µs
		Data Hold Time	$t_{HD:DAT}$		300			ns
		Data Set-Up Time	$t_{SU:DAT}$		100			ns
		Clock Low Timeout	$t_{TIMEOUT}$		25		35	ms
		Clock Low Period	t_{LOW}		1.3			µs
		Clock High Period	t_{HIGH}		0.6		50	µs
		Cumulative Clock Low Extend Time	$t_{LOW:SEXT}$				25	ms
		Clock or Data Fall Time	t_F		20		300	ns
		Clock or Data Rise Time	t_R		20		300	ns



Timing Diagram (Forward Direction)



Application Characteristics

Temperature controlled via pin-side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (high-voltage side to low-voltage side). See associated figures for general trend data.

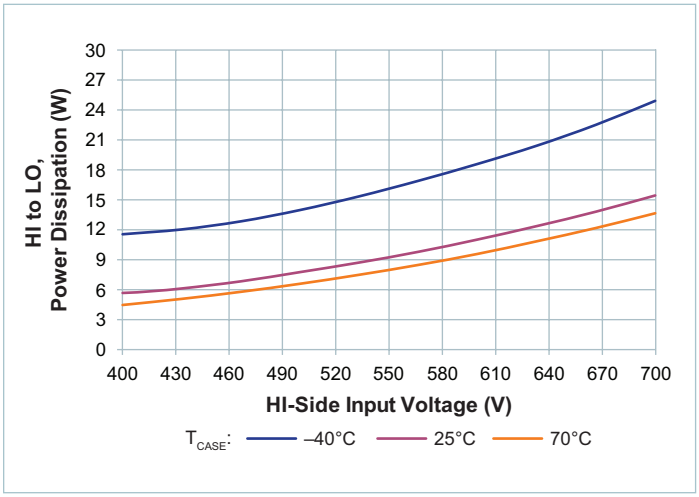


Figure 4 — *No-load power dissipation vs. V_{HI_DC}*

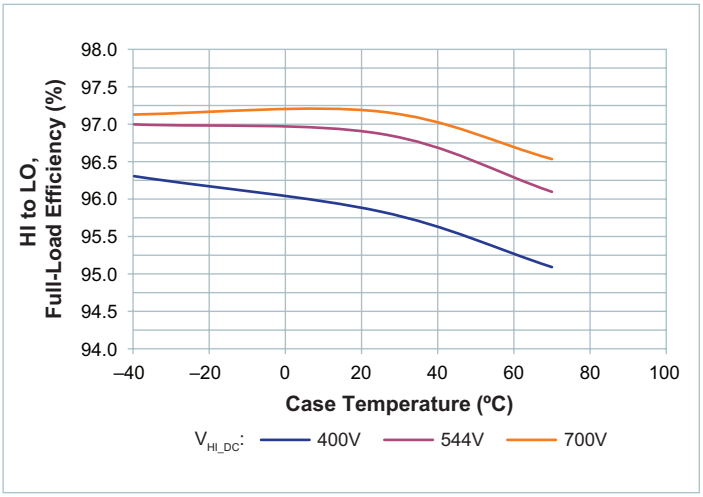


Figure 5 — *Full-load efficiency vs. temperature*

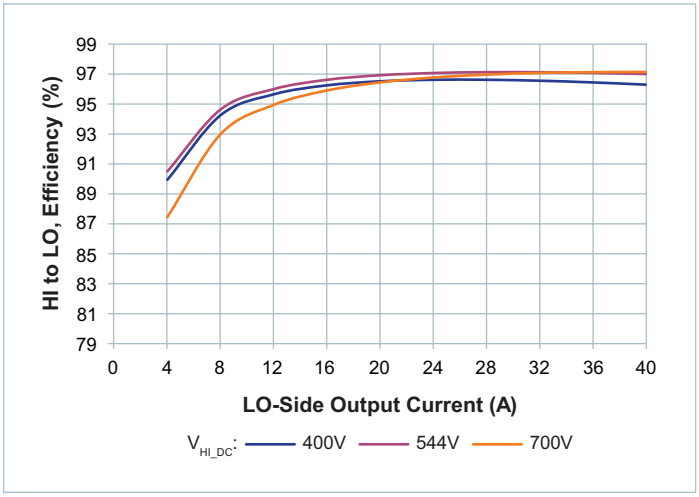


Figure 6 — *Efficiency at T_{CASE} = –40°C*

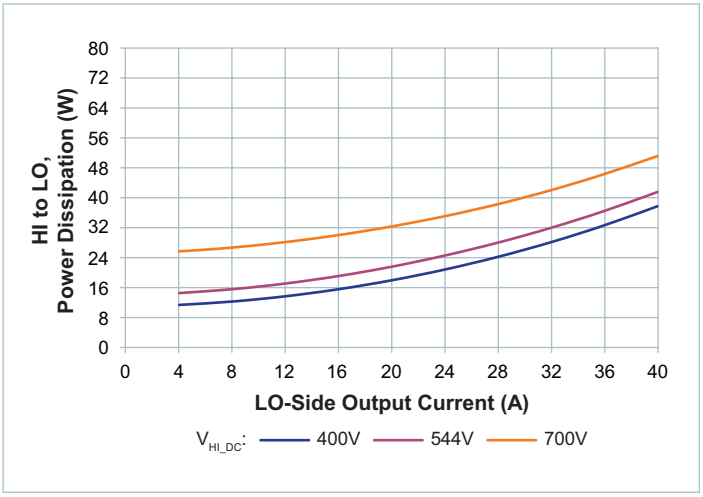


Figure 7 — *Power dissipation at T_{CASE} = –40°C*

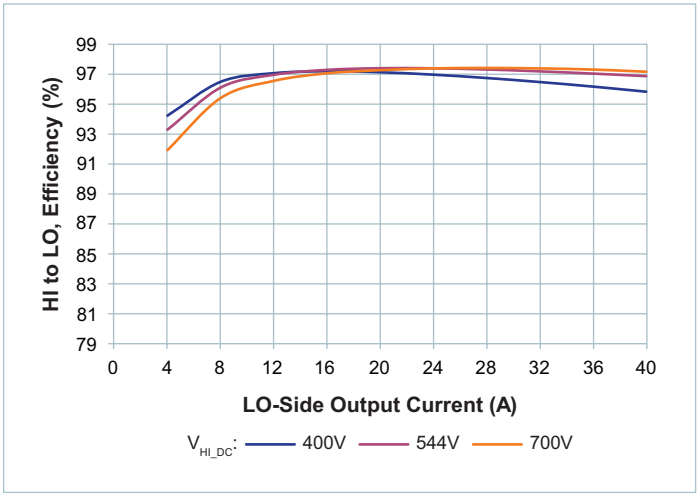


Figure 8 — *Efficiency at T_{CASE} = 25°C*

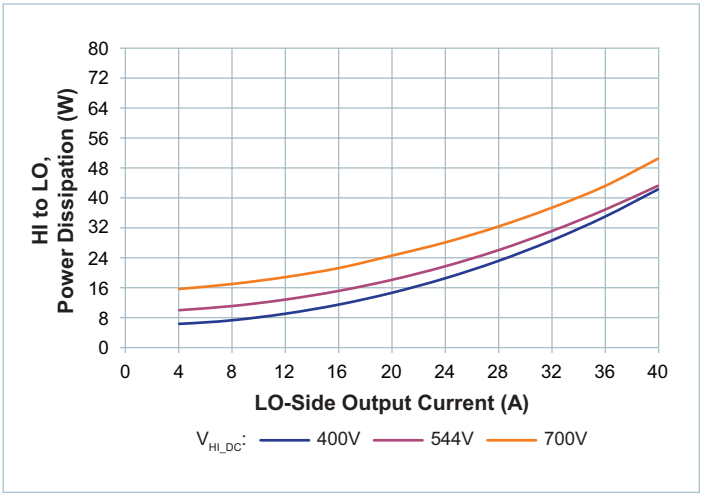


Figure 9 — *Power dissipation at T_{CASE} = 25°C*

Application Characteristics (Cont.)

Temperature controlled via pin-side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (high-voltage side to low-voltage side). See associated figures for general trend data.

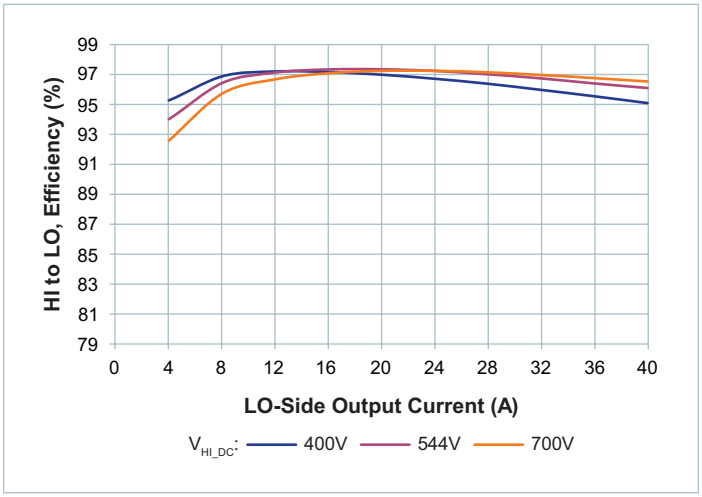


Figure 10 — *Efficiency at T_{CASE} = 70°C*

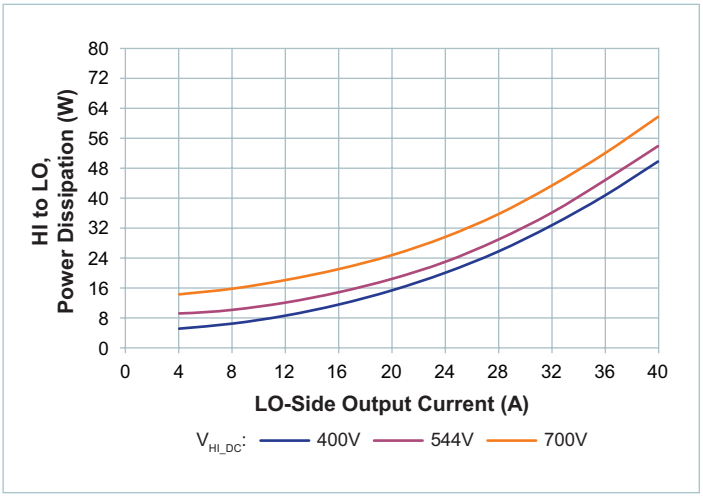


Figure 11 — *Power dissipation at T_{CASE} = 70°C*

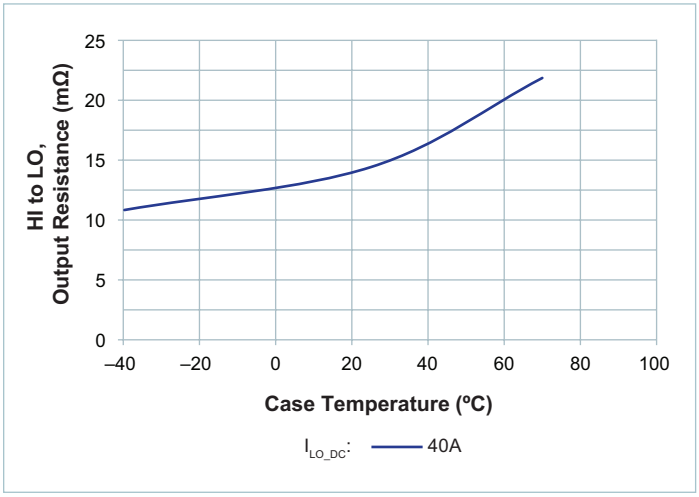


Figure 12 — *R_{LO} vs. temperature; nominal V_{HI_DC} I_{LO_DC} = 40A at T_{CASE} = 70°C*

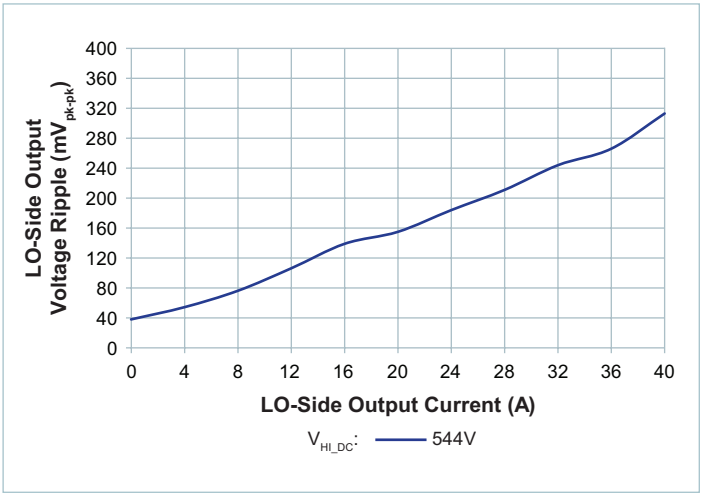


Figure 13 — *$V_{LO\_OUT\_PP}$ vs. I_{LO_DC} ; no external $C_{LO\_OUT\_EXT}$. Board-mounted module, scope setting: 20MHz analog BW*

Application Characteristics (Cont.)

Temperature controlled via pin-side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (high-voltage side to low-voltage side). See associated figures for general trend data.

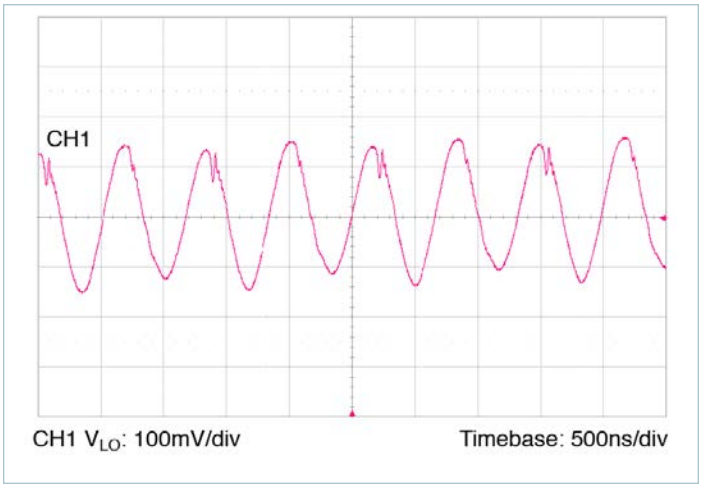


Figure 14 — *Full-load LO-side voltage ripple, no external $C_{HI\_IN\_EXT}$; no external $C_{LO\_OUT\_EXT}$. Board-mounted module, scope setting: 20MHz analog BW*

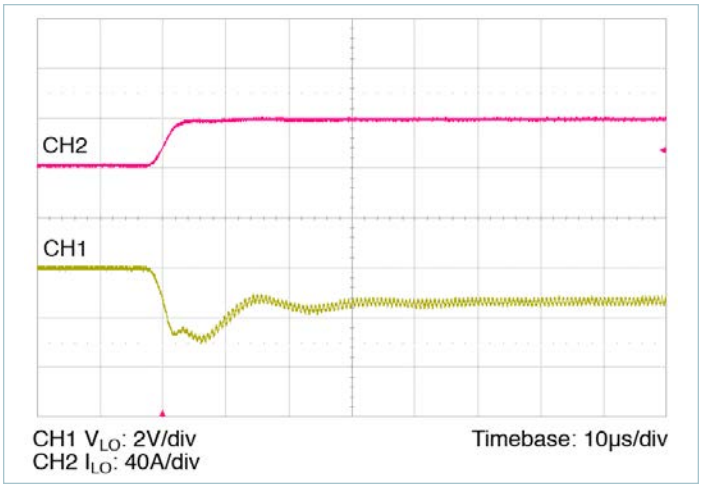


Figure 15 — *0 – 40A transient response: no external $C_{HI\_IN\_EXT}$, no external $C_{LO\_OUT\_EXT}$*

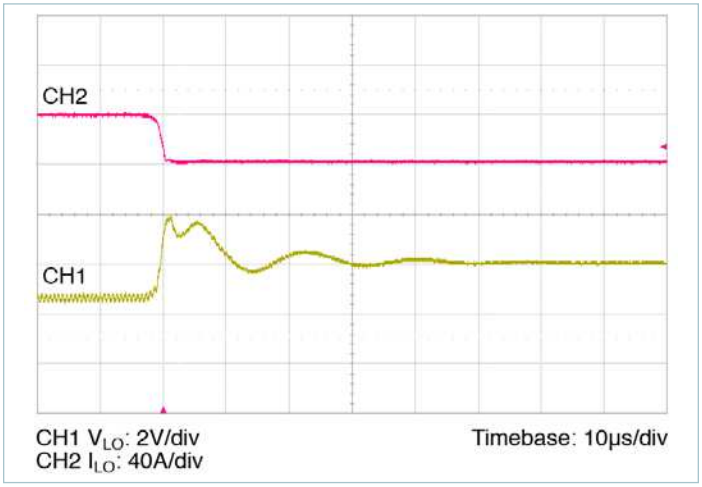


Figure 16 — *40 – 0A transient response: no external $C_{HI\_IN\_EXT}$, no external $C_{LO\_OUT\_EXT}$*

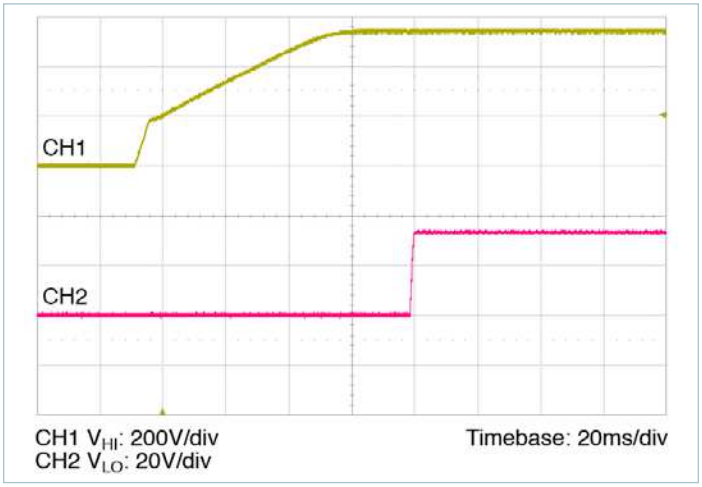


Figure 17 — *Start up from application of V_{HI_DC} = 544V, 20% I_{LO_DC}, 100% $C_{LO\_OUT\_EXT}$*

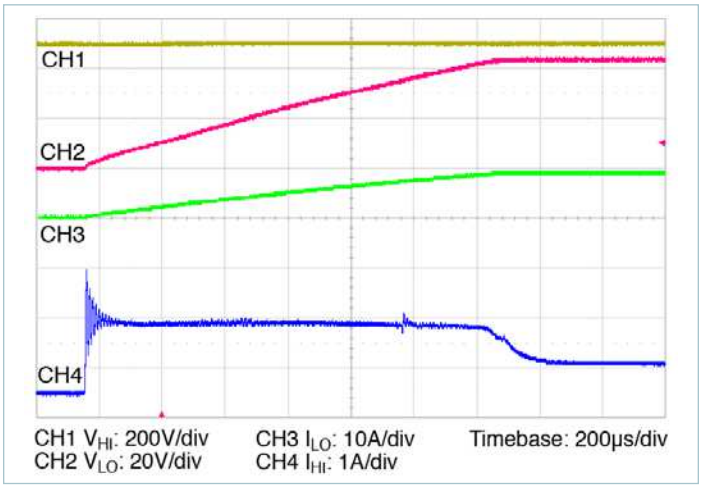


Figure 18 — *Start up from application of OPERATION COMMAND with pre-applied V_{HI_DC} = 700V, 20% I_{LO_DC}, 100% $C_{LO\_OUT\_EXT}$*

General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_{CASE} ≤ 100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L	Lug (Chassis) Mount	110.30 [4.34]	110.55 [4.35]	110.80 [4.36]	mm [in]
Length	L	PCB (Board) Mount	112.51 [4.43]	112.76 [4.44]	113.01 [4.45]	mm [in]
Width	W		35.29 [1.39]	35.54 [1.40]	35.79 [1.41]	mm [in]
Height	H		9.019 [0.355]	9.40 [0.37]	9.781 [0.385]	mm [in]
Volume	Vol	Without heatsink		36.93 [2.25]		cm^3 [in^3]
Weight	W			145 [5.115]		g [oz]
Pin Material		C145 copper				
Underplate		Low-stress ductile Nickel	50		100	µin
Pin Finish (Gold)		Palladium	0.8		6	µin
		Soft Gold	0.12		2	
Pin Finish (Tin)		Whisker-resistant matte Tin	200		400	µin
Thermal						
Operating Internal Temperature	T_{INT}	BCM4414xG0F4440yzz (T-Grade)	–40		125	°C
		BCM4414xG0F4440yzz (C-Grade)	–20		125	
Operating Case Temperature	T_{CASE}	BCM4414xG0F4440yzz (T-Grade), derating applied, see safe thermal operating area	–40		100	
		BCM4414xG0F4440yzz (C-Grade), derating applied, see safe thermal operating area	–20		100	
Thermal Resistance Pin Side	$\theta_{INT\_PIN\_SIDE}$	Estimated thermal resistance to maximum temperature internal component from isothermal pin/ terminal-side housing		1.5		°C/W
Thermal Resistance Housing	θ_{HOU}	Estimated thermal resistance of thermal coupling between the pin-side and non-pin-side case surfaces		0.28		°C/W
Thermal Resistance Non-Pin Side	$\theta_{INT\_NON\_PIN\_SIDE}$	Estimated thermal resistance to maximum temperature internal component from isothermal non-pin/ non-terminal housing		1.6		°C/W
Thermal Capacity				54		Ws/°C
Assembly						
Storage Temperature	T_{ST}	BCM4414xG0F4440yzz (T-Grade)	–40		125	°C
		BCM4414xG0F4440yzz (C-Grade)	–40		125	°C
ESD Withstand	ESD_{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2kV)	1000			
	ESD_{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V)	200			

General Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_{CASE} ≤ 100°C (T-Grade). All other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Safety						
Isolation Capacitance	C_{HI_LO}	Unpowered unit	620	780	940	pF
Isolation Resistance	R_{HI_LO}	At 500V_{DC}	10			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		1.5		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		1.8		MHrs
Agency Approvals / Standards		cTÜVus EN 60950-1				
		cURus UL 60950-1				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

BCM in a VIA Package

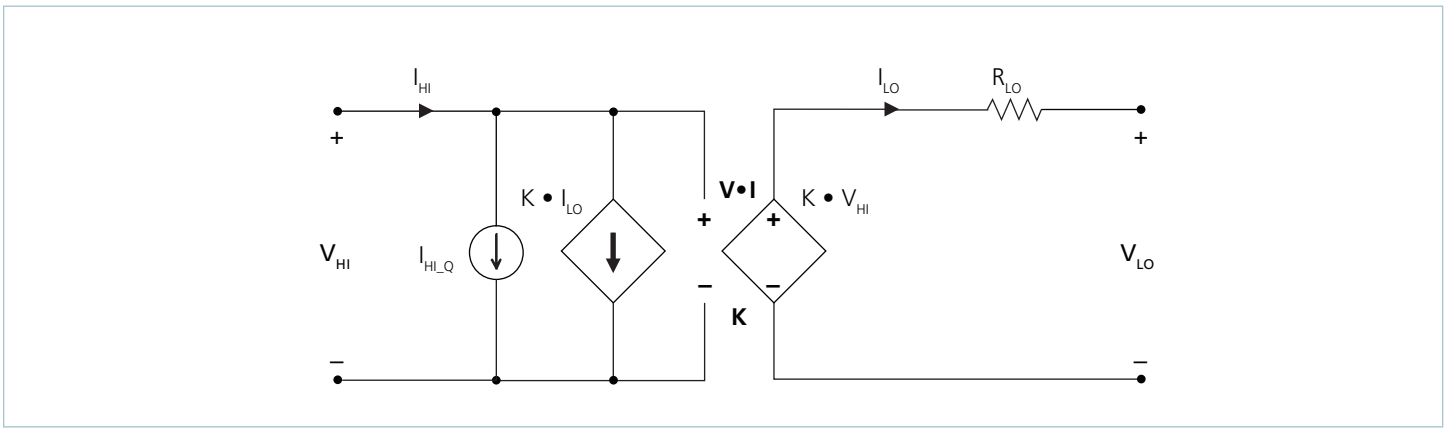


Figure 19 — *BCM DC model (Forward Direction)*

The BCM uses a high-frequency resonant tank to move energy from the high-voltage side to the low-voltage side and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of the HI-side voltage and the LO-side current. A small amount of capacitance embedded in the high-voltage-side and low-voltage-side stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM4414xG0F4440yzz can be simplified into the model shown in Figure 19.

At no load:

$$V_{LO} = V_{HI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the BCM.
Rearranging Equation 1:

$$K = \frac{V_{LO}}{V_{HI}} \qquad (2)$$

In the presence of a load, V_{LO} is represented by:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R_{LO} \qquad (3)$$

and I_{LO} is represented by:

$$I_{LO} = \frac{I_{HI} - I_{HI\_Q}}{K} \qquad (4)$$

R_{LO} represents the impedance of the BCM and is a function of the R_{DS_ON} of the HI-side and LO-side MOSFETs, PC board resistance of HI-side and LO-side boards and the winding resistance of the power transformer. I_{HI_Q} represents the HI-side quiescent current of the BCM controller, gate drive circuitry and core losses.

The effective DC voltage transformer action provides additional interesting attributes. Assuming that R_{LO} = 0Ω and I_{HI_Q} = 0A, Equation 3 now becomes Equation 1 and is essentially load independent, resistor R is now placed in series with V_{HI}.

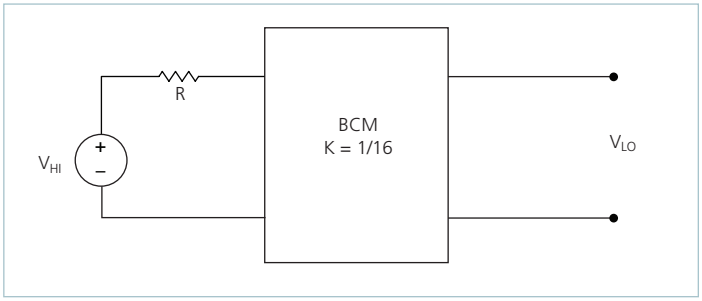


Figure 20 — *K = 1/16 BCM with series HI-side resistor*

The relationship between V_{HI} and V_{LO} becomes:

$$V_{LO} = \left(V_{HI} - I_{HI} \bullet R\right) \bullet K \qquad (5)$$

Substituting the simplified version of Equation 4 (I_{HI_Q} is assumed = 0A) into Equation 5 yields:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Equation 3, where R_{LO} is used to represent the characteristic impedance of the BCM. However, in this case a real resistor, R, on the high-voltage side of the BCM is effectively scaled by K^2 with respect to the low-voltage side.

Assuming that R = 1Ω, the effective R as seen from the low-voltage side is 3.9mΩ, with K = 1/16.

A similar exercise can be performed with the addition of a capacitor or shunt impedance at the high-voltage side of the BCM. A switch in series with V_{HI} is added to the circuit. This is depicted in Figure 21.

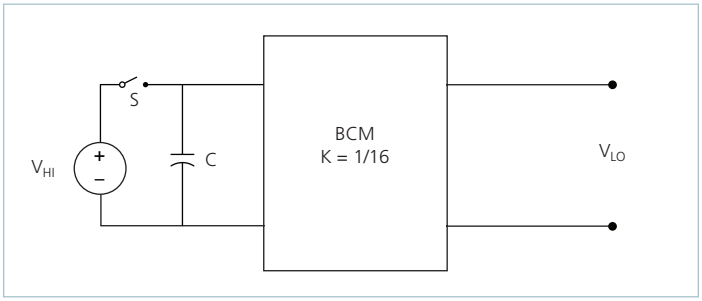


Figure 21 — *BCM with HI-side capacitor*

A change in V_{HI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{HI}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{HI}, the switch is opened and the capacitor is discharged through the idealized BCM. In this case,

$$I_C = I_{LO} \bullet K \qquad (8)$$

substituting Equation 1 and 8 into Equation 7 reveals:

$$I_{LO}(t) = \frac{C}{K^2} \bullet \frac{dV_{LO}}{dt} \qquad (9)$$

The equation in terms of the LO-side has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the low-voltage side when expressed in terms of the high-voltage side. With K = 1/16 as shown in Figure 21, C = 1µF would appear as C = 256µF when viewed from the low-voltage side.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a BCM between the regulation stage and the point-of-load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, these benefits are not achieved if the series impedance of the BCM is too high. The impedance of the BCM must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the BCM low involves switching at a high frequency. This enables the use of small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM module are:

- No-load power dissipation (P_{HI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{LO}}$): refers to the power loss across the BCM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{HI\_NL} + P_{R_{LO}} \qquad (10)$$

Therefore,

$$P_{LO\_OUT} = P_{HI\_IN} - P_{DISSIPATED} = P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{LO\_OUT}}{P_{HI\_IN}} = \frac{P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}}}{P_{HI\_IN}} \qquad (12)$$

$$= \frac{V_{HI} \bullet I_{HI} - P_{HI\_NL} - (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}$$

$$= 1 - \left(\frac{P_{HI\_NL} + (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}\right)$$

Thermal Considerations

The VIA package provides effective conduction cooling from either of the two module surfaces. Heat may be removed from the pin-side surface, the non-pin-side surface or both. The extent to which these two surfaces are cooled is a key component for determining the maximum power that can be processed by a BCM, as can be seen from the specified thermal operating area in Figure 1. Since the BCM has a maximum internal temperature rating, it is necessary to estimate this temperature based on a system-level thermal solution. For this purpose, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 22 shows the "thermal circuit" for the BCM in a VIA package.

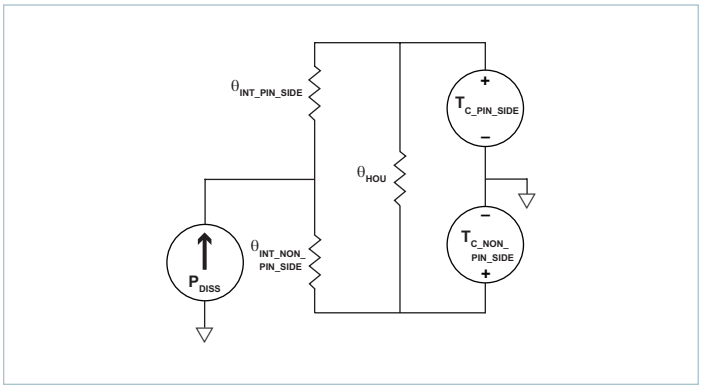


Figure 22 — *Double-sided cooling thermal model*

In this case, the internal power dissipation is P_{DISS}, $\theta_{INT\_PIN\_SIDE}$ and $\theta_{INT\_NON\_PIN\_SIDE}$ are the thermal resistance characteristics of the BCM and the pin-side and non-pin-side surface temperatures are represented as $T_{C\_PIN\_SIDE}$ and $T_{C\_NON\_PIN\_SIDE}$. It is interesting to note that the package itself provides a high degree of thermal coupling between the pin-side and non-pin-side case surfaces (represented in the model by the resistor θ_{HOU}). This feature enables two main options regarding thermal designs:

- Single-side cooling: the model of Figure 22 can be simplified by calculating the parallel resistor network and using one simple thermal resistance number and the internal power dissipation curves; an example for non-pin-side cooling only is shown in Figure 23.

In this case, θ_{INT} can be derived as follows:

$$\theta_{INT} = \frac{\left(\theta_{INT\_PIN\_SIDE} + \theta_{HOU}\right) \bullet \theta_{INT\_NON\_PIN\_SIDE}}{\theta_{INT\_PIN\_SIDE} + \theta_{HOU} + \theta_{INT\_NON\_PIN\_SIDE}} \qquad (13)$$

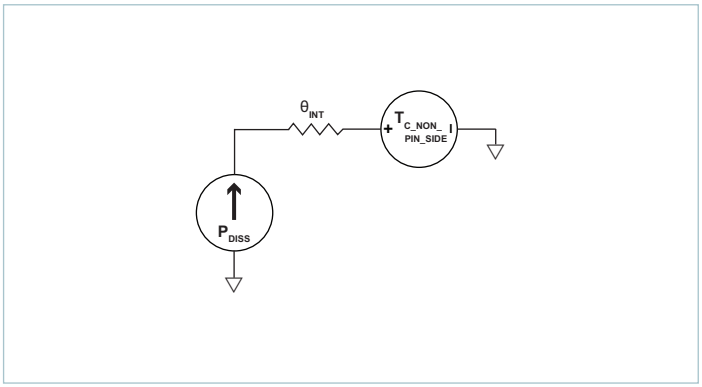


Figure 23 — *Single-sided cooling thermal model*

- Double-side cooling: while this option might bring limited advantage to the module internal components (given the surface-to-surface coupling provided), it might be appealing in cases where the external thermal system requires allocating power to two different elements, such as heat sinks with independent airflows or a combination of chassis/air cooling.

Current Sharing

The performance of the BCM is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point-of-load. Ensuring equal current sharing among modules requires that BCM array impedances be matched.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes/wires within the PCB/Chassis to deliver and return the current to the modules.
- Provide as symmetric a PCB/Wiring layout as possible among modules

For further details see AN:016 Using BCM Bus Converters in High Power Arrays.

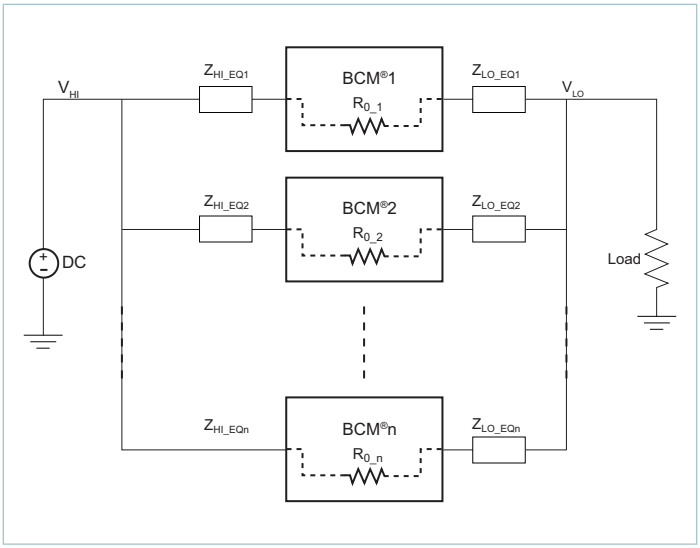


Figure 24 — *BCM module array*

Fuse Selection

In order to provide flexibility in configuring power systems, BCM in a VIA package modules are not internally fused. Input line fusing of BCM products is recommended at the system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of BCM module)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: see safety agency approvals (HI side)

Reverse Operation

BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from the low-voltage side back to the high-voltage side whenever the low side voltage exceeds $V_{HI} \bullet K$. The module will continue operation in this fashion as long as no faults occur.

The BCM4414xG0F4440yzz has not been qualified for continuous operation in a reverse power condition. However, fault protections that help to protect the module in forward operation will also protect the module in reverse operation.

Transient operation in reverse is expected in cases where there is significant energy storage on the low-voltage side and transient voltages appear on the high-voltage side.

Dielectric Withstand

The chassis of the BCM in a VIA package is required to be connected to Protective Earth when installed in the end application and must satisfy the requirements of IEC 60950-1 for Class I products.

Summary

The case is required to be connected to protective earth in the final installation.

The construction of the BCM in a VIA package can be summarized by describing it as a "Class II" component installed in a "Class I" subassembly.

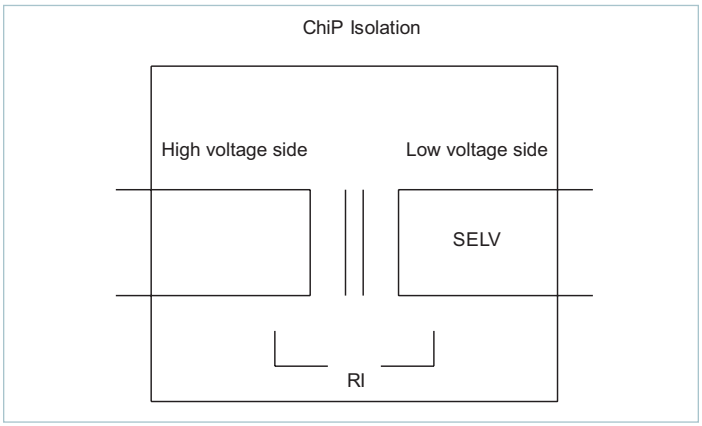


Figure 25 — *BCM in a ChiP™ package before final assembly in the VIA package*

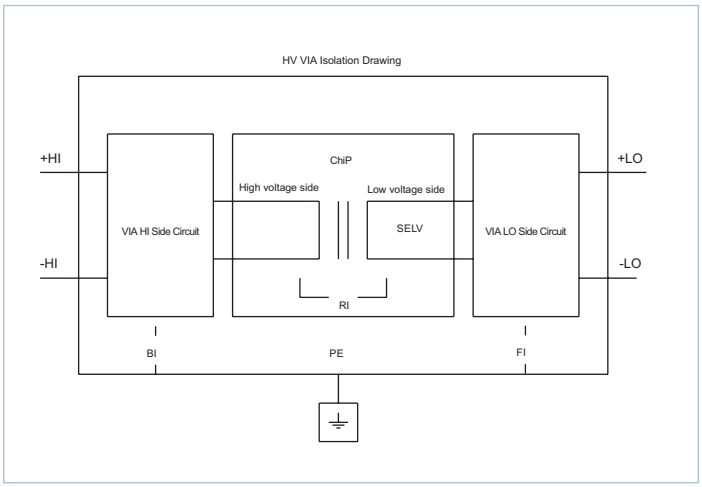


Figure 26 — *BCM in a VIA package after final assembly*

Filtering

The BCM in a VIA package has built-in single stage EMI filtering located on the high-voltage side. The integrated EMI filtering consists of a common mode choke and differential mode capacitors. However, it does not include Y2 capacitors for common mode filtering. Y2 common mode capacitors can be added externally on the high-voltage side between +HI and PE (Case), and –HI and PE (Case) to meet certain EMI requirements. A typical test set-up block diagram for conducted emissions is shown in Figure 27.

The integrated filtering reduces the voltage ripple on the high-voltage side. External LO-side filtering can be added as needed, with ceramic capacitance used as a LO-side bypass for this purpose. BCM HI-side and LO-side voltage ranges shall not be exceeded. An internal overvoltage function prevents operation outside of the normal operating HI-side range. However, the BCM is exposed to the applied voltage even when disabled, and must withstand it. External transient protection circuitry may be required to protect the BCM from overvoltage transients imposed by a system that would exceed maximum ratings.

The source response is generally the limiting factor in the overall system response, given the wide bandwidth of the BCM. Anomalies in the response of the source will appear at the LO side of the module multiplied by its K factor.

Total load capacitance at the LO side of the BCM shall not exceed the specified maximum to ensure correct operation in start up. Due to the wide bandwidth and small LO-side impedance of the BCM, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the HI-side of the BCM.

At frequencies less than 500kHz, the BCM appears as an impedance of R_{LO} between the source and load. Within this frequency range, capacitance connected at the HI side appears as an effective scaled capacitance on the LO side per the relationship defined in Equation 14.

$$C_{LO} = \frac{C_{HI}}{K^2} \qquad (14)$$

This enables a reduction in the size and number of capacitors used in a typical system.

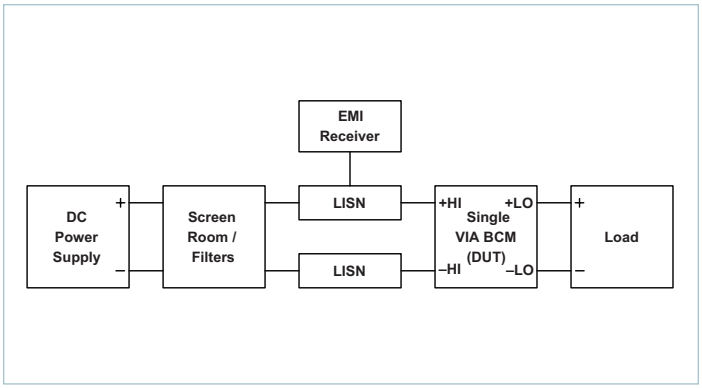
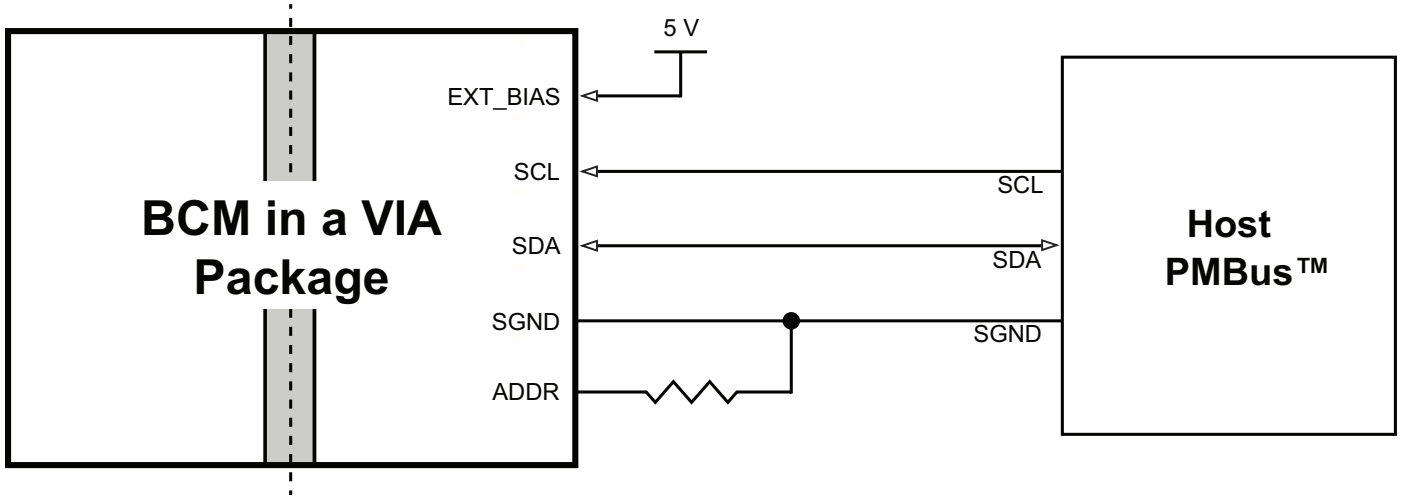


Figure 27 — *Typical test set up block diagram for Conducted Emissions*

System Diagram for PMBus™ Interface



The controller of the BCM in a VIA package is referenced to the low-voltage-side signal ground (SGND).

The BCM in a VIA package provides the Host PMBus system with accurate telemetry monitoring and reporting, threshold and warning limits adjustment, in addition to corresponding status flags. The standalone BCM is periodically polled for status by the host PMBus. Direct communication to the BCM is enabled by a page command. For example, the page (0x00) prior to a telemetry inquiry points to the controller data and page (0x01) prior to a telemetry inquiry points to the BCM parameters.

The BCM enables the PMBus compatible host interface with an operating bus speed of up to 400kHz. The BCM follows the PMBus command structure and specification.

PMBus™ Interface

Refer to "PMBus Power System Management Protocol Specification Revision 1.2, Part I and II" for complete PMBus specifications details at http://pmbus.org.

Device Address

The PMBus address (ADDR Pin) should be set to one of the predetermined 16 possible addresses shown in the table below using a resistor between the ADDR pin and SGND pin.

The BCM accepts only a fixed and persistent address and does not support SMBus address resolution protocol. At initial power-up, the BCM controller will sample the address pin voltage and will keep this address until device power is removed.

ID	Slave Address	HEX	Recommended Resistor R_{ADDR} (Ω)
1	1010 000b	50h	487
2	1010 001b	51h	1050
3	1010 010b	52h	1870
4	1010 011b	53h	2800
5	1010 100b	54h	3920
6	1010 101b	55h	5230
7	1010 110b	56h	6810
8	1010 111b	57h	8870
9	1011 000b	58h	11300
10	1011 001b	59h	14700
11	1011 010b	5Ah	19100
12	1011 011b	5Bh	25500
13	1011 100b	5Ch	35700
14	1011 101b	5Dh	53600
15	1011 110b	5Eh	97600
16	1011 111b	5Fh	316000

Reported DATA Formats

The BCM controller employs a direct data format where all reported measurements are in Volts, Amperes, Degrees Celsius, or Seconds. The host uses the following PMBus specification to interpret received values metric prefixes. Note that the COEFFICIENTS command is not supported:

$$X = \left(\frac{1}{m}\right) \bullet (Y \bullet 10^{-R} - b)$$

Where:

X, is a "real world" value in units (A, V, °C, s)

Y, is a two's complement integer received from the BCM controller

m, b and R are two's complement integers defined as follows:

Command	Code	m	R	b
TON_DELAY	60h	1	3	0
READ_VIN	88h	1	1	0
READ_IIN	89h	1	3	0
READ_VOUT [d]	8Bh	1	1	0
READ_IOUT	8Ch	1	2	0
READ_TEMPERATURE_1 [e]	8Dh	1	0	0
READ_POUT	96h	1	0	0
MFR_VIN_MIN	A0h	1	0	0
MFR_VIN_MAX	A1h	1	0	0
MFR_VOUT_MIN	A4h	1	0	0
MFR_VOUT_MAX	A5h	1	0	0
MFR_IOUT_MAX	A6h	1	0	0
MFR_POUT_MAX	A7h	1	0	0
READ_K_FACTOR	D1h	65536	0	0
READ_BCM_ROUT	D4h	1	5	0

[d] Default READ LO-side voltage returned when BCM unit is disabled = –300V.
[e] Default READ Temperature returned when BCM unit is disabled = –273°C.

No special formatting is required when lowering the supervisory limits and warnings.