Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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BROADCOM®

Connecting everything®

BCM5714C

PRODUCT Brief

PCI EXPRESS®-TO-PCI-X® I/O BRIDGE WITH INTEGRATED DUAL GIGABIT ETHERNET PORTS

FEATURES

- **Dual Gigabit Ethernet (GbE)**
- **PCI Express®-to-PCI-X® bridge**
- **Dual integrated 10BASE-T/100BASE-TX/1000/BASE-T BCM5714C transceivers**
- **Dual 10/100/1000 trispeed media access controllers (MACs)**
- **MACs**
  - Integrated high-speed RISC cores
  - 56 KB receive and 22 KB transmit buffers
  - CPU task offload features (TCP, IP, UDP checksum, and Microsoft® Large Send Offload)
- **TCP segmentation, IP fragmentation, and reassembly**
- **Robust manageability**
  - Preboot execution environment (PXE) 2.0 remote boot
  - Universal Management Port interface for high-speed system management traffic
  - IPMI-compliant server management interface
  - Out-of-Box Wake-on-LAN (OoB WOL)
  - Statistic gathering (SNMP MIB II, Ethernet-like MIB, Ethernet MIB) for 802.3x, clause 30
  - Comprehensive diagnostic and configuration software suite
  - SMBus 2.0 controller
- **Power management, ACPI 1.1a-compliant in multiple power modes**

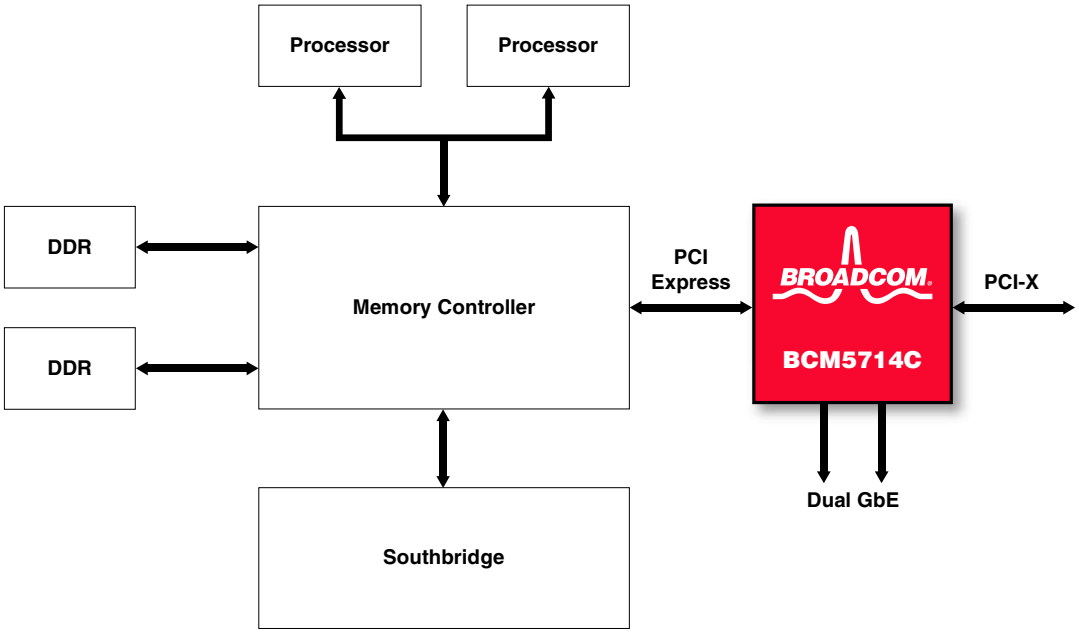
FEATURES (CONT.)

- **Advanced features**
  - Priority queuing—802.1p Layer 2 priority encoding
  - Virtual LANs—802.1q VLAN tagging and support for up to 64 VLANs
  - Jumbo frames (9 KB)
  - 802.3x flow control
  - Link aggregation—802.3ad, GEC/FEC, and Smart Load Balancing™
  - Failover
- **Performance features**
  - CPU task offload
  - Adaptive interrupts
  - PCI-X split transaction
  - Configurable, non-symmetric host interface access
- **484-pin PBGA package**
- **Power**
  - Rails—1.2V core, 2.5V I/O, and 3.3V I/O
  - Peak power dissipation of 5.4W
  - Average power dissipation of 4.6W

APPLICATIONS

- **Highly integrated LAN on Motherboard (LOM) designs**
- **Blade servers**
- **Rack-optimized servers**

OVERVIEW



System Block Diagram

The BCM5714C device is a highly integrated communication and storage bridge for entry-level servers and embedded applications. The primary applications of the BCM5714C are UP and DP servers featuring PCI Express connectivity for I/O expansion.

The BCM5714C provides these key features:

- Dual gigabit NIC ports (MAC and PHY)
- One full 64-bit/133 MHz PCI-X 1.0 bus
- Host interface of PCI Express

The BCM5714C connects to server chip sets with an x4 PCI Express interface and provides an independent PCI-X 1.0 bus for peripheral connectivity. The x4 PCI Express interface is a flexible design and supports x1 and x2 PCI Express connectivity as well. The PCI-X bus is 64 bits wide and runs at 133 MHz.

As an integrated I/O bridge that provides a high-performance data flow path between the PCI Express host interface and the integrated I/O subsystem, the PCI-X bus provides high-performance I/O expansion within the system, while the Gigabit Ethernet interfaces provide high performance network interfaces to the external world. The 64-bit PCI-X bus segment operates at 33 MHz, 66 MHz, 100 MHz, and 133 MHz. The GbE interface represents the fourth generation of Broadcom® server controllers with fully integrated copper transceivers.

The features of the PCI-X bridge include the following:

- Allow concurrency between the PCI Express and the PCI-X buses
- Eight-deep PCI Express-to-PCI-X memory write posting (PCI Express-to-PCI-X transactions)
- Four-deep PCI Express-to-PCI-X non-posted request queue (PCI Express-to-PCI-X transactions)
- Caching with a 16-deep, 32-byte I/O cache for PCI-to-main memory transactions for each PCI bus
- Support write-through caching protocol
- Support up to 14 outstanding split transactions (PCI-X-to-main memory transactions)
- Eight-deep PCI-X-to-PCI Express request queue (PCI-X-to-main memory transactions)
- Parity protection on the PCI-X bus in a conventional PCI and PCI-X mode1
- Optional ECC protection on the PCI-X bus in PCI-X mode1
- Three programmable regions each for PCI-X memory and one region for I/O
- VGA-compatible addressing support
- Multiple I/O APIC support
- Peer-to-peer transfer support
- Integrated PCI-X bus arbitration that supports up to four PCI-X bus masters
- PCI-X bus error reporting
- RAS features

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