Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

BCM8154

PRODUCT Brief

MULTIRATE LOW-POWER 10G NRZ/DUOBINARY TRANSCEIVER WITH 10G CLOCK

FEATURES

- Fully integrated multirate CDR, DEMUX, MUX, CMU
- 300-pin Multisource Agreement (MSA) compatible
- Compliant to ITU GR-253, XFP, and SFP+ specifications
- 16-bit LVDS interface compliant to Optical Internetworking Forum (OIF) SFI-4
- Programmable NRZ/duobinary modes
- RX equalization for ISI compensation
- Limiting amplifier
- RX phase adjustment
- Adaptable RX decision threshold adjustment
- 10G serial transmit clock output with adjustable phase
- 10G serial TX preemphasis
- PRBS generator/checker for built-in self-test (BIST)
- Line and system loopback modes
- Receiver and transmitter serial data polarity inversion
- LVDS polarity inversion and bit order reversal
- Analog loss-of-signal output (ALOSB) and loss-of-signal input (LOSIB)
- CMU and CDR lock detect
- FIFO overflow alarm
- Reference clock: 1/16 or 1/64 of the line data rate
- Selectable RX clock and RX data squelch
- Selectable timing modes/cleanup are field configurable
- Internal phase detector and charge pump for cleanup phase-locked loop (PLL) (external VCXO required)
- Broadcom Serial Control (BSC) interface compatible with Philips® I²C standard
- Optional SPI interface
- Core voltage, 1V
- Low-power: 650 mW

SUMMARY OF BENEFITS

- Compliant to OIF, Telcordia®, ITU-T, XFI specification, and IEEE 802.3ae standards
- Input sensitivity 10 mV peak-to-peak
- Fault isolation with loopbacks, pattern generator, and checker
- Reduces design cycle and time-to-market
- High-level of integration allows for higher port density solutions.
- Lowest power SFI-4 to 10G serial transceiver
- Standard CMOS 65-nm fabrication process

APPLICATIONS

- OC-192/STM-64/10-GbE/FEC transmission equipment
- SONET/SDH/10-GbE/10FC/FEC for NRZ or duobinary optical modules
- ADD/DROP multiplexers
- Digital cross-connects
- ATM switch backbone
- SONET/SDH/10-GbE/10FC/FEC for NRZ, RZ, or duobinary test equipment
- Terabit and edge routers
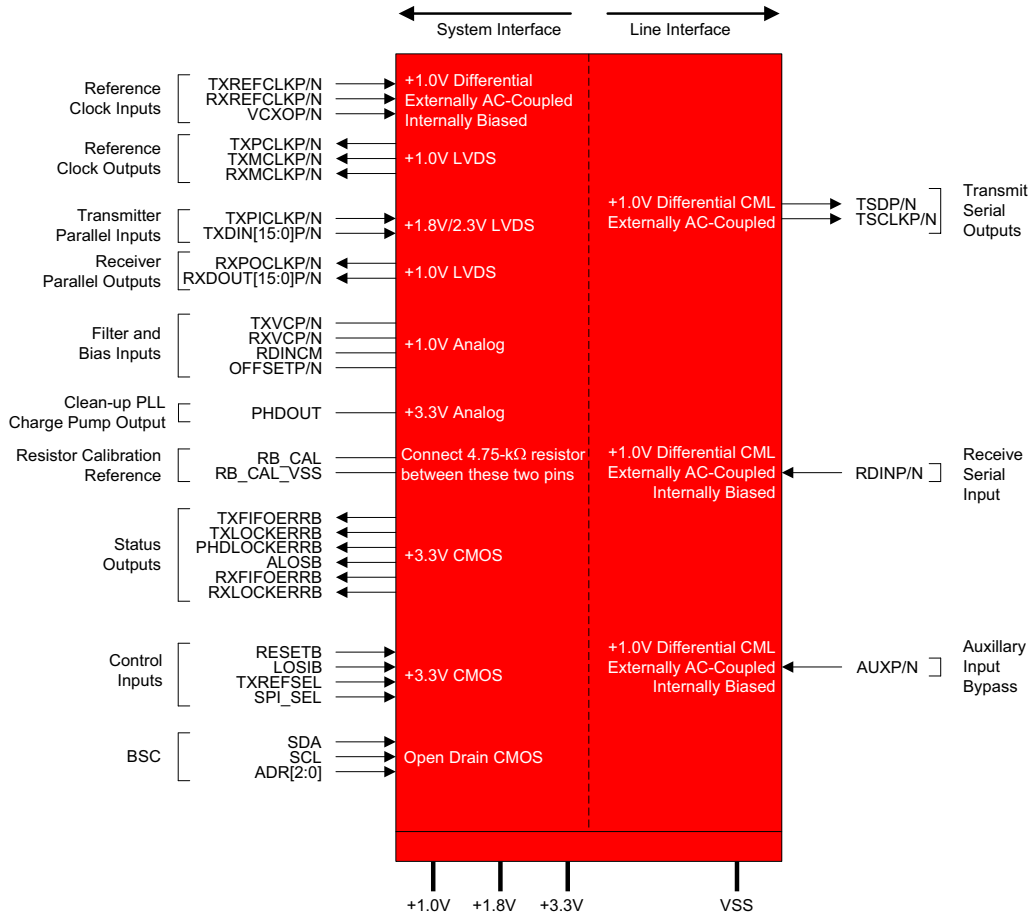
BCM8154 Interface Block Diagram

The BCM8154 is a fully integrated MSA-compatible multirate SONET/SDH/10-GbE/Fibre-Channel/FEC transceiver operating at 9.953 Gbps, 10.3125 Gbps, 10.519 Gbps, 10.664 Gbps, 10.709 Gbps, 11.095 Gbps, 11.318 Gbps, or 11.352 Gbps. On-chip clock synthesis is performed by the high-frequency, low-jitter PLL, allowing the use of a low-frequency reference clock selectable to the line rate divided by either 16 or 64. The 10G TX clock phase is adjustable for clocked driver applications. An on-chip phase detector and charge pump plus external VCXO implement a cleanup PLL. The cleanup PLL can be used to attenuate jitter on the CDR recovered clock for loop timing applications or to provide a low-jitter reference clock from a noisy system clock. Any SONET timing mode may be configured with the new BCM8154 timing architecture, making the timing mode and cleanup functions user-selectable in the field rather than during manufacturing, therefore, simplifying engineering and manufacturing requirements.

New features added to the BCM8154 include:

- PRBS generator/checker for BIST
- Adaptive decision threshold adjustment
- Adjustable 10G TX clock phase
- 10G RX equalization for ISI compensation
- 10G TX preemphasis
- Differential duobinary precoder
- BSC interface (compatible with Philips I^2C standard) or optional SPI interface

The low-jitter LVDS interface guarantees compliance with the bit error rate requirements of the Telcordia (formerly Bellcore), ANSI, and ITU-T standards. The BCM8154 is offered in two different packages:

1. 15 mm x 15 mm, 301-pin BGA compatible with the BCM8152 (0.8-mm ball pitch)
2. 15 mm x 15 mm, 196-pin BGA (1-mm ball pitch)

Connecting
everything®