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## NPN/PNP Silicon Digital Transistor Array

- Switching circuit, inverter, interface circuit, driver circuit
- Two (galvanic) internal isolated NPN/PNP

Transistors in one package

- Built in bias resistor NPN and PNP

$$
\left(R_{1}=10 \mathrm{k} \Omega, R_{2}=10 \mathrm{k} \Omega\right)
$$

- Pb-free (RoHS compliant) package
- Qualified according AEC Q101



## Tape loading orientation




EHAO7193

| Type | Marking | Pin Configuration |  |  |  |  |  | Package |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| BCR10PN | W1s | 1=E1 | 2=B1 | $3=C 2$ | 4=E2 | 5=B2 | 6=C1 | SOT363 |

Maximum Ratings for NPN and PNP Types

| Parameter | Symbol | Value | Unit |
| :--- | :--- | :---: | :--- |
| Collector-emitter voltage | $V_{\mathrm{CEO}}$ | 50 | V |
| Collector-base voltage | $V_{\mathrm{CBO}}$ | 50 |  |
| Input forward voltage | $V_{\mathrm{i}(\mathrm{fwd})}$ | 40 |  |
| Input reverse voltage | $V_{\mathrm{i}(\mathrm{rev})}$ | 10 |  |
| DC collector current | $I_{\mathrm{C}}$ | 100 | mA |
| Total power dissipation, $T_{\mathrm{S}}=115^{\circ} \mathrm{C}$ | $P_{\text {tot }}$ | 250 | mW |
| Junction temperature | $T_{\mathrm{j}}$ | ${ }^{\circ} \mathrm{C}$ |  |
| Storage temperature | $T_{\text {stg }}$ | $-65 \ldots 150$ |  |

Thermal Resistance

| Junction - soldering point ${ }^{1}$ ) | $R_{\text {thJs }}$ | $\leq 140$ | K/W |
| :--- | :--- | :--- | :--- |

[^0]Electrical Characteristics at $T_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise specified

| Parameter | Symbol | Values |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | min. | typ. | max. |  |
| DC Characteristics for NPN and PNP Types |  |  |  |  |  |
| Collector-emitter breakdown voltage $I_{C}=100 \mu \mathrm{~A}, I_{B}=0$ | $V_{(\mathrm{BR}) \mathrm{CEO}}$ | 50 | - | - | V |
| Collector-base breakdown voltage $I_{\mathrm{C}}=10 \mu \mathrm{~A}, I_{\mathrm{E}}=0$ | $V_{(\mathrm{BR}) \mathrm{CBO}}$ | 50 | - | - |  |
| Collector cutoff current $V_{\mathrm{CB}}=40 \mathrm{~V}, I_{\mathrm{E}}=0$ | $I_{\text {CBO }}$ | - | - | 100 | nA |
| Emitter cutoff current $V_{E B}=10 \mathrm{~V}, I_{\mathrm{C}}=0$ | IEBO | - | - | 0.75 | mA |
| DC current gain 1) $I_{\mathrm{C}}=5 \mathrm{~mA}, V_{\mathrm{CE}}=5 \mathrm{~V}$ | $h_{\text {FE }}$ | 30 | - | - | - |
| Collector-emitter saturation voltage1) $I_{\mathrm{C}}=10 \mathrm{~mA}, I_{\mathrm{B}}=0.5 \mathrm{~mA}$ | $V_{\text {CEsat }}$ | - | - | 0.3 | V |
| Input off voltage $I_{C}=100 \mu \mathrm{~A}, V_{\mathrm{CE}}=5 \mathrm{~V}$ | $V_{i(\text { (off })}$ | 0.8 | - | 1.5 |  |
| Input on Voltage $I_{\mathrm{C}}=2 \mathrm{~mA}, V_{\mathrm{CE}}=0.3 \mathrm{~V}$ | $V_{\mathrm{i}(\mathrm{on})}$ | 1 | - | 2.5 |  |
| Input resistor | $R_{1}$ | 7 | 10 | 13 | k $\Omega$ |
| Resistor ratio | $R_{1} / R_{2}$ | 0.9 | 1 | 1.1 | - |

AC Characteristics for NPN and PNP Types

| Transition frequency <br> $I_{\mathrm{C}}=10 \mathrm{~mA}, V_{\mathrm{CE}}=5 \mathrm{~V}, f=100 \mathrm{MHz}$ | $f_{\mathrm{T}}$ | - | 130 | - | MHz |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Collector-base capacitance <br> $V_{\mathrm{CB}}=10 \mathrm{~V}, f=1 \mathrm{MHz}$ | $C_{\mathrm{cb}}$ | - | 3 | - | pF |

1) Pulse test: $\mathrm{t}<300 \mu \mathrm{~s} ; \mathrm{D}<2 \%$

## NPN Type

DC Current Gain $h_{\text {FE }}=f\left(I_{C}\right)$
$V_{C E}=5 \mathrm{~V}$ (common emitter configuration)


Input on Voltage $V_{i(o n)}=f\left(I_{C}\right)$
$V_{C E}=0.3 \mathrm{~V}$ (common emitter configuration)


## Collector-Emitter Saturation Voltage

$V_{\text {CEsat }}=f\left(I_{\mathrm{C}}\right), h_{\text {FE }}=20$


Input off voltage $V_{i(\text { off })}=f\left(I_{\mathrm{C}}\right)$
$V_{C E}=5 \mathrm{~V}$ (common emitter configuration)


## PNP Type

DC Current Gain $h_{\text {FE }}=f\left(I_{\mathrm{C}}\right)$
$V_{C E}=5 \mathrm{~V}$ (common emitter configuration)


Input on Voltage $V_{i(o n)}=f\left(I_{C}\right)$
$V_{C E}=0.3 \mathrm{~V}$ (common emitter configuration)


## Collector-Emitter Saturation Voltage

$V_{\text {CEsat }}=f\left(I_{\mathrm{C}}\right), h_{\text {FE }}=20$


Input off voltage $V_{\mathrm{i}(\text { off })}=f\left(I_{\mathrm{C}}\right)$
$V_{C E}=5 \mathrm{~V}$ (common emitter configuration)


Total power dissipation $P_{\text {tot }}=f\left(T_{\mathrm{S}}\right)$


Permissible Pulse Load $R_{\text {thJS }}=f\left(t_{\mathrm{p}}\right)$


## Package Outline



Foot Print


## Marking Layout (Example)

Small variations in positioning of
Date code, Type code and Manufacture are possible.


## Standard Packing

Reel $\varnothing 180 \mathrm{~mm}=3.000$ Pieces/Reel
Reel $\varnothing 330 \mathrm{~mm}=10.000$ Pieces/Reel
For symmetric types no defined Pin 1 orientation in reel.


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[^0]:    ${ }^{1}$ For calculation of $R_{\text {thJA }}$ please refer to Application Note ANO77 (Thermal Resistance Calculation)

