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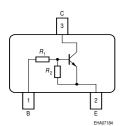


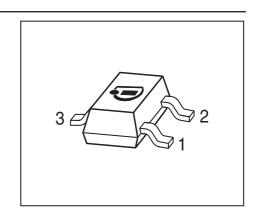
NPN Silicon Digital Transistor

- Built in bias resistor (R_1 = 10 k Ω , R_2 = 10 k Ω)
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101









Туре	Marking	Pin Configuration P			Package
BCR533	XCs	1=B	2=E	3=C	SOT23

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	50	V
Collector-base voltage	V_{CBO}	50	
Input forward voltage	$V_{i(fwd)}$	50	
Input reverse voltage	V _{i(rev)}	10	
Collector current	I _C	500	mA
Total power dissipation-	P _{tot}	330	mW
<i>T</i> _S ≤ 79 °C			
Junction temperature	T _j	150	°C
Storage temperature	$T_{ m stg}$	-65 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾	R _{thJS}	≤ 215	K/W

 $^{^{1}}$ For calculation of R_{thJA} please refer to Application Note AN077 (Thermal Resistance Calculation)



Electrical Characteristics at $T_A = 25$ °C, unless otherwise specified

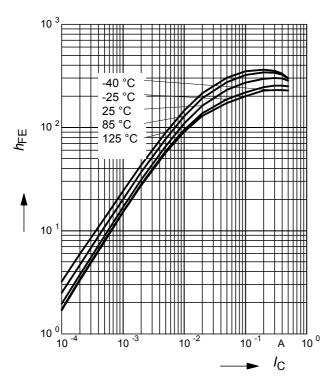
Parameter	Symbol		Values		
		min.	typ.	max.	
DC Characteristics					
Collector-emitter breakdown voltage	V _{(BR)CEO}	50	-	-	V
$I_{\rm C} = 100 \ \mu \text{A}, \ I_{\rm B} = 0$					
Collector-base breakdown voltage	V _{(BR)CBO}	50	-	-	
$I_{\rm C} = 10 \ \mu \text{A}, \ I_{\rm E} = 0$					
Collector-base cutoff current	I _{CBO}	-	-	100	nA
$V_{\rm CB} = 50 \text{ V}, I_{\rm E} = 0$					
Emitter-base cutoff current	I _{EBO}	-	-	0.75	mA
$V_{\rm EB}$ = 10 V, $I_{\rm C}$ = 0					
DC current gain-	h _{FE}	70	-	-	-
$I_{\rm C}$ = 50 mA, $V_{\rm CE}$ = 5 V					
Collector-emitter saturation voltage ¹⁾	V _{CEsat}	-	-	0.3	V
$I_{\rm C}$ = 50 mA, $I_{\rm B}$ = 2.5 mA					
Input off voltage	V _{i(off)}	0.6	-	1.5	
$I_{\rm C}$ = 100 μ A, $V_{\rm CE}$ = 5 V					
Input on voltage	V _{i(on)}	1	-	2.5	
$I_{\rm C}$ = 10 mA, $V_{\rm CE}$ = 0.3 V					
Input resistor	R ₁	7	10	13	kΩ
Resistor ratio	R_1/R_2	0.9	1	1.1	-
AC Characteristics				-	
Transition frequency	f _T	-	100	-	MHz
$I_{\rm C}$ = 50 mA, $V_{\rm CE}$ = 5 V, f = 100 MHz					

 $^{^{1}}$ Pulse test: t < 300 μ s; D < 2%



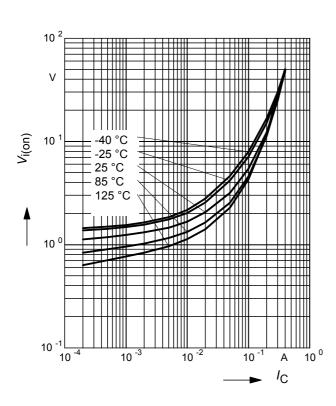
DC current gain $h_{FE} = f(I_C)$

 V_{CE} = 5 V (common emitter configuration)



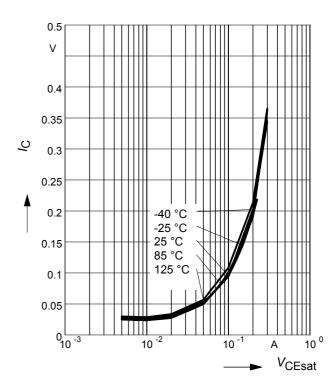
Input on Voltage $Vi_{(On)} = f(I_C)$

 $V_{CE} = 0.3V$ (common emitter configuration)



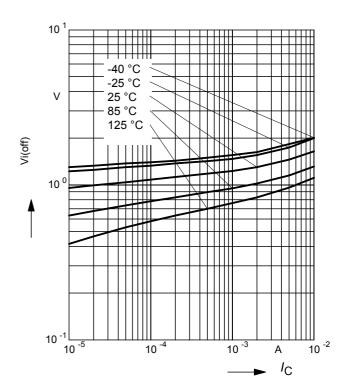
Collector-emitter saturation voltage

 $V_{\text{CEsat}} = f(I_{\text{C}}), h_{\text{FE}} = 20$



Input off voltage $V_{i(off)} = f(I_C)$

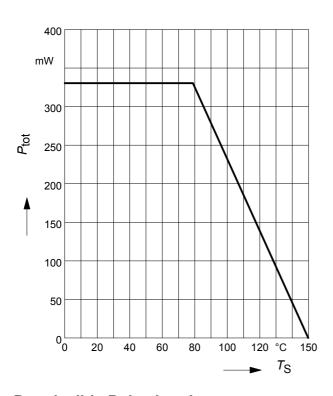
 V_{CE} = 5V (common emitter configuration)

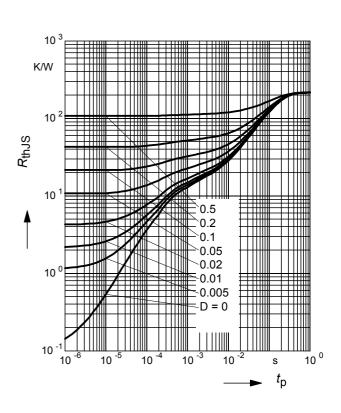




Total power dissipation $P_{tot} = f(T_S)$

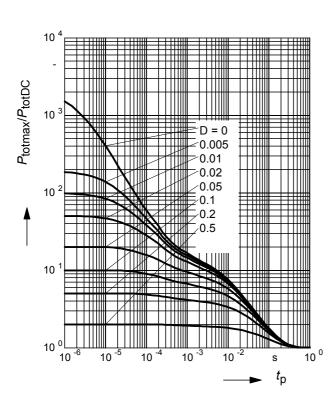
Permissible Pulse Load $R_{thJS} = f(t_p)$





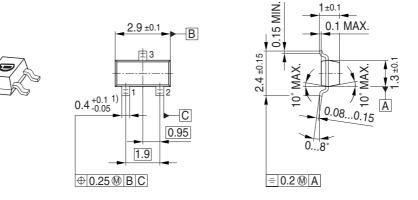
Permissible Pulse Load

$$P_{\text{totmax}}/P_{\text{totDC}} = f(t_{p})$$

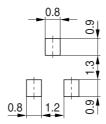




Package Outline

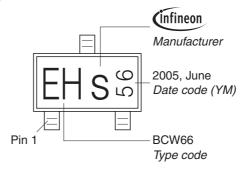


Foot Print



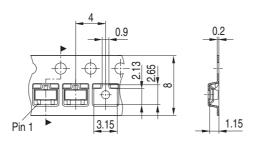
1) Lead width can be 0.6 max. in dambar area

Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel Reel ø330 mm = 10.000 Pieces/Reel





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