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2ch Half-Bridge Gate Driver

BD16952EFV-M

General Description

The BD16952EFV is an AEC-Q100 automotive qualified 2-channel Half-Bridge Gate Driver, controlled by an external MCU through a 16-bit Serial Peripheral Interface (SPI). Independent control of low-side and high-side N-MOSFETS allows for several MCU controlled modes. A programmable drive current is available to adjust slew-rates, in order to meet EMI and power dissipation requirements. Diagnostics can be read and reset by an external MCU.

Features

- AEC-Q100 Qualified(Note1)
- 2ch Half-Bridge Gate Drivers
- 4 external MOSFETs are Controlled Independently
- Half-Bridge Control Modes are Selected by SPI
- Slew Rates are Controlled with Constant Source /Sink Current.
- 500 kHz Oscillation for Charge Pump.
- 16bit SPI

(Note1) Grade1

Applications

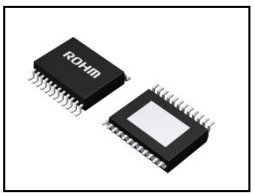
- Power window Lifter, Sun Roof Module, Wiper, Seat Belt Tensioner, Seat Positioning etc.

Key Specifications

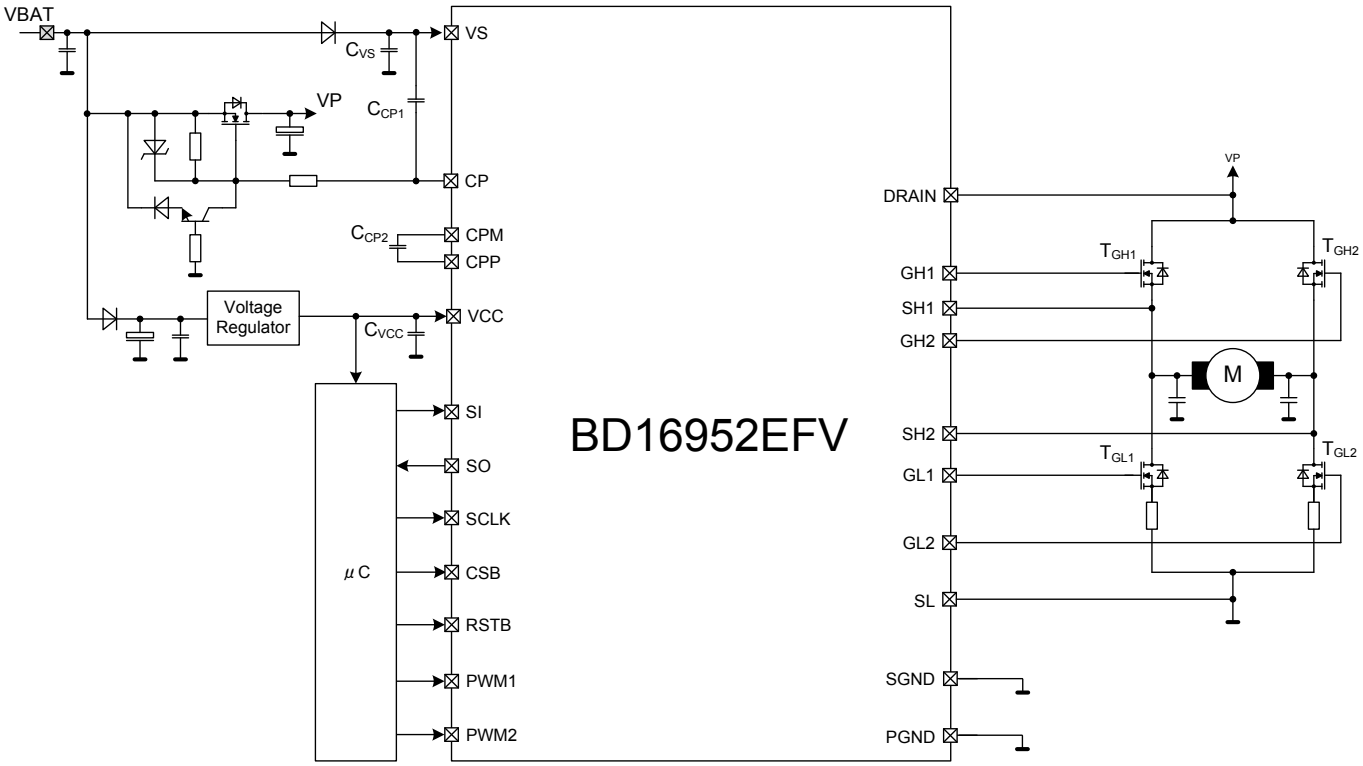
■ Input Voltage VS:	5.5V to 40V
■ Input Voltage VCC:	3.0V to 5.5V
■ Gate Drive Voltage for Half-Bridge:	11V(Typ)
■ VS Quiescent Supply Current:	0μA(Typ)
■ VCC Quiescent Supply Current:	2μA(Typ)
■ Gate Driver Current	1mA to 31mA with 1mA step
■ Cross Current Protection Time	0.25μs to 92μs
■ SPI clock	7MHz (Max)

Package

	W (Typ)	x D (Typ)	x H (Max)
HTSSOP-B24	7.8mm	× 7.6mm	× 1.00mm

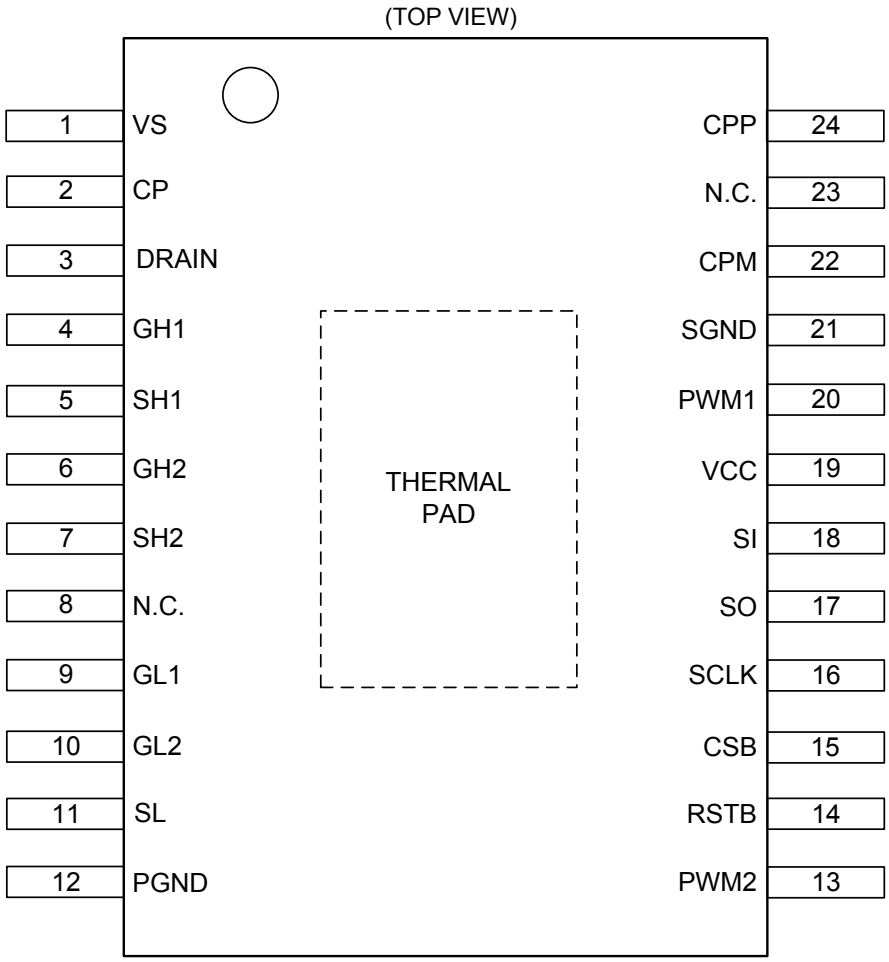


Typical Application Circuit



◯Product structure: Silicon monolithic integrated circuit ◯This product has no designed protection against radioactive rays.

Pin Configuration



Pin Description

Pin No.	Pin Name	Function
1	VS	Power supply terminal used for charge pump and low side driver. A capacitor (C_{VS} =1.0μF (Typ)) is recommended to be located as close as possible to this pin and PGND.
2	CP	Charge pump output. Connect C_{CP1}=0.1μF to VS.
3	DRAIN	High side monitor input from external MOSFET drain for over current and under voltage protection.
4	GH1	Gate driver output to external MOSFET high-side switch in half-bridge. Connect to Gate terminal of high-side external MOSFET.
5	SH1	Source/Drain of half-bridge. Connect to Source / Drain terminal of external MOSFET high/low-side.
6	GH2	Gate driver output to external MOSFET high-side switch in half-bridge. Connect to Gate terminal of high-side external MOSFET.
7	SH2	Source/Drain of half-bridge. Connect to Source / Drain terminal of external MOSFET high/low-side.
8	N.C.	Pin not connected internally.(Note1)
9	GL1	Gate driver output to external MOSFET low-side switch in half-bridge. Connect to Gate terminal of low-side external MOSFET.
10	GL2	Gate driver output to external MOSFET low-side switch in half-bridge. Connect to Gate terminal of low-side external MOSFET.
11	SL	Low-side monitor at external MOSFET Source for over current protection
12	PGND	Power Ground Connector. Connected to Charge pump, High side driver and Low side driver.
13	PWM2	PWM2 input for Half-bridge (GH2 and GL2) control. This input has a pull-down resister.
14	RSTB	Reset input. The Reset input has a pull-down resistor. RSTB=Low will put the BD16952EFV into Reset condition from any state.
15	CSB	Chip Select Bar: this input is low active and requires CMOS logic levels. The serial data transfer between BD16952EFV and MCU is enabled by pulling the input CSB to low-level. This input has a pull-up resister.
16	SCLK	Serial clock input: this input controls the internal shift register of the SPI and requires CMOS logic levels. This input has a pull-down resister.
17	SO	Serial data out: SPI data sent to the MCU by the BD16952EFV. When CSB is High, the pin is in the high-impedance state.
18	SI	Serial data in: the input requires CMOS logic levels and receives serial data from the MCU. The communication is organized in 16bit control words and the most significant bit (MSB) is transferred first. This input has a pull-down resister.
19	VCC	Analog blocks and logic voltage supply 3.3V or 5V : for this input a C_{VCC} =0.1μF (Typ) capacitor as close as possible to SGND is recommended.
20	PWM1	PWM1 input for Half-bridge (GH1 and GL1) control. This input has a pull-down resister.
21	SGND	Ground terminal Connect to THERMAL PAD for heat dissipation. Connected to Logic and analog circuit.
22	CPM	Charge pump pin for capacitor, negative side. Connect C_{CP2} =0.1μF (Typ) to CPP terminal.
23	N.C.	Pin not connected internally.(Note1)
24	CPP	Charge pump pin for capacitor, positive side. Connect C_{CP2} =0.1μF (Typ) to CPM terminal.
THERMAL PAD		THERMAL PAD for heat dissipation. Connect to SGND terminal.

(Note1) Please be sure to floating at N.C. pin.

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may damage the IC. Avoid nearby pins being shorted to each other especially to ground, power supply or output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) or unintentional solder bridge deposited in between pins during assembly.

Selection of Components Externally Connected

Input Capacitor C_{VS}

The input capacitor (C_{VS}) lowers the power supply impedance and averages the input current. The C_{VS} value is selected according to the impedance of the power supply that is used. A ceramic capacitor with a small equivalent series resistance (ESR) should be used. Although the capacitance requirement varies according to the impedance of the power supply that is used as well as the load current value, it is generally in the range of 1.0μF.

Input Capacitor C_{VCC}

The input capacitor (C_{VCC}) lowers the power supply impedance and averages the input current. The C_{VCC} value is selected according to the impedance of the power supply that is used. A ceramic capacitor with a small equivalent series resistance (ESR) should be used. A capacitor value of 0.1μF is recommended.

Charge Pump Capacitor C_{CP1}

The Charge pump capacitor C_{CP1} is required for smoothing the ripple voltage. A capacitor value of 0.1μF is recommended. Using a capacitor with a capacitance lower than 0.1μF, results in a larger ripple voltage. Conversely, using a capacitor with a capacitance greater than 0.1μF results in a larger rush current during start-up, but ripple voltage becomes lower.

Charge Pump Capacitor C_{CP2}

The charge pump capacitor C_{CP2} is required for charging up the voltage. A capacitor value of 0.1μF is recommended. Using a capacitor with a capacitance lower than 0.1μF, results in a larger ripple voltage. Conversely, using a capacitor with a capacitance greater than 0.1μF results in a larger rush current during start-up, but ripple voltage becomes lower.

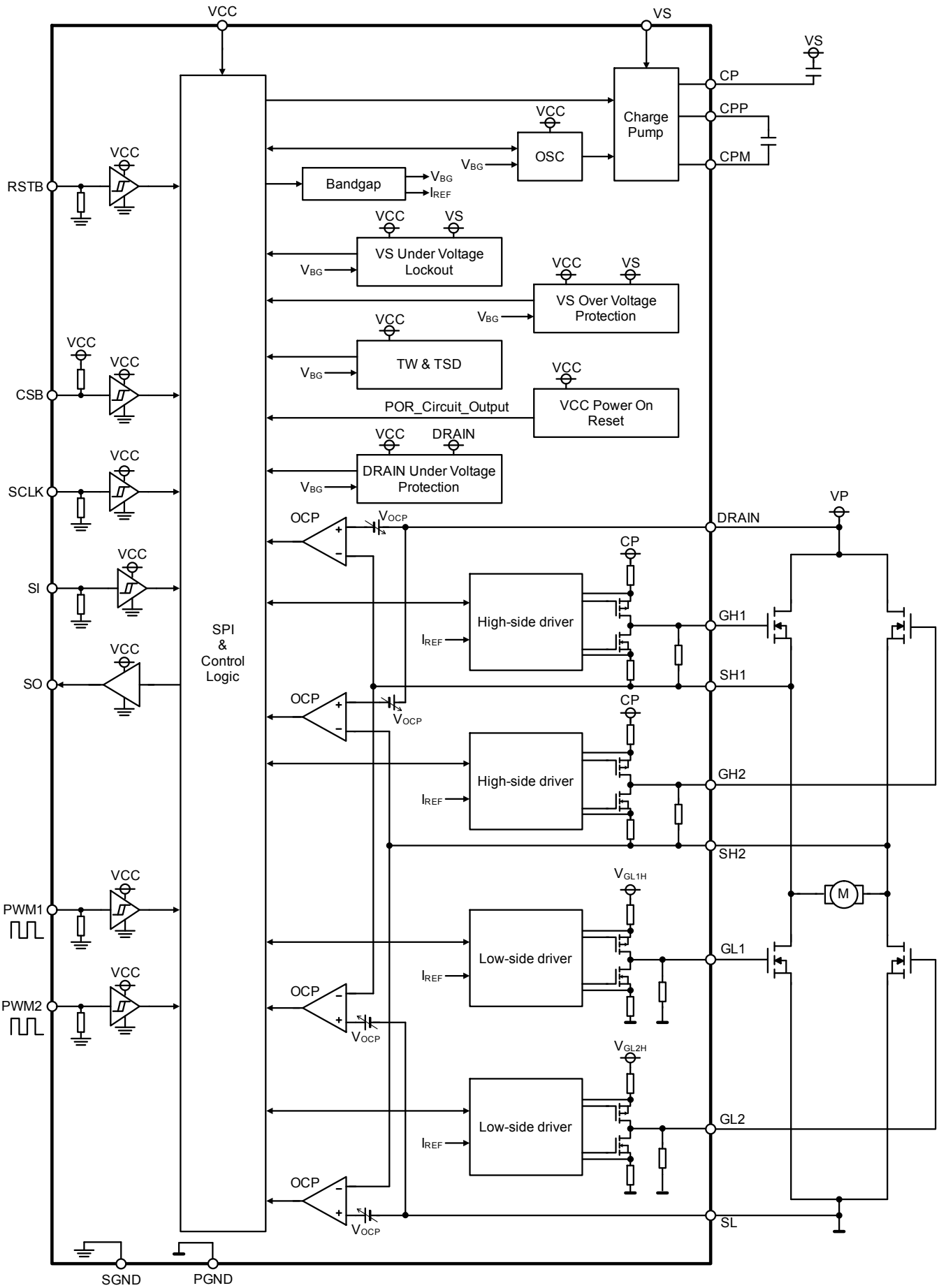
External N-ch MOSFET

BD16952EFV is the gate driver for high side and low side N-channel MOSFETs. Select MOSFETs with the required current capacity to drive the motor and a Gate-Source breakdown voltage ≥ 12V.

External Parts

Symbol	Part
C_{VS}	1.0μF, -/+10%
C_{VCC}	0.1μF, -/+10%
C_{CP1}	0.1μF, -/+10%
C_{CP2}	0.1μF, -/+10%
T_{GH1}, T_{GH2}, T_{GL1}, T_{GL2}	N-Channel MOSFET

Block Diagram



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
VS Voltage	VS	-0.3 to 40	V
VCC Voltage	VCC	-0.3 to 7.0	V
Digital I/O Voltage (SI, SO, SCLK, CSB, RSTB, PWM1, PWM2)	V_{IO}	-0.3 to 7.0	V
CP Voltage	V_{CP}	VS to VS+20	V
CPM Voltage	V_{CPM}	-0.3 to +12V+0.3V (V_{CPM} < VS)	V
CPP Voltage	V_{CPP}	VS to VS+20	V
Gate Voltage for High Side (GH1,GH2)	V_{GH1}, V_{GH2}	-0.3 to 60 (CP-VS < 12V)	V
Gate Voltage for Low Side (GL1,GL2)	V_{GL1}, V_{GL2}	-0.3 to +12V+0.3V (V_{GL1}, V_{GL2} < VS)	V
Bridge output (SH1,SH2)	V_{SH1}, V_{SH2}	-4 to 40	V
Drain Voltage for High Side	V_{DRAIN}	-0.3 to 40	V
Source Voltage for Low Side	V_{SL}	-0.3 to 7.0	V
Operating Temperature Range (Ambient temperature range)	T_{amb}	-40 to 125	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C
Maximum Junction Temperature	T_{jmax}	150	°C
Human Body Model (HBM Global Pin) (Note1)	$V_{ESD,HBM}$	±4	kV
Human Body Model (HBM Local Pin) (Note2)	$V_{ESD,HBM}$	±2	kV
Charged Device Model (CDM Corner Pin) (Note3)	$V_{ESD,CDM}$	±750	V
Charged Device Model (CDM Other Pin) (Note 4)	$V_{ESD,CDM}$	±500	V

(Note 1)Global pins are VS, SH1 and SH2 (A 'global' pin carries signal or power, which enters or leaves the application board).
These voltages are guaranteed by design.
(Note 2)Local pins are except VS, SH1 and SH2 (A 'local' pin carries a signal or power, which does not leave the application board).
These voltages are guaranteed by design.
(Note3)Corner pins are VS, PGND, PWM2 and CPP. These voltages are guaranteed by design.
(Note 4)Other pins are except VS, PGND, PWM2 and CPP. These voltages are guaranteed by design.

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
HTSSOP-B24				
Junction to Ambient	θ_{JA}	143.8	26.4	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	7	2	°C/W

(Note 1)Based on JESD51-2A(Still-Air)
(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4)Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(NOTE 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5)This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage1	VS	5.5	13.5	40	V
Supply Voltage2	VCC	3.0	5	5.5	V
Digital Input Voltage	SI, SCLK, CSB, RSTB, PWM1, PWM2	-0.3	-	VCC	V
Junction Temperature Range	Tj	-40	-	150	°C

Electrical Characteristics

(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Consumption Current						
VS Quiescent Supply Current1 (Reset / Sleep State) (Note 1)	I_{VS_qui1}	-	0	10	μA	0V ≤ VS ≤ V_{s_OVP1} -40 °C ≤ Tj ≤ +105 °C
VS Quiescent Supply Current2 (Reset / Sleep State) (Note 1)	I_{VS_qui2}	-	0	50	μA	0V ≤ VS ≤ V_{s_OVP1} -40 °C ≤ Tj ≤ +150 °C
VS Active Current (Normal State) (Note 1)	I_{VS_act}	-	3.2	6.4	mA	SH1=SH2=PGND CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
VCC Quiescent Supply Current1 (Reset / Sleep State) (Note 1)	$I_{VCC\ qui1}$	-	2	10	μA	V_{CC_POR1} ≤ VCC ≤ 5.5V -40 °C ≤ Tj ≤ +105 °C
VCC Quiescent Supply Current2 (Reset / Sleep state) (Note 1)	$I_{VCC\ qui2}$	-	2	100	μA	V_{CC_POR1} ≤ VCC ≤ 5.5V -40 °C ≤ Tj ≤ +150 °C
VCC Active Current (Normal state) (Note 1)	I_{VCC_act}	-	1.2	2.4	mA	SH1=SH2=PGND CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
Input / Output Terminal						
Input High Voltage(PWM1, PWM2, SI, SCLK, CSB, RSTB)	V_{IH}	VCC x 0.7	-	-	V	
Input Low Voltage(PWM1, PWM2, SI, SCLK, CSB, RSTB)	V_{IL}	-	-	VCC x 0.3	V	
Hysteresis Width	V_{HYS}	-	VCC x 0.1	-	V	
Pull-Down Resistance (PWM1, PWM2, SI, SCLK, RSTB)	R_{In1}	40	100	160	kΩ	
Input Current (PWM1, PWM2, SI, SCLK, RSTB)	I_{IL}	-1	0	-	μA	PWM1, PWM2, SI, SCLK, RSTB=0V
Pull-Up Resistance at CSB	R_{In2}	40	100	160	kΩ	
Input Current at CSB	I_{IH}	-1	0	-	μA	CSB=VCC
Output Voltage High at SO	V_{OH}	VCC x 0.8	-	VCC	V	ISO=-1mA (into the pin)
Output Voltage Low at SO	V_{OL}	-	-	VCC x 0.2	V	ISO=1mA
PWM Frequency Range	f_{PWM}	-	-	25	kHz	
SH1,SH2 Output Current (Reset/Sleep state) (Note 1)	$I_{SH1,2\_LEAK}$	-10	0	-	μA	GH1-SH1,GH2-SH2=0V
SH1, SH2 Outflow Current1 (Normal state) (Note 1)	$I_{SH1,2\_out1}$	-280	-155	-70	μA	GH1=GH2=SH1=SH2=0 EN=CPEN=DRVEN=1 CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
SH1, SH2 Outflow Current2 (Normal state) (Note 1)	$I_{SH1,2\_out2}$	-280	-155	-70	μA	GH1=GH2=SH1=SH2=VS EN=CPEN=DRVEN=1 CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
GH1,GH2 Pull-Down Resistance (Gate-Source Pull-Down Current) (Reset/Sleep State) (Note 1)	$R_{GH1,2\_pulldown}$	6	15	24	kΩ	
SL Output Current (Reset/Sleep State) (Note 1)	$I_{SL1,2\_LEAK}$	-10	0	-	μA	GL1-SL,GL2-SL=0V
GL1,GL2 Pull Down Resistance (Gate-Source Pull-Down Current) (Reset/Sleep State) (Note 1)	$R_{GL1,2\_pulldown}$	6	15	24	kΩ	

(Note 1) Functional statement control is shown on the figure 13.

Electrical Characteristics(continued)
(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Charge Pump						
Output Voltage1 (Normal State) (Note 1)	V_{CP1}	V_S+10	V_S+11	V_S+12	V	VS = 13.5V, I_{CP}=0mA CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
Output Voltage2 (Normal State) (Note 1)	V_{CP2}	V_S+5.0	-	V_S+6.0	V	VS = 6V, I_{CP}=0mA CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
Voltage Drop of Charge Pump1 (Normal State) (Note 1)	V_{CP_Drop1}	-	-	1.0	V	VS = 13.5V, I_{CP}= -10mA CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
Voltage Drop of Charge Pump2 (Normal State) (Note 1)	V_{CP_Drop2}	-	-	0.5	V	VS = 6V, I_{CP}= -2mA CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
Charge Pump Operating Frequency (Normal State) (Note 1)	f_{CP}	400	500	667	kHz	Charge Pump operating frequency is divided by Clock frequency
Clock Frequency (Internal Oscillator)	f_{CLK}	3.20	4.00	5.34	MHz	
CP Input Current (Reset/Sleep State) (Note 1)	I_{CP_LEAK}	-	0	10	μA	EN=0, V_{CP}=25.5V, VS=13.5V

(Note 1) Functional statement control is shown on the figure 13.

Electrical Characteristics(continued)
(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Drivers for External MOSFETs						
Accuracy of Gate Driver Current	ACC_{ISR}	-25	-	+25	%	CUR_SOURCE[4:0]= 00001 to 11111 (Note 1) CUR_SINK[4:0]= 00001 to 11111 (Note 1) 1mA to 31mA setting with 1mA step
Pull Down Current (Note 2) (Reset/Sleep State) (Note 3)	$I_{pulldown}$	83	133	334	µA	GH1=SH1+2V, GH1=SH2+2V GL1=2V, GL2=2V
DNL of Gate Driver Current	ACC_{DNLISR}	-	-	1	LSB	
GH1/GH2 Output High Voltage for High Side(Normal State) (Note 3)	V_{GHxH}	V_S+10	V_S+11	V_S+12	V	VS = 13.5V, Icp=0mA
GL1/GL2 Output High Voltage for Low Side(Normal State) (Note 3)	V_{GLxH}	10	11	12	V	VS = 13.5V
Cross Current Protection Time	t_{CCPT}	-25	-	25	%	CCPT[5:0]=00000 to 111111 0.25µs to 92µs setting
DNL of Cross Current Protection Time	$t_{DNLCCPT}$	-	-	1	LSB	
Synchronization Delay Time (Note 4)	t_{syn}	0.56	-	1.25	µs	
Propagation Delay Time (Note 5)	t_{propa}	100	250	400	ns	SH1=SH2=VS CUR_SOURCE[4:0]=11111 CUR_SINK[4:0]=11111
Output on Resistance	$R_{ds\_on\_gate}$	-	10	20	Ω	Output on resistance CUR_SOURCE[4:0]=11111

(Note 1) High side source current : GH1=SH1, GH2=SH2, Low side source current : GL1=PGND, GL2=PGND
High side sink current : Isink(GH1=GH2=11V, SH1=SH2=PGND) - 15 kΩ pull down current(CPEN=0)
Low side sink current : Isink(GL1=GL2=11V) - 15 kΩ pull down current(CPEN=0)

(Note 2) (External MOSFET's gate driver current) = (Accuracy of gate driver current) – (Pull down current)
e.g. condition : CUR_SOURCE[4:0]=01010(10mA setting),GH1=SH1+2V,
(External MOSFET's gate driver current of GH1) = 10mA(Typ) – 133uA(Typ) = 9.867mA.
Maximum inflow current of pull down resistance is 2mA(12V/6kΩ).GH1/GH2/GL1/GL2 outputs do not rise high voltage in 1mA or 2mA setting.

(Note 3) Functional statement control is shown on the figure 13.

(Note 4) Synchronization delay time : Asynchronous internal delay between PWM signal and high-side or low side of logic signal.
This delay time is guaranteed by design.

(Note 5) Propagation delay time : internal delay between high-side or low side of logic signal and GHx or GLx outputs.
This delay time is guaranteed by design.

Electrical Characteristics(continued)
(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Protection						
UVLO Voltage Rising	V_{S_UVLO1}	4.5	5.0	5.5	V	VS UVLO
Under Voltage Hysteresis	$V_{S\_UV\_hys}$	300	500	700	mV	
OVP Voltage Rising	V_{S_OVP1}	20	22	24	V	VS OVP
Over Voltage Hysteresis	$V_{S\_OVP\_hys}$	0.6	1	1.4	V	
Power On Reset Rising	V_{CC_POR1}	0.75	2.00	2.95	V	VCC POR
Power On Reset Hysteresis	$V_{CC\_POR\_hys}$	0.03	0.1	0.25	V	
Thermal Warning Trigger(Note 1)	T_{TW_TR}	125	137.5	150	ºC	
Thermal Warning Release(Note 1)	T_{TW_RL}	105	117.5	130	ºC	
Thermal Warning Hysteresis(Note1)	T_{TWHYS}	15	20	25	ºC	
Thermal Shut Down Trigger(Note 1)	T_{TSD_TR}	150	175	200	ºC	
Thermal Shut Down Release(Note 1)	T_{TSD_RL}	135	160	185	ºC	
Thermal Shut Down Hysteresis(Note 1)	T_{TSDHYS}	-	15	-	ºC	
DRAIN Quiescent Current (Reset/Sleep State) (Note 1)	I_{DRAIN_qui}	-	-	1	µA	
DRAIN Active Current (Normal State)	I_{DRAIN_act}	-	120	180	µA	
DRAIN Under Voltage Protection Falling	V_{UVP}	4.4	4.9	5.4	V	
OCP Detect Voltage (Drain-SH and SH –SL)	V_{OCP}	-15	-	+15	%	OCPHD[2:0]=000 to 111 OCPLD[2:0]=000 to 111 0.2V, 0.3V, 0.4V, 0.5V, 0.75V, 1.0V, 1.25V and 1.5V setting
OCP Detect FILTER Time	t_{ocp_filter}	-25	-	+25	%	OCP_FILTER[5:0]=000000 to 111111 1µs and 63µs setting with 1µs step
POR Detect Blanking Time	$t_{por\_blanking}$	0.8	2	3.8	µs	
UVLO Detect Blanking Time	$t_{uvlo\_blanking}$	48	64	80	µs	
OVP Detect Blanking Time	$t_{ovp\_blanking}$	48	64	80	µs	

(Note 1) This temperature is guaranteed by design.

Typical Performance Curves (Reference Data)
(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

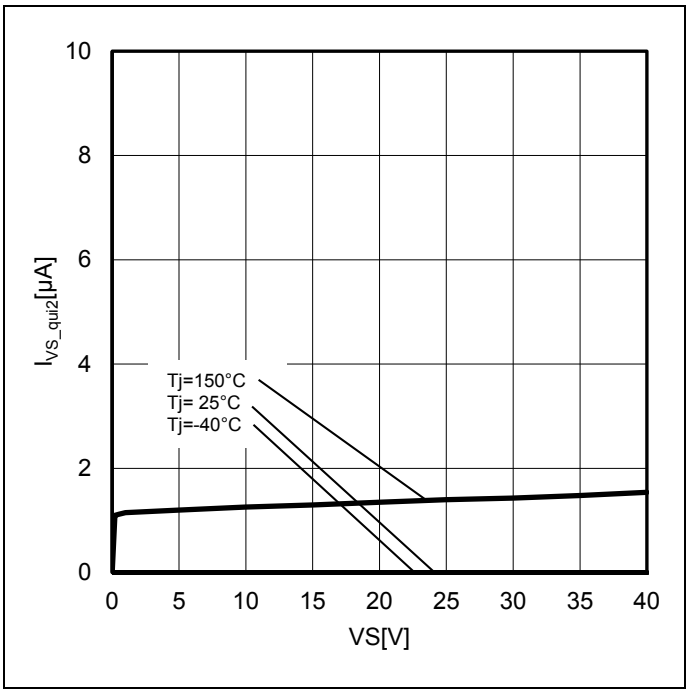


Figure 1. I_{VS_qui2} vs VS (Reset State)
(RSTB=0V)

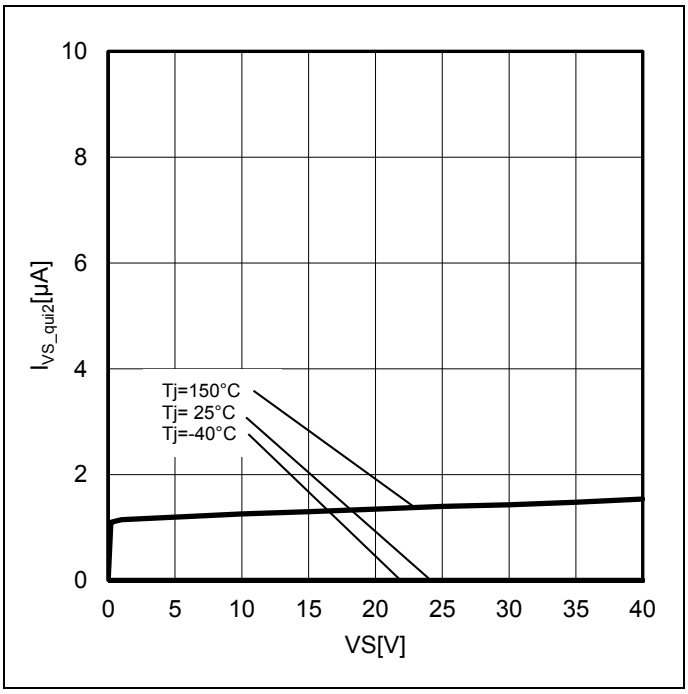


Figure 2. I_{VS_qui2} vs VS (Sleep State)
(RSTB=5V, Enable Register[2:0]=000)

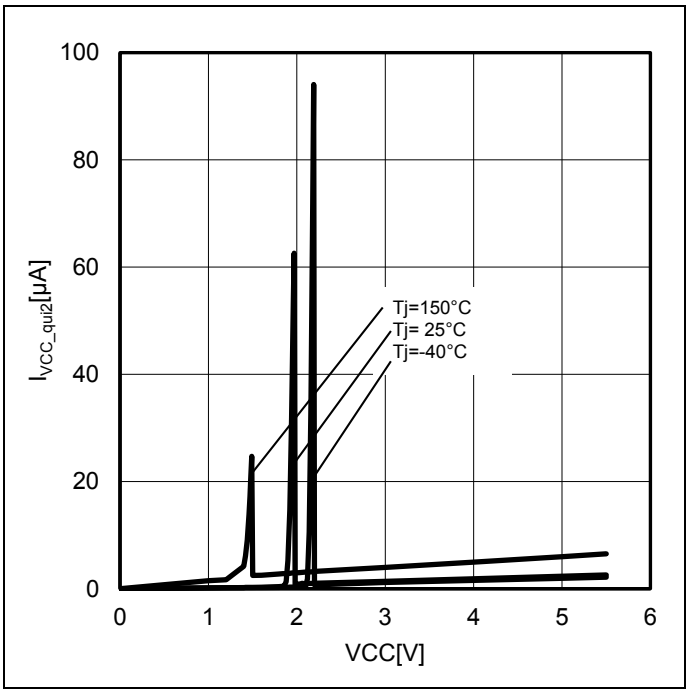


Figure 3. I_{VCC_qui2} vs VCC (Reset State)
(RSTB=0V)

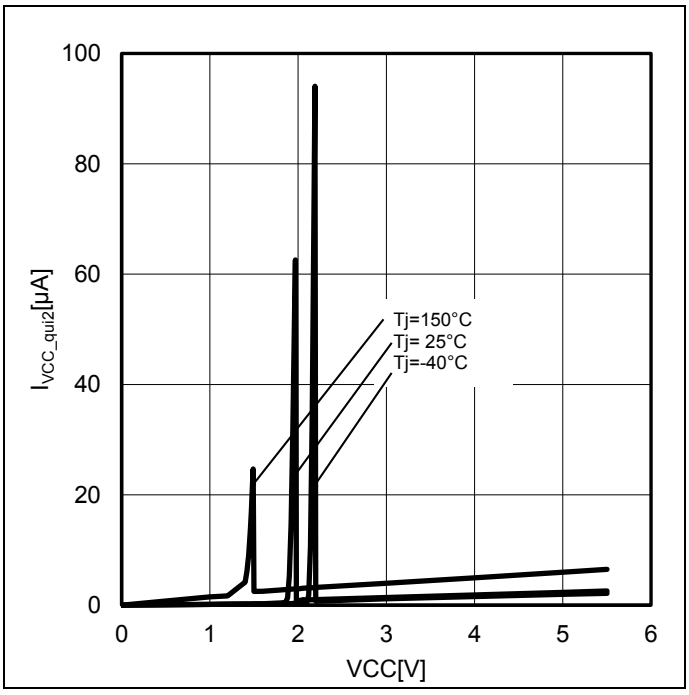


Figure 4. I_{VCC_qui2} vs VCC (Sleep State)
(RSTB=VCC, Enable Register[2:0]=000)

Typical Performance Curves (Reference Data)
(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

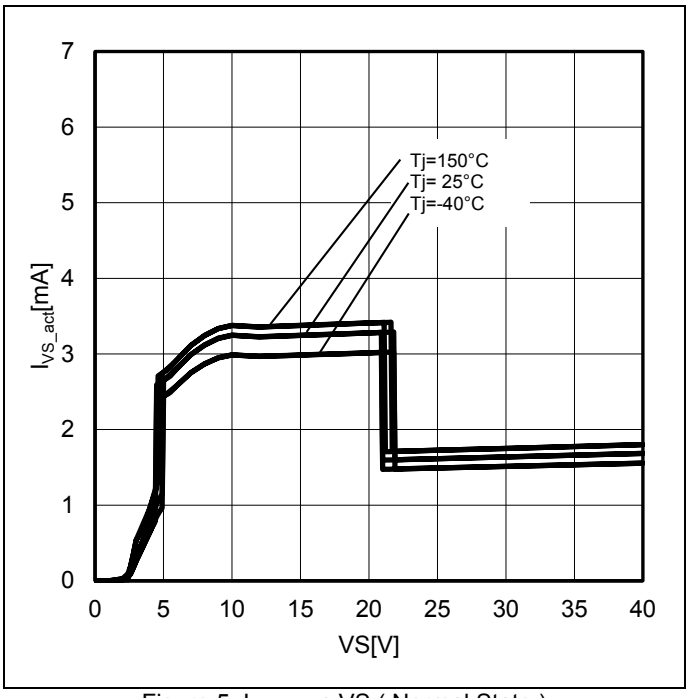


Figure 5. I_{VS_act} vs VS (Normal State)
(RSTB=VCC, SH1=SH2=PGND, Enable Register[2:0]=111,
CUR_SOURCE[4:0]=00000, CUR_SINK[4:0]=00000,
Protection Mode Setting[7:0]=00000000
Other address data is default value)

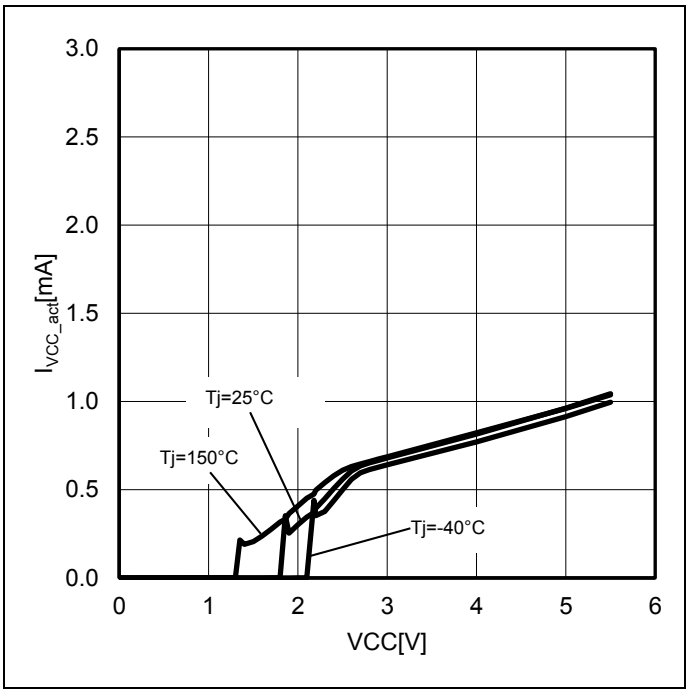


Figure 6. I_{VCC_act} vs VCC (Normal State)
(RSTB=VCC, SH1=SH2=PGND, Enable Register[2:0]=111,
CUR_SOURCE[4:0]=00000, CUR_SINK[4:0]=00000,
Other address data is default value)

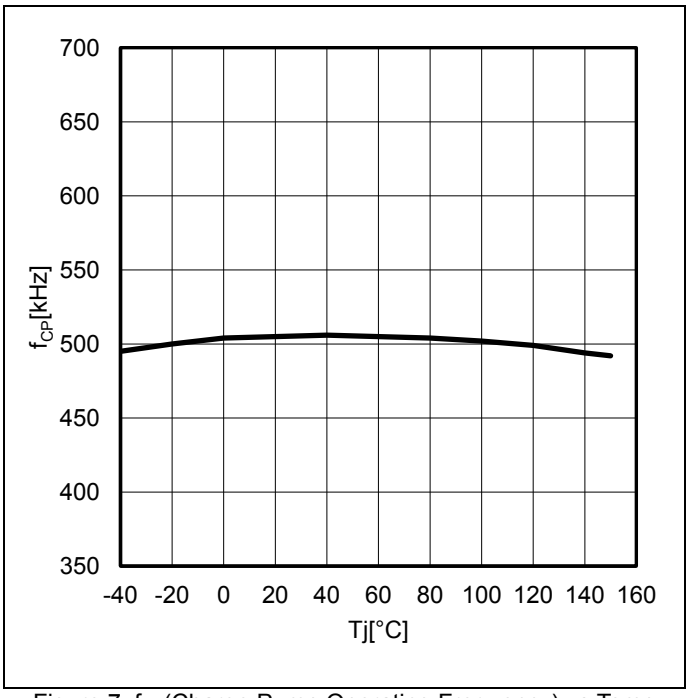


Figure 7. f_{CP}(Charge Pump Operating Frequency) vs Temp
(RSTB=VCC, Enable Register[2:0]=111,
Other address data is default value)

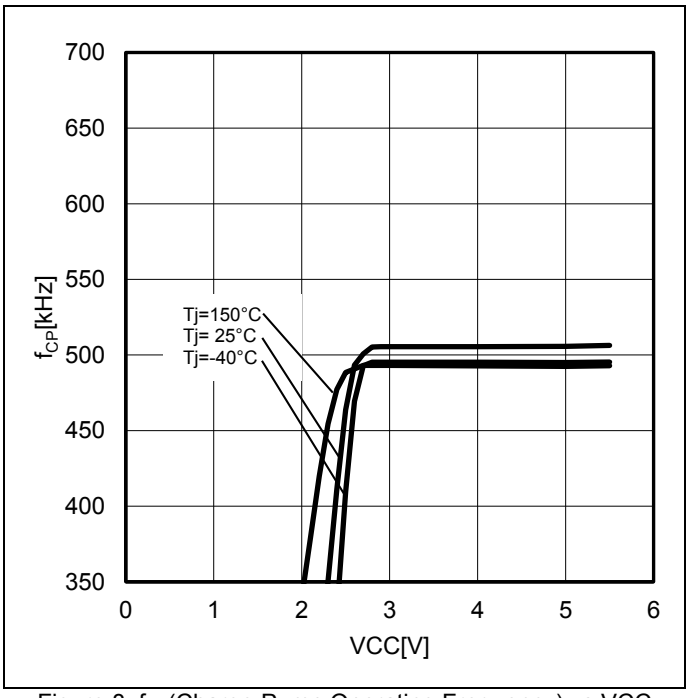


Figure 8. f_{CP}(Charge Pump Operating Frequency) vs VCC
(RSTB=VCC, Enable Register[2:0]=111,
Other address data is default value)

Typical Performance Curves (Reference Data)
(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

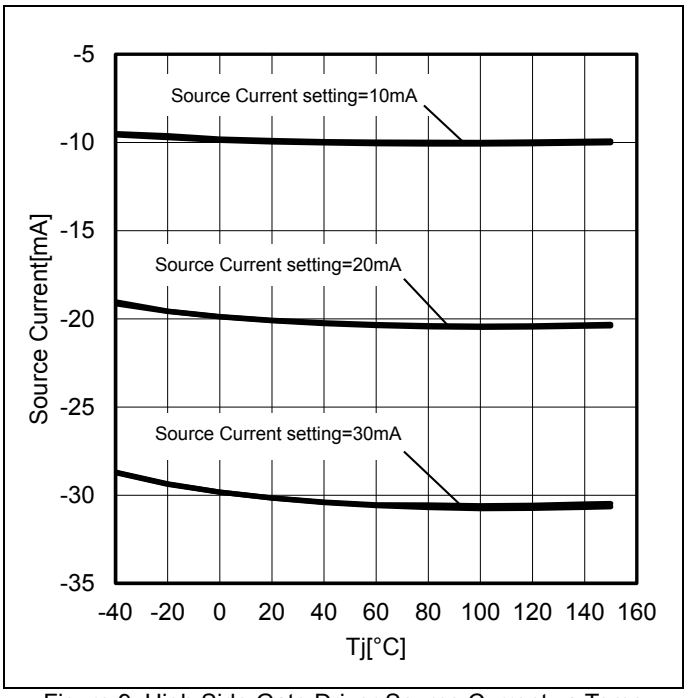


Figure 9. High Side Gate Driver Source Current vs Temp
(RSTB=VCC, PWM1=PWM2=VCC, GH1=SH1+2V,
GH2=SH2+2V, Enable Register[2:0]=111,
CH1_MODE[3:0]=1000, CH2_MODE[3:0]=1000,
CUR_SOURCE[4:0]=01010, 10100, 11110
CUR_SINK[4:0]=00000, Other address data is default value)

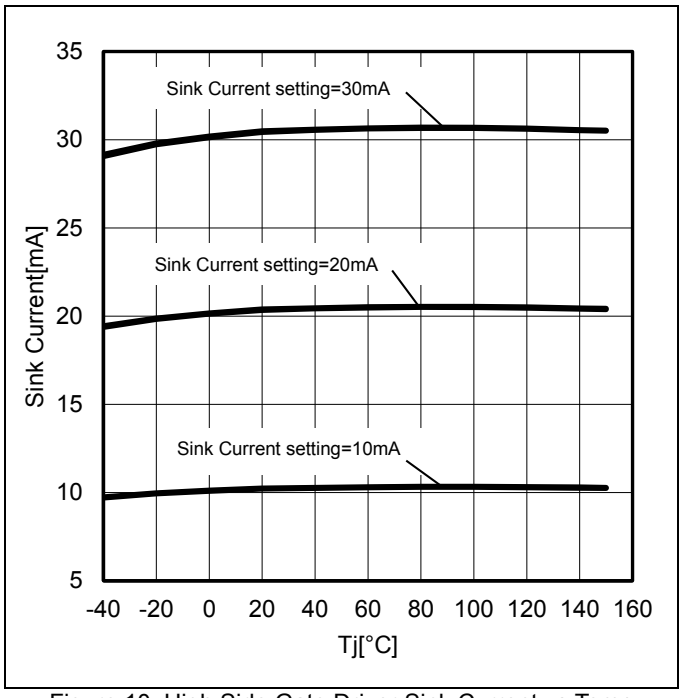


Figure 10. High Side Gate Driver Sink Current vs Temp
(RSTB=VCC, PWM1=PWM2=0V, GH1=SH1+2V,
GH2=SH2+2V, Enable Register[2:0]=111,
CH1_MODE[3:0]=1000, CH2_MODE[3:0]=1000,
CUR_SOURCE[4:0]=00000,
CUR_SINK[4:0]= 01010, 10100, 11110,
Other address data is default value)

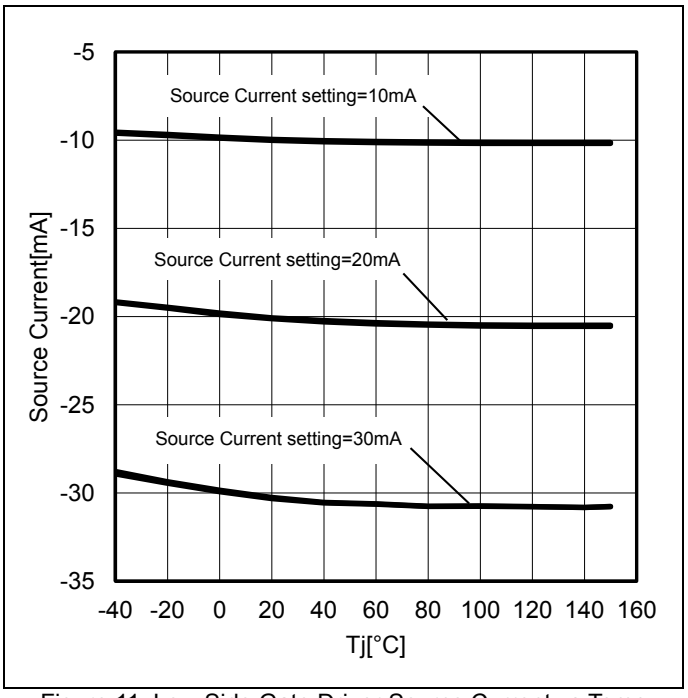


Figure 11. Low Side Gate Driver Source Current vs Temp
(RSTB=VCC, PWM1=PWM2=0V, GL1=2V, GL2=2V,
Enable Register[2:0]=111, CH1_MODE[3:0]=1000,
CH2_MODE[3:0]=1000,
CUR_SOURCE[4:0]=01010, 10100, 11110
CUR_SINK[4:0]=00000, Other address data is default value)

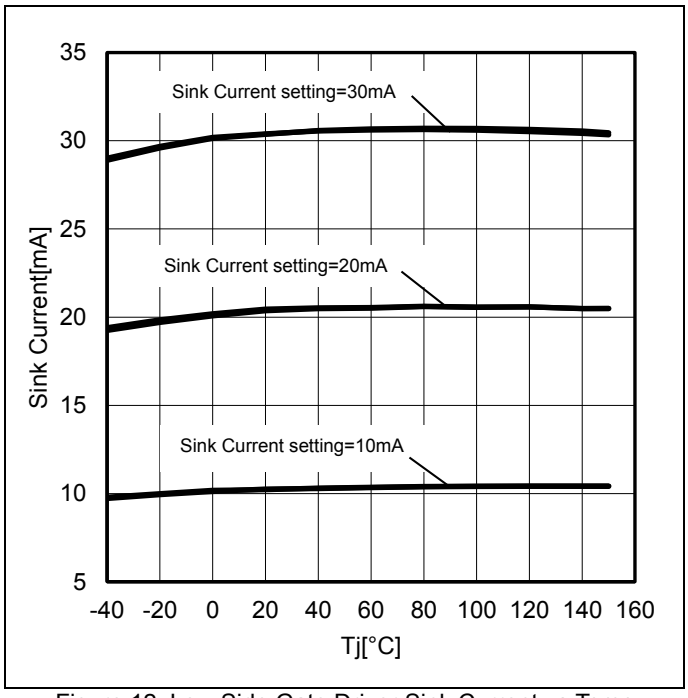
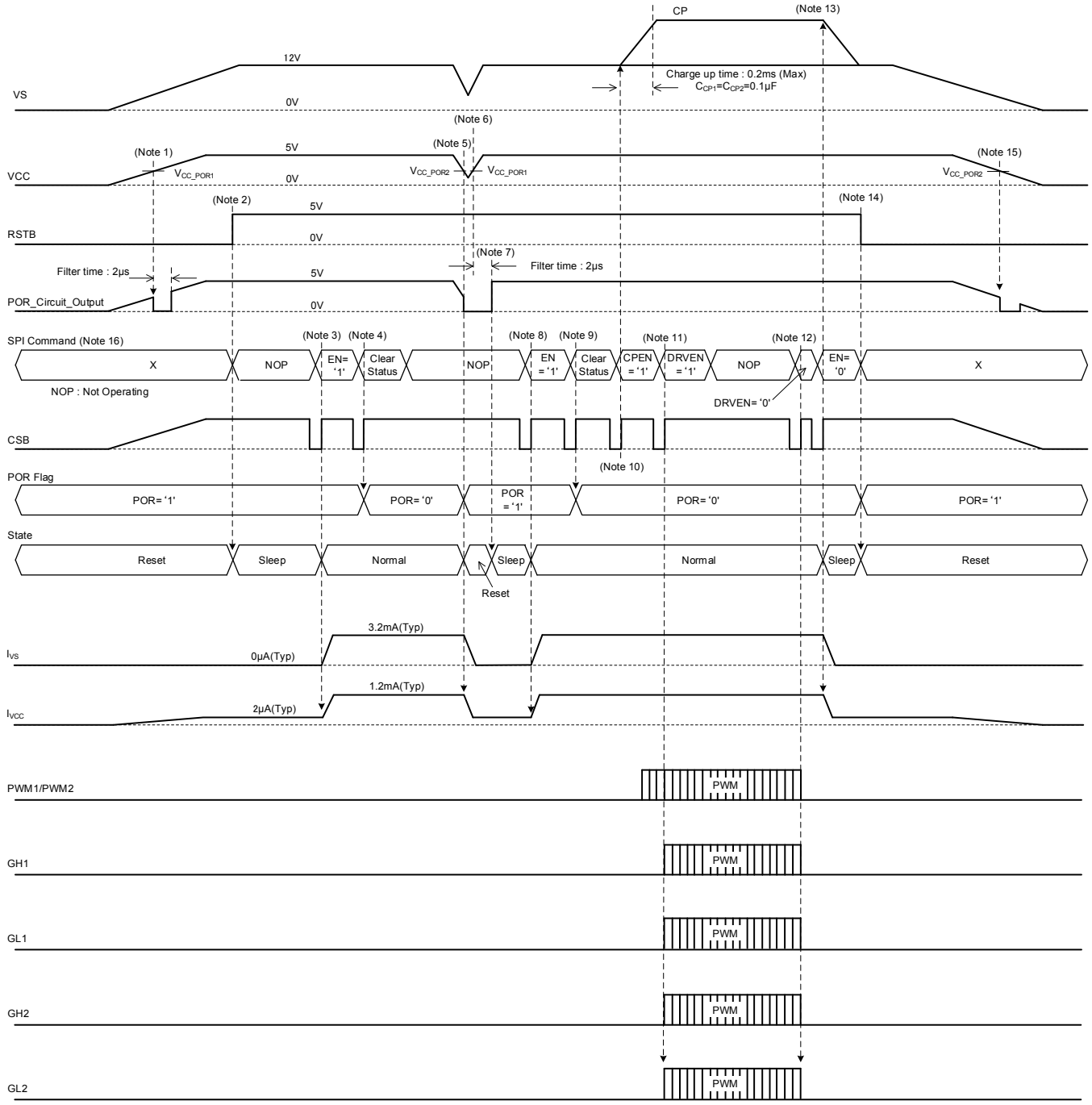


Figure 12. Low Side Gate Driver Sink Current vs Temp
(RSTB=VCC, PWM1=PWM2=0V, GL1=2V, GL2=2V,
Enable Register[2:0]=111, CH1_MODE[3:0]=1000,
CH2_MODE[3:0]=1000,CUR_SOURCE[4:0]=00000,
CUR_SINK[4:0]= 01010, 10100, 11110,
Other address data is default value)

Timing Chart



(Note 1) The Power-On-Reset circuit (POR) monitors the VCC voltage. At power-up, POR is released when VCC ≥ V_{CC_POR1} voltage. The POR circuit has a blanking time for 2μs (Typ) to reject noise.
The POR Flag in status resister is set to '1' in reset and is kept after recovery reset.

(Note 2) RSTB is set high by MCU. State is changed to Sleep state.

(Note 3) MCU sends the EN='1' command. State is changed to Normal state.
EN='1' command can be sent after 1μs(min) to change RSTB from "Low" to "High".
Consequently, analog circuit becomes active (I_{VS_act}=3.2mA Typ and I_{VCC_act}=1.2mA Typ).
Transition time is 50μs(Max) from "Sleep state" to "Normal state".

(Note 4) MCU sends "Clear Status" Command. Therefore, POR bit in status register is set to '0' (POR='1' to POR='0').

(Note 5) VCC voltage drops below $V_{CC\_POR1} – V_{CC\_POR\_hys}$. POR_Circuit_Output voltage is low (logic reset signal).
POR bit register is set to ‘1’. State is changed to Reset state.
Consequently, the analog circuit is OFF (I_{VS_qui1}=0μA Typ and I_{VCC_qui1}=2μA Typ).

(Note 6) VCC voltage rises above V_{CC_POR1}. POR_Circuit_Output level is high (logic reset release)
after filter time(2μs Typ).

(Note 7) POR_Circuit_Output level is high. Therefore, State is changed to Sleep state.

(Note 8) MCU sends the EN=’1’ command. State is changed to Normal state.
Therefore, analog circuit becomes active(I_{VS_act}=3.2mA Typ and I_{VCC_act}=1.2mA Typ).

(Note 9) MCU sends the “Clear Status” Command. Therefore, the POR bit register is set to ‘0’(POR=’1’ to POR=’0’).

(Note 10) MCU sends the CPEN=’1’ command. Charge pump circuit is activated. Charge time is 0.2ms(Max).

(Note 11) MCU sends the DRVEN=’1’ command. GH1, GL1, GH2 and GL2 outputs are active(Constant current driving).
Each register setting is set before DRVEN=’1’.

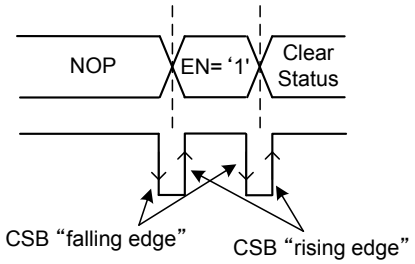
(Note 12) MCU sends the DRVEN=’0’ command. GH1, GL1, GH2 and GL2 outputs are pulled low with a 10Ω pull down.

(Note 13) MCU sends the EN=’0’ command. State is changed to Sleep state.
Therefore, analog circuit turns OFF(I_{VS_qui1}=0μA Typ, I_{VCC_qui1}=2μA Typ and charge pump circuit is OFF).

(Note 14) RSTB input is set to low level by MCU. State is changed to Reset state.
POR bit register is to ‘1’.Therefore, the SPI interface can’t be communicable.

(Note 15) VCC voltage falls below $V_{CC\_POR1} – V_{CC\_POR\_hys}$. POR_Circuit_Output level is low (logic reset signal).

(Note 16) CSB falling edge and rising edge are described as below.



State Description

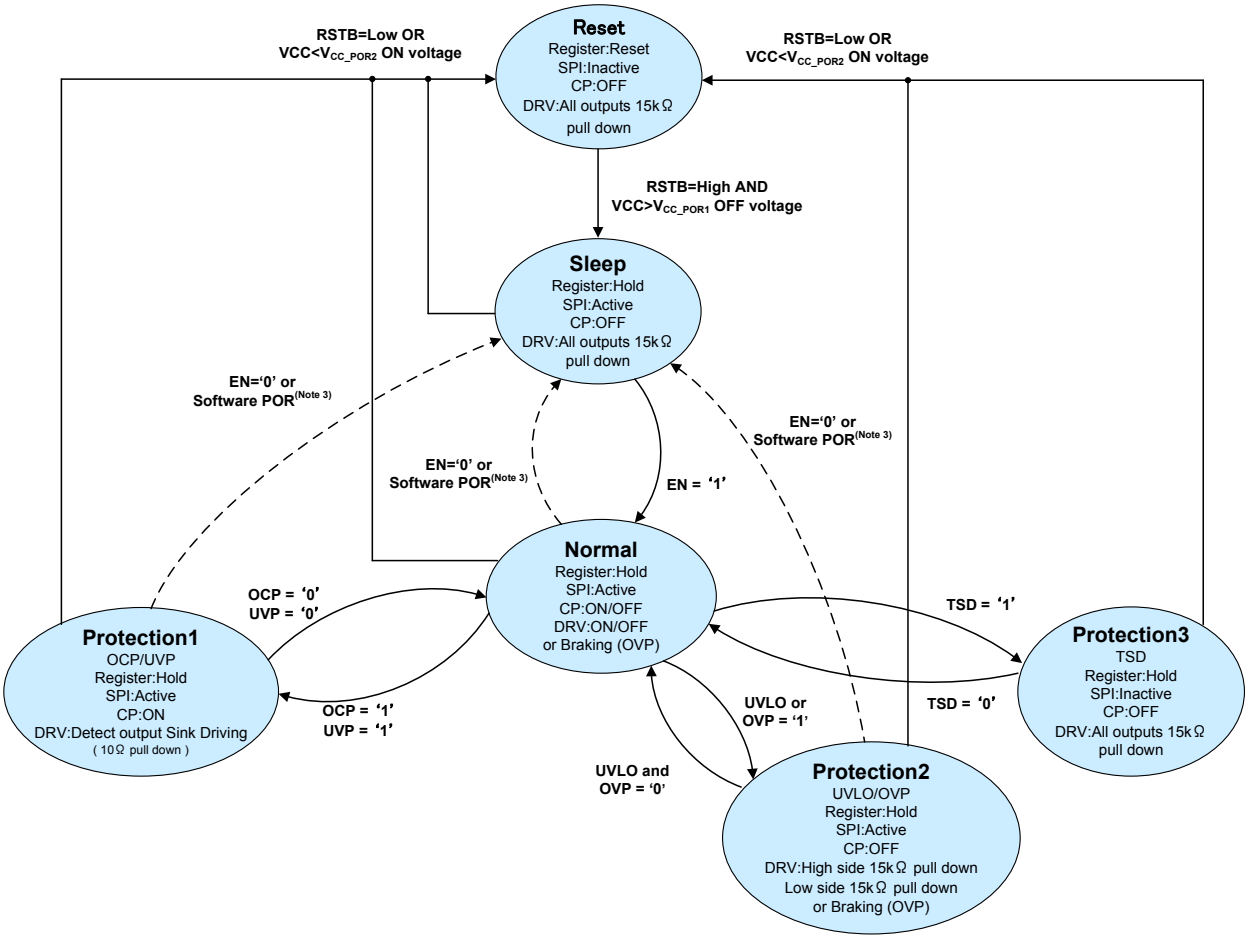
Table 1. State Description

State	CP	GH1,GH2	GL1,GL2	SPI
Reset	OFF	15kΩ pull down	15kΩ pull down	Inactive
Sleep	OFF	15kΩ pull down	15kΩ pull down	Active
Normal	ON	ON(DRVEN=1): Output is synchronous with PWM1(Note 1) or PWM2(Note 2) input	ON(DRVEN=1): Output is synchronous with PWM1(Note 1) or PWM2(Note 2) input	Active
		OFF(DRVEN=0): Outputs are Sink Driving Mode (10Ω pull down)	OFF(DRVEN=0): Outputs are Sink Driving Mode (10Ω pull down)	Active
	OFF	15kΩ pull down	15kΩ pull down / braking mode	Active
Protection1	ON	Output is Sink Driving Mode (10Ω pull down)	Output is Sink Driving Mode (10Ω pull down)	Active
Protection2	OFF	15kΩ pull down	15kΩ pull down / braking	Active
Protection3	OFF	15kΩ pull down	15kΩ pull down	Inactive

(Note 1) GH1 and GL1 outputs are synchronized to the PWM1 input.

(Note 2) GH2 and GL2 outputs are synchronized to the PWM2 input.

Functional Description State Control



(Note 3) This is Software POR command. It will set all register to default value. Note default value for POR register is 1.

Figure 13. Functional Description State Control

Transition time is 2μs(Typ) between each state. This does not include any relevant the blanking time. (e.g. UVLO detect blanking time, OVP detect blanking time etc.).

If settings are changed while IC is in one of the Protection states, the settings become valid except for those which can influence the transition to that particular protection state itself. Transition from Protection states to Reset state or Sleep state occurs immediately. Transition to normal state is only possible when the particular protection condition (e.g. OCP, OVP, UVLO or TSD) is no more existing. Furthermore, only the channels which are having over current move to OCP Protection state. Other channels with normal currents stay in Normal state.

The following table describes validity of individual command settings when changed in Protection states.

Command	Address	Protection1	Protection2
Software POR, Enable Register, Status Read/Clear Status	00h, 01h, 09h	Valid immediately	Valid immediately
Other Commands	02h, 03h, 04h, 05h, 06h, 07h	Valid immediately(note1)	Valid immediately(note2)

(note1) Settings become immediately valid except for the Channel which is in OCP. For those channel, settings would become effective only when they move out of OCP. E.g. if OCP threshold value is changed while a channel is in OCP, the new value would be effective only when the channel moves out of OCP.

(note2) Settings become immediately valid except for those which can influence the transition to protection mode itself. E.g. when state is Protection2 due to UVLO, it cannot be disabled by setting UVLOM as '0'.

Reset State (Refer to Table 1, Table 2, Figure 13 and Figure 16)

If RSTB=Low or VCC < V_{CC_POR1} – $V_{CC\_POR\_hys}$ Voltage, the state changes to Reset state.
Logic is in Reset state, therefore SPI communication is impossible. All register data is cleared. In the Reset State all analog circuits are OFF, therefore I_{VS_qui1}=0μA and I_{VCC_qui1}=2μA. The driver outputs of BD16952EFV are pulled down by a 15kΩ (Typ) internal resistor. The Reset state changes to Sleep state when RSTB=High and VCC > V_{CC_POR1} Voltage.

Transition to Reset State

Transition to Reset State can be made with 2 type of operation methods.

1. when RSTB=Low.
2. when VCC < V_{CC_POR1} – $V_{CC\_POR\_hys}$ Voltage.

Sleep State (Refer to Table 1, Table 2, Figure 13 and Figure 16)

When RSTB=High and VCC > V_{CC_POR1}, the state changes to the Sleep state. The logic is released from reset, therefore SPI communication is possible and all registers can be set. In the Sleep State, all analog circuits are OFF, therefore I_{VS_qui1}=0μA and I_{VCC_qui1}=2μA. The driver outputs of BD16952EFV are pulled down by a 15kΩ (Typ) internal resistor. However, the POR circuit remains active in Sleep State. When VCC < V_{CC_POR1} – $V_{CC\_POR\_hys}$, is detected, the logic is reset and the state changes to the Reset State.

Transition to Sleep State

Transition to the Sleep State can be made with 2 type of operation methods.

1. when EN=0 (RSTB=High and VCC > V_{CC_POR1})
2. by software reset (RSTB=High and VCC > V_{CC_POR1}).

Normal State (Refer to Table 1 and Figure 13)

The Normal State is the standard operating state for BD16952EFV. When the enable register EN is set to '1', the state changes from Sleep State to Normal State. In the Normal State, all analog circuits are active and SPI communication is possible. Additionally, ON/OFF control of the charge pump and the driver output is possible by setting the registers CPEN and DRVEN. The driver outputs are pulled down with 15kΩ (Typ) when CPEN=0. However, when both DRVEN=1 and DRVEN=0, the driver outputs are actively driven low with 10Ω (Typ). When CPEN='1' and DRVEN='1' the driver outputs are synchronized with the PWM1 or PWM2 input.

Protection1 State (Refer to Table 1, Table 2, Figure 13 and Figure 25 to 27)

When Over Current Protection (OCP) or DRAIN terminal Under Voltage Protection (UVP) event is detected, the state changes to Protection1 State. In this state, the SPI registers hold their values, SPI communication remains possible and the Charge pump is kept in charged-up state. The driver outputs are actively pulled low with 10Ω (Typ). For driver output OFF operation of the over current detection, a latch mode and auto recovery mode can be selected. Only the output at which an OCP event is detected will be turned OFF.

Protection2 State (Refer to Table 1, Table 2, Figure 13 and Figure 17 to 22)

When a UVLO or OVP event is detected at the VS terminal, the state changes to the Protection2 state. In this state, the SPI registers hold their values, SPI communication remains possible and the charge pump stops charging. The driver outputs can either be pulled down with 15kΩ (Typ) or operate in braking mode, which is controlled by the MCU in case of a user-generated over-voltage event that is detected by the MCU. Both (UVLO and OVP) detection functions can be disabled, but not during an already detected OVP or UVLO event.

Protection3 State (Refer to Table 1, Table 2, Figure 13 and Figure 23)

When a TSD event is detected, the state changes to Protection3 State. In Protection3 state SPI registers hold their values, but SPI is disabled and the charge pump stops charging. The driver outputs are pulled down with 15kΩ (Typ).

Dual Power Supply: VS and VCC

The supply voltage VS supplies the charge-pump and low-side driver. An internal charge-pump is used to drive the high-side switches. The supply voltage VCC (3.3V/5V) is used for analog blocks and digital core of the BD16952EFV. Due to the independent VCC supply voltage, the logic control and logic status information is not lost even if the VS supply voltage is switched OFF. In case of power-on (VCC increases above the POR threshold V_{CC_POR1} = 2.00V Typ), the circuit is initialized by an internally generated power-on reset (POR). If the VCC voltage decreases under the POR threshold V_{CC_POR1} – $V_{CC\_POR\_hys}$ = 1.90V(Typ), the driver outputs (GH1, GH2, GL1 and GL2) are switched-off and the logic registers are set to default values.

Constant Current Control

The controlled constant source and sink current values of the gate driver can be set individually by the SPI register. Setting ranges are ‘Drivers OFF’ and 1mA - 31mA in steps of 1mA. In the ‘Drivers OFF’ setting, the drivers are set to 0mA setting (CUR_SINK [4:0] = 5’b00000). They can be synchronized with PWM1 or PWM2 input signal depending on the Half-bridge driver mode.

In Figure 14, the high-side constant current circuit is shown. Figure 15 shows the low-side constant current circuit. The global reference current ‘IREF’ is mirrored into the channel current to generate a local reference voltage while amplifier A1 forces the voltage across the current sense resistor to match the local reference voltage.

The output device is scaled to give a 5 bit output range so that the source/sink current values can be achieved in range of 1mA to 31mA by steps of 1mA. The source /sink current values do not contain the 15 kΩ pull down current.

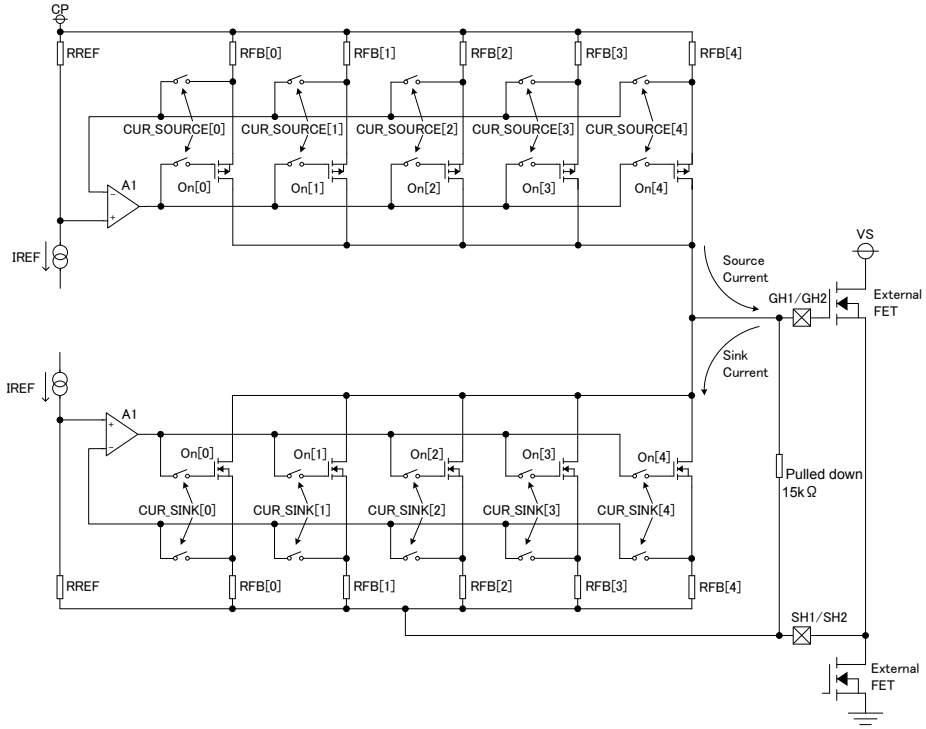


Figure 14. High Side Constant Current Circuit

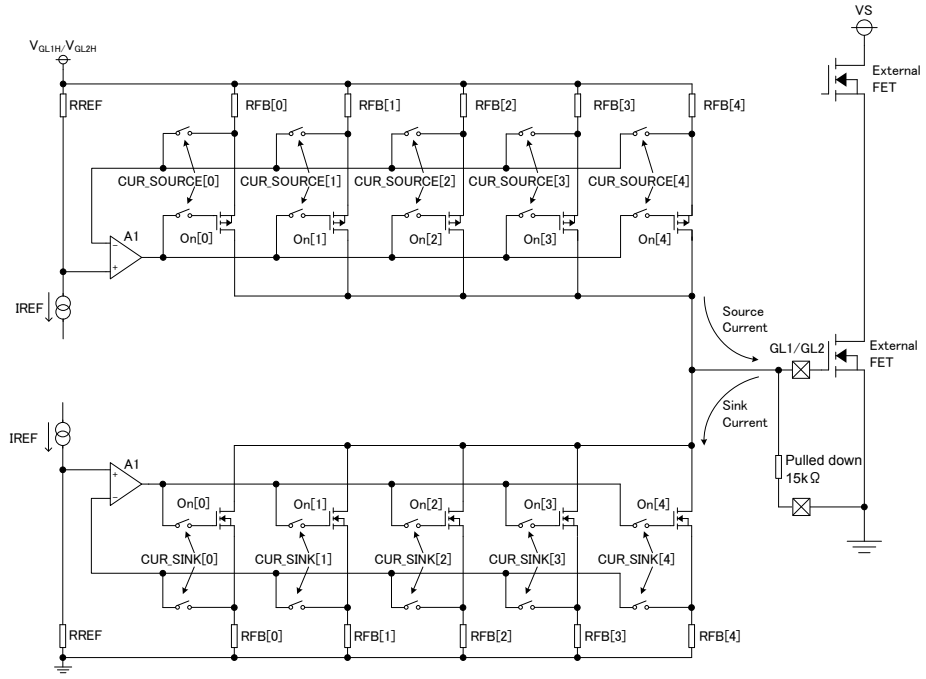
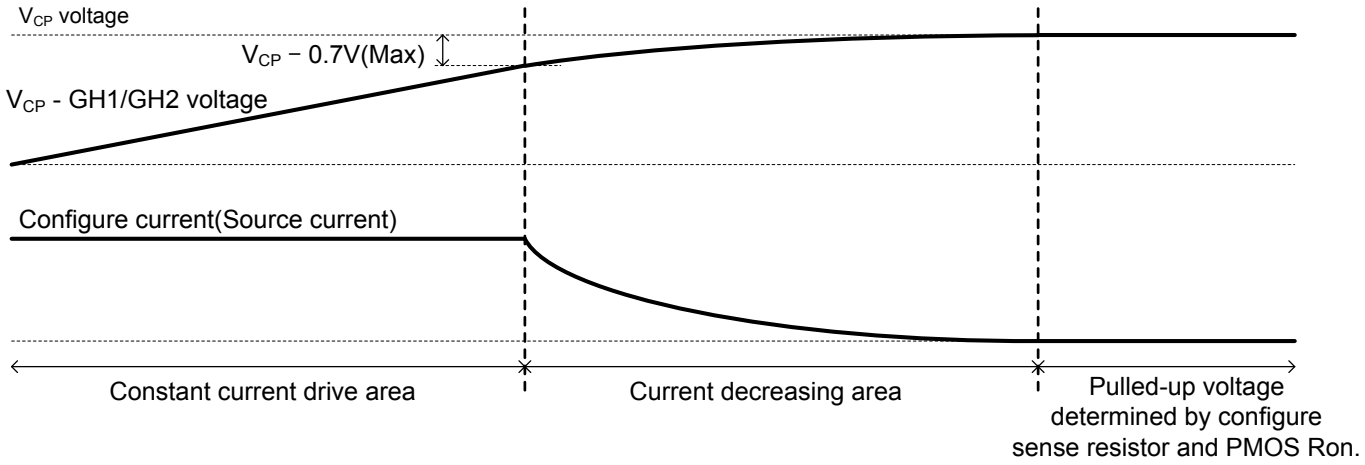


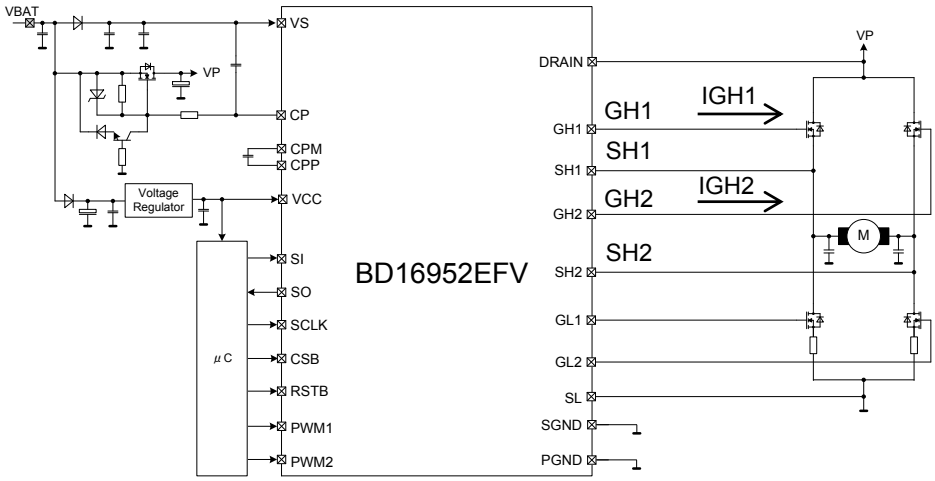
Figure 15. Low Side Constant Current Circuit

High Side Gate Driver Outputs at Saturation Source Current Control

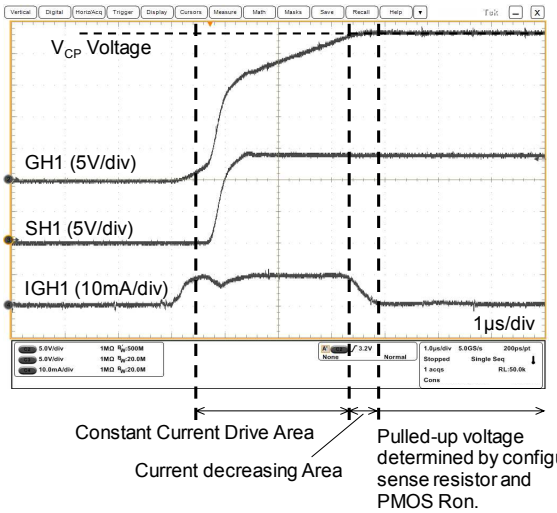
When the GH1/GH2 terminal voltage exceeds V_{CP}-0.7V (Max), the source current decreases from the setting value. Therefore, the constant current drive range is within GH1/GH2 terminal voltage < V_{CP}-0.7V(Max). After constant current drive, GH1 and GH2 terminals are pulled up by the current sense resistor and PMOS ON-resistance (current sense resistor(RFB[0], RFB[1], RFB[2], RFB[3] and RFB[4]) and PMOS). The effective resistance value of the pulled-up is determined by current sense resistor and PMOS Ron.



Evaluation Example (High Side Gate Voltage and Gate Current)

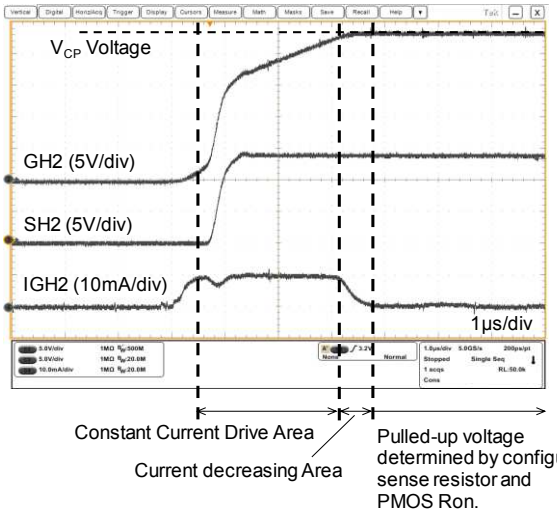


Channel 1 side waveform
(CUR_SOURCE[4:0]=01010)



Constant Current Drive Area
Current decreasing Area
Pulled-up voltage determined by configure sense resistor and PMOS Ron.

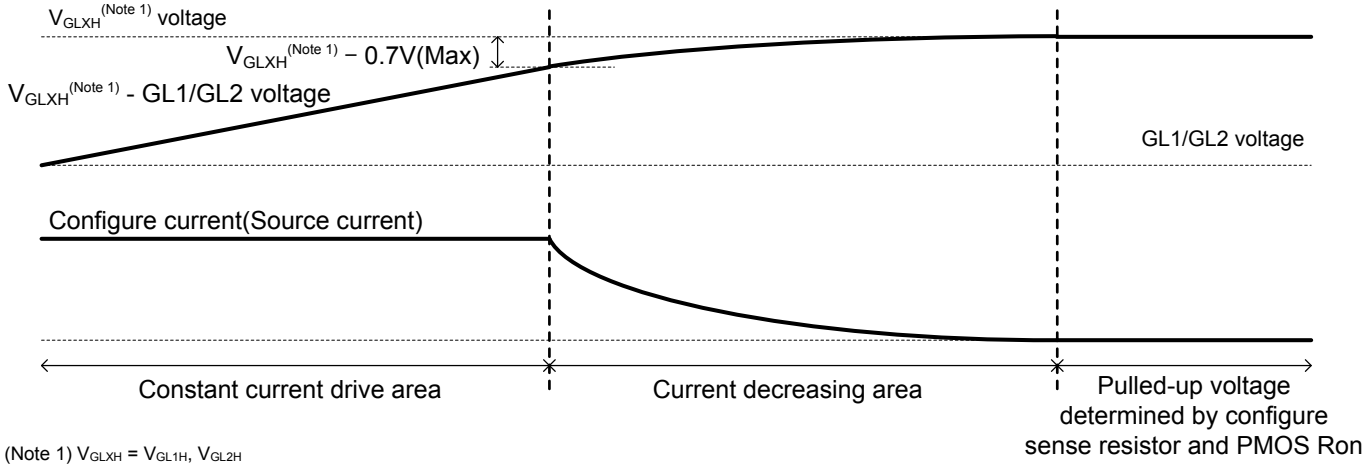
Channel 2 side waveform
(CUR_SOURCE[4:0]=01010)



Constant Current Drive Area
Current decreasing Area
Pulled-up voltage determined by configure sense resistor and PMOS Ron.

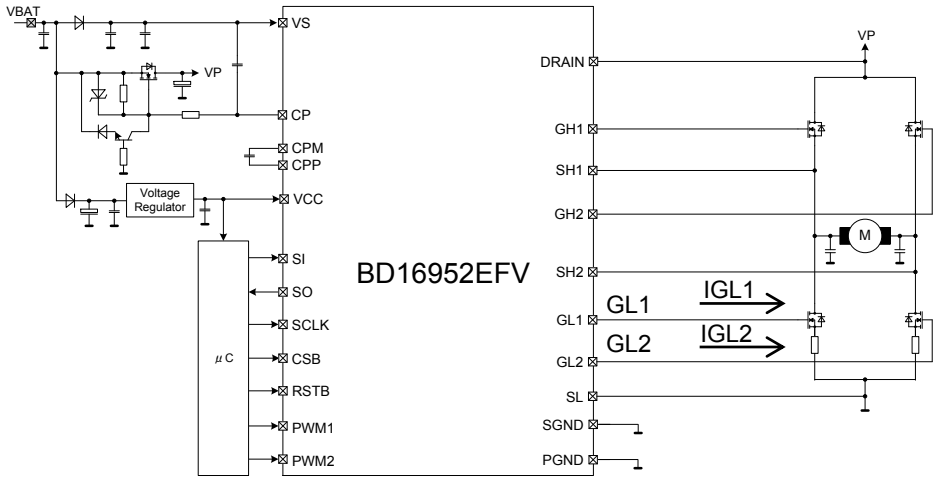
Low Side Gate Driver Outputs at Saturation Source Current Control

When the GL1/GL2 terminal voltage exceeds V_{CLAMP}-0.7V (Max), the source current decreases from the setting value. Therefore, the constant current drive range is within GL1/GL2 terminal voltage < V_{GLXH}-0.7V (Max). After constant current drive, GL1 and GL2 terminals are pulled up on a current sense resistor and PMOS Ron (current sense resistor(RFB[0], RFB[1], RFB[2], RFB[3] and RFB[4]) and PMOS). The effective resistance value of the pulled-up is determined by current sense resistor and PMOS Ron.

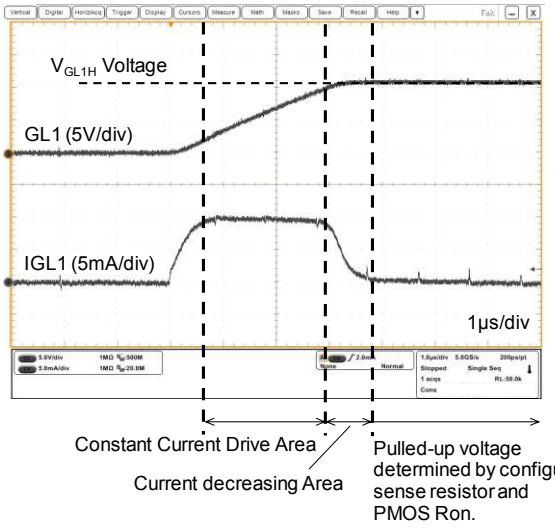


(Note 1) $V_{GLXH} = V_{GL1H}, V_{GL2H}$

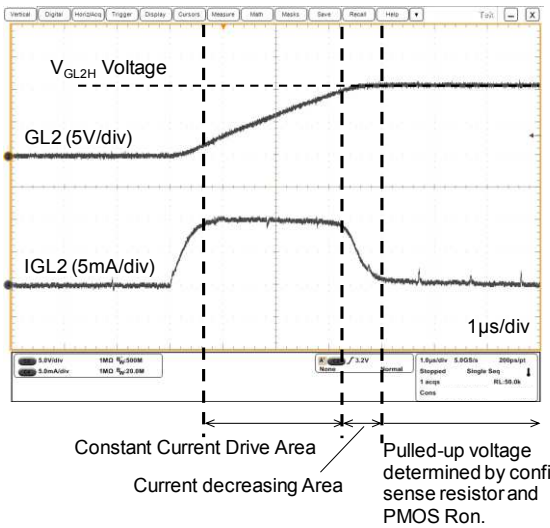
Evaluation Example (High Side Gate Voltage and Gate Current)



Channel 1 side waveform
(CUR_SOURCE[4:0]=01010)

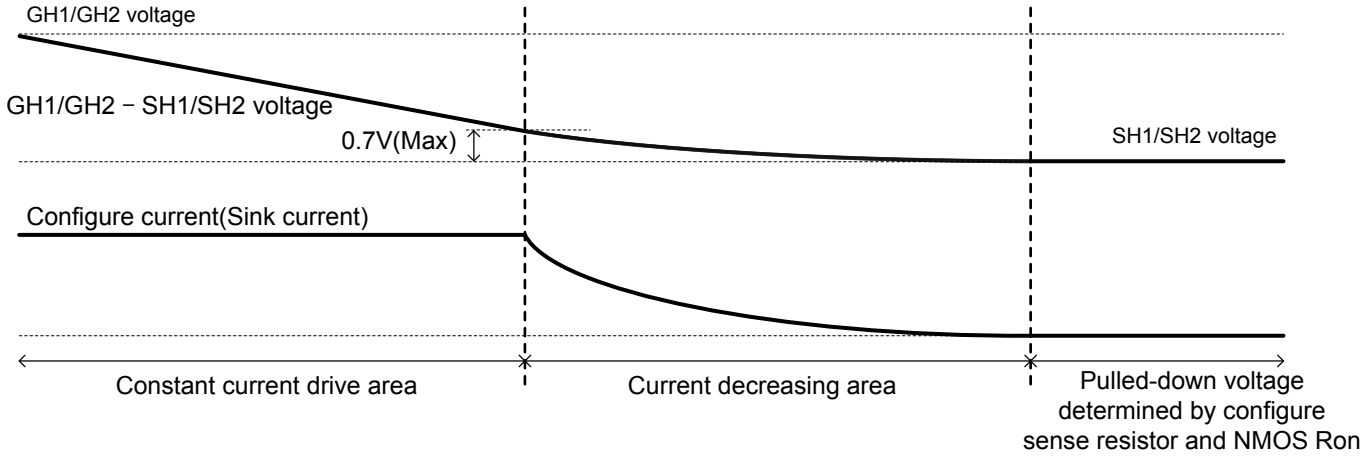


Channel 2 side waveform
(CUR_SOURCE[4:0]=01010)

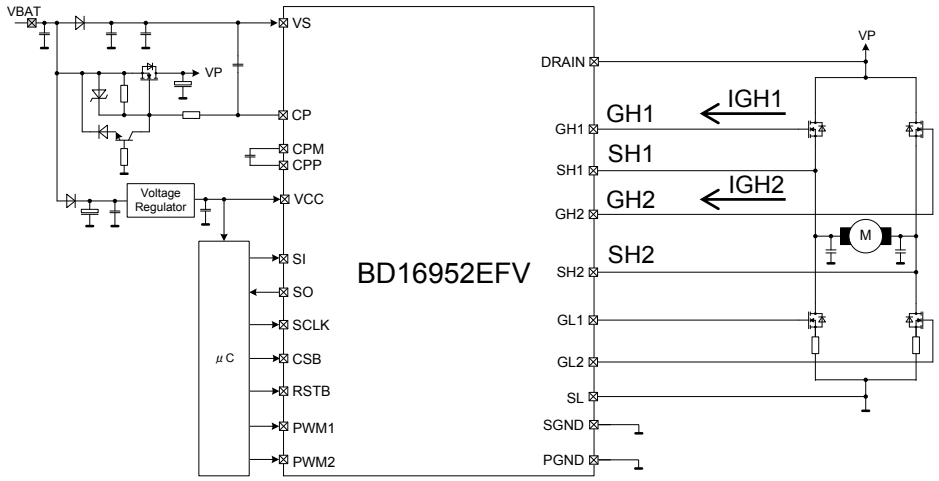


High Side Gate Driver Outputs at Saturation Sink Current Control

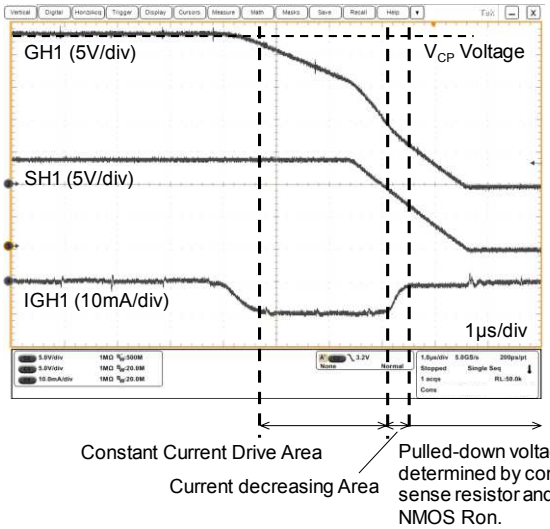
When GH1/GH2 terminal voltage falls below 0.7V (Max), the sink current decreases from the setting value. Therefore, constant current drive range is within GH1/GH2 terminal voltage > 0.7V (Max). Beyond this range, GH1 and GH2 terminals are pulled down on a current sense resistor and NMOS Ron (current sense resistors RFB[0], RFB[1], RFB[2], RFB[3] and RFB[4] and NMOS). The effective resistance value of the pulled-down is determined by current sense resistor and NMOS Ron.



Evaluation Example (High Side Gate Voltage and Gate Current)

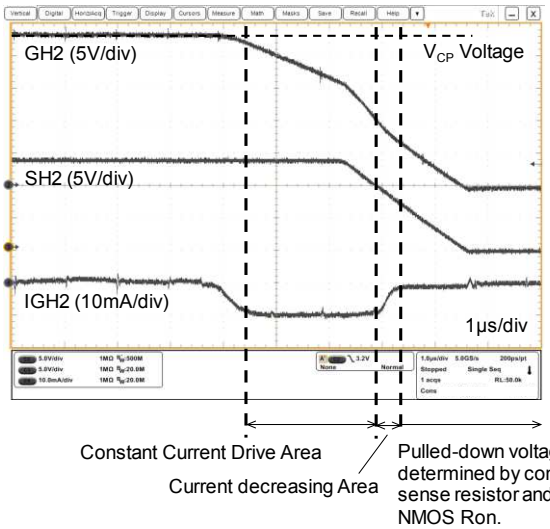


Channel 1 side waveform
(CUR_SINK[4:0]=01010)



Constant Current Drive Area
Current decreasing Area
Pulled-down voltage determined by configure sense resistor and NMOS Ron.

Channel 2 side waveform
(CUR_SINK[4:0]=01010)

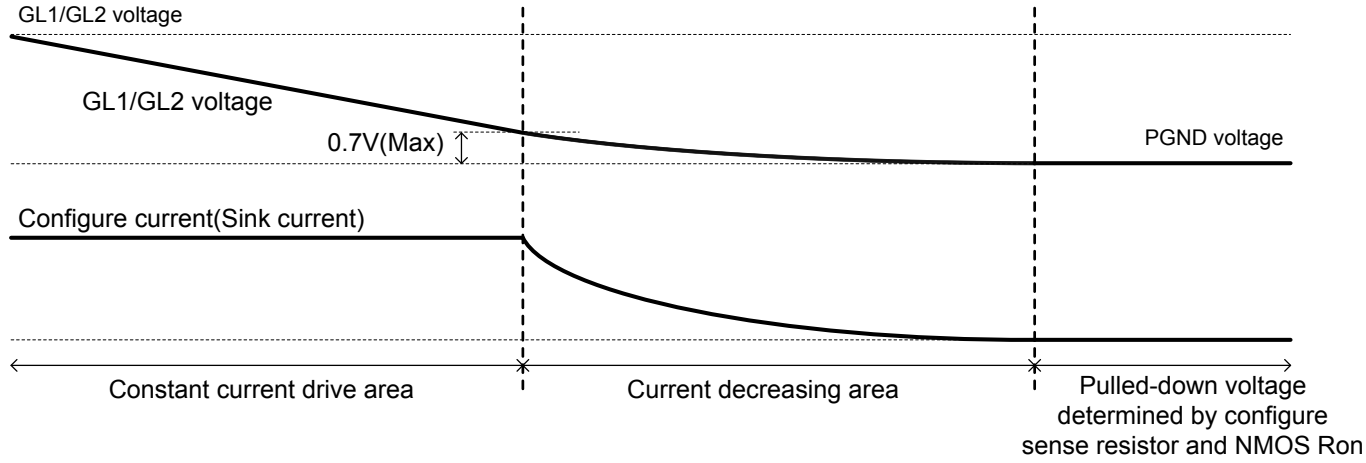


Constant Current Drive Area
Current decreasing Area
Pulled-down voltage determined by configure sense resistor and NMOS Ron.

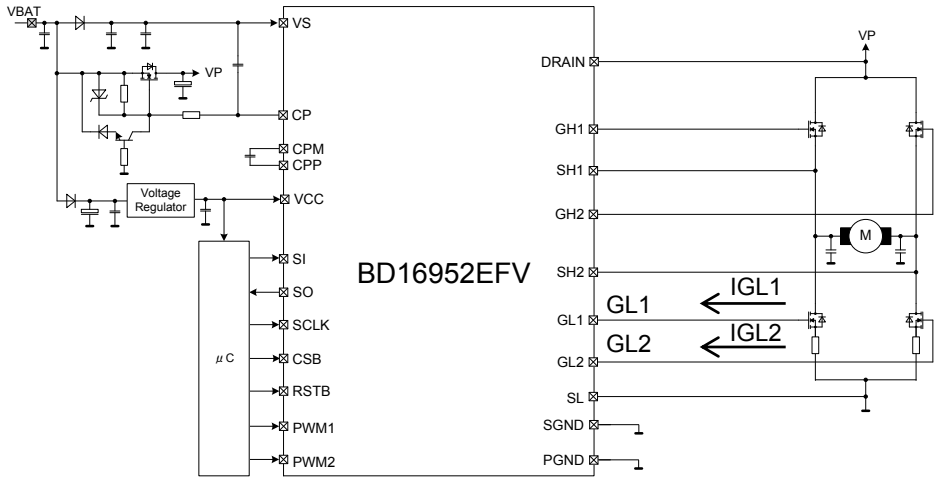
Low Side Gate Driver Outputs at Saturation Sink Current Control

When GL1/GL2 terminal voltage falls below 0.7V (Max), the sink current decreases from the setting value. Therefore, constant current drive range is within GL1/GL2 terminal voltage > 0.7V (Max). Beyond this range, GL1 and GL2 terminals are pulled down on a current sense resistor and NMOS Ron (current sense resistors RFB[0], RFB[1], RFB[2], RFB[3] and RFB[4] and NMOS).

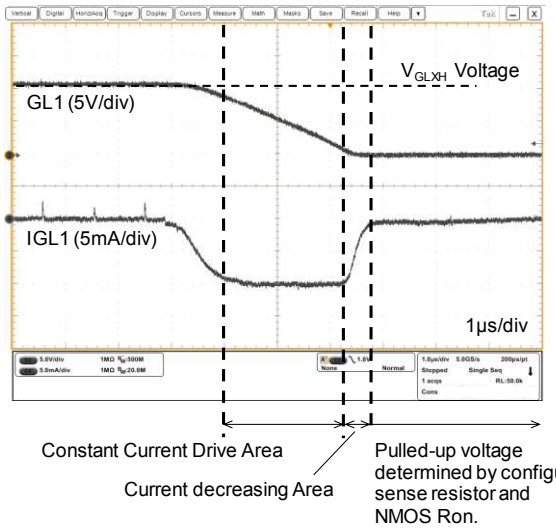
The effective resistance value of the pulled-down is determined by current sense resistor and NMOS Ron.



Evaluation Example (High Side Gate Voltage and Gate Current)

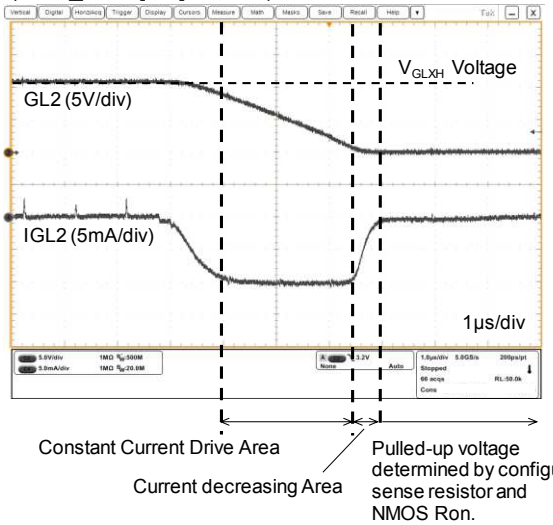


Channel 1 side waveform
(CUR_SINK[4:0]=01010)



Constant Current Drive Area
Current decreasing Area
Pulled-up voltage determined by configure sense resistor and NMOS Ron.

Channel 2 side waveform
(CUR_SINK[4:0]=01010)



Constant Current Drive Area
Current decreasing Area
Pulled-up voltage determined by configure sense resistor and NMOS Ron.

PWM Control

(Active Free Wheeling : Half-Bridge Control Mode=1000. See Mode Configuration on page 37)

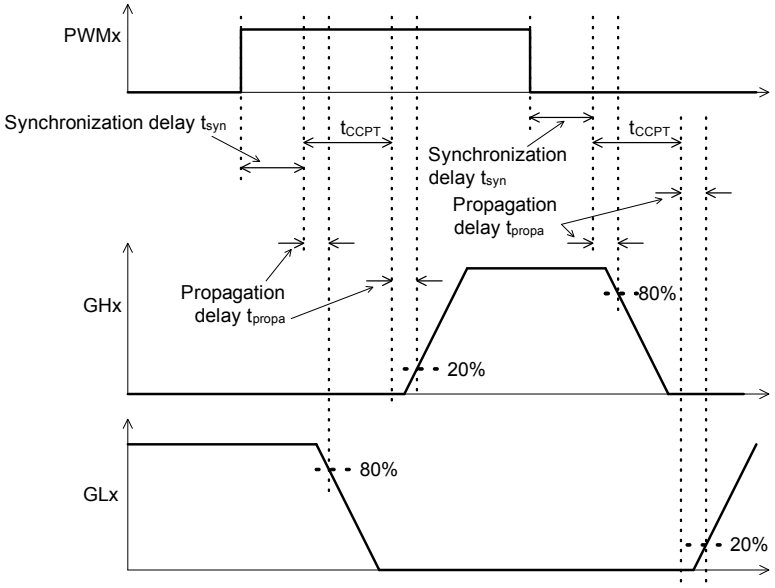
The relationship of PWM, GHx and GLx outputs signal are as below. When the BD16952EFV detects the rising edge of the PWM signal, the GHx or GLx are turned on, after an asynchronous delay (Synchronization delay t_{syn}). There is also an internal delay time(Propagation delay t_{propa}). before GHx or GLx outputs are turned on.

The external MOSFETs in Half-bridge configuration are switched ON with an additional delay time t_{CCPT} (Cross Current Protection Time) between the sink current start of GL1 / GL2 and the source current start of GH1/GH2 to prevent cross current in the half-bridge. This value can be set by the SPI register in the range:

0.25µs…4µs (0.25µs steps)

4µs…12µs (1µs steps)

12µs…92µs (2µs steps)



PWM Control

(Passive Free Wheeling : Independent Control Mode : PWM Control Mode. See Mode Configuration on page 37)

The relationship of PWM, GHx and GLx outputs signal are shown below. When the BD16952EFV is detecting the high edge of the PWM signal, an asynchronous delay is present (Synchronization delay t_{syn}) between the PWM signal and high-side source/sink or low-side source/sink of internal logic signal. Then, GHx or GLx are turned on. However, there is an internal delay time(Propagation delay t_{propa}) before GHx or GLx outputs are turned on.

The GHx or GLx are switched ON with an additional delay time t_{INCCPT} (Internal Cross Current Protection Time) between the sink current end of GHx / GLx and the source current start of GHx / GLx to prevent cross current.