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LED driver IC series for Automotive lamps

LED Driver with Built-in PWM Signal Generation Circuit

BD18351EFV-M

General Description

BD18351EFV-M is an LED driver with built-in 1ch boost controller. It is an optimal IC for LED drive for head lamp / DRL, tail lamp and turn lamp capable of realizing boost and buck boost with high-side detection of LED current setting against output voltage.
Further, cost saving and downsizing of the set can be realized, since it contains CRTIMER which enables PWM dimming without microcomputer for applications requiring PWM dimming of DRL, etc.

Key Specifications

- Input Voltage Range: 4.5 V to 65 V
- Output Voltage Range: 6.0 V to 65 V
- Absolute Maximum Input / Output Voltage: 70 V
- Minimum PWM Dimming Pulse Width: 100 µs

Features

- AEC-Q100 qualified. *(Note1)*
- Built-in Switching DC / DC Controller.
- LED Current Setting High Side Detection Method
- LED Current Precision: ±3.0% (–40 °C to 125 °C)
- PWM Signal Generation Circuit with Built-in CRTIMER (External PWM Dimming Control is possible.)
- Built-in Spread Spectrum Function
- Built-in LED Open Detection Function
- Built-in LED Anode to Ground Short Function

(Note1: Grade 1)

Package

Package	W(Typ) × D(Typ) × H(Max)
HTSSOP-B24	7.80 mm × 7.60 mm × 1.00 mm

HTSSOP-B24

Applications

Head lamp, DRL, front position lamp, tail lamp, turn lamp

Typical Application Circuit

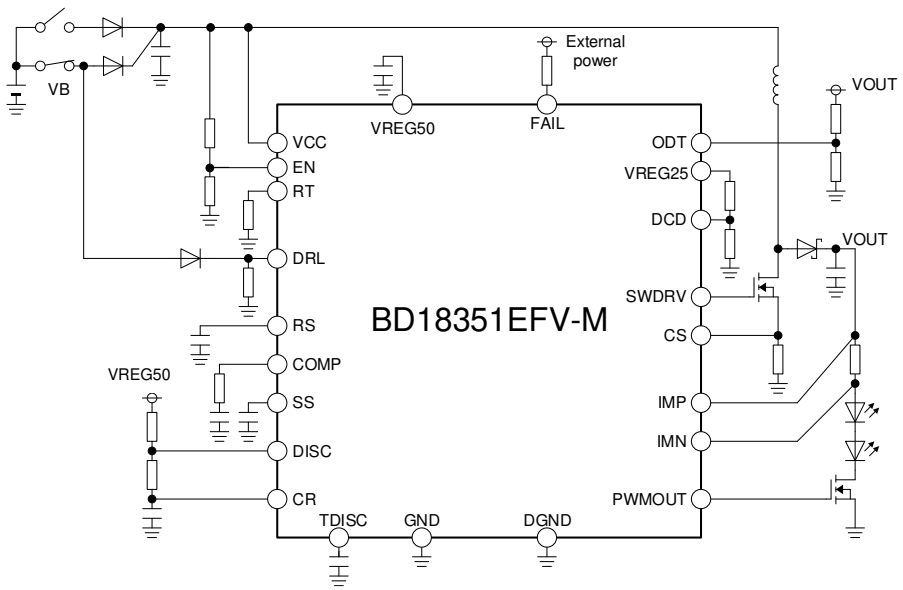


Figure 1. Typical Application Circuit

○Product structure: Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

HTSSOP-B24

(TOP VIEW)

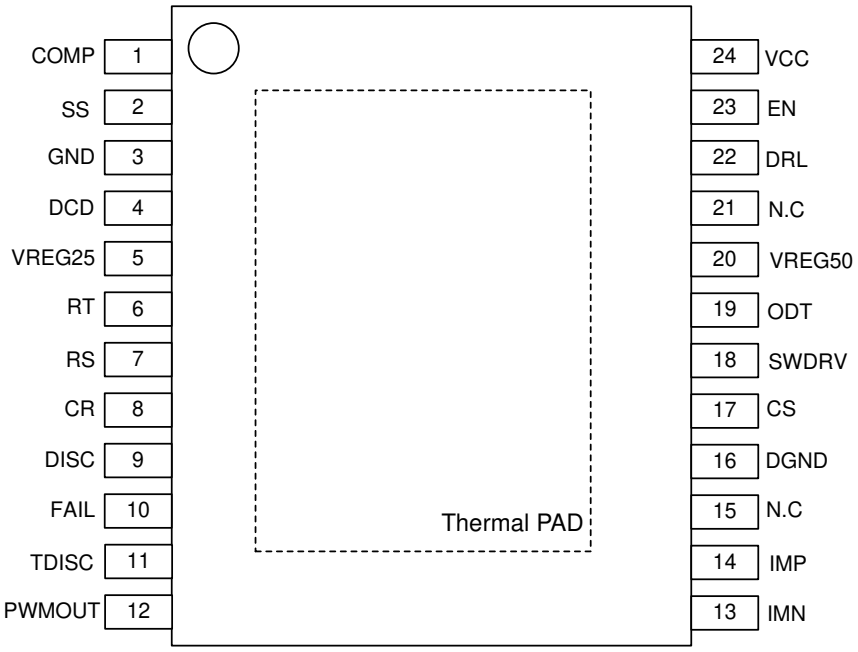


Figure 2. Pin Configuration

Pin Description

Terminal No.	Symbol	Function	Terminal No.	Symbol	Function
1	COMP	Error amplifier output phase compensation terminal	13	IMN	LED current detection terminal (-)
2	SS	Soft start setting terminal	14	IMP	LED current detection terminal (+)
3	GND	Small signal GND	15	N.C.	-
4	DCD	DC dimming terminal	16	DGND	Power GND
5	VREG25	2.5V standard voltage (DCD Exclusive terminal)	17	CS	Over current detection setting terminal
6	RT	DC / DC oscillation frequency setting terminal	18	SWDRV	External FET gate drive terminal
7	RS	Spread spectrum frequency setting terminal	19	ODT	LED open detection setting terminal
8	CR	Built-in CRTIMER PWM dimming frequency / Duty setting terminal	20	VREG50	Internal constant voltage 5.0 V output terminal
9	DISC	Built-in CRTIMER Discharge setting terminal	21	N.C.	-
10	FAIL	Error flag output terminal	22	DRL	Terminal for DRL control switching (High: 100 % mode)
11	TDISC	Discharge time setting terminal	23	EN	EN control terminal (High: Active)
12	PWMOUT	External for PWM dimming FET gate drive terminal	24	VCC	Power voltage terminal

(Pay attention that it does not correspond to reverse insertion.)

Block Diagram

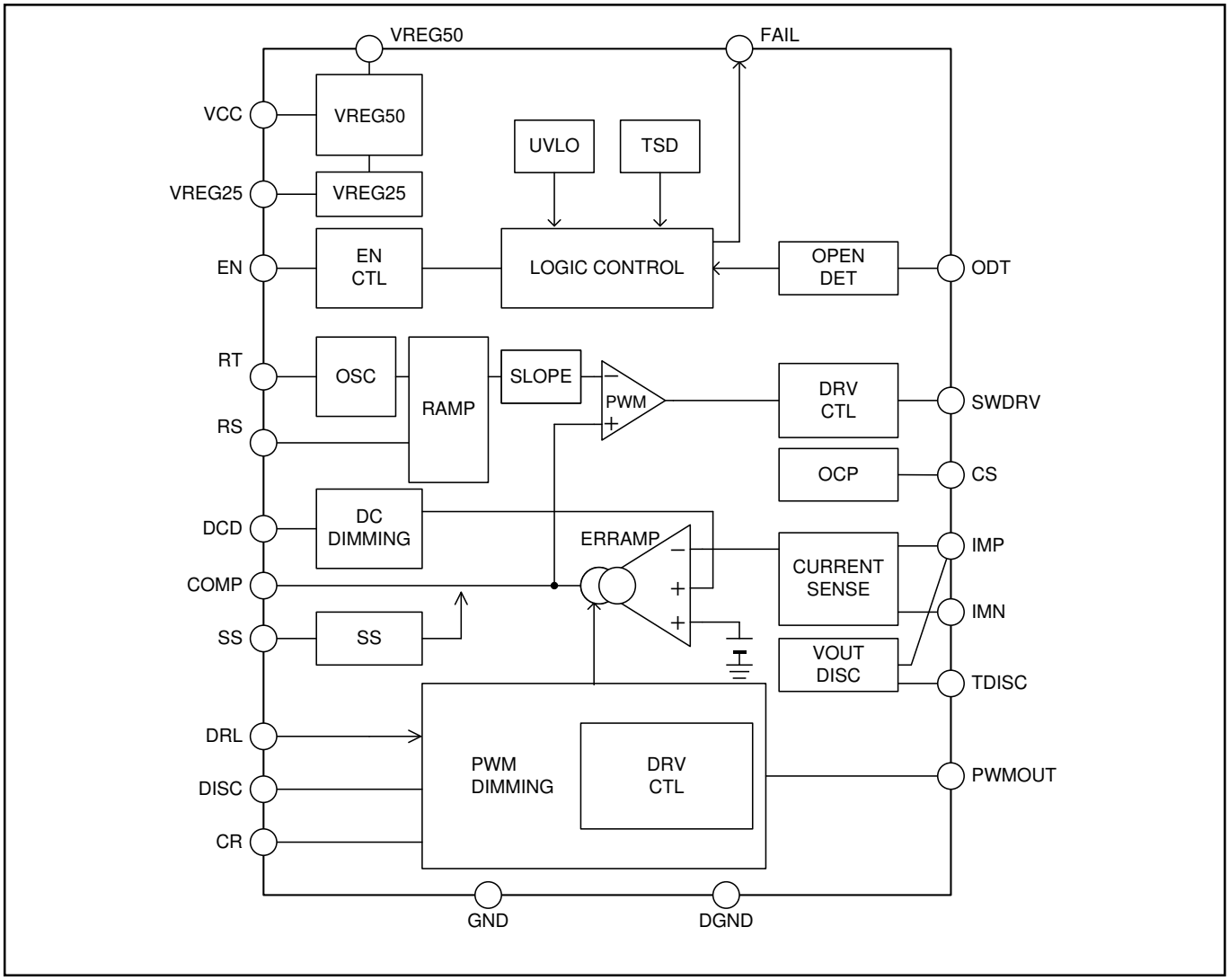


Figure 3. Block Diagram

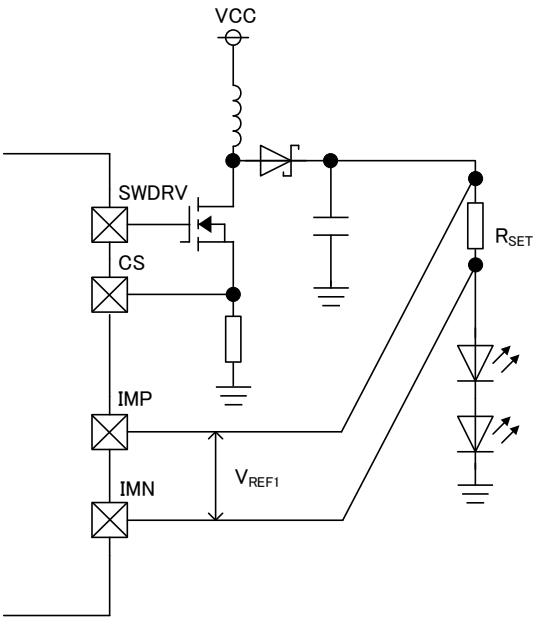
Description of Blocks

1. Standard voltage (VREG50)

5 V (Typ) is generated from VCC input voltage. This voltage (VREG) is used as power supply for internal circuit, and is also used to fix terminal at high voltage outside the IC. Please connect C_{VREG50} = 2.2 µF (Typ) as phase compensation capacity for VREG50 terminal. If C_{VREG50} is not connected, circuit operation will become markedly unstable. In addition, please do not use VREG50 as a power supply except this IC.

2. Concerning LED current setting and luminance adjustment(CURRENTSENSE)

(1) Concerning LED current setting method



LED current can be calculated by the following formula.

$$I_{LED} = \frac{V_{REF1}}{R_{SET}} \times \frac{V_{DCD}}{1.21V}$$

However, assign V_{DCD} = 1.21 V in the case of V_{DCD} > 1.21 V.

(Example)
In the case of connection of R_{SET} = 0.4 Ω, V_{DCD} = 0.6 V,

$$I_{LED} = \frac{0.2V}{0.4\Omega} \times \frac{0.6V}{1.21V} \fallingdotseq 0.25A$$

I_{LED}: LED current
V_{REF1}: Standard voltage for LED current setting (200 mV (Typ)
R_{SET}: Resistance for LED current setting
V_{DCD}: DCD terminal voltage

Figure 4. LED Current Setting Method

(2) Concerning luminance adjustment by PWM dimming control(PWM DIMMING)

PWM dimming control with built-in CR timer

PWM dimming is operated in 100 % by connecting Di to DRL terminal and turning DRL terminal to High as shown in Figure 1 On the other hand, when DRL terminal is turned low and configuration is made as shown in Figure 5, internal CR timer will operate, triangle wave is generated by CR terminal, PWMOUT terminal will be controlled to turn LED current off in CR voltage rise zone and turn LED current on in CR voltage fall zone. CR voltage rise / fall time can be set by the values of external parts (C_{CR}, R_{DISC1}, R_{DISC2}). Refer to the next page for setting method. In addition, the recommended operation frequency is 100 Hz to 2 kHz, On Duty 2 % to 45 %, and the recommended range of the external component values are 0.01 µF to 1.0 µF for C_{CR} and 10 kΩ to 33 kΩ for R_{DISC2}.(PWM min pulse width=100 μ s)

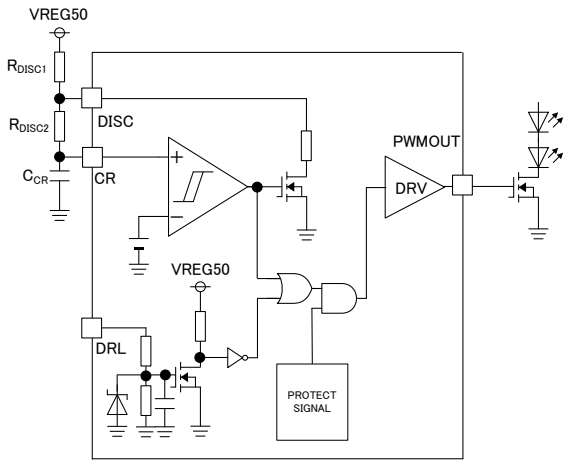


Figure 5. Example of Application Using Built-in CR Timer

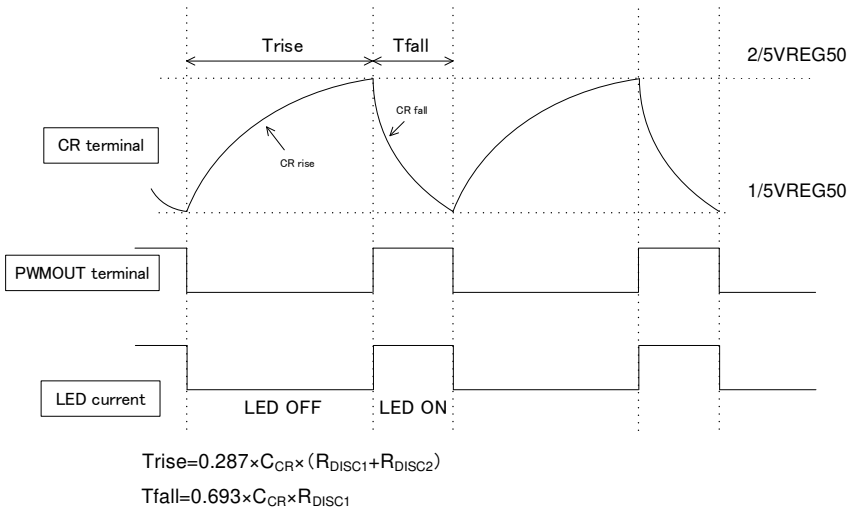


Figure 6. PWM Dimming Operation

CR terminal rise / fall time can be calculated as shown below.

① CR terminal rise time T_{rise}

$$T_{rise} = 0.287 \times C_{CR} \times (R_{DISC1} + R_{DISC2}) \ [s]$$

② CR terminal fall time T_{fall}

$$T_{fall} = 0.693 \times C_{CR} \times R_{DISC2} \ [s]$$

③ PWM dimming frequency F_{PWM}
PWM frequency is determined by T_{rise} and T_{fall}.

$$F_{PWM} = \frac{1}{(T_{rise} + T_{fall})} \ [Hz]$$

④ PWM dimming (ON Duty (D_{PWM})
ON Duty of PWM is determined by T_{rise} and T_{fall} as shown in the description above.

$$D_{PWM} = \frac{T_{fall}}{(T_{rise} + T_{fall})} \times 100 \ [\%]$$

(Example) when C_{CR} = 0.1 μF, R_{DISC1} = 100 kΩ, R_{DISC2} = 20 kΩ (Typ)

$$T_{rise} = 0.287 \times C_{CR} \times (R_{DISC1} + R_{DISC2}) = 3.444 \ [ms]$$

$$T_{fall} = 0.693 \times C_{CR} \times R_{DISC2} = 1.386 \ [ms]$$

$$F_{PWM} = \frac{1}{(T_{rise} + T_{fall})} = 207 \ [Hz]$$

$$D_{PWM} = \frac{T_{fall}}{(T_{rise} + T_{fall})} \times 100 = 28.7 \ [\%]$$

PWM dimming control with external signal (microcomputer, etc.)

Dimming is possible by direct input of PWM signal from external microcomputer, etc. Input PWM signal in CR terminal. Set 'High' level voltage of input signal from microcomputer at no less than 2.5 V for CR threshold voltage, and set 'Low' level voltage at no more than 0.5 V of CR threshold voltage. Recommended input frequency range is 100 Hz to 2 kHz. Minimum pulse width is 100 µs. It's necessary that 51kΩ resister need between µ-con and CR terminal like Figure 7. When filter is required, configure filter in high side of Figure 7 51kΩ.
However verification with actual application is required as filter may cause difference between Input signal to CR terminal and PWMOUT terminal.

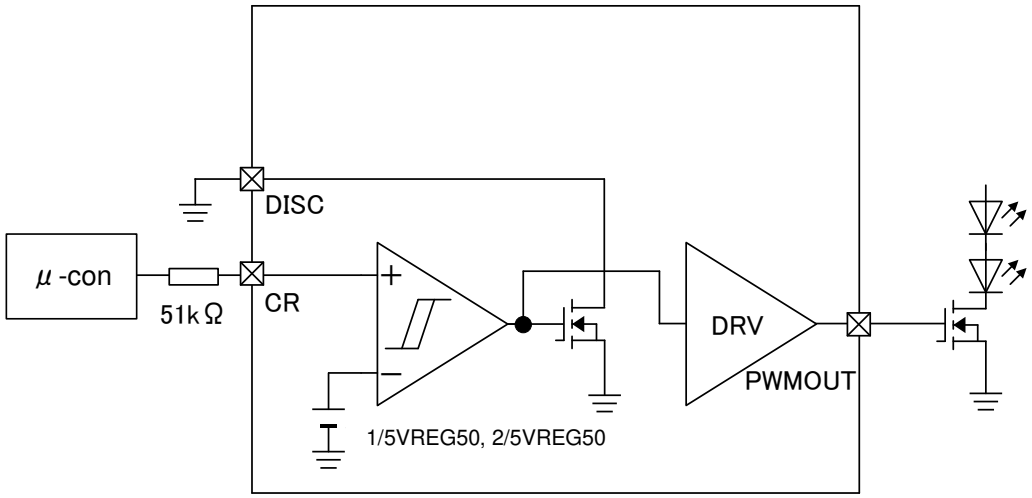


Figure 7. External Input of PWM Signal

(3) PWM Dimming with PchMOS

PWM dimming can be performed by PchMOS (Figure 8 (a) Q3) with Figure 8 configuration. In this configuration, RPWM1 / RPWM2 / RPWM3 controls gate voltage of PchMOS. If RPWM2, RPWM3 are bigger and gate capacitance of Q3 is high, this result in discrepancy in PWM ON width generated by PWMOUT pin output and LED current ON width controlled by Q3 . Please thereby perform the evaluation with the actual equipment by the constitution using PchMOS enough because it may cause instable operation such as high brightness lighting or the acoustic noise of capacitor and inductor.

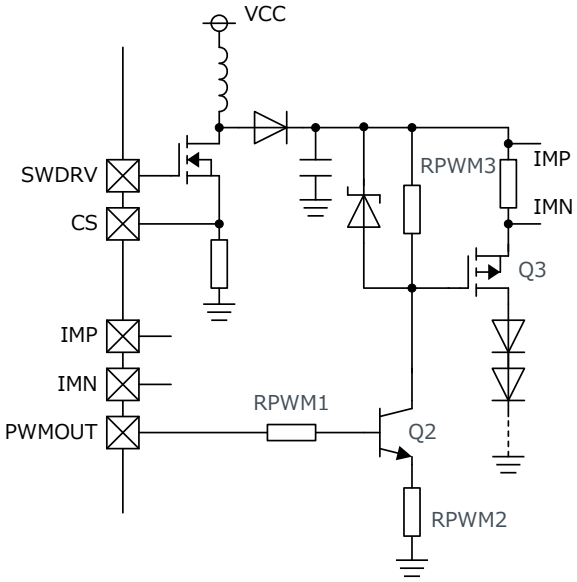


Figure 8 (a). PWM Dimming with PchMOS

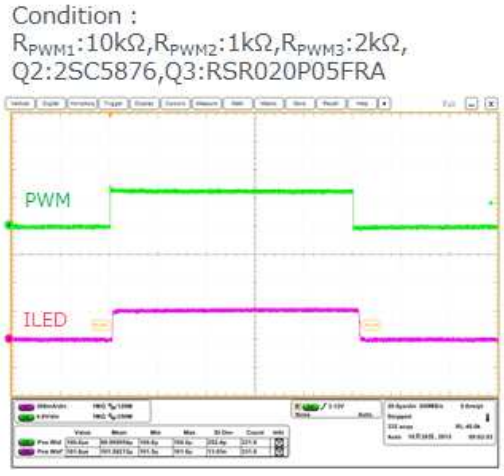
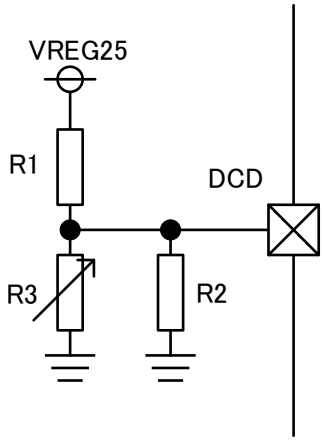
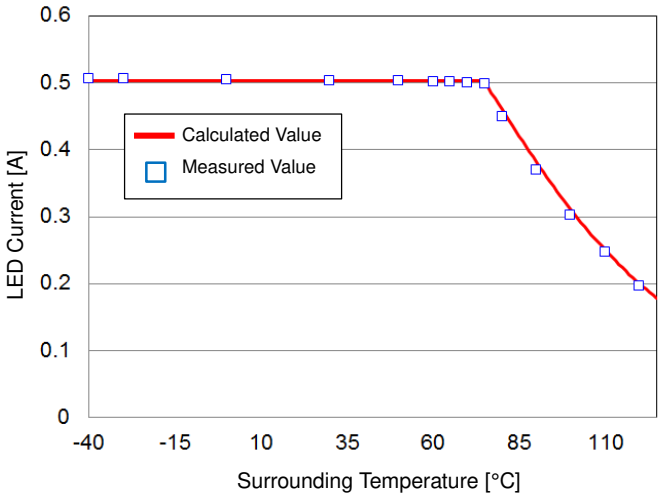


Figure 8 (b). PWM Dimming with PchMOS

(4) Brightness control by DC dimming control(DC DIMMING / VREG25)

LED current is linearly controllable corresponding to DCD terminal voltage. DCD terminal is mainly used for derating, and is used to control deterioration of LED at high temperature or to limit over current to external parts under conditions which power supply voltage fluctuates by idling stop functions, etc. (Refer to Figure 9). Recommended input range is $0.4 \leq V_{DCD} \leq$ VREG25 and LED current control starts in $V_{DCD} \leq 1.21$ V. In addition, the power supply voltage to control DCD can be controlled with high precision by using VREG25. When DC dimming is not used, short to VREG25 terminal directly.





R1: 12kΩ
R2: 100 kΩ
R3: NTCG104EF104F

Figure 9. Example of Derating Setting Using Thermistor Resistance

3. Boost DC / DC controller

(1) Concerning open detection voltage setting(OPEN DET)

Open of LED is detectable by inputting resistance division connected to anode side of LED (DC / DC output V_{OUT}) in ODT terminal. LED open detection voltage is detectable by connecting external resistors (R_{ODT1}, R_{ODT2}) as shown in Figure 10, and output voltage VOUT_ODT at the time of LED open detection voltage is calculable as shown below.

$$V_{OUT\_ODT} = \frac{(R_{ODT1} + R_{ODT2})}{R_{ODT2}} \times 1.5V(Typ)$$

(Example)
LED open detection will operate with V_{OUT_ODT} = 34.5 V when R_{ODT1} = 660 kΩ and R_{ODT2} = 30 kΩ.

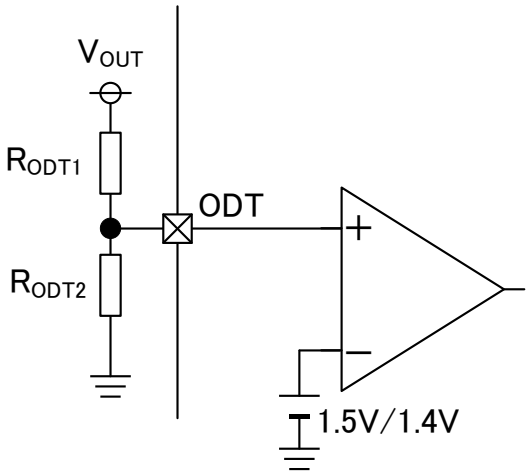


Figure 10. ODT terminal Equivalent Circuit

Recommended setting range is ODT terminal voltage at the time of normal LED drive of 1.1 V < V_{ODT} < 1.35 V. Start-up failure may occur due to overshoot of output voltage during start up when V_{ODT} > 1.35 V, and withstand voltage of external parts needs to be raised because LED open detection voltage becomes higher when V_{ODT} < 1.1 V. ODT resistor will be the current discharge path for the output capacitor when PWM = Low. Recommended value for R_{ODT1} is 600 kΩ to 1000 kΩ as Vout ripple may be large and cause LED flickering when PWM = Low with inadequate ohmic value range. Moreover, the behavior differs by characteristic of output capacitor or LED, therefore sufficient verification with actual application is required.(Vout drop can be prevented by inserting bigger output capacitor or ODT resistance.)

(2) Concerning number of LED series stages

As shown in Figure 11, although IMP terminal is connected to boost DC / DC output at highest voltage among applications.
The number of the steps of the LED which can be driven is decided by the LED opening detection voltage instead of 65V that is withstand voltage. The recommended operating ratings of the ODT pin becomes 1.1 V < VODT < 1.35 V. Therefore real maximum voltage VOUT_MAX which can be output is as follows.

$$65 \times \frac{1.35V}{1.65V} \fallingdotseq 53.2V$$

In other words, drivable LED series stage N is calculable by the formula below.

$$V_{F\_MAX} \times N + V_{REF\_MAX} < 53.2V$$

VF_MAX: maximum value of VF of LED
N: number of LED series stages
VREF_MAX: maximum value of standard voltage for LED current setting

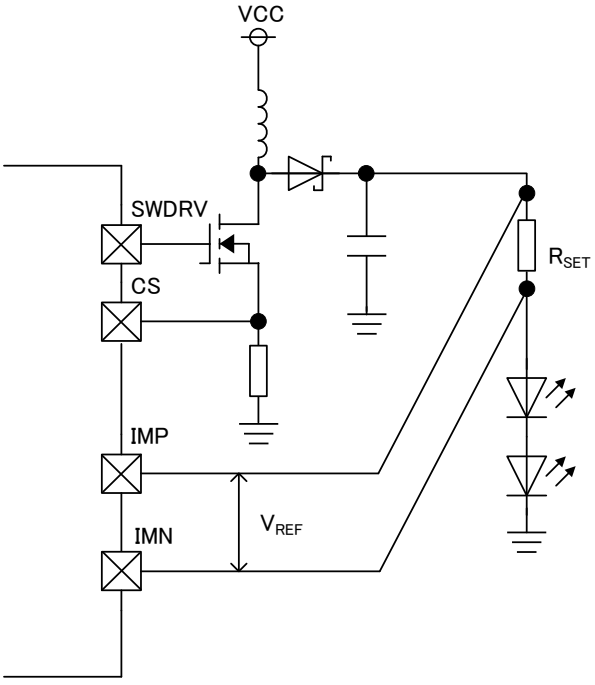


Figure 11. Example of Application Circuit

(Example)
When V_{F_MAX} = 3.5 V and V_{REF_MAX} = 0.206 V, number of drivable LED series stages N is as shown below.

$$N < (53.2V - 0.206V) / 3.5V = 15.14$$

LED drivable number of LED stages is 15.

(3) Concerning oscillation frequency F_{osc}(OSC)

Connection of resistance with RT terminal enables setting of oscillation frequency as shown in Figure 12. Connection of R_{RT} decides charge and discharge current for internal capacitor and changes DC / DC oscillation frequency. Set R_{RT} by reference to the theoretical formula below. Recommended range is 14 kΩ to 51 kΩ. Pay attention that switching may stop if recommended frequency setting range is exceeded, and operation assurance is not possible.

$$F_{OSC} = \frac{99 \times 10^2}{R_{RT}[k\Omega]}[kHz]$$

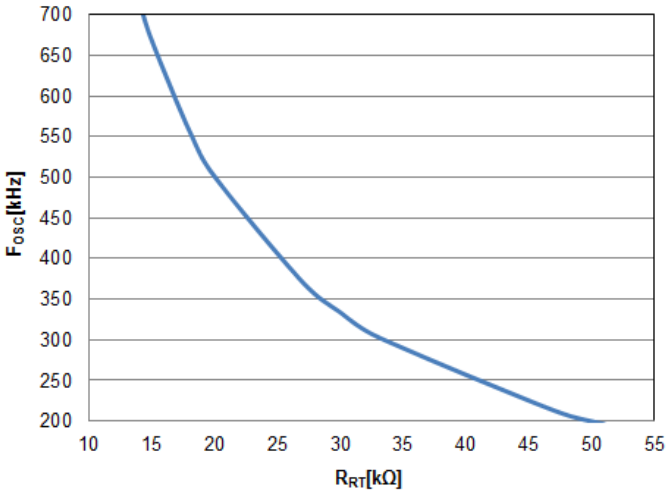


Figure 12. R_{RT} vs DC / DC Oscillation Frequency F_{OSC}

(4) Concerning spread spectrum setting(RAMP)

Connection of capacitor to RS terminal enables operation in Spread spectrum mode (SSCG mode). Comparator of 0.6 V (Typ) / 0.75 V (Typ) standard voltage is built in RS terminal, and DC / DC oscillation frequency is diffused by changing RT terminal voltage to triangle waveform with the capacitor connected to RS terminal in SSCG mode. Theoretical attenuation ΔD [dB] is calculable by the formula below.

$$\Delta D[dB] = 10 \times \log\left(\frac{F_{RS}\,[kHz]}{F_{OSC\_RAMP}[kHz] \times 0.222}\right)$$

F_{OSC_RAMP}: oscillation frequency when SSCG mode is ON (Center)
F_{OSC}: oscillation frequency when SSCG mode is OFF
C_{RS}: RS terminal connection capacitor
R_{RT}: RT terminal connection resistance

However, setting value of DC / DC oscillation frequency differs depending on ON / OFF of SSCG mode. In order to operate when SSCG mode is ON in the same frequency zone as when SSCG mode is OFF, select from Figure 12 RT resistance for 1.18 times as high DC / DC oscillation frequency as the DC / DC oscillation frequency. When SSCG mode is not used, short-circuit RS terminal and VREG50 terminal.

Further, F_{RS} can be calculated by the formula below. Setting should satisfy the formula of 0.3 kHz ≤ F_{RS} ≤ 10 kHz.

$$F_{RS}[kHz] = \frac{9}{8 \times R_{RT}[k\Omega] \times C_{RS}[\mu F]}$$

(Example) When using at DC / DC oscillation frequency (F_{OSC_RAMP}) of 300 kHz with SSCG mode is ON, select RRT ≒ 28 kΩ from Figure 12 to make DC / DC oscillation frequency (F_{OSC}) to be 354 kHz. When operating under this condition with connection of CRS = 0.047μF and with SSCG mode ON, effect of ΔD = -18.9 dB can be predicted.

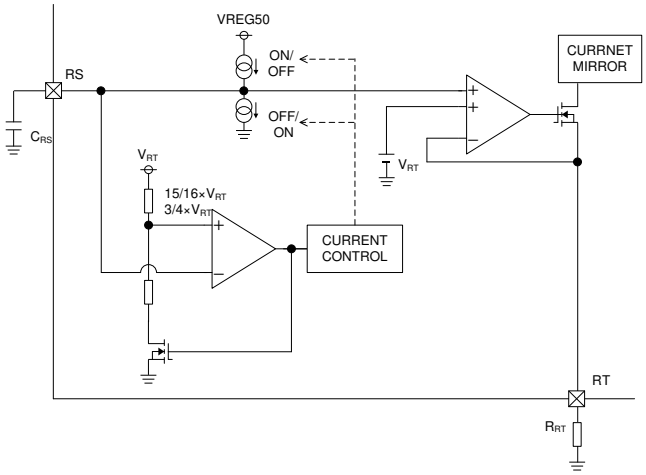


Figure 13. Equivalent Circuit Diagram of RS and RT terminals

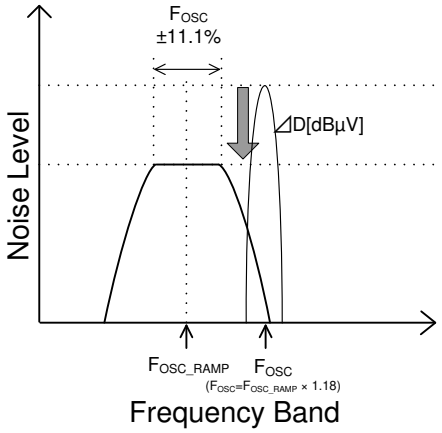


Figure 14. Noise Level Comparison with SSCG Mode ON / OFF

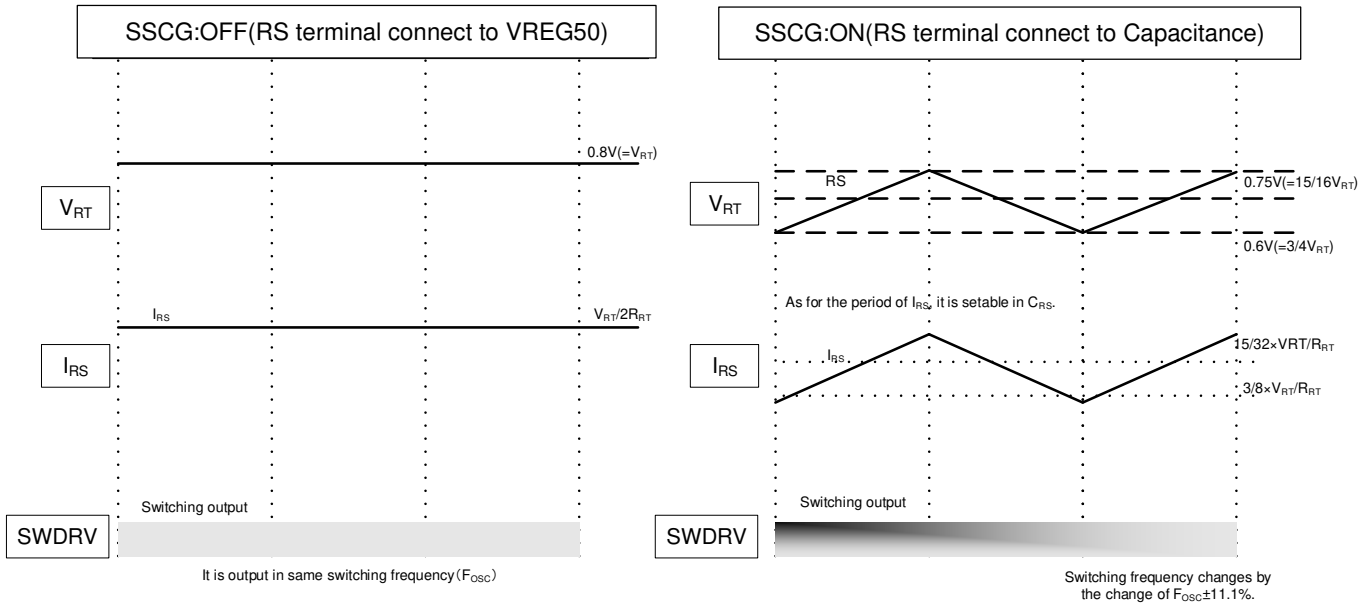


Figure 15. Timing Chart when SSCG Mode is ON / OFF

Because switching frequency changes in High section of the PWM like Figure 16 when spectrum spreading is controlled in a PWM dimming, an output voltage ripple changes in A and B. In addition, the LED current is also affected by the ripple as it may seem that LED flickers when this occurs periodically, please thoroughly verify with the actual equipment. As countermeasures, make the frequency of the RS pin fast to reduce a ripple in High section of the PWM.

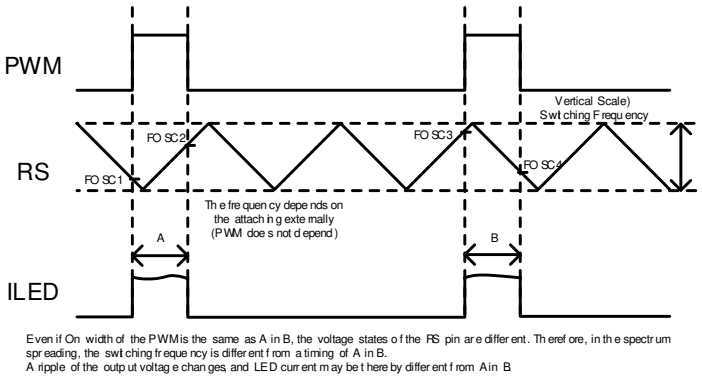


Figure 16. Spectrum Spread Action in the PWM Dimming

(5) Soft start function(SS)

Soft start function is built-in so that incoming current can be prevented by insertion of external capacitor. The charge current of the soft start is 5 μA (Typ) and will be as Figure 17 independent to PWM. The inrush current can be suppressed by increasing soft start capacity, but boot-time becomes longer. On the other hand, as for the boot-time, it becomes faster by lowering soft start capacity, attention is necessary because an inrush current becomes bigger, and may cause acoustic noise of the coil during the startup. The soft start capacity is recommend to be 0.01 μF to 1 μF to suspend the overshoot of the LED current during start up.

The RS terminal is pulled up by VREG50 until SS terminal arrives at 70%of VREG50 as soon as EN terminal is inputted High voltage . After that, RS terminal starts to be controlled.
(See the timing chart of SS terminal and RS terminal in the P.28 Figure.44)
Therefore, Spread spectrum don't operate as soon as EN terminal is inputted High voltage, even if connect a capacitor to RS terminal

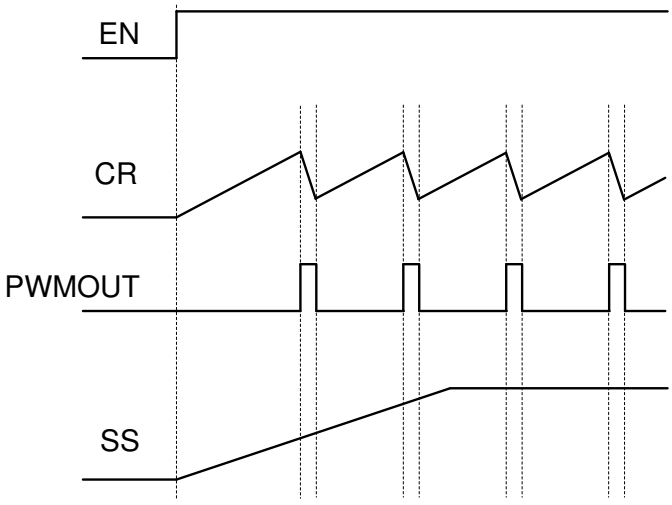


Figure 17. SS Operation Timing Chart

(6) Concerning start up time(ERRAMP)

Startup time difference between PWM = 100 % (DRL = High) and PWM dimming control is described in this paragraph

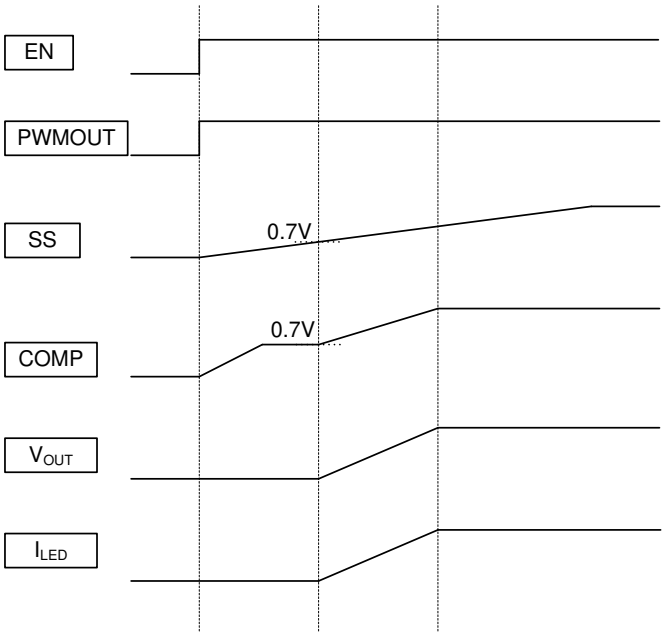


Figure 18 (a). PWM = 100% start up

SS terminal and COMP terminal is charged, When EN is inputted. Until SS terminal reaches 0.7 V, COMP terminal is fixed at 0.7 V. When SS terminal exceeds 0.7V, COMP terminal starts to rise up to voltage which can output required switching duty determined by input/output voltage difference.

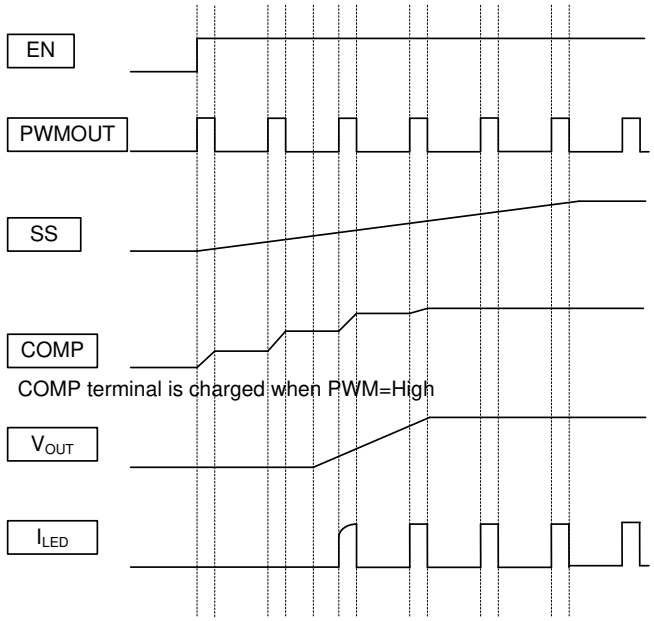


Figure 18 (b). PWM Dimming start up

During PWM control, SS terminal is charged synchronized with EN while COMP terminal is charged synchronized with PWM. Startup time is basically same with previous description but as charge of COMP terminal is synchronized with PWM, COMP voltage rise to the voltage which can output required switching duty will be slower resulting In longer start up time compared with PWM = 100 % operation. Especially by reducing PWM dimming rate, start up time will be longer.

Figure 19 describes actual measurement result of startup time.
Measurement Condition: V_{CC} = 12 V, F_{PWM} = 200 Hz, V_{OUT} = 25 V (LED 7series), Ta = 27deg, other condition as described in P.38.
(Startup time will be from UVLO release to V_{OUT} reaching 90 %.)

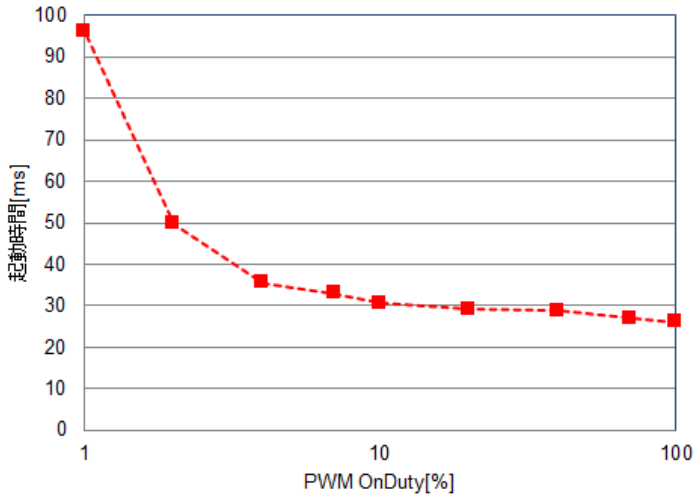


Figure 19. Startup time measurement data

Larger the C_{PC} constant is, and smaller D_{PWM} is, start up time will be longer. Startup time shall be sufficiently evaluated in actual application.

4. Self-assessment function

Table 1. Concerning detection condition and operation after detection of each protection function (when VCC = 13 V)

Protection function	Detection condition		Operation after detection	Error flag output (Note 1)
	[Detection]	[Release]		
UVLO	V_{CC} < 3.9 V	V_{CC} > 4.25 V	Shut down of all blocks (Other than VREG50 / VREG25)	At time of detection: FAIL High⇒Low At time of recovery: FAIL Low⇒High
TSD	Tj > 175 °C	Tj < 150 °C	Shut down of all blocks (VREG50 / VREG25 are included)	-
OCP	V_{CS} ≥ 300 mV	V_{CS} < 300 mV	Switching output is Off	-
SCP	V_{IMP}-V_{IMN} ≥ 0.3 V	V_{IMP} - V_{IMN} < 0.3 V (Timer time depends on TDISC setting)	Shut down of all blocks (Other than VREG50 / VREG25)	At time of detection: FAIL High⇒Low At time of recovery: FAIL Low⇒High
LED open detection	V_{ODT} > 1.5 V	V_{ODT} < 1.4 V	Shut down of all blocks (Other than VREG50 / VREG25)	At time of detection: FAIL High⇒Low At time of recovery: FAIL Low⇒High

(Note1) FAIL output shown above is FAIL terminal voltage in the case of pull-up resistance such ad external power.

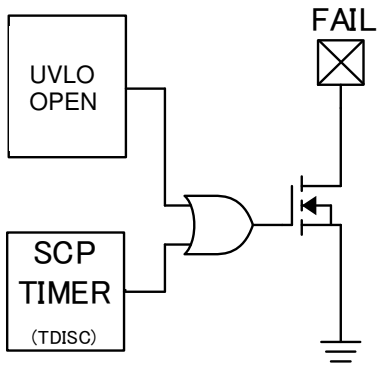


Figure 20. Protection Flag Output Part Block Diagram

(1)Low voltage malfunction protection function (UVLO)
The UVLO shuts down all the circuits except VREG50, VREG25 when V_{CC} < 3.9V (Typ) And UVLO is released by Vcc > 4.25 V (Typ).

(2) Temperature protection function (TSD)
TSD shuts circuits other than VREG at 175 °C (Typ) and recovers them at 150 °C (Typ).

(3) Over current protection function (OCP)
Over current is detected by the detection resistance with which current flowing in power FET is connected to source side. Over current protection function operates when CS terminal voltage is no less than 300 mV (Typ).The over current protection function controls DC / DC switching outputs.

(4) Output ground detection function (SCP)
When, in an application circuit such as Figure 45, LED Anode- GND short-circuits, the potential difference of IMP terminal and the IMN terminal is more than 0.3 V (Typ), and a ground detection function works, and the output is off. When ground protection is activated, charge (11 μA (Typ)) is started to a capacitor connected to TDISC terminal (recommend range: 0.01μF to 0.47μF). After TDISC terminal voltage arrived at 1.0V (Typ), the TDISC terminal discharges and Low⇒High outputs SWDRV / PWMOUT again. A ground detection function works again afterwards when the potential difference of IMP terminal and the IMN terminal becomes than 0.3 V (Typ). In addition, it works normally when TDISC terminal voltage becomes less than 0.3V (Typ), and the potential differences of IMP terminal and the IMN terminal become less than 0.3 V (Typ). As for the details, please refer to Figure 21. (Note that GND short-circuit of the IMP terminal cannot be detected.)

(5) LED open detection function
When ODT terminal voltage is above 1.5 V (Typ), LED open detection operates to reset SWDRV / PWMOUT = Low, and discharges SS again, outputs Fail High → Low, and the output voltage decreases by ODT resistance. When ODT terminal voltage is less than 1.4 V (Typ), begins to recharge SS, re-starts DC / DC operation and outputs FAIL Low→High.

Timing chart at the time of protection circuit operation (DRL = High)

・Output ground short protection function

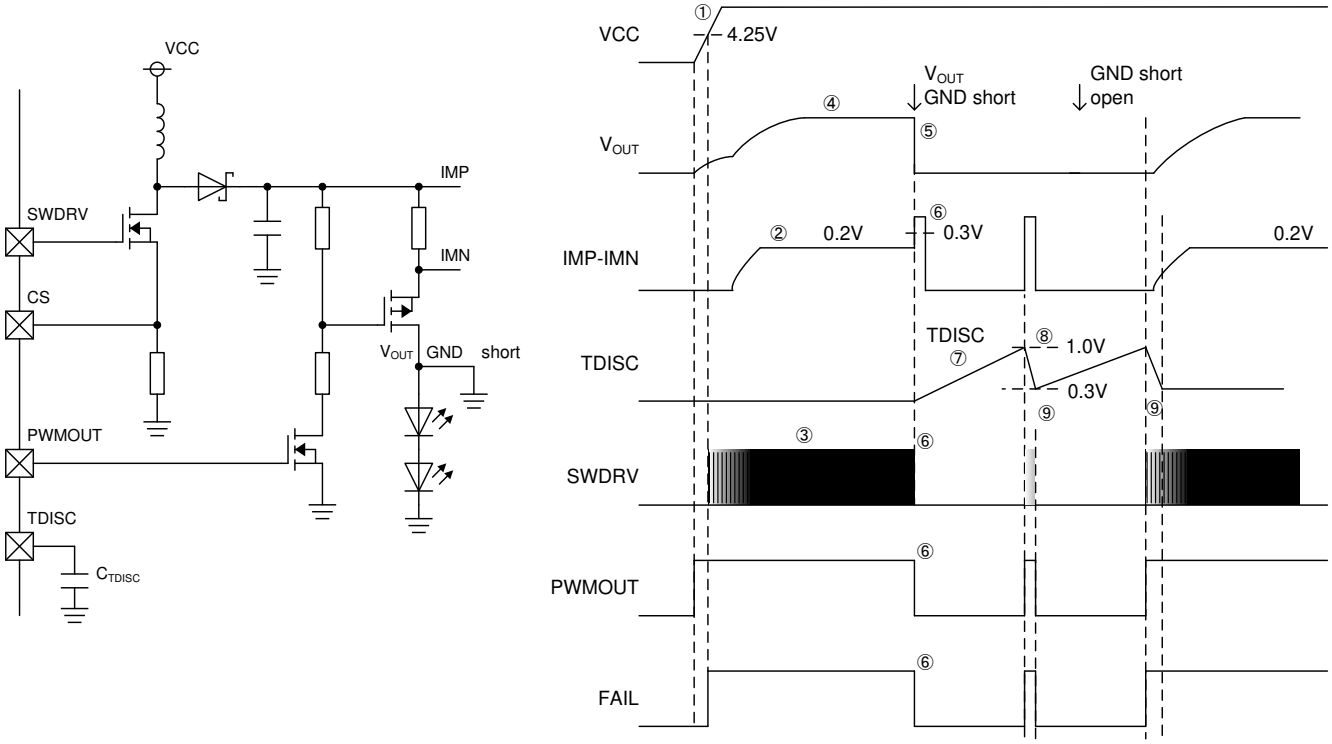


Figure 21. Output Ground short protection operation timing chart

When GND short circuit occurs in such conformation as shown in Figure 1, large current continues to flow from VCC.

① UVLO is cancelled when VCC > 4.25 V (Typ).
② IMP-IMN terminal voltage rises to become 200 mV.
③ Switching Duty gradually expands and is stabilized at IMP-IMN of 200 mV.
④ Output voltage is stabilized.
⑤ LED Anode-GND short-circuits.
⑥ It becomes IMP-IMN ≥ 0.3 V (Typ) and performs output Short circuit detection (SCP) and outputs SWDRV / PWMOUT = Low. Discharges an SS terminal and the FAIL terminal changes into High ⇒ Low.
⑦ When SCP is detected, capacitor connected to TDISC will be charged (11 μA (Typ)) until V_{TDISC} becomes 1.0 V (Typ).
⑧ Once SCP detection is released at V_{TDISC} ≥ 1.0 V (Typ), capacitor connected to TDISC starts to discharge, and SS charging, SWDRV / PWMOUT operate normally.
⑨ If SCP condition V_{TDISC} ≥ 0.3 V (Typ) is fulfilled restarts from condition ⑥ operates normally if SCP condition is not fulfilled.

Operation described above is performed in the LED anode ground short fault. However, even if SCP is detected by the potential difference of IMP pin and the IMN pin, there is delay time of internal circuit after detection and require time before PchMOS is off. Therefore allowable current of PchMOS may be exceeded transiently.(It may be exceeded in ⑧ of the timing mentioned above.) Therefore, like Figure 22, PMOS can be turned off on an expressway by adding PNP Tr externally.
When Output shorts to ground while supply voltage dropping, Gate voltage may not be turned off. If sufficient Gate voltage cannot be secured SCP may not be detected.

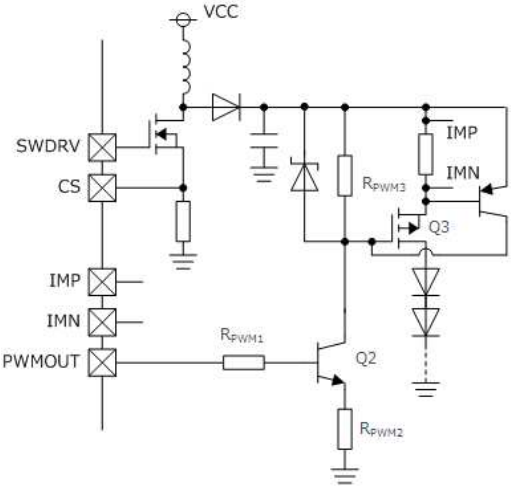


Figure 22. LED Anode Ground Fault Protection Attaching Externally Circuitry

・LED open protection function (DRL = High)

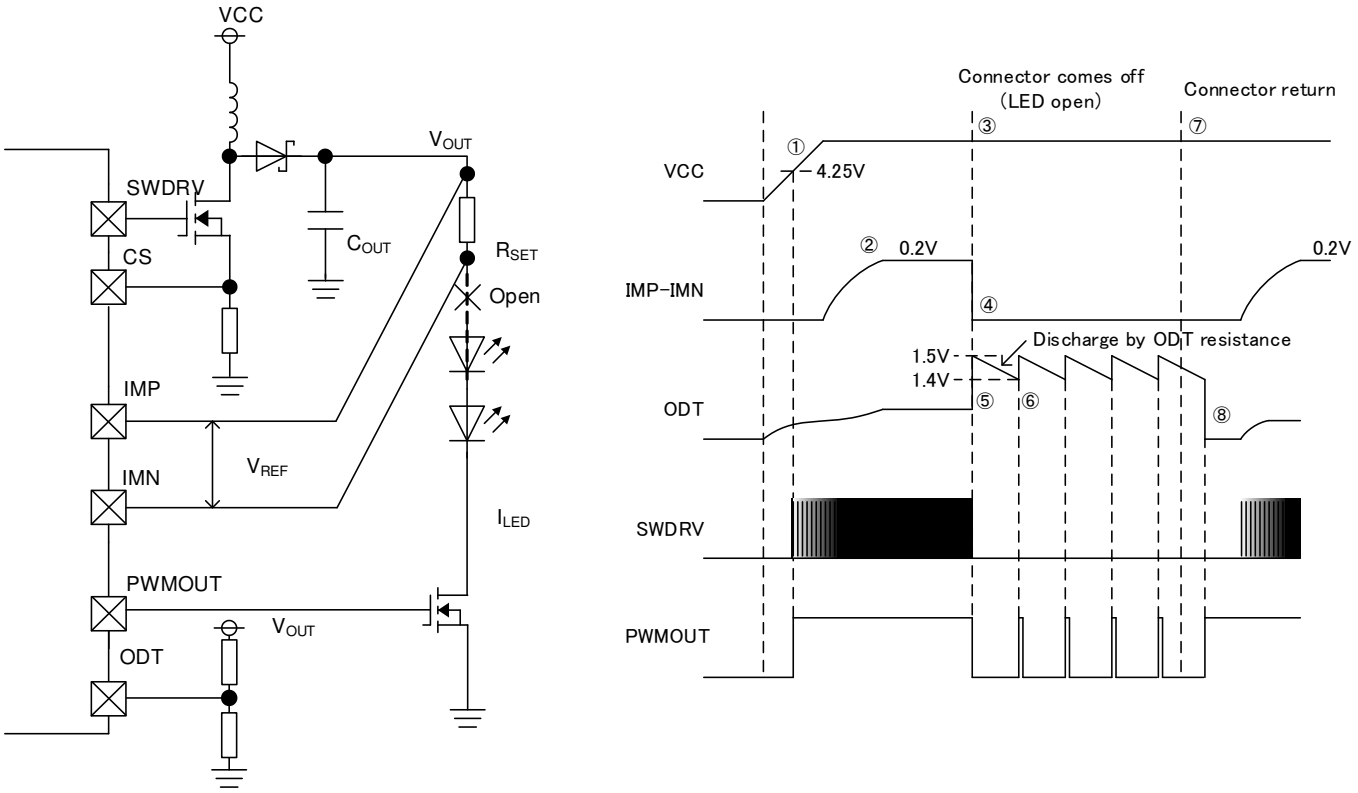


Figure 23. Output Ground Short Protection Operation Timing Chart

① UVLO is released when VCC > 4.25 V (Typ).
② IMP-IMN terminal voltage rises to become 200 mV.
③ Connector of LED opens.
④ Output voltage over boost due to IMP-IMN ≒ 0 V. (ODT which is resistor divided voltage of output voltage will steeply rise.)
⑤ When ODT ≥ 1.5 V, LED open is detected and SWDRV / PWMOUT becomes Low. Also, SS pin will be discharged and Fail pin becomes High = > Low.
⑥ The LED open detection is released at ODT ≤ 1.4 V, and the FAIL terminal becomes Low ⇒ High.
Then DC / DC restarts the operation, however due to LED open condition voltage will be over boosted again.
⑦ LED is connected again.
⑧ When ODT ≤ 1.4 V, will be re-started and resumes to normal operation.
(During ⑧ condition if PWMOUT = High is applied while capacitors are still charged above nominal Vout, it could detect SCP detection due to IMP-IMN ≥ 0.3 V. After T_{TDISC} resumes to normal operation.)

5. Output electric charge electric discharge circuit (VOUTDISC)

When supply voltage of LSI is turned off in such configuration as shown in Figure 24, output capacitor may not be fully discharged and may remain charged in some cases. When power is supplied again while output capacitor is charged,transient current flows through the route of output capacitor→R_{SET}→LED→PWM dimming FET→GND which cause LED flashing. Later, when switching duty is output, LED is lit. In order to suppress such a flash phenomenon, this LSI incorporates output charge discharge circuit.

In order for output discharge circuit to operate, discharge of output capacitor starts when either one of the conditions of ① UVLO is detected (VCC ≤ 3.9 V) or ② V_{EN} ≤ 1.35 V are satisfied. (Output discharge circuit is also operated at LED open detection.)

Turn off PWM after EN turned off power supply OFF sequence when PWM input is controlled with an external signal.

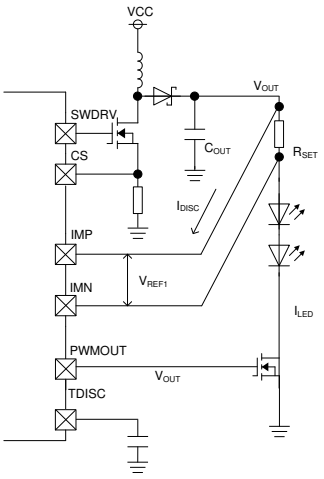
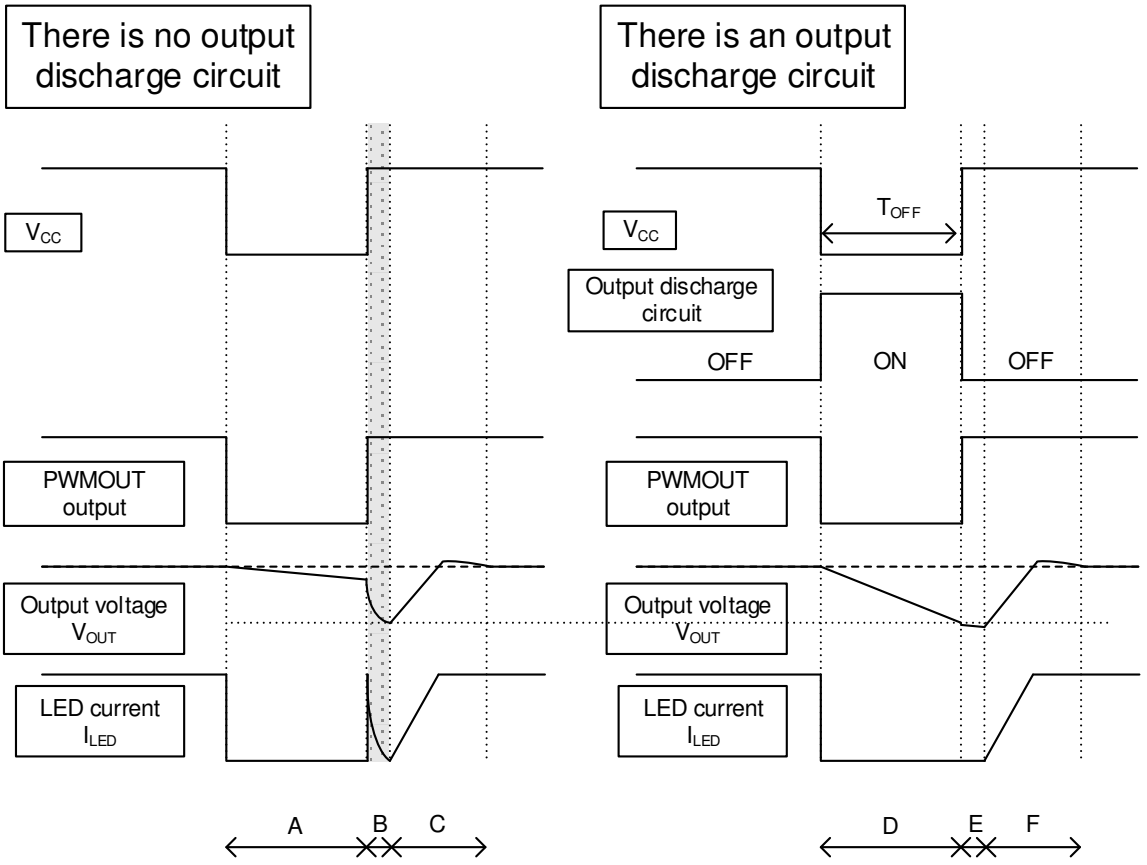


Figure 24. Application Example



A. Because V_{CC} is off, and the PWMOUT terminal is off, the LED current does not flow. Because PWMOUT terminal is OFF, output capacitor C_{OUT} is discharged by resistance connected to ODT terminal, and output voltage V_{OUT} gradually decreases.

B. When V_{CC} is turned on again, getting started of output voltage V_{OUT} is late by a soft start function. On the other hand, the PWMOUT terminal is turned on in sync with a reintroduction of V_{CC}. Therefore LED current flows from an output capacitor transiently, and LED shines for an instant, and LED darkens when the electric charge of the output capacitor is discharged besides.

C. Output voltage stands up, and LED turns on again.

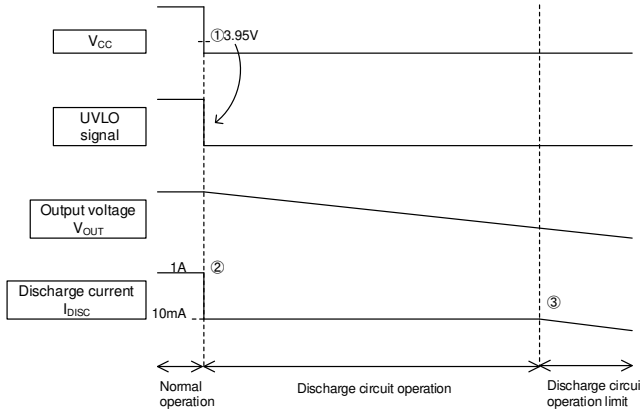
D. Because V_{CC} is off, and the PWMOUT terminal is off, the LED current does not flow. Because PWMOUT terminal is OFF, output capacitor COUT is discharged by resistance connected to ODT terminal. However, the output electric charge electric discharge circuit in the IMP terminal works, and output voltage V_{OUT} greatly decreases.

E. When V_{CC} is turned on again, getting started of output voltage V_{OUT} is late by a soft start function. On the other hand, the PWMOUT terminla is turned on in sync with a reintroduction of V_{CC}, but the LED does not shine because V_F cannot open.

F. Output voltage stands up, and LED turns on.

Figure 25. Output Discharge Circuit Operation Explanation at the time of the VCC Drop

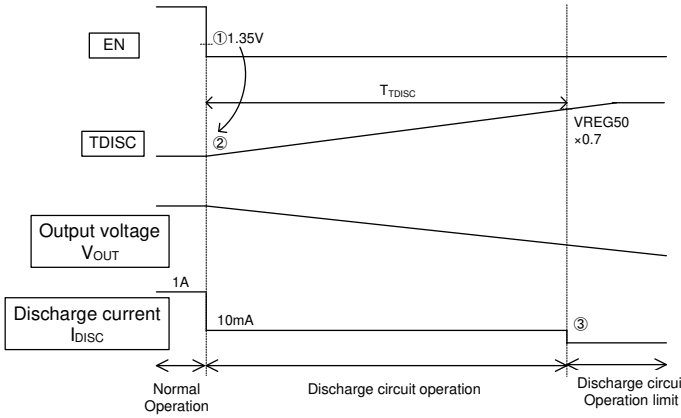
Concerning output discharge circuit operation at the time of UVLO detection



① UVLO is detected when VCC < 3.95 V.
② When UVLO is detected, discharge circuit is turned on to discharge charge accumulated in output capacitor, and output voltage falls by I_{DISC}.
③ I_{DISC} falls accompanying fall of output voltage.
(Refer to electric properties of output voltage V_{OUT} and discharge current I_{DISC}.)

Figure 26. Explanation of Output Discharge Circuit Operation at UVLO Detection

Concerning output discharge circuit operation by EN control



①When EN ≤ 1.35 V, EN is turned off.
②Output is discharged during output discharge time (T_{TDISC}) set by capacitor connected to TDISC.

$$T_{\mathrm{TDISC}} = \frac{VREG50 \times 0.7 \times C_{TDISC}}{11\mu A}$$

③When discharge time T_{TDISC} elapsed, output discharge circuit stops operation.

Figure 27. Explanation of Output Discharge Circuit Operation when EN is off

The recommended capacitance value for this function is 0.01 μF to 0.47 μF, Please do not to connect TDISC to GND. Caution that even if the values are within recommended range, when output voltage is higher and C_{TISC} is higher heat dissipation by discharge is to be considered. Sufficient verification by actual application is required.
Flash phenomena is affected by Vf characteristic of LED and time to re-enter power supply. This is also to be sufficiently verified with actual application.

6. About EN terminal setting (EN CTL)

ON / OFF of the LSI can be controlled by applying resistor devided voltage from power supply to EN terminal. Setting of the EN terminal voltage to control ON / OFF of the LSI is as follows.

$$V_{\mathrm{CCON}} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times 1.45V(Typ)$$

$$V_{\mathrm{CCOFF}} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times 1.35V(Typ)$$

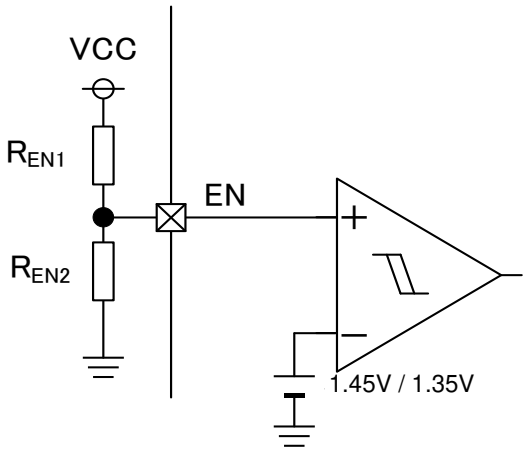


Figure 28. About EN terminal setting

Ex)
The VCC terminal voltage to stop / start operation is as follows with REN1 = 150 kΩ, REN2 = 51 kΩ condition

The operation start voltage

$$V_{\mathrm{CCON}} = \frac{(150k\Omega + 51k\Omega)}{51k\Omega} \times 1.45V(Typ) = 5.71V$$

The operation stop voltage

$$V_{\mathrm{CCOFF}} = \frac{(150k\Omega + 51k\Omega)}{51k\Omega} \times 1.35V(Typ) = 5.32V$$

For PWM dimming, do not control PWM with the EN terminal as it may result in unstable operation.
PWM dimming, is to be controlled with CR terminal. (Please refer to P.4 to 6 for the details.)

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Power Voltage	V_{CC}	-0.3 to 70	V
EN, DRL Terminal Voltage	V_{EN}, V_{DRL}	-0.3 to VCC+0.3	V
IMP, IMN Terminal Voltage	V_{IMP}, V_{IMN}	-0.3 to 70	V
The Voltage between IMP and IMN	$V_{IMP}-V_{IMN}$	3	V
VREG50, CS, RS, RT, VREG25, DISC, ODT, PWMOUT, DCD, SS COMP, SWDRV, FAIL , TDISC terminal voltage	V_{VREG50}, V_{CS}, V_{RS}, V_{RT}, V_{VREG25} V_{CR}, V_{DISC}, V_{ODT}, V_{PWMOUT}, V_{DCD}, V_{SS}, V_{COMP}, V_{SWDRV}, V_{FAIL}, V_{TDISC}	-0.3 to 7 < VCC	V
Operation Temperature Range	Topr	-40 to 125	°C
Storage Temperature Range	Tstg	-55 to 150	°C
Junction Temperature	Tjmax	150	°C

Caution: Deterioration or break may occur when absolute maximum ratings of applied voltage, operation temperature range, etc. are exceeded. Also, breaking situation such as short circuit mode or open mode cannot be assumed. If special mode exceeding absolute maximum rating is assumed, please consider physical safety measures such as fuse.

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
HTSSOP-B24				
Junction to Ambient	θ_{JA}	143.8	26.4	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	7	2	°C/W

(Note 1) Based on JESD51-2A (Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(NOTE 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Ratings (Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Power Voltage *(Note 1)*	V_{CC}	4.5	12	65	V
Output Voltage *(Note 2)*	V_{IMP}	6.0	40	65	V
DC / DC Switching Frequency (With Spread Spectrum Control OFF)	F_{OSC1}	200	-	700	kHz
DC / DC Switching Frequency (With Spread Spectrum Control ON)	F_{OSC2}	200	-	600	kHz
CRTIMER Frequency	F_{PWM}	100	-	2000	Hz
CRTIMER Output Duty	F_{DUTY}	2	-	45	%
Spectrum Spread Frequency	F_{RS}	0.3	-	10	kHz

(Note 1) Apply voltage of no less than 5 V once at the time of stat-up. The value is voltage range after once setting at no less than 5 V.
(Note 2) When become the condition mentioned above except for startup at Boost application, it's possible that large current flow in LED.

Operating Condition (External Constant Range)

Parameter	Symbol	Min	Max	Unit
Capacitance for CRTIMER Frequency/Duty Setting	C_{CR}	0.01	1.0	μF
Resistance for CRTIMER Frequency/Duty Setting	R_{DISC2}	10	33	kΩ
Resistance for DC/DC Frequency	R_{RT}	14	51	kΩ
Capacitance for Soft-Start Setting	C_{SS}	0.01	1.0	μF
Capacitance for TDISC Setting	C_{TDISC}	0.01	0.47	μF
Resistance of OVP Setting of VOUT Side	R_{OVP1}	600	1000	kΩ

Electrical Characteristics (Unless otherwise specified V_{CC} = 13 V, V_{IMP} = 40 V, Ta = -40 °C to 125 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Circuit Current	I_{CC}	-	3	6	mA	C_{VREG} = 2.2 µF, V_{CS} = V_{ODT} = 0 V V_{EN} = V_{DRL} = V_{CR} = GND V_{RS} = V_{VREG50} V_{DCD} = V_{RT} = V_{VREG25}
[VREG]						
VREG50 Standard Voltage	V_{VREG50}	4.5	5.0	5.5	V	C_{VREG50} = 2.2 µF
VREG25 Standard Voltage	V_{VREG25}	2.425	2.50	2.575	V	I_{VREG25} = 0µA
VREG25 Load Regulation Voltage	ΔV_{VREG25}	-	50	100	mV	I_{VREG25} = 0µA to 250 µA
[SWDRV]						
SWDRV Upper Side ON Resistance	R_{SWP}	-	4	8	Ω	I_{ON} = -10 mA
SWDRV Lower Side ON Resistance	R_{SWN}	-	3	6	Ω	I_{ON} = 10 mA
Overcurrent Protection Voltage	V_{OCP}	250	300	350	mV	V_{CS}: Sweep up
[LED Current Setting Block]						
LED Current Setting Standard Voltage	V_{REF1}	194	200	206	mV	Voltage between V_{IMP} - V_{IMN} terminals.
LED Ground Short Detection Voltage	V_{SCPON}	0.24	0.3	0.36	V	$V_{SCP} \geq V_{IMP} - V_{IMN}$
LED Open Detection Voltage	V_{OPEN}	1.35	1.5	1.65	V	V_{ODT}: Sweep up
LED Open Hysteresis Voltage	$V_{HYSOPEN}$	-	0.1	-	V	V_{ODT}: Sweep down
TDISC Charge Current	I_{TDISC}	4	11	18	µA	V_{TDISC} = 0V
TDISC Short Timer Detection Voltage	V_{DTDISC}	0.9	1.0	1.1	V	V_{TDISC}: Sweep up
TDISC Short Timer Release Voltage	V_{RTDISC}	0.2	0.3	0.4	V	V_{TDISC}: Sweep down
EN OFF TDISC Discharge Stop Voltage	V_{TDISC}	V_{VREG50} × 0.55	V_{VREG50} × 0.7	V_{VREG50} × 0.85	V	
Vout Discharge Time	T_{TDISC}	20	35	55	ms	C_{TDISC} = 0.1 µF
Output Charge Discharge Current	I_{DISC}	3	10	-	mA	V_{IMP} = 12 V
[CR TIMER]						
CR Threshold Voltage 1	V_{CRTH1}	V_{VREG50} × 0.18	V_{VREG50} × 0.20	V_{VREG50} × 0.22	V	
CR Threshold Voltage 2	V_{CRTH2}	V_{VREG50} × 0.36	V_{VREG50} × 0.40	V_{VREG50} × 0.44	V	
PWM Minimum Pulse Width	T_{PWM}	100	-	-	µs	
PWMOUT Upper Side ON Resistance	$R_{PWMOUTP}$	-	20	40	Ω	I_{ON} = -10 mA
PWMOUT Lower Side ON Resistance	$R_{PWMOUTN}$	-	5	10	Ω	I_{ON} = 10 mA

Electrical Characteristics (Unless otherwise specified V_{CC} = 13 V, V_{IMP} = 40 V, Ta = -40 °C to 125 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
[ERRAMP]						
COMP Source Current	I_{COMPSO}	-90	-60	-30	µA	V_{COMP} = 1.2 V, V_{DCD} = VREG25 V_{IMP} - V_{IMN} = 0 mV
COMP Sink Current	I_{COMPSI}	30	60	90	µA	V_{COMP} = 1.2 V, V_{DCD} = VREG25 V_{IMP} - V_{IMN} = 400 mV
[Soft start]						
Soft Start Charge Current	I_{SS}	3	5	7	µA	V_{SS} = 0 V
[Oscillator]						
DC / DC Switching Frequency	F_{OSC}	270	300	330	kHz	R_{RT} = 33 kΩ
Max Duty Output	D_{MAX}	-	95	-	%	R_{RT} = 33 kΩ
[RAMP]						
RS Frequency	F_{RS}	-	0.75	-	kHz	R_{RT} = 33 kΩ, C_{RS} = 0.047 µF
RS Terminal High Voltage	V_{RSH}	-	0.75	-	V	V_{RS}: Sweep up
RS Terminal Low Voltage	V_{RSL}	-	0.60	-	V	V_{RS}: Sweep down
[UVLO]						
UVLO Detection Voltage	V_{UVLO}	3.6	3.9	4.2	V	V_{CC}: Sweep down
UVLO Hysteresis Width	V_{UHYS}	250	350	450	mV	V_{CC}: Sweep up
[EN/DRL]						
EN Terminal ON Threshold Voltage	V_{ENON}	1.35	1.45	1.55	V	V_{EN}: Sweep up
EN Terminal Hysteresis Voltage Width	V_{HYSEN}	-	100	-	mV	V_{EN}: Sweep down
DRL Terminal Input Current	I_{DRL}	4	13	22	µA	V_{DRL} = 13 V
DRL Terminal ON Threshold Voltage	V_{DRLON}	3	-	-	V	V_{DRL}: Sweep up
DRL Terminal OFF Threshold Voltage	V_{DRLOFF}	-	-	0.8	V	V_{DRL}: Sweep down

Typical Performance Curves (Reference Data)

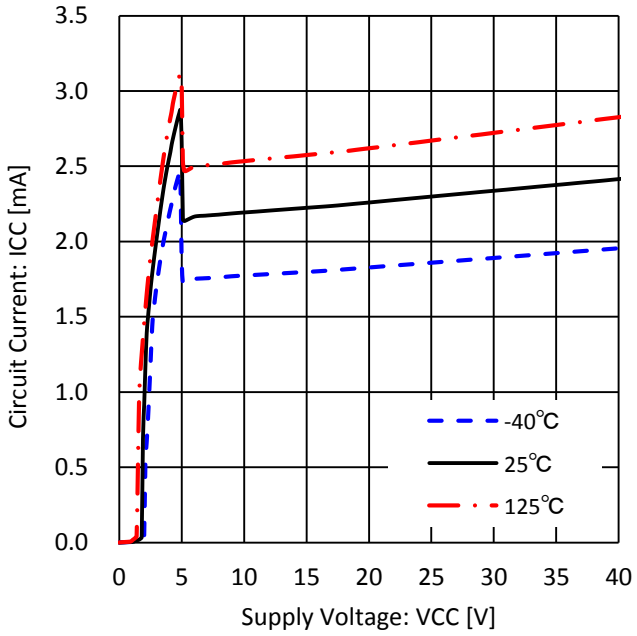


Figure 29. Circuit Current vs Supply Voltage

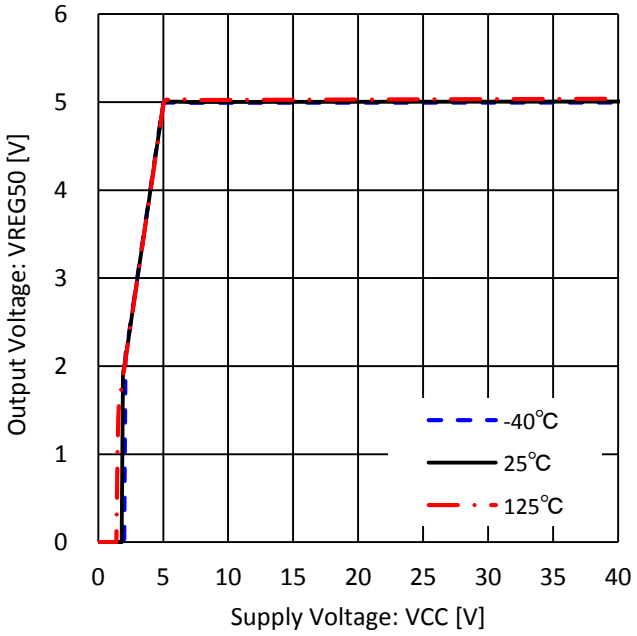


Figure 30. Output Voltage vs Supply Voltage (VREG50)

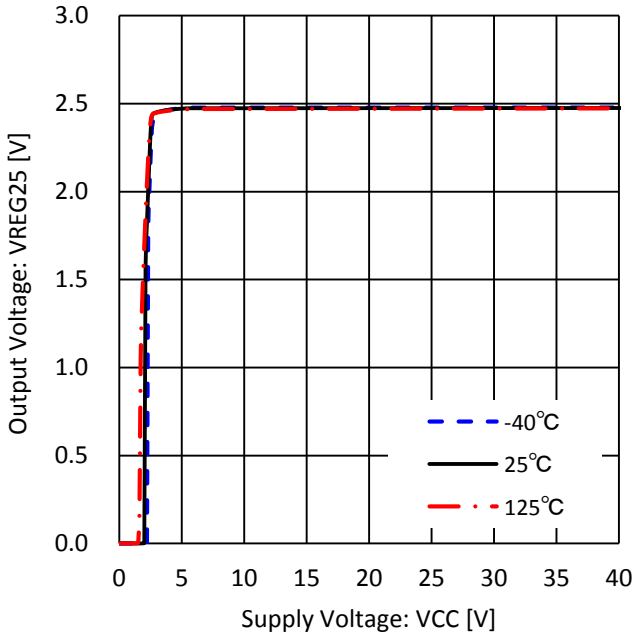


Figure 31. Output Voltage vs Supply Voltage (VREG25)

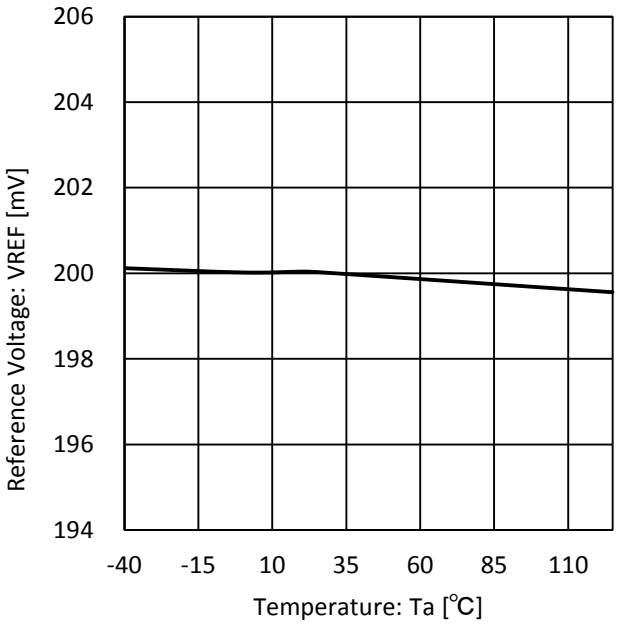


Figure 32. Reference voltage vs Temperature

Typical Performance Curves (Reference Data) - Continued

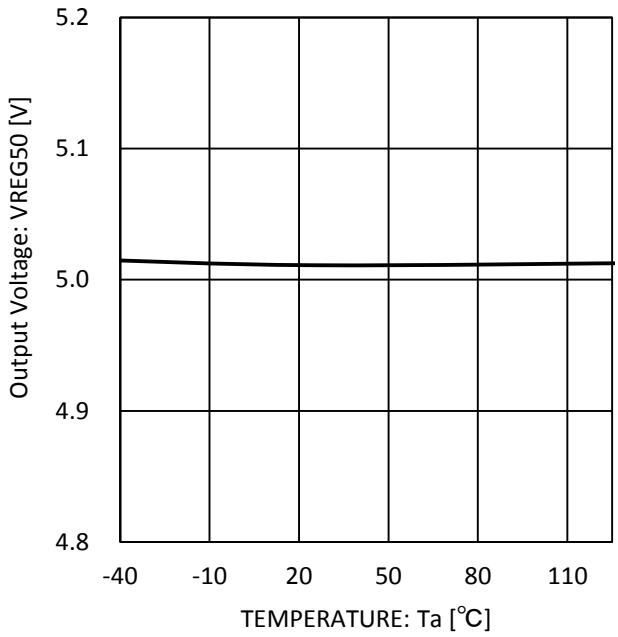


Figure 33. Output Voltage vs Temperature (VREG50)

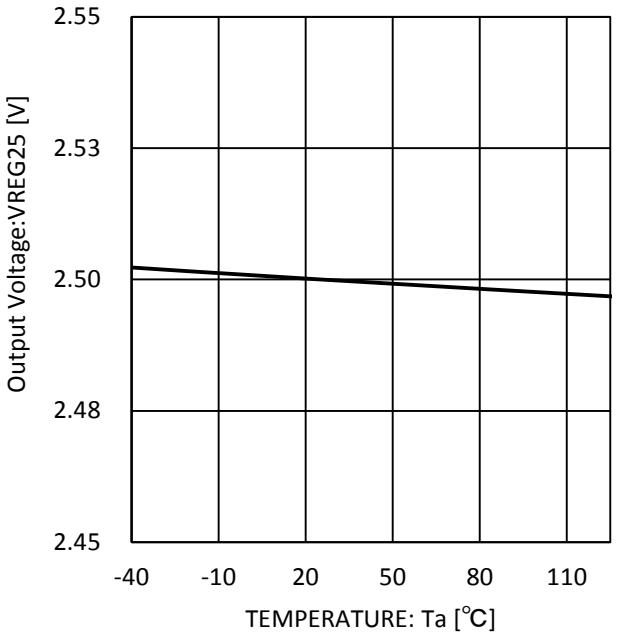


Figure 34. Output Voltage vs Temperature (VREG25)

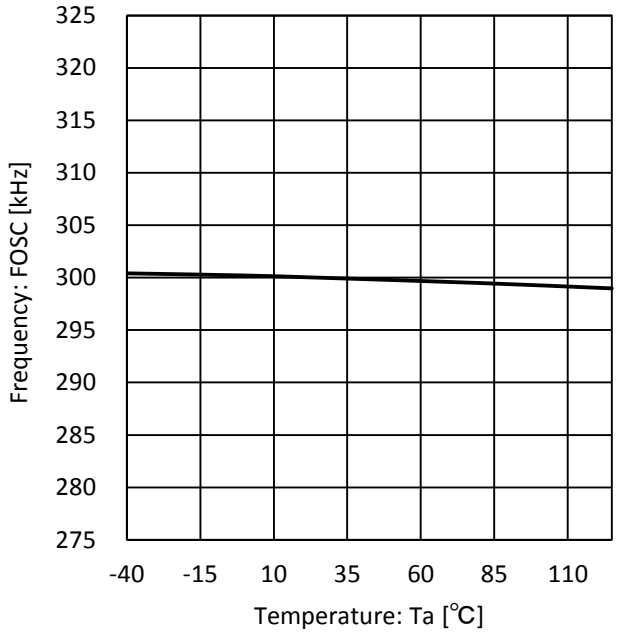


Figure 35. Frequency vs Temperature

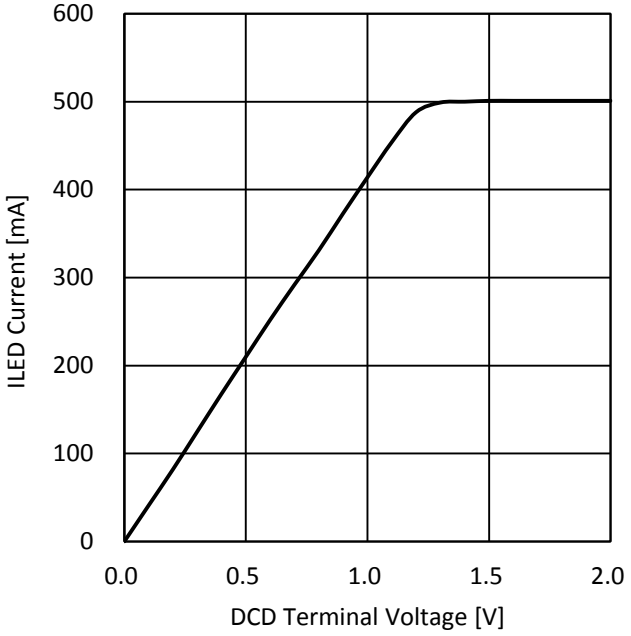


Figure 36. ILED Current vs DCD Terminal Voltage

Typical Performance Curves (Reference Data) - Continued

Figure 37. Spectrum Spread (ON)

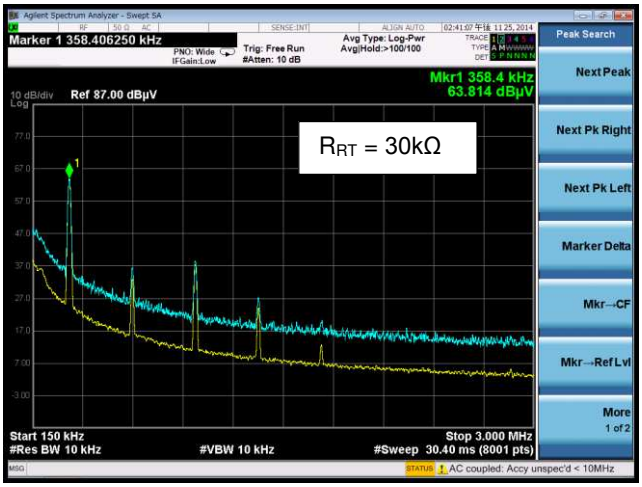


Figure 38. Spectrum Spread (OFF)
(RS = VREG50 Short)

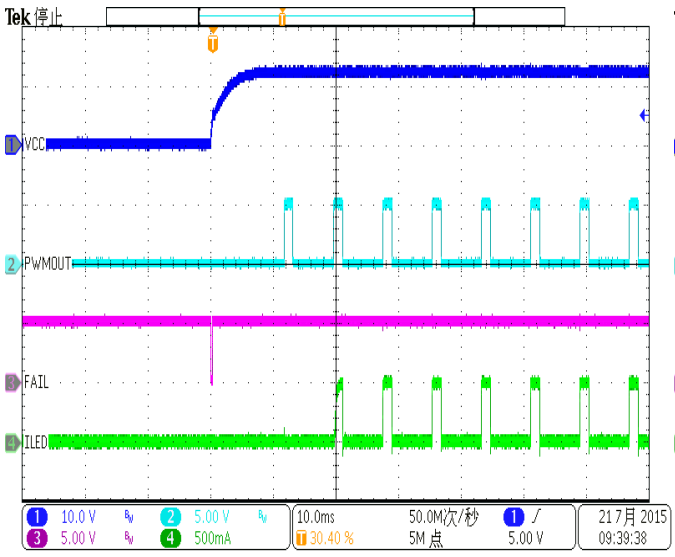


Figure 39. PWM Control Operation Start (DRL = Low)

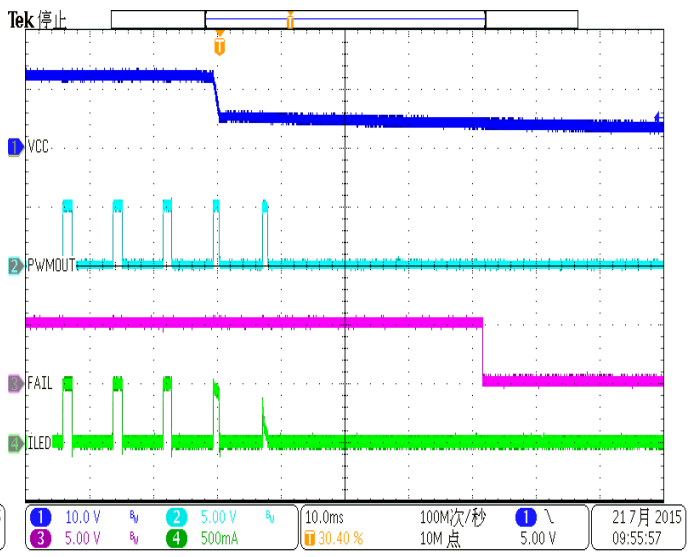


Figure 40. PWM Control Start (DRL = Low)