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System LED Drivers for Mobile Phones

# 7x17(Max.) Dot Matrix LED Display Driver

## BD26503GUL

### ●Description

BD26503GUL is “Matrix LED Driver” that is the most suitable for the cellular phone.
It can control 7x17(119 dot) LED Matrix by internal 7-channel PMOS SWs and 17-channel LED drivers.
It can control the luminance and firefly lighting of the LED matrix by the setting of the internal register.
It supports SPI and I2C interface.
VCSP50L3 (3.6mm□0.55mm height max), small and thin type chip size package.
It adopts the very thin CSP package that is the most suitable for the slim phone.

### ●Features

1) LED Matrix driver (7x17)
   - It has 7-channel PMOS SWs and 17-channel current drivers with 1/7 timing driven sequentially.
   - Put ON/OFF(for every dot).
   - The current drivers can drive 0-20.00mA current with 16 step(for every dot).
   - 64 steps of the luminance control by PWM (common setting for all dots)
   - Continuous (TDMA off ) lighting function for LED14-LED17
   - Easy register setting by A/B 2-side map for each dot.
2) Automatic Slope function
   - Cycle time, Slope time can be set for each dot.
3) 8-direction automatic scroll function.
4) Interface
   - SPI and $I^2C$ BUS FS mode(max 400kHz)Compatibility
   - For $I^2C$ mode, $I^2C$ Device address is selectable (74h or 75h)
5) Thermal shutdown
6) Small and thin CSP package
   - 48pin VCSP50L3 (3.6mm□ 0.55mm height max) 0.5mm ball pitch

*This chip is not designed to protect itself against radioactive rays.
*This material may be changed on its way to designing.
*This material is not the official specification.

### ●Absolute Maximum Ratings (Ta=25 °C)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Maximum voltage (note2) | VMAX | 7 | V |
| Maximum voltage (note1) | VIOMAX | 4.5 | V |
| Power Dissipation (note3) | Pd | 1550 | mW |
| Operating Temperature Range | Topr | -40 ~ +85 | ℃ |
| Storage Temperature Range | Tstg | -55 ~ +150 | ℃ |

note1) VIO,RESETB,CE,SDA,SCL,IFMODE,SYNC,CLKIN,CLKOUT,TEST1,TEST2,TEST3,TESTO, DO terminal
note2) Except the above
note3) Power dissipation deleting is 12.4mW/°C , when it’s used in over 25 °C. (ROHM’s standard board has been mounted.)
The power dissipation of the IC has to be less than the one of the package.

### ●Operating Conditions (VBAT≥VIO, VINSW≥VBAT, Ta=-40~85 °C)

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| VBAT input voltage | VBAT | 2.7 ~ 5.5 | V |
| VINSW input voltage | VINSW | 2.7 ~ 5.5 | V |
| VIO pin voltage | VIO | 1.65 ~ 5.5 | V |

●**Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VINSW=3.6V, VIO=1.8V)**

| Parameter | Symbol | Limit | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **[ Circuit Current ]** | | | | | | |
| VBAT Circuit current 1 | IBAT1 | - | 0 | 3.0 | µA | RESETB=0V, VIO=0V |
| VBAT Circuit current 2 | IBAT2 | - | 0.8 | 5.0 | µA | RESETB=0V, VIO=1.8V |
| VBAT Circuit current 3 | IBAT3 | - | 2.0 | 3.5 | mA | When LED1-17 are active with default settings. |
| **[ UVLO ]** | | | | | | |
| UVLO Threshold | VUVLO | - | 2.1 | 2.5 | V | VBAT falling |
| UVLO Hysteresis | VHYUVLO | 50 | - | - | mV | |
| **[ LED Driver ] (LED1-17)** | | | | | | |
| Maximum output current | ILEDMax1 | - | 20.00 | - | mA | LED1-17 ,ISET＝100kΩ |
| | ILEDMax2 | - | 30.00 | - | mA | LED1-17 ,ISET＝68kΩ |
| Output current | ILED | -7.0% | 10.67 | +7.0% | mA | I=10.67mA setting, VLED=1V, ISET = 100k Ω |
| LED current Matching | ILEDMT | - | - | 5 | % | ILEDMT= (ILEDMax-ILEDMin)/(ILEDMax+ILEDMin) I=10.67mA setting, VLED=1V ISET = 100k Ω |
| Driver pin voltage range | VLED1 | 0.2 | - | VBAT-1.4 | V | LED1-17 ,ISET＝100kΩ |
| | VLED2 | 0.3 | - | VBAT-1.4 | V | LED1-17 ,ISET＝68kΩ |
| LED OFF Leak current | ILKLED | - | - | 1.0 | µA | |
| **[ PMOS switch ]** | | | | | | |
| Leak current at OFF | ILEAKP | - | - | 1.0 | µA | |
| Resistor at ON | RonP | - | 1.0 | - | Ω | Isw=170mA, VINSW=4.5V |
| **[ OSC ]** | | | | | | |
| OSC frequency | fosc | 0.96 | 1.2 | 1.44 | MHz | |
| **[ CE, SYNC, CLKIN, IFMODE ]** | | | | | | |
| L level input voltage | VIL1 | -0.3 | - | 0.25 x VIO | V | |
| H level input voltage | VIH1 | 0.75 x VIO | - | VIO +0.3 | V | |
| L level input current | Iin1 | - | 0 | 1 | µA | Input voltage = from (0.1 x VIO) to (0.9 x VIO) |
| **[ SDA, SCL ]** | | | | | | |
| L level input voltage | VIL2 | -0.3 | - | 0.25 x VIO | V | |
| H level input voltage | VIH2 | 0.75 x VIO | - | VIO +0.3 | V | |
| Input hysteresis | Vhys | 0.05 x VIO | - | - | V | |
| L level output voltage (for SDA pin) | VOL2 | 0 | - | 0.3 | V | At 3mA sink current |
| Input current | Iin2 | -3 | - | 3 | µA | Input voltage = from (0.1 x VIO) to (0.9 x VIO) |
| **[ RESETB ]** | | | | | | |
| L level input voltage | VIL3 | -0.3 | - | 0.25 x VIO | V | |
| H level input voltage | VIH3 | 0.75 x VIO | - | VIO +0.3 | V | |
| Input current | Iin3 | - | 0 | 1 | µA | Input voltage = from (0.1 x VIO) to (0.9 x VIO) |
| **[ CLKOUT ]** | | | | | | |
| L level output voltage | VOL1 | - | - | 0.4 | V | IOL=2mA |
| H level output voltage | VOH1 | 0.75 x VIO | - | - | V | IOH=-2mA |

**●Power Dissipation (on the ROHM's Standard Board)**

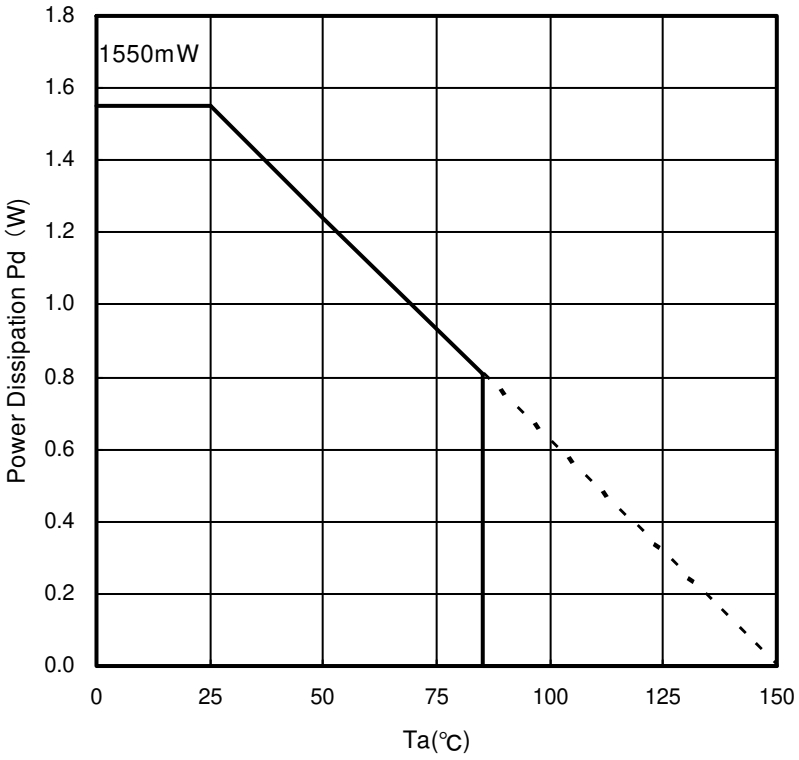


Fig.1

Information of the ROHM's standard board
Material: glass-epoxy
Size : 50mm × 58mm × 1.75mm($8^{th}$ layer)
Wiring pattern figure Refer to after page.

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## ●Block Diagram / Application Circuit Example 1

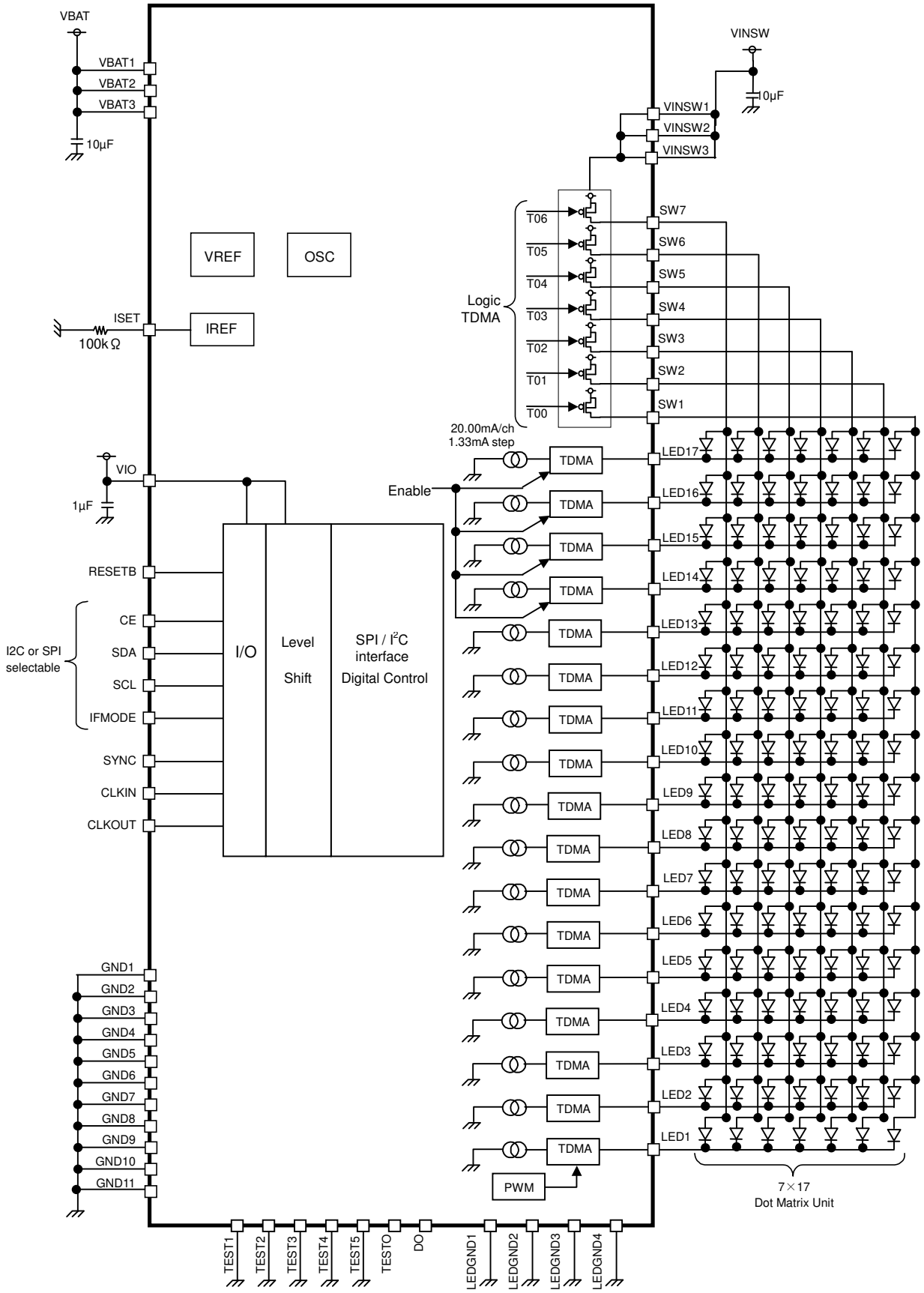



Fig.2 Block Diagram / Application Circuit example 1

## ●Block Diagram / Application Circuit Example 2

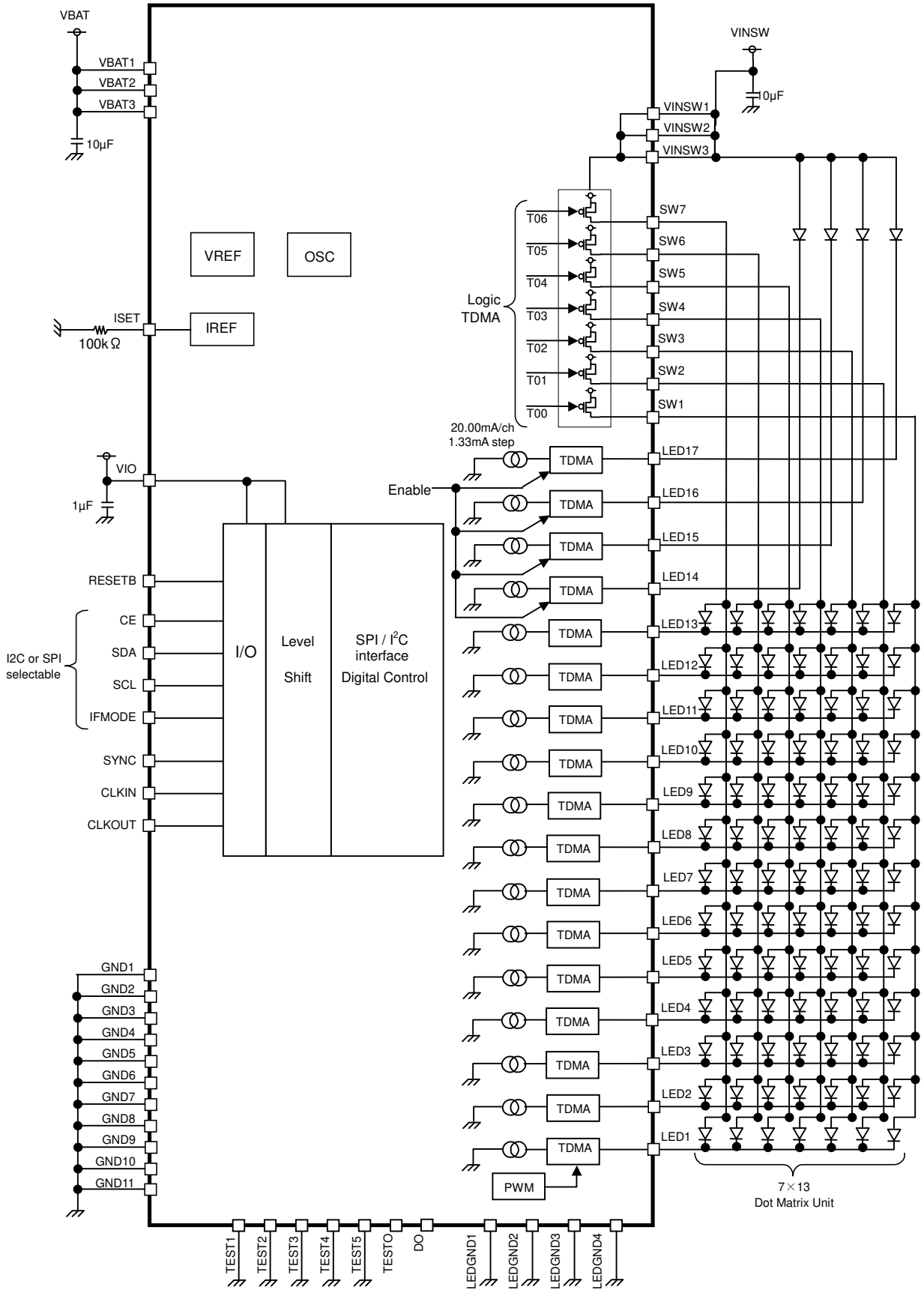
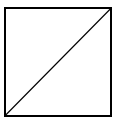



Fig.3 Block Diagram / Application Circuit example 2

**●Pin Arrangement ［Bottom View］**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| G | TEST4 | VBAT1 | LED11 | LED13 | LED15 | LED17 | TEST1 |
| F | ISET | GND1 | LED10 | LED12 | LED16 | CLKOUT | TESTO |
| E | LED8 | LED9 | LEDGND2 | TEST2 | LED14 | SDA | CE |
| D | LED6 | LED7 | LED5 | LEDGND1 | RESETB | SCL | VIO |
| C | LED4 | LED3 | | SW4 | SYNC | IFMODE | CLKIN |
| B | LED2 | LED1 | SW2 | VINSW1 | SW6 | DO | VBAT2 |
| A | TEST5 | SW1 | SW3 | VINSW2 | SW5 | SW7 | TEST3 |

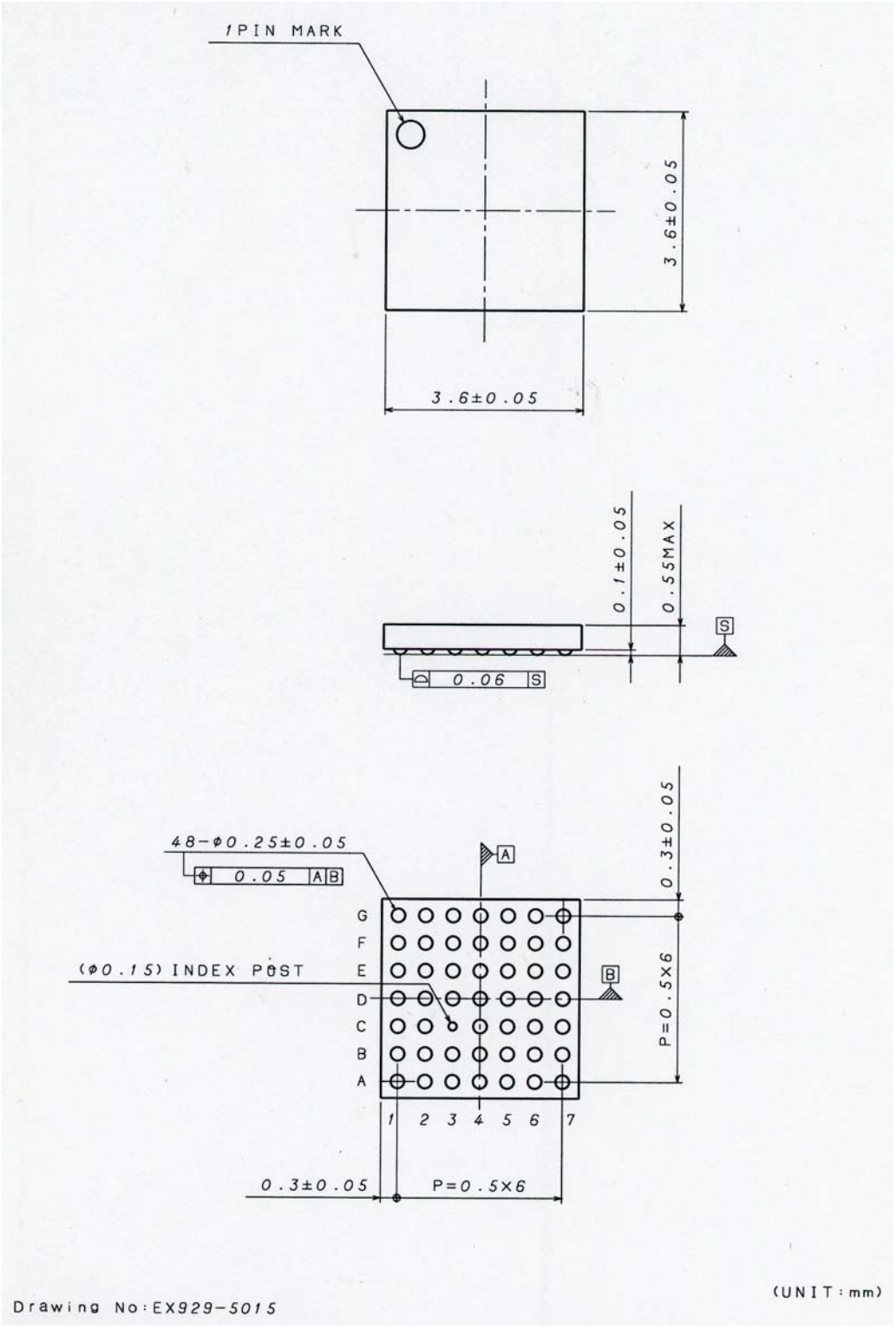
Total 48Balls



Index

**●Package**

48Pin VCSP50L3　CSP small package
SIZE : 3.60mm□
A ball pitch : 0.5mm
Height : 0.55mm max




*INDEX POST has No Solder Ball

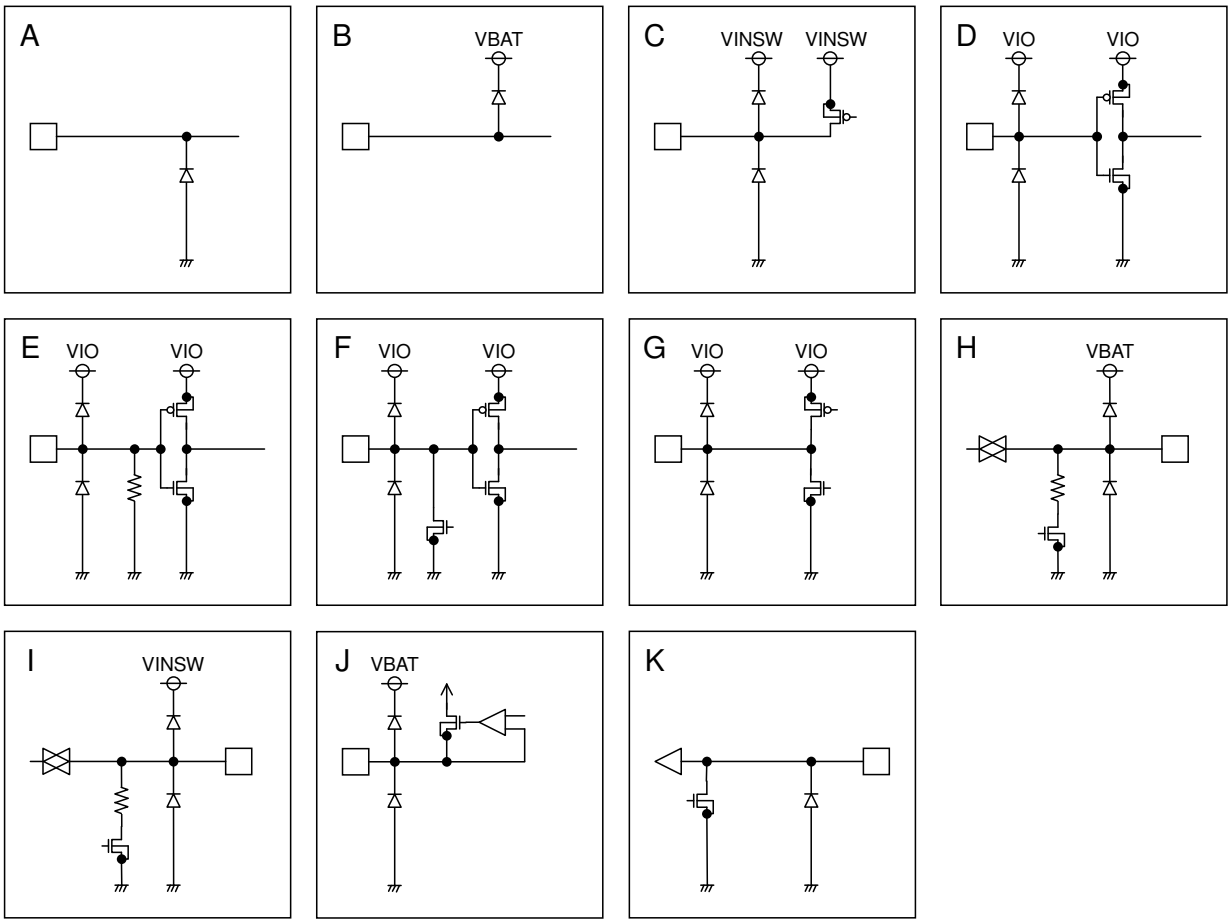
## ●Pin Functions

| No | Ball No. | Pin Name | I/O | Pull down | Unused processing setting | ESD Diode | | Functions | Equivalent Circuit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | For Power | For Ground | | |
| 1 | A7 | TEST3 | I | 94kohm | GND | VIO | GND | Test input pin 3 | E |
| 2 | A1 | TEST5 | O | - | GND | VINSW | GND | Test input pin 5 | I |
| 3 | B1 | LED2 | O | - | GND | – | GND | LED2 driver output | K |
| 4 | B2 | LED1 | O | - | GND | – | GND | LED1 driver output | K |
| 5 | B5 | SW6 | O | - | VINSW | VINSW | GND | P-MOS SW6 output | C |
| 6 | A6 | SW7 | O | - | VINSW | VINSW | GND | P-MOS SW 7 output | C |
| 7 | C2 | LED3 | O | - | GND | – | GND | LED3 driver output | K |
| 8 | D4 | LEDGND1 | - | - | - | VBAT | - | Ground | B |
| 9 | E4 | TEST2 | I | 94kohm | GND | VIO | GND | Test input pin 2 | E |
| 10 | A5 | SW5 | O | - | VINSW | VINSW | GND | P-MOS SW 5 output | C |
| 11 | C4 | SW4 | O | - | VINSW | VINSW | GND | P-MOS SW4 output | C |
| 12 | D3 | LED5 | O | - | GND | – | GND | LED5 driver output | K |
| 13 | D1 | LED6 | O | - | GND | – | GND | LED6 driver output | K |
| 14 | C1 | LED4 | O | - | GND | – | GND | LED4 driver output | K |
| 15 | A3 | SW3 | O | - | VINSW | VINSW | GND | P-MOS SW3 output | C |
| 16 | B3 | SW2 | O | - | VINSW | VINSW | GND | P-MOS SW2 output | C |
| 17 | A2 | SW1 | O | - | VINSW | VINSW | GND | P-MOS SW 1 output | C |
| 18 | B4 | VINSW1 | - | - | - | – | GND | Power supply for SW1-7 | A |
| 19 | E3 | LEDGND2 | - | - | - | VBAT | - | Ground | B |
| 20 | D2 | LED7 | O | - | GND | – | GND | LED7 driver output | K |
| 21 | G2 | VBAT1 | - | - | - | – | GND | Battery is connected | A |
| 22 | D5 | RESETB | I | - | GND | VIO | GND | Reset input pin (L: reset, H: reset cancel) | D |
| 23 | C7 | CLKIN | I | - | GND | VIO | GND | External CLK input pin | D |
| 24 | C5 | SYNC | I | - | GND | VIO | GND | External synchronous input pin | D |
| 25 | B6 | DO | O | - | OPEN | VIO | GND | Test output pin2 | G |
| 26 | E1 | LED8 | O | - | GND | – | GND | LED8 driver output | K |
| 27 | F1 | ISET | I | - | - | VBAT | GND | LED Constant Current Driver Current setting pin | J |
| 28 | A4 | VINSW2 | - | - | - | - | GND | Power supply for SW1-7 | A |
| 29 | G7 | TEST1 | I | 94kohm | GND | VIO | GND | Test input pin 1 | E |
| 30 | C6 | IFMODE | I | - | GND | VIO | GND | $I^2C$/SPI select pin (L: $I^2C$, H: SPI) | D |
| 31 | D6 | SCL | I | - | - | VIO | GND | SPI, $I^2C$ CLK input pin | D |
| 32 | D7 | VIO | - | - | - | – | GND | I/O Power supply is connected | A |
| 33 | E2 | LED9 | O | - | GND | – | GND | LED9 driver output | K |
| 34 | F3 | LED10 | O | - | GND | – | GND | LED10 driver output | K |
| 35 | G4 | LED13 | O | - | GND | – | GND | LED13 driver output | K |
| 36 | E5 | LED14 | O | - | GND | – | GND | LED14 driver output | K |
| 37 | F6 | CLKOUT | O | - | OPEN | VIO | GND | Reference CLK output pin | G |
| 38 | E7 | CE | I | - | GND | VIO | GND | SPI enable pin(H;Enable), or<br>$I^2C$ slave address selection (L: 74h, H: 75h) | D |
| 39 | E6 | SDA | I/O | - | - | VIO | GND | SPI DATA input / $I^2C$ DATA input-output pin | F |
| 40 | G1 | TEST4 | O | - | GND | VBAT | GND | Test input pin 4 | H |
| 41 | G3 | LED11 | O | - | GND | – | GND | LED11 driver output | K |
| 42 | F4 | LED12 | O | - | GND | – | GND | LED12 driver output | K |
| 43 | F2 | GND1 | - | - | - | VBAT | - | Ground | B |
| 44 | G5 | LED15 | O | - | GND | – | GND | LED15 driver output | K |
| 45 | F5 | LED16 | O | - | GND | – | GND | LED16 driver output | K |
| 46 | G6 | LED17 | O | - | GND | – | GND | LED17 driver output | K |
| 47 | F7 | TESTO | O | - | OPEN | VIO | GND | Test output pin1 | G |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 48 | B7 | VBAT2 | - | - | - | – | GND | Battery is connected | A |

* Please connect the unused LED pins to the ground.
* It is prohibition to set the registers for unused LED.
Total 48 pins

**●Equivalent Circuit**



## ●Serial Interface

1. SPI format
   - ・When IFMODE is set to “H”, it can interface with SPI format.
   - ・The serial interface is four terminals (serial clock terminal (SCL), serial data input terminal (SDA), and chip selection input terminal (CE)).

(1)Write operation
- ・Data is taken into an internal shift register with rising edge of CLK. (Max of the frequency is 13MHz.)
- ・The receive data becomes enable in the “H” section of CE. (Active “H”.)
- ・The transmit data is forwarded (with MSB-First) in the order of write command “0”(1bit), the control register address (7bit) and data (8bit).

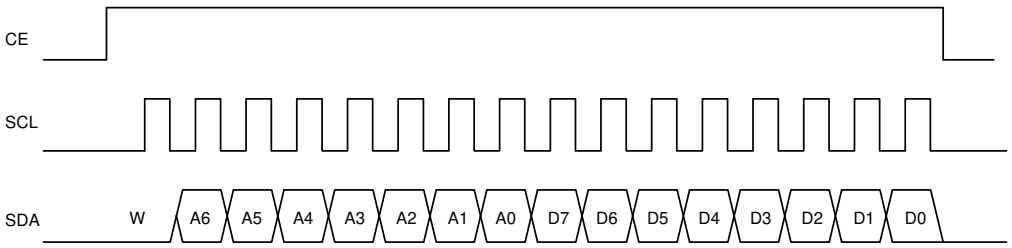



Fig.4 Writing format

(2)Timing diagram

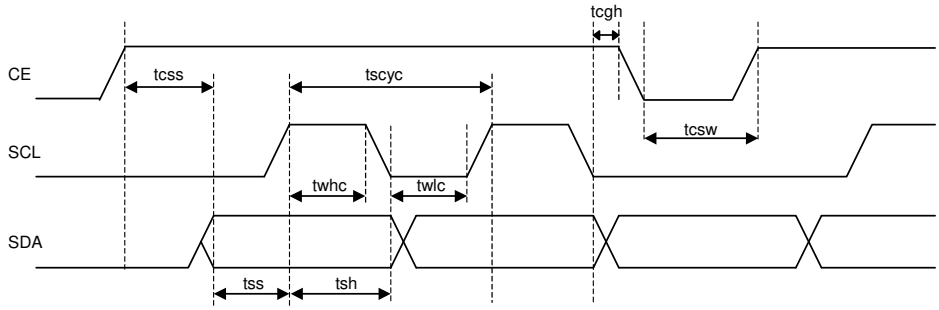



Fig.5 Timing diagram (SPI format)

(3) Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VINSW=3.6V, VIO=1.8V)

| Parameter | Symbol | Limit | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| SCL cycle time | tscyc | 76 | - | - | ns | |
| H period of SCL cycle | Twhc | 35 | - | - | ns | |
| L period of SCL cycle | Twlc | 35 | - | - | ns | |
| SDA setup time | Tss | 38 | - | - | ns | |
| SDA hold time | Tsh | 38 | - | - | ns | |
| Write interval | Tcsw | 38 | - | - | ns | |
| Write interval (after A or B RAM accsess) | | 2.1 | - | - | µs | *1 |
| | | ECLK x 2 | - | - | s | *2 |
| CE setup time | Tcss | 55 | - | - | ns | |
| CE hold time | Tcgh | 48 | - | - | ns | |

*1 When it used internal clock.
*2 When it used external clock. (ECLK means the cycle of external clock.)

2. $I^2C$ BUS format

When IFMODE is set to “L”, it can interface with $I^2C$ BUS format.

(1) Slave address

| CE | A7 | A6 | A5 | A4 | A3 | A2 | A1 | R/W |
|---|---|---|---|---|---|---|---|---|
| L | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| H | 1 | 1 | 1 | 0 | 1 | 0 | 1 | |

(2) Bit Transfer

SCL transfers 1-bit data during H. During H of SCL, SDA cannot be changed at the time of bit transfer. If SDA changes while SCL is H, START conditions or STOP conditions will occur and it will be interpreted as a control signal.

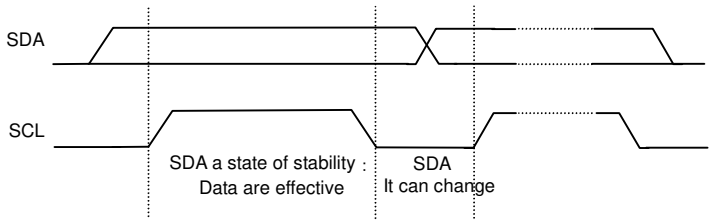



Fig.6 Bit transfer ($I^2C$ format)

(3) START and STOP condition

When SDA and SCL are H, data is not transferred on the $I^2C$- bus. This condition indicates, if SDA changes from H to L while SCL has been H, it will become START (S) conditions, and an access start, if SDA changes from L to H while SCL has been H, it will become STOP (P) conditions and an access end.

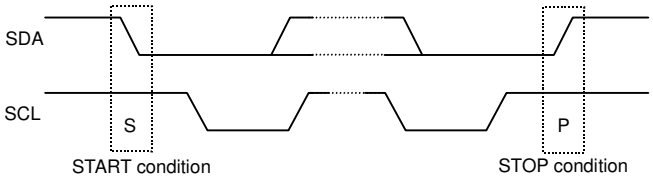



Fig.7 START/STOP condition ($I^2C$ format)

(4) Acknowledge

It transfers data 8 bits each after the occurrence of START condition. A transmitter opens SDA after transfer 8bits data, and a receiver returns the acknowledge signal by setting SDA to L.

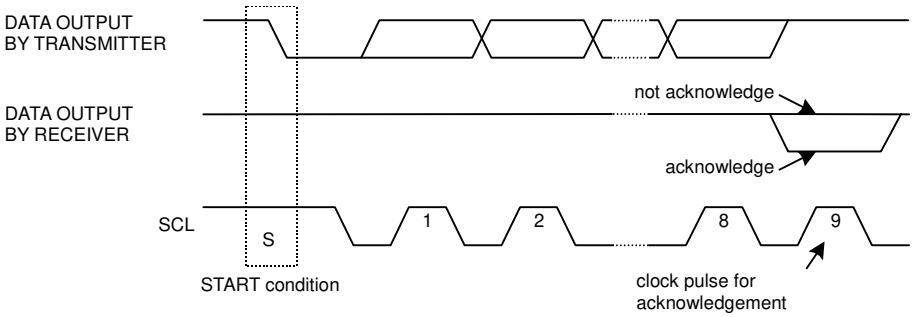
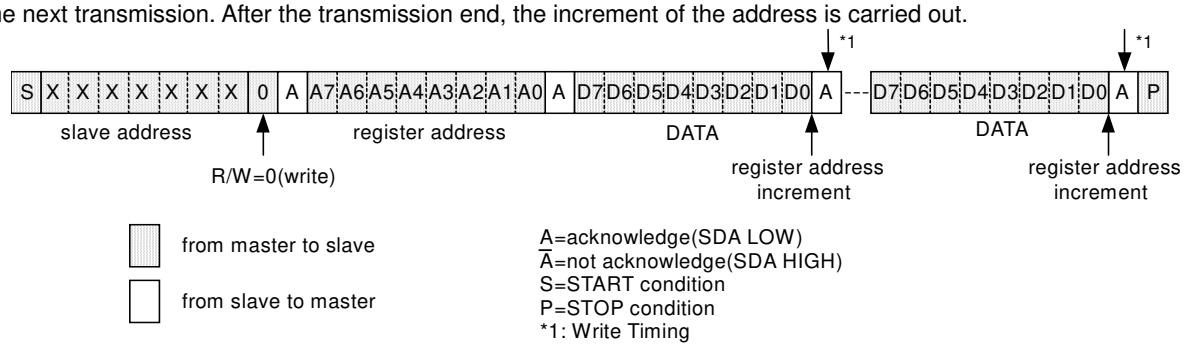



Fig.8 Acknowledge ($I^2C$ format)

(5) Writing protocol

A register address is transferred by the next 1 byte that transferred the slave address and the write-in command. The 3rd byte writes data in the internal register written in by the 2nd byte, and after 4th byte or, the increment of register address is carried out automatically. However, when a register address turns into the last address (77h), it is set to 00h by the next transmission. After the transmission end, the increment of the address is carried out.




(6) Timing diagram

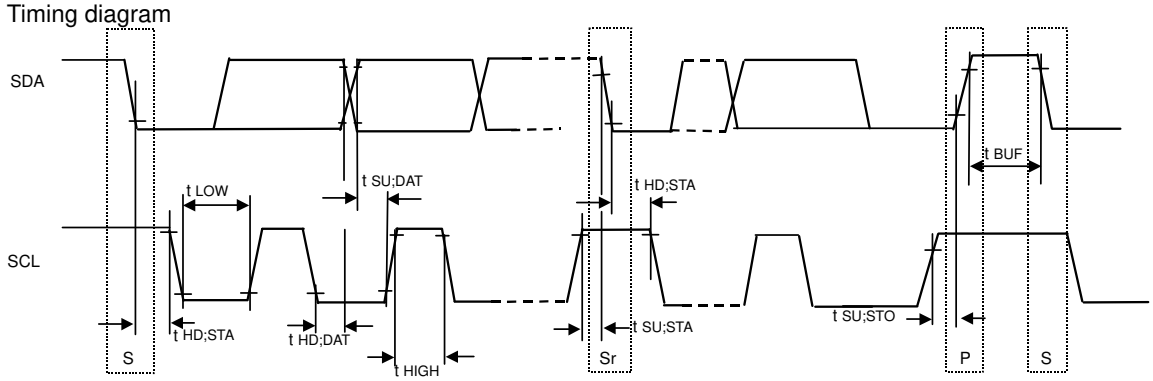



Fig.9 Timing diagram (I2C format)

(7) Electrical Characteristics(Unless otherwise specified, Ta=25 °C, VBAT=3.6V, VINSW=3.6V, VIO=1.8V)

| Parameter | Symbol | Standard-mode | | | Fast-mode | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| 【I²C BUS format】 | | | | | | | | |
| SCL clock frequency | fSCL | 0 | - | 100 | 0 | - | 400 | kHz |
| LOW period of the SCL clock | tLOW | 4.7 | - | - | 1.3 | - | - | µs |
| HIGH period of the SCL clock | tHIGH | 4.0 | - | - | 0.6 | - | - | µs |
| Hold time (repeated) START condition After this period, the first clock is generated | tHD;STA | 4.0 | - | - | 0.6 | - | - | µs |
| Set-up time for a repeated START condition | tSU;STA | 4.7 | - | - | 0.6 | - | - | µs |
| Data hold time | tHD;DAT | 0 | - | 3.45 | 0 | - | 0.9 | µs |
| Data set-up time | tSU;DAT | 250 | - | - | 100 | - | - | ns |
| Set-up time for STOP condition | tSU;STO | 4.0 | - | - | 0.6 | - | - | µs |
| Bus free time between a STOP and START condition | tBUF | 4.7 | - | - | 1.3 | - | - | µs |

## ●Register List

* Please be sure to write “0” in the register which is not assigned.
* It is prohibition to write data to the address which is not assigned.

Control register

| Address | Default | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Block | R/W | Remark |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | 00h | - | - | - | - | - | - | - | SFTRST | RESET | W | Software Reset |
| 01h | 00h | - | - | - | - | OSCEN | - | - | - | OSC | W | OSC ON/OFF control |
| 11h | 00h | - | - | LED6ON | LED5ON | LED4ON | LED3ON | LED2ON | LED1ON | LED driver | W | LED1-6 Enable |
| 12h | 00h | - | - | LED12ON | LED11ON | LED10ON | LED9ON | LED8ON | LED7ON | | W | LED7-12 Enable |
| 13h | 00h | - | - | - | LED17ON | LED16ON | LED15ON | LED14ON | LED13ON | | W | LED13-17 Enable |
| 17h | 0Fh | - | - | - | - | LED17 TDMAON | LED16 TDMAON | LED15 TDMAON | LED14 TDMAON | | W | LED14-17 TDMA Enable |
| 20h | 00h | - | - | PWMSET[5:0] | | | | | | PWM | W | LED1-17PWM DutySetting |
| 21h | 00h | - | - | - | - | SYNCACT | SYNCON | CLKOUT | CLKIN | CLK | W | CLK selection, SYNC operation control |
| 2Dh | 00h | - | - | - | - | - | PWMEN | SLPEN | SCLEN | MATRIX | W | PWM,SLOPE,SCROLL ON/OFF setting |
| 2Eh | 00h | - | - | - | - | - | - | - | SCLRST | | W | Reset SCROLL |
| 2Fh | 00h | - | SCLSPEED[2:0] | | | UP | DOWN | RIGHT | LEFT | | W | SCROLL Setting |
| 30h | 00h | - | - | - | - | - | - | - | START | | W | LED matrix control |
| 31h | 00h | - | - | - | - | - | - | CLRB | CLRA | | W | Matrix data clear |
| 7Fh | 00h | - | - | - | - | - | IAB | OAB | RMCG | RMAP | W | Resister map change |

A-pattern register

| Address | default | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Block | R/W | Remark |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 01h | 08h | SCYCA00[1:0] | | SDLYA00[1:0] | | ILEDA00SET[3:0] | | | | MATRIX Data | W | Data for Matrix 00(DA00) |
| 02h | 08h | SCYCA01[1:0] | | SDLYA01[1:0] | | ILEDA01SET[3:0] | | | | | W | Data for Matrix 01(DA01) |
| 03h | 08h | SCYCA02[1:0] | | SDLYA02[1:0] | | ILEDA02SET[3:0] | | | | | W | Data for Matrix 02(DA02) |
| 04h | 08h | SCYCA03[1:0] | | SDLYA03[1:0] | | ILEDA03SET[3:0] | | | | | W | Data for Matrix 03(DA03) |
| 05h | 08h | SCYCA04[1:0] | | SDLYA04[1:0] | | ILEDA04SET[3:0] | | | | | W | Data for Matrix 04(DA04) |
| 06h | 08h | SCYCA05[1:0] | | SDLYA05[1:0] | | ILEDA05SET[3:0] | | | | | W | Data for Matrix 05(DA05) |
| 07h | 08h | SCYCA06[1:0] | | SDLYA06[1:0] | | ILEDA06SET[3:0] | | | | | W | Data for Matrix 06(DA06) |
| 08h | 08h | SCYCA10[1:0] | | SDLYA10[1:0] | | ILEDA10SET[3:0] | | | | | W | Data for Matrix 10(DA10) |
| 09h | 08h | SCYCA11[1:0] | | SDLYA11[1:0] | | ILEDA11SET[3:0] | | | | | W | Data for Matrix 11(DA11) |
| 0Ah | 08h | SCYCA12[1:0] | | SDLYA12[1:0] | | ILEDA12SET[3:0] | | | | | W | Data for Matrix 12(DA12) |
| 0Bh | 08h | SCYCA13[1:0] | | SDLYA13[1:0] | | ILEDA13SET[3:0] | | | | | W | Data for Matrix 13(DA13) |
| 0Ch | 08h | SCYCA14[1:0] | | SDLYA14[1:0] | | ILEDA14SET[3:0] | | | | | W | Data for Matrix 14(DA14) |
| 0Dh | 08h | SCYCA15[1:0] | | SDLYA15[1:0] | | ILEDA15SET[3:0] | | | | | W | Data for Matrix 15(DA15) |
| 0Eh | 08h | SCYCA16[1:0] | | SDLYA16[1:0] | | ILEDA16SET[3:0] | | | | | W | Data for Matrix 16(DA16) |
| 0Fh | 08h | SCYCA20[1:0] | | SDLYA20[1:0] | | ILEDA20SET[3:0] | | | | | W | Data for Matrix 20(DA20) |
| 10h | 08h | SCYCA21[1:0] | | SDLYA21[1:0] | | ILEDA21SET[3:0] | | | | | W | Data for Matrix 21(DA21) |
| 11h | 08h | SCYCA22[1:0] | | SDLYA22[1:0] | | ILEDA22SET[3:0] | | | | | W | Data for Matrix 22(DA22) |
| 12h | 08h | SCYCA23[1:0] | | SDLYA23[1:0] | | ILEDA23SET[3:0] | | | | | W | Data for Matrix 23(DA23) |
| 13h | 08h | SCYCA24[1:0] | | SDLYA24[1:0] | | ILEDA24SET[3:0] | | | | | W | Data for Matrix 24(DA24) |
| 14h | 08h | SCYCA25[1:0] | | SDLYA25[1:0] | | ILEDA25SET[3:0] | | | | | W | Data for Matrix 25(DA25) |
| 15h | 08h | SCYCA26[1:0] | | SDLYA26[1:0] | | ILEDA26SET[3:0] | | | | | W | Data for Matrix 26(DA26) |
| 16h | 08h | SCYCA30[1:0] | | SDLYA30[1:0] | | ILEDA30SET[3:0] | | | | | W | Data for Matrix 30(DA30) |
| 17h | 08h | SCYCA31[1:0] | | SDLYA31[1:0] | | ILEDA31SET[3:0] | | | | | W | Data for Matrix 31(DA31) |
| 18h | 08h | SCYCA32[1:0] | | SDLYA32[1:0] | | ILEDA32SET[3:0] | | | | | W | Data for Matrix 32(DA32) |
| 19h | 08h | SCYCA33[1:0] | | SDLYA33[1:0] | | ILEDA33SET[3:0] | | | | | W | Data for Matrix 33(DA33) |
| 1Ah | 08h | SCYCA34[1:0] | | SDLYA34[1:0] | | ILEDA34SET[3:0] | | | | | W | Data for Matrix 34(DA34) |
| 1Bh | 08h | SCYCA35[1:0] | | SDLYA35[1:0] | | ILEDA35SET[3:0] | | | | | W | Data for Matrix 35(DA35) |
| 1Ch | 08h | SCYCA36[1:0] | | SDLYA36[1:0] | | ILEDA36SET[3:0] | | | | | W | Data for Matrix 36(DA36) |
| 1Dh | 08h | SCYCA40[1:0] | | SDLYA40[1:0] | | ILEDA40SET[3:0] | | | | | W | Data for Matrix 40(DA40) |
| 1Eh | 08h | SCYCA41[1:0] | | SDLYA41[1:0] | | ILEDA41SET[3:0] | | | | | W | Data for Matrix 41(DA41) |
| 1Fh | 08h | SCYCA42[1:0] | | SDLYA42[1:0] | | ILEDA42SET[3:0] | | | | | W | Data for Matrix 42(DA42) |
| 20h | 08h | SCYCA43[1:0] | | SDLYA43[1:0] | | ILEDA43SET[3:0] | | | | | W | Data for Matrix 43(DA43) |
| 21h | 08h | SCYCA44[1:0] | | SDLYA44[1:0] | | ILEDA44SET[3:0] | | | | | W | Data for Matrix 44(DA44) |
| 22h | 08h | SCYCA45[1:0] | | SDLYA45[1:0] | | ILEDA45SET[3:0] | | | | | W | Data for Matrix 45(DA45) |
| 23h | 08h | SCYCA46[1:0] | | SDLYA46[1:0] | | ILEDA46SET[3:0] | | | | | W | Data for Matrix 46(DA46) |
| 24h | 08h | SCYCA50[1:0] | | SDLYA50[1:0] | | ILEDA50SET[3:0] | | | | | W | Data for Matrix 50(DA50) |
| 25h | 08h | SCYCA51[1:0] | | SDLYA51[1:0] | | ILEDA51SET[3:0] | | | | | W | Data for Matrix 51(DA51) |
| 26h | 08h | SCYCA52[1:0] | | SDLYA52[1:0] | | ILEDA52SET[3:0] | | | | | W | Data for Matrix 52(DA52) |
| 27h | 08h | SCYCA53[1:0] | | SDLYA53[1:0] | | ILEDA53SET[3:0] | | | | | W | Data for Matrix 53(DA53) |
| 28h | 08h | SCYCA54[1:0] | | SDLYA54[1:0] | | ILEDA54SET[3:0] | | | | | W | Data for Matrix 54(DA54) |
| 29h | 08h | SCYCA55[1:0] | | SDLYA55[1:0] | | ILEDA55SET[3:0] | | | | | W | Data for Matrix 55(DA55) |
| 2Ah | 08h | SCYCA56[1:0] | | SDLYA56[1:0] | | ILEDA56SET[3:0] | | | | | W | Data for Matrix 56(DA56) |
| 2Bh | 08h | SCYCA60[1:0] | | SDLYA60[1:0] | | ILEDA60SET[3:0] | | | | | W | Data for Matrix 60(DA60) |
| 2Ch | 08h | SCYCA61[1:0] | | SDLYA61[1:0] | | ILEDA61SET[3:0] | | | | | W | Data for Matrix 61(DA61) |
| 2Dh | 08h | SCYCA62[1:0] | | SDLYA62[1:0] | | ILEDA62SET[3:0] | | | | | W | Data for Matrix 62(DA62) |
| 2Eh | 08h | SCYCA63[1:0] | | SDLYA63[1:0] | | ILEDA63SET[3:0] | | | | | W | Data for Matrix 63(DA63) |
| 2Fh | 08h | SCYCA64[1:0] | | SDLYA64[1:0] | | ILEDA64SET[3:0] | | | | | W | Data for Matrix 64(DA64) |
| 30h | 08h | SCYCA65[1:0] | | SDLYA65[1:0] | | ILEDA65SET[3:0] | | | | | W | Data for Matrix 65(DA65) |

| Address | default | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Block | R/W | Remark |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31h | 08h | SCYCA66[1:0] | | SDLYA66[1:0] | | ILEDA66SET[3:0] | | | | MATRIX Data | W | Data for Matrix 66(DA66) |
| 32h | 08h | SCYCA70[1:0] | | SDLYA70[1:0] | | ILEDA70SET[3:0] | | | | | W | Data for Matrix 70(DA70) |
| 33h | 08h | SCYCA71[1:0] | | SDLYA71[1:0] | | ILEDA71SET[3:0] | | | | | W | Data for Matrix 71(DA71) |
| 34h | 08h | SCYCA72[1:0] | | SDLYA72[1:0] | | ILEDA72SET[3:0] | | | | | W | Data for Matrix 72(DA72) |
| 35h | 08h | SCYCA73[1:0] | | SDLYA73[1:0] | | ILEDA73SET[3:0] | | | | | W | Data for Matrix 73(DA73) |
| 36h | 08h | SCYCA74[1:0] | | SDLYA74[1:0] | | ILEDA74SET[3:0] | | | | | W | Data for Matrix 74(DA74) |
| 37h | 08h | SCYCA75[1:0] | | SDLYA75[1:0] | | ILEDA75SET[3:0] | | | | | W | Data for Matrix 75(DA75) |
| 38h | 08h | SCYCA76[1:0] | | SDLYA76[1:0] | | ILEDA76SET[3:0] | | | | | W | Data for Matrix 76(DA76) |
| 39h | 08h | SCYCA80[1:0] | | SDLYA80[1:0] | | ILEDA80SET[3:0] | | | | | W | Data for Matrix 80(DA80) |
| 3Ah | 08h | SCYCA81[1:0] | | SDLYA81[1:0] | | ILEDA81SET[3:0] | | | | | W | Data for Matrix 81(DA81) |
| 3Bh | 08h | SCYCA82[1:0] | | SDLYA82[1:0] | | ILEDA82SET[3:0] | | | | | W | Data for Matrix 82(DA82) |
| 3Ch | 08h | SCYCA83[1:0] | | SDLYA83[1:0] | | ILEDA83SET[3:0] | | | | | W | Data for Matrix 83(DA83) |
| 3Dh | 08h | SCYCA84[1:0] | | SDLYA84[1:0] | | ILEDA84SET[3:0] | | | | | W | Data for Matrix 84(DA84) |
| 3Eh | 08h | SCYCA85[1:0] | | SDLYA85[1:0] | | ILEDA85SET[3:0] | | | | | W | Data for Matrix 85(DA85) |
| 3Fh | 08h | SCYCA86[1:0] | | SDLYA86[1:0] | | ILEDA86SET[3:0] | | | | | W | Data for Matrix 86(DA86) |
| 40h | 08h | SCYCA90[1:0] | | SDLYA90[1:0] | | ILEDA90SET[3:0] | | | | | W | Data for Matrix 90(DA90) |
| 41h | 08h | SCYCA91[1:0] | | SDLYA91[1:0] | | ILEDA91SET[3:0] | | | | | W | Data for Matrix 91(DA91) |
| 42h | 08h | SCYCA92[1:0] | | SDLYA92[1:0] | | ILEDA92SET[3:0] | | | | | W | Data for Matrix 92(DA92) |
| 43h | 08h | SCYCA93[1:0] | | SDLYA93[1:0] | | ILEDA93SET[3:0] | | | | | W | Data for Matrix 93(DA93) |
| 44h | 08h | SCYCA94[1:0] | | SDLYA94[1:0] | | ILEDA94SET[3:0] | | | | | W | Data for Matrix 94(DA94) |
| 45h | 08h | SCYCA95[1:0] | | SDLYA95[1:0] | | ILEDA95SET[3:0] | | | | | W | Data for Matrix 95(DA95) |
| 46h | 08h | SCYCA96[1:0] | | SDLYA96[1:0] | | ILEDA96SET[3:0] | | | | | W | Data for Matrix 96(DA96) |
| 47h | 08h | SCYCAA0[1:0] | | SDLYAA0[1:0] | | ILEDAA0SET[3:0] | | | | | W | Data for Matrix A0(DAA0) |
| 48h | 08h | SCYCAA1[1:0] | | SDLYAA1[1:0] | | ILEDAA1SET[3:0] | | | | | W | Data for Matrix A1(DAA1) |
| 49h | 08h | SCYCAA2[1:0] | | SDLYAA2[1:0] | | ILEDAA2SET[3:0] | | | | | W | Data for Matrix A2(DAA2) |
| 4Ah | 08h | SCYCAA3[1:0] | | SDLYAA3[1:0] | | ILEDAA3SET[3:0] | | | | | W | Data for Matrix A3(DAA3) |
| 4Bh | 08h | SCYCAA4[1:0] | | SDLYAA4[1:0] | | ILEDAA4SET[3:0] | | | | | W | Data for Matrix A4(DAA4) |
| 4Ch | 08h | SCYCAA5[1:0] | | SDLYAA5[1:0] | | ILEDAA5SET[3:0] | | | | | W | Data for Matrix A5(DAA5) |
| 4Dh | 08h | SCYCAA6[1:0] | | SDLYAA6[1:0] | | ILEDAA6SET[3:0] | | | | | W | Data for Matrix A6(DAA6) |
| 4Eh | 08h | SCYCAB0[1:0] | | SDLYAB0[1:0] | | ILEDAB0SET[3:0] | | | | | W | Data for Matrix B0(DAB0) |
| 4Fh | 08h | SCYCAB1[1:0] | | SDLYAB1[1:0] | | ILEDAB1SET[3:0] | | | | | W | Data for Matrix B1(DAB1) |
| 50h | 08h | SCYCAB2[1:0] | | SDLYAB2[1:0] | | ILEDAB2SET[3:0] | | | | | W | Data for Matrix B2(DAB2) |
| 51h | 08h | SCYCAB3[1:0] | | SDLYAB3[1:0] | | ILEDAB3SET[3:0] | | | | | W | Data for Matrix B3(DAB3) |
| 52h | 08h | SCYCAB4[1:0] | | SDLYAB4[1:0] | | ILEDAB4SET[3:0] | | | | | W | Data for Matrix B4(DAB4) |
| 53h | 08h | SCYCAB5[1:0] | | SDLYAB5[1:0] | | ILEDAB5SET[3:0] | | | | | W | Data for Matrix B5(DAB5) |
| 54h | 08h | SCYCAB6[1:0] | | SDLYAB6[1:0] | | ILEDAB6SET[3:0] | | | | | W | Data for Matrix B6(DAB6) |
| 55h | 08h | SCYCAC0[1:0] | | SDLYAC0[1:0] | | ILEDAC0SET[3:0] | | | | | W | Data for Matrix C0(DAC0) |
| 56h | 08h | SCYCAC1[1:0] | | SDLYAC1[1:0] | | ILEDAC1SET[3:0] | | | | | W | Data for Matrix C1(DAC1) |
| 57h | 08h | SCYCAC2[1:0] | | SDLYAC2[1:0] | | ILEDAC2SET[3:0] | | | | | W | Data for Matrix C2(DAC2) |
| 58h | 08h | SCYCAC3[1:0] | | SDLYAC3[1:0] | | ILEDAC3SET[3:0] | | | | | W | Data for Matrix C3(DAC3) |
| 59h | 08h | SCYCAC4[1:0] | | SDLYAC4[1:0] | | ILEDAC4SET[3:0] | | | | | W | Data for Matrix C4(DAC4) |
| 5Ah | 08h | SCYCAC5[1:0] | | SDLYAC5[1:0] | | ILEDAC5SET[3:0] | | | | | W | Data for Matrix C5(DAC5) |
| 5Bh | 08h | SCYCAC6[1:0] | | SDLYAC6[1:0] | | ILEDAC6SET[3:0] | | | | | W | Data for Matrix C6(DAC6) |
| 5Ch | 08h | SCYCAD0[1:0] | | SDLYAD0[1:0] | | ILEDAD0SET[3:0] | | | | | W | Data for Matrix D0(DAD0) |
| 5Dh | 08h | SCYCAD1[1:0] | | SDLYAD1[1:0] | | ILEDAD1SET[3:0] | | | | | W | Data for Matrix D1(DAD1) |
| 5Eh | 08h | SCYCAD2[1:0] | | SDLYAD2[1:0] | | ILEDAD2SET[3:0] | | | | | W | Data for Matrix D2(DAD2) |
| 5Fh | 08h | SCYCAD3[1:0] | | SDLYAD3[1:0] | | ILEDAD3SET[3:0] | | | | | W | Data for Matrix D3(DAD3) |
| 60h | 08h | SCYCAD4[1:0] | | SDLYAD4[1:0] | | ILEDAD4SET[3:0] | | | | | W | Data for Matrix D4(DAD4) |

| Address | default | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Block | R/W | Remark |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61h | 08h | SCYCAD5[1:0] | | SDLYAD5[1:0] | | ILEDAD5SET[3:0] | | | | MATRIX Data | W | Data for Matrix D5(DAD5) |
| 62h | 08h | SCYCAD6[1:0] | | SDLYAD6[1:0] | | ILEDAD6SET[3:0] | | | | | W | Data for Matrix D6(DAD6) |
| 63h | 08h | SCYCAE0[1:0] | | SDLYAE0[1:0] | | ILEDAE0SET[3:0] | | | | | W | Data for Matrix E0(DAE0) |
| 64h | 08h | SCYCAE1[1:0] | | SDLYAE1[1:0] | | ILEDAE1SET[3:0] | | | | | W | Data for Matrix E1(DAE1) |
| 65h | 08h | SCYCAE2[1:0] | | SDLYAE2[1:0] | | ILEDAE2SET[3:0] | | | | | W | Data for Matrix E2(DAE2) |
| 66h | 08h | SCYCAE3[1:0] | | SDLYAE3[1:0] | | ILEDAE3SET[3:0] | | | | | W | Data for Matrix E3(DAE3) |
| 67h | 08h | SCYCAE4[1:0] | | SDLYAE4[1:0] | | ILEDAE4SET[3:0] | | | | | W | Data for Matrix E4(DAE4) |
| 68h | 08h | SCYCAE5[1:0] | | SDLYAE5[1:0] | | ILEDAE5SET[3:0] | | | | | W | Data for Matrix E5(DAE5) |
| 69h | 08h | SCYCAE6[1:0] | | SDLYAE6[1:0] | | ILEDAE6SET[3:0] | | | | | W | Data for Matrix E6(DAE6) |
| 6Ah | 08h | SCYCAF0[1:0] | | SDLYAF0[1:0] | | ILEDAF0SET[3:0] | | | | | W | Data for Matrix F0(DAF0) |
| 6Bh | 08h | SCYCAF1[1:0] | | SDLYAF1[1:0] | | ILEDAF1SET[3:0] | | | | | W | Data for Matrix F1(DAF1) |
| 6Ch | 08h | SCYCAF2[1:0] | | SDLYAF2[1:0] | | ILEDAF2SET[3:0] | | | | | W | Data for Matrix F2(DAF2) |
| 6Dh | 08h | SCYCAF3[1:0] | | SDLYAF3[1:0] | | ILEDAF3SET[3:0] | | | | | W | Data for Matrix F3(DAF3) |
| 6Eh | 08h | SCYCAF4[1:0] | | SDLYAF4[1:0] | | ILEDAF4SET[3:0] | | | | | W | Data for Matrix F4(DAF4) |
| 6Fh | 08h | SCYCAF5[1:0] | | SDLYAF5[1:0] | | ILEDAF5SET[3:0] | | | | | W | Data for Matrix F5(DAF5) |
| 70h | 08h | SCYCAF6[1:0] | | SDLYAF6[1:0] | | ILEDAF6SET[3:0] | | | | | W | Data for Matrix F6(DAF6) |
| 71h | 08h | SCYCAG0[1:0] | | SDLYAG0[1:0] | | ILEDAG0SET[3:0] | | | | | W | Data for Matrix G0(DAG0) |
| 72h | 08h | SCYCAG1[1:0] | | SDLYAG1[1:0] | | ILEDAG1SET[3:0] | | | | | W | Data for Matrix G1(DAG1) |
| 73h | 08h | SCYCAG2[1:0] | | SDLYAG2[1:0] | | ILEDAG2SET[3:0] | | | | | W | Data for Matrix G2(DAG2) |
| 74h | 08h | SCYCAG3[1:0] | | SDLYAG3[1:0] | | ILEDAG3SET[3:0] | | | | | W | Data for Matrix G3(DAG3) |
| 75h | 08h | SCYCAG4[1:0] | | SDLYAG4[1:0] | | ILEDAG4SET[3:0] | | | | | W | Data for Matrix G4(DAG4) |
| 76h | 08h | SCYCAG5[1:0] | | SDLYAG5[1:0] | | ILEDAG5SET[3:0] | | | | | W | Data for Matrix G5(DAG5) |
| 77h | 08h | SCYCAG6[1:0] | | SDLYAG6[1:0] | | ILEDAG6SET[3:0] | | | | | W | Data for Matrix G6(DAG6) |

B-pattern register

| Address | default | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Block | R/W | Remark |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 01h | 08h | SCYCB00[1:0] | | SDLYB00[1:0] | | ILEDB00SET[3:0] | | | | MATRIX Data | W | Data for Matrix 00(DB00) |
| 02h | 08h | SCYCB01[1:0] | | SDLYB01[1:0] | | ILEDB01SET[3:0] | | | | | W | Data for Matrix 01(DB01) |
| 03h | 08h | SCYCB02[1:0] | | SDLYB02[1:0] | | ILEDB02SET[3:0] | | | | | W | Data for Matrix 02(DB02) |
| 04h | 08h | SCYCB03[1:0] | | SDLYB03[1:0] | | ILEDB03SET[3:0] | | | | | W | Data for Matrix 03(DB03) |
| 05h | 08h | SCYCB04[1:0] | | SDLYB04[1:0] | | ILEDB04SET[3:0] | | | | | W | Data for Matrix 04(DB04) |
| 06h | 08h | SCYCB05[1:0] | | SDLYB05[1:0] | | ILEDB05SET[3:0] | | | | | W | Data for Matrix 05(DB05) |
| 07h | 08h | SCYCB06[1:0] | | SDLYB06[1:0] | | ILEDB06SET[3:0] | | | | | W | Data for Matrix 06(DB06) |
| 08h | 08h | SCYCB10[1:0] | | SDLYB10[1:0] | | ILEDB10SET[3:0] | | | | | W | Data for Matrix 10(DB10) |
| 09h | 08h | SCYCB11[1:0] | | SDLYB11[1:0] | | ILEDB11SET[3:0] | | | | | W | Data for Matrix 11(DB11) |
| 0Ah | 08h | SCYCB12[1:0] | | SDLYB12[1:0] | | ILEDB12SET[3:0] | | | | | W | Data for Matrix 12(DB12) |
| 0Bh | 08h | SCYCB13[1:0] | | SDLYB13[1:0] | | ILEDB13SET[3:0] | | | | | W | Data for Matrix 13(DB13) |
| 0Ch | 08h | SCYCB14[1:0] | | SDLYB14[1:0] | | ILEDB14SET[3:0] | | | | | W | Data for Matrix 14(DB14) |
| 0Dh | 08h | SCYCB15[1:0] | | SDLYB15[1:0] | | ILEDB15SET[3:0] | | | | | W | Data for Matrix 15(DB15) |
| 0Eh | 08h | SCYCB16[1:0] | | SDLYB16[1:0] | | ILEDB16SET[3:0] | | | | | W | Data for Matrix 16(DB16) |
| 0Fh | 08h | SCYCB20[1:0] | | SDLYB20[1:0] | | ILEDB20SET[3:0] | | | | | W | Data for Matrix 20(DB20) |
| 10h | 08h | SCYCB21[1:0] | | SDLYB21[1:0] | | ILEDB21SET[3:0] | | | | | W | Data for Matrix 21(DB21) |
| 11h | 08h | SCYCB22[1:0] | | SDLYB22[1:0] | | ILEDB22SET[3:0] | | | | | W | Data for Matrix 22(DB22) |
| 12h | 08h | SCYCB23[1:0] | | SDLYB23[1:0] | | ILEDB23SET[3:0] | | | | | W | Data for Matrix 23(DB23) |
| 13h | 08h | SCYCB24[1:0] | | SDLYB24[1:0] | | ILEDB24SET[3:0] | | | | | W | Data for Matrix 24(DB24) |
| 14h | 08h | SCYCB25[1:0] | | SDLYB25[1:0] | | ILEDB25SET[3:0] | | | | | W | Data for Matrix 25(DB25) |
| 15h | 08h | SCYCB26[1:0] | | SDLYB26[1:0] | | ILEDB26SET[3:0] | | | | | W | Data for Matrix 26(DB26) |
| 16h | 08h | SCYCB30[1:0] | | SDLYB30[1:0] | | ILEDB30SET[3:0] | | | | | W | Data for Matrix 30(DB30) |
| 17h | 08h | SCYCB31[1:0] | | SDLYB31[1:0] | | ILEDB31SET[3:0] | | | | | W | Data for Matrix 31(DB31) |
| 18h | 08h | SCYCB32[1:0] | | SDLYB32[1:0] | | ILEDB32SET[3:0] | | | | | W | Data for Matrix 32(DB32) |
| 19h | 08h | SCYCB33[1:0] | | SDLYB33[1:0] | | ILEDB33SET[3:0] | | | | | W | Data for Matrix 33(DB33) |
| 1Ah | 08h | SCYCB34[1:0] | | SDLYB34[1:0] | | ILEDB34SET[3:0] | | | | | W | Data for Matrix 34(DB34) |
| 1Bh | 08h | SCYCB35[1:0] | | SDLYB35[1:0] | | ILEDB35SET[3:0] | | | | | W | Data for Matrix 35(DB35) |
| 1Ch | 08h | SCYCB36[1:0] | | SDLYB36[1:0] | | ILEDB36SET[3:0] | | | | | W | Data for Matrix 36(DB36) |
| 1Dh | 08h | SCYCB40[1:0] | | SDLYB40[1:0] | | ILEDB40SET[3:0] | | | | | W | Data for Matrix 40(DB40) |
| 1Eh | 08h | SCYCB41[1:0] | | SDLYB41[1:0] | | ILEDB41SET[3:0] | | | | | W | Data for Matrix 41(DB41) |
| 1Fh | 08h | SCYCB42[1:0] | | SDLYB42[1:0] | | ILEDB42SET[3:0] | | | | | W | Data for Matrix 42(DB42) |
| 20h | 08h | SCYCB43[1:0] | | SDLYB43[1:0] | | ILEDB43SET[3:0] | | | | | W | Data for Matrix 43(DB43) |
| 21h | 08h | SCYCB44[1:0] | | SDLYB44[1:0] | | ILEDB44SET[3:0] | | | | | W | Data for Matrix 44(DB44) |
| 22h | 08h | SCYCB45[1:0] | | SDLYB45[1:0] | | ILEDB45SET[3:0] | | | | | W | Data for Matrix 45(DB45) |
| 23h | 08h | SCYCB46[1:0] | | SDLYB46[1:0] | | ILEDB46SET[3:0] | | | | | W | Data for Matrix 46(DB46) |
| 24h | 08h | SCYCB50[1:0] | | SDLYB50[1:0] | | ILEDB50SET[3:0] | | | | | W | Data for Matrix 50(DB50) |
| 25h | 08h | SCYCB51[1:0] | | SDLYB51[1:0] | | ILEDB51SET[3:0] | | | | | W | Data for Matrix 51(DB51) |
| 26h | 08h | SCYCB52[1:0] | | SDLYB52[1:0] | | ILEDB52SET[3:0] | | | | | W | Data for Matrix 52(DB52) |
| 27h | 08h | SCYCB53[1:0] | | SDLYB53[1:0] | | ILEDB53SET[3:0] | | | | | W | Data for Matrix 53(DB53) |
| 28h | 08h | SCYCB54[1:0] | | SDLYB54[1:0] | | ILEDB54SET[3:0] | | | | | W | Data for Matrix 54(DB54) |
| 29h | 08h | SCYCB55[1:0] | | SDLYB55[1:0] | | ILEDB55SET[3:0] | | | | | W | Data for Matrix 55(DB55) |
| 2Ah | 08h | SCYCB56[1:0] | | SDLYB56[1:0] | | ILEDB56SET[3:0] | | | | | W | Data for Matrix 56(DB56) |
| 2Bh | 08h | SCYCB60[1:0] | | SDLYB60[1:0] | | ILEDB60SET[3:0] | | | | | W | Data for Matrix 60(DB60) |
| 2Ch | 08h | SCYCB61[1:0] | | SDLYB61[1:0] | | ILEDB61SET[3:0] | | | | | W | Data for Matrix 61(DB61) |
| 2Dh | 08h | SCYCB62[1:0] | | SDLYB62[1:0] | | ILEDB62SET[3:0] | | | | | W | Data for Matrix 62(DB62) |
| 2Eh | 08h | SCYCB63[1:0] | | SDLYB63[1:0] | | ILEDB63SET[3:0] | | | | | W | Data for Matrix 63(DB63) |
| 2Fh | 08h | SCYCB64[1:0] | | SDLYB64[1:0] | | ILEDB64SET[3:0] | | | | | W | Data for Matrix 64(DB64) |
| 30h | 08h | SCYCB65[1:0] | | SDLYB65[1:0] | | ILEDB65SET[3:0] | | | | | W | Data for Matrix 65(DB65) |

| Address | default | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Block | R/W | Remark |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31h | 08h | SCYCB66[1:0] | | SDLYB66[1:0] | | ILEDB66SET[3:0] | | | | MATRIX Data | W | Data for Matrix 66(DB66) |
| 32h | 08h | SCYCB70[1:0] | | SDLYB70[1:0] | | ILEDB70SET[3:0] | | | | | W | Data for Matrix 70(DB70) |
| 33h | 08h | SCYCB71[1:0] | | SDLYB71[1:0] | | ILEDB71SET[3:0] | | | | | W | Data for Matrix 71(DB71) |
| 34h | 08h | SCYCB72[1:0] | | SDLYB72[1:0] | | ILEDB72SET[3:0] | | | | | W | Data for Matrix 72(DB72) |
| 35h | 08h | SCYCB73[1:0] | | SDLYB73[1:0] | | ILEDB73SET[3:0] | | | | | W | Data for Matrix 73(DB73) |
| 36h | 08h | SCYCB74[1:0] | | SDLYB74[1:0] | | ILEDB74SET[3:0] | | | | | W | Data for Matrix 74(DB74) |
| 37h | 08h | SCYCB75[1:0] | | SDLYB75[1:0] | | ILEDB75SET[3:0] | | | | | W | Data for Matrix 75(DB75) |
| 38h | 08h | SCYCB76[1:0] | | SDLYB76[1:0] | | ILEDB76SET[3:0] | | | | | W | Data for Matrix 76(DB76) |
| 39h | 08h | SCYCB80[1:0] | | SDLYB80[1:0] | | ILEDB80SET[3:0] | | | | | W | Data for Matrix 80(DB80) |
| 3Ah | 08h | SCYCB81[1:0] | | SDLYB81[1:0] | | ILEDB81SET[3:0] | | | | | W | Data for Matrix 81(DB81) |
| 3Bh | 08h | SCYCB82[1:0] | | SDLYB82[1:0] | | ILEDB82SET[3:0] | | | | | W | Data for Matrix 82(DB82) |
| 3Ch | 08h | SCYCB83[1:0] | | SDLYB83[1:0] | | ILEDB83SET[3:0] | | | | | W | Data for Matrix 83(DB83) |
| 3Dh | 08h | SCYCB84[1:0] | | SDLYB84[1:0] | | ILEDB84SET[3:0] | | | | | W | Data for Matrix 84(DB84) |
| 3Eh | 08h | SCYCB85[1:0] | | SDLYB85[1:0] | | ILEDB85SET[3:0] | | | | | W | Data for Matrix 85(DB85) |
| 3Fh | 08h | SCYCB86[1:0] | | SDLYB86[1:0] | | ILEDB86SET[3:0] | | | | | W | Data for Matrix 86(DB86) |
| 40h | 08h | SCYCB90[1:0] | | SDLYB90[1:0] | | ILEDB90SET[3:0] | | | | | W | Data for Matrix 90(DB90) |
| 41h | 08h | SCYCB91[1:0] | | SDLYB91[1:0] | | ILEDB91SET[3:0] | | | | | W | Data for Matrix 91(DB91) |
| 42h | 08h | SCYCB92[1:0] | | SDLYB92[1:0] | | ILEDB92SET[3:0] | | | | | W | Data for Matrix 92(DB92) |
| 43h | 08h | SCYCB93[1:0] | | SDLYB93[1:0] | | ILEDB93SET[3:0] | | | | | W | Data for Matrix 93(DB93) |
| 44h | 08h | SCYCB94[1:0] | | SDLYB94[1:0] | | ILEDB94SET[3:0] | | | | | W | Data for Matrix 94(DB94) |
| 45h | 08h | SCYCB95[1:0] | | SDLYB95[1:0] | | ILEDB95SET[3:0] | | | | | W | Data for Matrix 95(DB95) |
| 46h | 08h | SCYCB96[1:0] | | SDLYB96[1:0] | | ILEDB96SET[3:0] | | | | | W | Data for Matrix 96(DB96) |
| 47h | 08h | SCYCBA0[1:0] | | SDLYBA0[1:0] | | ILEDBA0SET[3:0] | | | | | W | Data for Matrix A0(DBA0) |
| 48h | 08h | SCYCBA1[1:0] | | SDLYBA1[1:0] | | ILEDBA1SET[3:0] | | | | | W | Data for Matrix A1(DBA1) |
| 49h | 08h | SCYCBA2[1:0] | | SDLYBA2[1:0] | | ILEDBA2SET[3:0] | | | | | W | Data for Matrix A2(DBA2) |
| 4Ah | 08h | SCYCBA3[1:0] | | SDLYBA3[1:0] | | ILEDBA3SET[3:0] | | | | | W | Data for Matrix A3(DBA3) |
| 4Bh | 08h | SCYCBA4[1:0] | | SDLYBA4[1:0] | | ILEDBA4SET[3:0] | | | | | W | Data for Matrix A4(DBA4) |
| 4Ch | 08h | SCYCBA5[1:0] | | SDLYBA5[1:0] | | ILEDBA5SET[3:0] | | | | | W | Data for Matrix A5(DBA5) |
| 4Dh | 08h | SCYCBA6[1:0] | | SDLYBA6[1:0] | | ILEDBA6SET[3:0] | | | | | W | Data for Matrix A6(DBA6) |
| 4Eh | 08h | SCYCBB0[1:0] | | SDLYBB0[1:0] | | ILEDBB0SET[3:0] | | | | | W | Data for Matrix B0(DBB0) |
| 4Fh | 08h | SCYCBB1[1:0] | | SDLYBB1[1:0] | | ILEDBB1SET[3:0] | | | | | W | Data for Matrix B1(DBB1) |
| 50h | 08h | SCYCBB2[1:0] | | SDLYBB2[1:0] | | ILEDBB2SET[3:0] | | | | | W | Data for Matrix B2(DBB2) |
| 51h | 08h | SCYCBB3[1:0] | | SDLYBB3[1:0] | | ILEDBB3SET[3:0] | | | | | W | Data for Matrix B3(DBB3) |
| 52h | 08h | SCYCBB4[1:0] | | SDLYBB4[1:0] | | ILEDBB4SET[3:0] | | | | | W | Data for Matrix B4(DBB4) |
| 53h | 08h | SCYCBB5[1:0] | | SDLYBB5[1:0] | | ILEDBB5SET[3:0] | | | | | W | Data for Matrix B5(DBB5) |
| 54h | 08h | SCYCBB6[1:0] | | SDLYBB6[1:0] | | ILEDBB6SET[3:0] | | | | | W | Data for Matrix B6(DBB6) |
| 55h | 08h | SCYCBC0[1:0] | | SDLYBC0[1:0] | | ILEDBC0SET[3:0] | | | | | W | Data for Matrix C0(DBC0) |
| 56h | 08h | SCYCBC1[1:0] | | SDLYBC1[1:0] | | ILEDBC1SET[3:0] | | | | | W | Data for Matrix C1(DBC1) |
| 57h | 08h | SCYCBC2[1:0] | | SDLYBC2[1:0] | | ILEDBC2SET[3:0] | | | | | W | Data for Matrix C2(DBC2) |
| 58h | 08h | SCYCBC3[1:0] | | SDLYBC3[1:0] | | ILEDBC3SET[3:0] | | | | | W | Data for Matrix C3(DBC3) |
| 59h | 08h | SCYCBC4[1:0] | | SDLYBC4[1:0] | | ILEDBC4SET[3:0] | | | | | W | Data for Matrix C4(DBC4) |
| 5Ah | 08h | SCYCBC5[1:0] | | SDLYBC5[1:0] | | ILEDBC5SET[3:0] | | | | | W | Data for Matrix C5(DBC5) |
| 5Bh | 08h | SCYCBC6[1:0] | | SDLYBC6[1:0] | | ILEDBC6SET[3:0] | | | | | W | Data for Matrix C6(DBC6) |
| 5Ch | 08h | SCYCBD0[1:0] | | SDLYBD0[1:0] | | ILEDBD0SET[3:0] | | | | | W | Data for Matrix D0(DBD0) |
| 5Dh | 08h | SCYCBD1[1:0] | | SDLYBD1[1:0] | | ILEDBD1SET[3:0] | | | | | W | Data for Matrix D1(DBD1) |
| 5Eh | 08h | SCYCBD2[1:0] | | SDLYBD2[1:0] | | ILEDBD2SET[3:0] | | | | | W | Data for Matrix D2(DBD2) |
| 5Fh | 08h | SCYCBD3[1:0] | | SDLYBD3[1:0] | | ILEDBD3SET[3:0] | | | | | W | Data for Matrix D3(DBD3) |
| 60h | 08h | SCYCBD4[1:0] | | SDLYBD4[1:0] | | ILEDBD4SET[3:0] | | | | | W | Data for Matrix D4(DBD4) |

| Address | default | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Block | R/W | Remark |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 61h | 08h | SCYCBD5[1:0] | | SDLYBD5[1:0] | | ILEDBD5SET[3:0] | | | | MATRIX Data | W | Data for Matrix D5(DBD5) |
| 62h | 08h | SCYCBD6[1:0] | | SDLYBD6[1:0] | | ILEDBD6SET[3:0] | | | | | W | Data for Matrix D6(DBD6) |
| 63h | 08h | SCYCBE0[1:0] | | SDLYBE0[1:0] | | ILEDBE0SET[3:0] | | | | | W | Data for Matrix E0(DBE0) |
| 64h | 08h | SCYCBE1[1:0] | | SDLYBE1[1:0] | | ILEDBE1SET[3:0] | | | | | W | Data for Matrix E1(DBE1) |
| 65h | 08h | SCYCBE2[1:0] | | SDLYBE2[1:0] | | ILEDBE2SET[3:0] | | | | | W | Data for Matrix E2(DBE2) |
| 66h | 08h | SCYCBE3[1:0] | | SDLYBE3[1:0] | | ILEDBE3SET[3:0] | | | | | W | Data for Matrix E3(DBE3) |
| 67h | 08h | SCYCBE4[1:0] | | SDLYBE4[1:0] | | ILEDBE4SET[3:0] | | | | | W | Data for Matrix E4(DBE4) |
| 68h | 08h | SCYCBE5[1:0] | | SDLYBE5[1:0] | | ILEDBE5SET[3:0] | | | | | W | Data for Matrix E5(DBE5) |
| 69h | 08h | SCYCBE6[1:0] | | SDLYBE6[1:0] | | ILEDBE6SET[3:0] | | | | | W | Data for Matrix E6(DBE6) |
| 6Ah | 08h | SCYCBF0[1:0] | | SDLYBF0[1:0] | | ILEDBF0SET[3:0] | | | | | W | Data for Matrix F0(DBF0) |
| 6Bh | 08h | SCYCBF1[1:0] | | SDLYBF1[1:0] | | ILEDBF1SET[3:0] | | | | | W | Data for Matrix F1(DBF1) |
| 6Ch | 08h | SCYCBF2[1:0] | | SDLYBF2[1:0] | | ILEDBF2SET[3:0] | | | | | W | Data for Matrix F2(DBF2) |
| 6Dh | 08h | SCYCBF3[1:0] | | SDLYBF3[1:0] | | ILEDBF3SET[3:0] | | | | | W | Data for Matrix F3(DBF3) |
| 6Eh | 08h | SCYCBF4[1:0] | | SDLYBF4[1:0] | | ILEDBF4SET[3:0] | | | | | W | Data for Matrix F4(DBF4) |
| 6Fh | 08h | SCYCBF5[1:0] | | SDLYBF5[1:0] | | ILEDBF5SET[3:0] | | | | | W | Data for Matrix F5(DBF5) |
| 70h | 08h | SCYCBF6[1:0] | | SDLYBF6[1:0] | | ILEDBF6SET[3:0] | | | | | W | Data for Matrix F6(DBF6) |
| 71h | 08h | SCYCBG0[1:0] | | SDLYBG0[1:0] | | ILEDBG0SET[3:0] | | | | | W | Data for Matrix G0(DBG0) |
| 72h | 08h | SCYCBG1[1:0] | | SDLYBG1[1:0] | | ILEDBG1SET[3:0] | | | | | W | Data for Matrix G1(DBG1) |
| 73h | 08h | SCYCBG2[1:0] | | SDLYBG2[1:0] | | ILEDBG2SET[3:0] | | | | | W | Data for Matrix G2(DBG2) |
| 74h | 08h | SCYCBG3[1:0] | | SDLYBG3[1:0] | | ILEDBG3SET[3:0] | | | | | W | Data for Matrix G3(DBG3) |
| 75h | 08h | SCYCBG4[1:0] | | SDLYBG4[1:0] | | ILEDBG4SET[3:0] | | | | | W | Data for Matrix G4(DBG4) |
| 76h | 08h | SCYCBG5[1:0] | | SDLYBG5[1:0] | | ILEDBG5SET[3:0] | | | | | W | Data for Matrix G5(DBG5) |
| 77h | 08h | SCYCBG6[1:0] | | SDLYBG6[1:0] | | ILEDBG6SET[3:0] | | | | | W | Data for Matrix G6(DBG6) |

## ●Register Map

Address 00H < Software Reset >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | W | - | - | - | - | - | - | - | SFTRST |
| Initial value | 00H | - | - | - | - | - | - | - | 0 |

Bit 0 : SFTRST Software Reset
"0" : Reset cancel
"1" : Reset(All register initializing)

*SFTRST register return to 0 automatically.

Address 01H <OSC control >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 01H | W | - | - | - | - | OSCEN | - | - | - |
| Initial value | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3 : OSCEN OSC block ON/OFF control
"0" : OFF(Initial)
"1" : ON

This register should not change into "1 "→" 0" at the time of START (30h, D0) register ="1" setup (under lighting operation).
This register must be set to "0" after LED putting out lights ("START register = 0"), and please surely stop an internal oscillation circuit.

Address 11H < LED1-6 Enable >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 11H | W | - | - | LED6ON | LED5ON | LED4ON | LED3ON | LED2ON | LED1ON |
| Initial value | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0 : LED1ON LED1 ON/OFF setting
"0" : LED1 OFF(initial)
"1" : LED1 ON

Bit 1 : LED2ON LED2 ON/OFF setting
"0" : LED2 OFF(initial)
"1" : LED2 ON

Bit 2 : LED3ON LED3 ON/OFF setting
"0" : LED3 OFF(initial)
"1" : LED3 ON

Bit 3 : LED4ON LED4 ON/OFF setting
"0" : LED4 OFF(initial)
"1" : LED4 ON

Bit 4 : LED5ON LED5 ON/OFF setting
"0" : LED5 OFF(initial)
"1" : LED5 ON

Bit 5 : LED6ON LED6 ON/OFF setting
"0" : LED6 OFF(initial)
"1" : LED6 ON

* Current setting follows ILEDAXXSET[3:0] or ILEDBXXSET[3:0] register.

Address 12H < LED7-12 Enable >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 12H | W | - | - | LED12ON | LED11ON | LED10ON | LED9ON | LED8ON | LED7ON |
| Initial value | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0 : LED7ON LED7 ON/OFF setting
"0" : LED7 OFF(initial)
"1" : LED7 ON

Bit 1 : LED8ON LED8 ON/OFF setting
"0" : LED8 OFF(initial)
"1" : LED8 ON

Bit 2 : LED9ON LED9 ON/OFF setting
"0" : LED9 OFF(initial)
"1" : LED9 ON

Bit 3 : LED10ON LED10 ON/OFF setting
"0" : LED10 OFF(initial)
"1" : LED10 ON

Bit 4 : LED11ON LED11 ON/OFF setting
"0" : LED11 OFF(initial)
"1" : LED11 ON

Bit 5 : LED12ON LED12 ON/OFF setting
"0" : LED12 OFF(initial)
"1" : LED12 ON

* Current setting follows ILEDAXXSET[3:0] or ILEDBXXSET[3:0] register.

Address 13H < LED13-17 Enable >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 13H | W | - | - | - | LED17ON | LED16ON | LED15ON | LED14ON | LED13ON |
| Initial value | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0 : LED13ON LED13 ON/OFF setting
"0" : LED13 OFF(initial)
"1" : LED13 ON

Bit 1 : LED14ON LED14 ON/OFF setting
"0" : LED14 OFF(initial)
"1" : LED14 ON

Bit 2 : LED15ON LED15 ON/OFF setting
"0" : LED15 OFF(initial)
"1" : LED15 ON

Bit 3 : LED16ON LED16 ON/OFF setting
"0" : LED16 OFF(initial)
"1" : LED16 ON

Bit 4 : LED17ON LED17 ON/OFF setting
"0" : LED17 OFF(initial)
"1" : LED17 ON

* Current setting follows ILEDAXXSET[3:0] or ILEDBXXSET[3:0] register.

Address 17H < LED14-17 TDMA Enable >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 17H | W | - | - | - | - | LED17 TDMAON | LED16 TDMAON | LED15 TDMAON | LED14 TDMAON |
| Initial value | 0FH | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

Bit 0 : LED14TDMAON TDMA control Enable setting for LED14
"0" : TDMA control for LED14 is OFF
LED current value is set by ILEDAD0SET[3:0] or ILEDBD0SET[3:0] (it changes by the OAB [7Fh, D1] register).
It becomes the setting value of ILEDAD0SET [3:0] until scroll reset is carried out
by SCLRST (2Eh, D0) register ="1" after a scroll stop, under scrolling.
"1" : TDMA control for LED14 is ON (initial)

Bit 1 : LED15TDMAON TDMA control Enable setting for LED15
"0" : TDMA control for LED15 is OFF
LED current value is set by ILEDAE0SET[3:0] or ILEDBE0SET[3:0]. (it changes by the OAB [7Fh, D1] register).
It becomes the setting value of ILEDAE0SET [3:0] until scroll reset is carried out
by SCLRST (2Eh, D0) register ="1" after a scroll stop, under scrolling.
"1" : TDMA control for LED15 is ON (initial)

Bit 2 : LED16TDMAON TDMA control Enable setting for LED16
"0" : TDMA control for LED16 is OFF
LED current value is set by ILEDAF0SET[3:0] or ILEDBF0SET[3:0]. (it changes by the OAB [7Fh, D1] register).
It becomes the setting value of ILEDAF0SET [3:0] until scroll reset is carried out
by SCLRST (2Eh, D0) register ="1" after a scroll stop, under scrolling.
"1" : TDMA control for LED16 is ON (initial)

Bit 3 : LED17TDMAON TDMA control Enable setting for LED17
"0" : TDMA control for LED17 is OFF
LED current value is set by ILEDAG0SET[3:0] or ILEDBG0SET[3:0]. (it changes by the OAB [7Fh, D1] register).
It becomes the setting value of ILEDAG0SET [3:0] until scroll reset is carried out
by SCLRST (2Eh, D0) register ="1" after a scroll stop, under scrolling.
"1" : TDMA control for LED17 is ON (initial)

* The setting change at the time of START (30h, D0) register ="1" of this register is prohibition.
* LED, which is set to "0"(TDMA off), is put on and not controlled by SYNC terminal however SYNCON (21h,D2) register is set to "1".
* Please use this register only in the following combination.

| LED17TDMAON | LED16TDMAON | LED15TDMAON | LED14TDMAON |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 |
| Except the above: Prohibition | | | |

Address 20H < LED1-17 PWM setting >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 20H | W | - | - | PWMSET [5:0] | | | | | |
| Initial value | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5-0 : PWMSET[5:0] LED1-17 PWM DUTY setting
"000000" : 0/63＝0%(initial)
"000001" : 1/63＝1.59%
:
:
"100000" : 32/63＝50.8%
:
:
"111110" : 62/63＝98.4%
"111111" : 63/63＝100%

*Please refer to Description of operation, chapter 2

Address 21H < SYNC operation control >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 21H | W | - | - | - | - | SYNCACT | SYNCON | CLKOUT | CLKIN |
| Initial value | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0 : CLKIN Selection CLK for PWM control
"0" : Internal OSC (initial)
"1" : External CLK input

Bit 1 : CLKOUT Output CLK enable
"0" : CLK is not output (initial)
"1" : Output selected CLK from CLKOUT pin

As for CLKIN & CLKOUT, setting change is forbidden under OSCEN (01h, D3) register ="1" and also under clock input to CLKIN terminal.

Bit 2 : SYNCON SYNC operation enable
"0" : Disable SYNC operation (initial)
"1" : SYNC pin control LED driver ON/OFF

Bit 3 : SYNCACT SYNC operation setting
"0" : When SYNC pin is "L", LED drivers are ON (initial)
"1" : When SYNC pin is "H", LED drivers are ON

Address 2DH < PWM, SLOPE, SCROLL ON/OFF setting >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 2DH | W | - | - | - | - | - | PWMEN | SLPEN | SCLEN |
| Initial value | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0 : SCLEN SCROLL operation ON/OFF setting
"0" : SCROL operation OFF(initial value)
"1" : SCROL operation ON

Bit 1 : SLPEN SLOPE operation ON/OFF setting
"0" : SLOPE operation OFF(initial value)
"1" : SLOPE operation ON

Bit 2 : PWMEN PWM control at LED1-17 ON/OFF setting
"0" : PWM operation is invalid(initial value)
"1" : PWM operation is valid

*Please refer to Description of operation, chapter 2

Address 2EH < Reset scroll >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 2EH | W | - | - | - | - | - | - | - | SCLRST |
| Initial value | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0 : SCLRST Reset scroll state
"0" : Not reset(initial value)
"1" : Reset scroll state

* SCLRST register return to 0 automatically

Address 2FH < Scroll setting >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 2FH | W | - | SCLSPEED [2:0] | | | UP | DOWN | RIGHT | LEFT |
| Initial value | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0 : LEFT Setting the scroll operation from right to left
"0" : Scroll operation OFF (initial value)
"1" : Scroll operation ON

Bit 1 : RIGHT Setting the scroll operation from left to right
"0" : Scroll operation OFF (initial value)
"1" : Scroll operation ON

*When LEFT operation is valid, RIGHT setting is ignored.

Bit 2 : DOWN Setting the scroll operation from top to bottom
"0" : Scroll operation OFF (initial value)
"1" : Scroll operation ON

Bit 3 : UP Setting the scroll operation from bottom to top
"0" : Scroll operation OFF (initial value)
"1" : Scroll operation ON

*When UP operation is valid, DOWN setting is ignored.

Bit 6-4 : SCLSPEED[2:0] Setting the scroll speed
"000" : 0.1s (initial value)
"001" : 0.2s
"010" : 0.3s
"011" : 0.4s
"100" : 0.5s
"101" : 0.6s
"110" : 0.7s
"111" : 0.8s

*Setting time is based on OSC frequency, and the above-mentioned shows the value under Typ (1.2MHz).
*Setting time changes on CLKIN terminal input frequency at the external clock operation.

Example)
CLKIN input frequency=1.2MHz→"000": 0.1sec (it is the same as the above)
CLKIN input frequency=2.4MHz→"000": 0.05sec
CLKIN input frequency= 0.6MHz→"000": 0.2sec

Address 30H < LED Matrix control >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 30H | W | - | - | - | - | - | - | - | START |
| Initial value | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0 : START Lighting/turning off bit of MATRIX LED(LED1-17)
"0" : MATRIX LED(LED1-17) Lights out
"1" : MATRIX LED(LED1-17) Lighting, SLOPE and SCROLL sequence start

Address 31H < Matrix data clear >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 31H | W | - | - | - | - | - | - | CLRB | CLRA |
| Initial value | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0 : CLRA Reset A-pattern register
"0" : A-pattern register is not reset and writable(initial value)
"1" : A-pattern register is reset

Bit 0 : CLRB Reset B-pattern register
"0" : B-pattern register is not reset and writable(initial value)
"1" : B-pattern register is reset

*CLRA and CLRB register return to 0 automatically.

Address 7FH < Register map change >

| Address (Index) | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 7FH | W | - | - | - | - | - | IAB | OAB | RMCG |
| Initial value | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0 : RMCG Change register map
"0" : Control register is selected(initial value)
"1" : A-pattern register or B-pattern register is selected

Bit 1 : OAB Select register to output for matrix
"0" : A-pattern register is selected(initial value)
"1" : B-pattern register is selected

Bit 2 : IAB Select register to write matrix data
"0" : A-pattern register is selected(initial value)
"1" : B-pattern register is selected

* It is prohibition to write A-pattern data when A-pattern is displaying (OAB=0).
Also, it is prohibition to write B-pattern data when B-pattern is displaying (OAB=1).
Change of a display picture should be done by change of the OAB register, after updating of a non-displaying pattern register.