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Low Consumption Power Class D Amplifier

9W+9W Analog Input Class D Speaker Amplifier

BD28411MUV

General Description

BD28411MUV is 9W+9W stereo class D amplifier which does not require an external heat sink.
This IC is incorporated with a precise oscillator to generate multiple switching frequencies that can avoid the AM radio interference. In addition, 2.1Ch audio system can be realized by master and slave operation without beat noise caused by interference between two ICs. Furthermore, this IC realizes lower power consumption during small power output, so this product is most suitable for battery equipped speaker systems such as wireless speakers.

Features

- Analog Differential Input
- Low Standby Current
- Output Feedback Circuitry prevents sound quality degradation caused by power supply voltage fluctuation, achieves low noise and low distortion, eliminates the need of large electrolytic-capacitors for decoupling.
- Power limit function (Linearly-programmable)
- Selectable switching frequency (AM avoidance function)
- Synchronization control is supported (Selectable Master and Slave operation)
- Parallel BTL (PBTL) is supported
- Wide voltage range (V_{CC}=4.5V to 13V)
- High efficiency and low-heat-generation make the system smaller, thinner, and more power-saving
- Pop noise prevention during power supply ON/OFF
- High reliability design by built-in protection circuits
  - Overheat protection
  - Under voltage protection
  - Output short protection
  - Output DC voltage protection
- Small package (VQFN032V5050) achieves mount area reduction

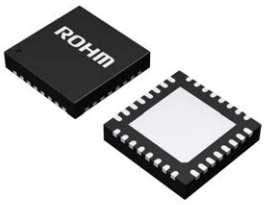
Applications

- Wireless speaker, Small active speaker, Portable audio equipment, etc.

Key Specifications

- Supply Voltage Range: 4.5V to 13V
- Speaker Output Power: 9W+9W (Typ)
  (V_{CC}=12V, R_L=8Ω, PLIMIT=0V)
- Total Harmonic Distortion Ratio:
  0.03% (Typ) @Po=1W
  (V_{CC}=11V, R_L=8Ω, PLIMIT=0V)
- Crosstalk: 100dB (Typ)
- PSRR: 55dB (Typ)
- Output Noise Voltage: -80dBV (Typ)
- Standby Current: 0.1μA (Typ)
- Operating Current: 16mA (Typ)
  (No load or filter, No signal)
- Operating Temperature Range: -25°C to +85°C

Package W(Typ) x D(Typ) x H(Max)



VQFN032V5050
5.00mm x 5.00mm x 1.00mm

Typical Application Circuit

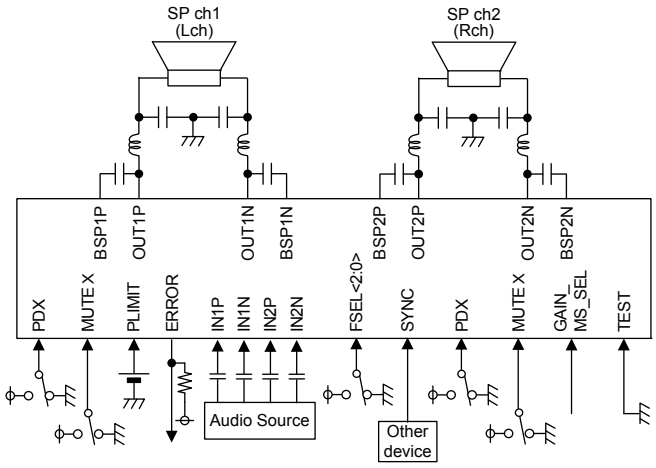


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

(TOP VIEW)

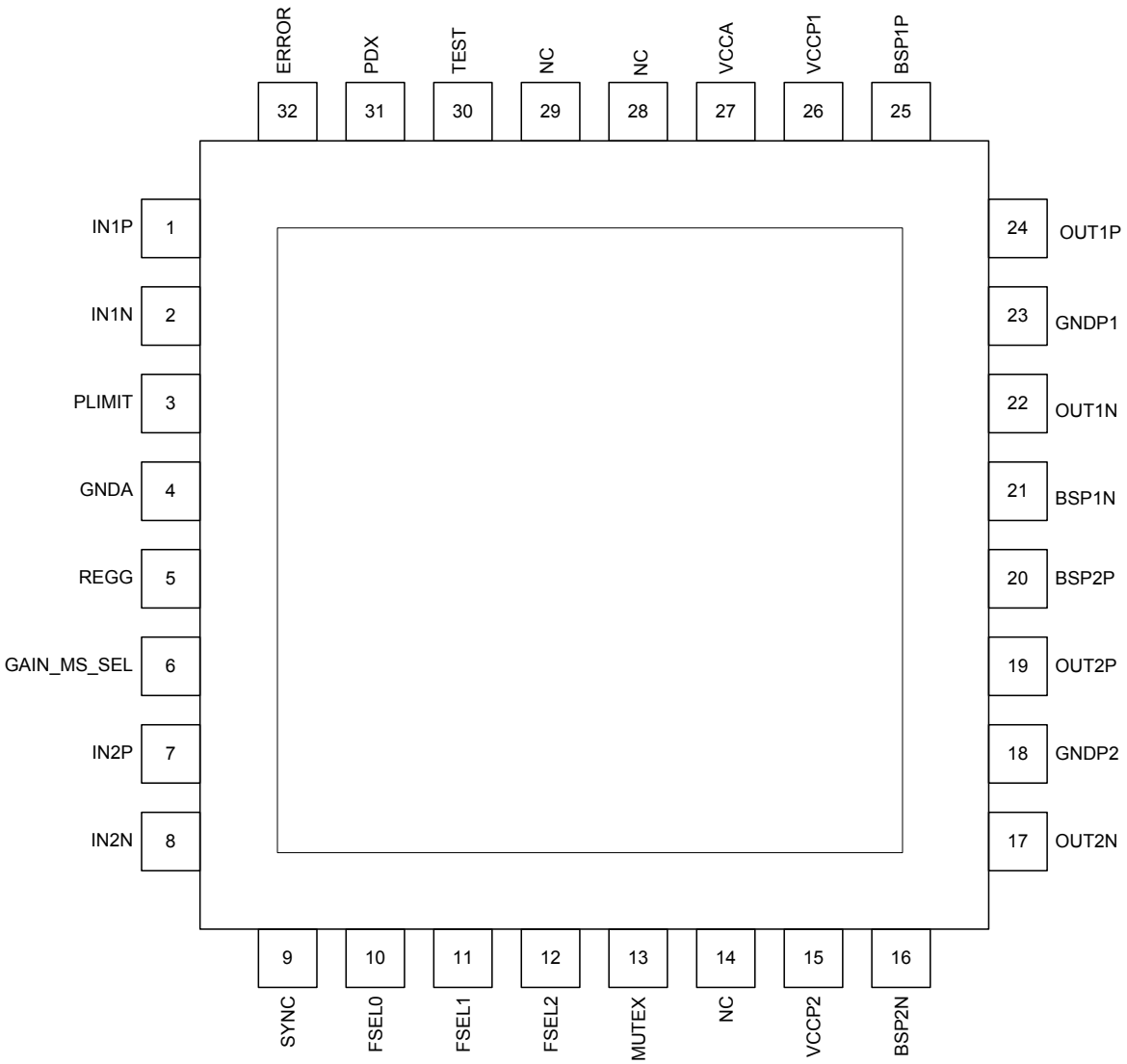
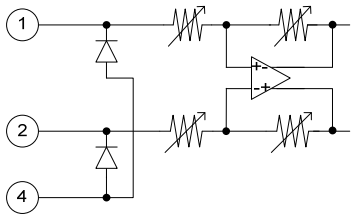
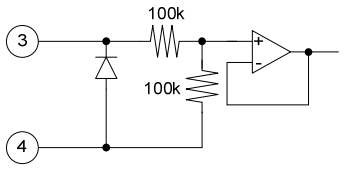
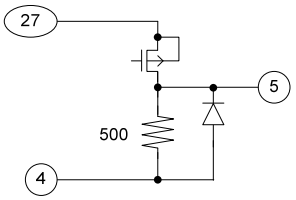
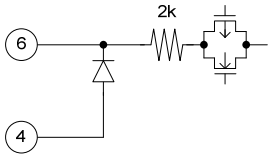
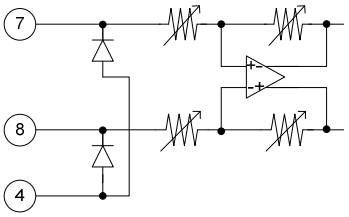
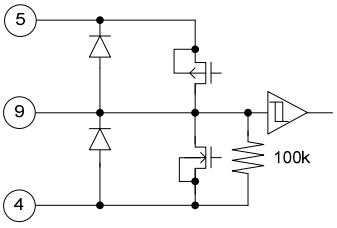
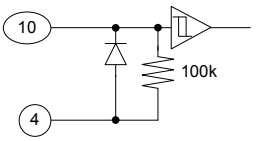
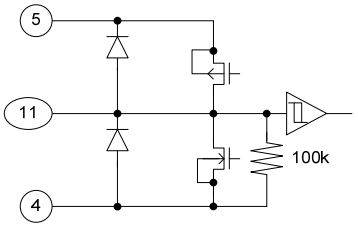
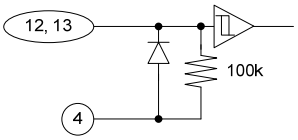
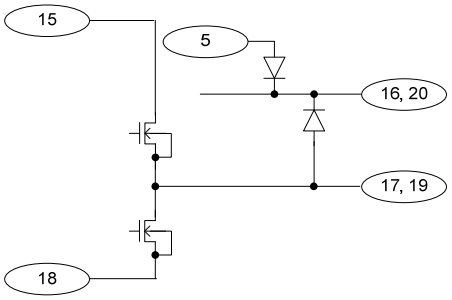
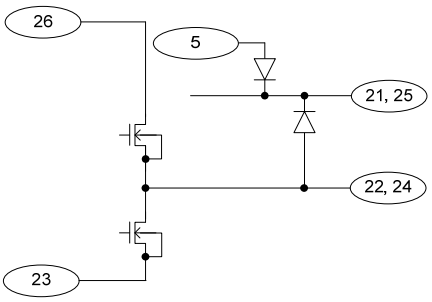
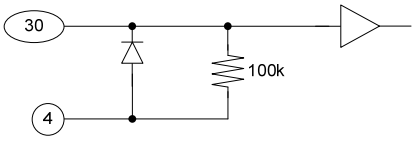


Figure 2. Pin Configuration

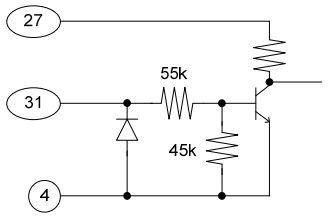
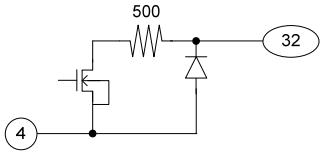
Pin Description

Pin No.	Pin Name	IO	Function	Internal Equivalent Circuit
1	IN1P	I	Positive input pin for Ch1	
2	IN1N	I	Negative input pin for Ch1	
3	PLIMIT	I	Power limit level setting pin	
4	GNDA	-	GND pin for Analog signal	
5	REGG	O	Internal power supply pin for Gate driver Please connect a capacitor. *The REGG terminal of BD28411MUV should not be used as external supply. Therefore, do not connect anything except the capacitor for stabilization and the resistors for setting of GAIN_MS_SEL and PLIMIT.	
6	GAIN_MS_SEL	I	Gain and Master/Slave mode Setting pin	
7	IN2P	I	Positive input pin for Ch2	
8	IN2N	I	Negative input pin for Ch2	
9	SYNC	I/O	Clock input/output pin to synchronize multiple class D amplifiers	

Pin Description – continued

10	FSEL0	I	PWM frequency setting pin	
11	FSEL1	I	PWM frequency setting pin	
12	FSEL2	I	PWM frequency setting pin	
13	MUTEX	I	Speaker output mute control pin H: Mute OFF L: Mute ON	
14	NC	-	Non connection	
15	VCCP2	-	Power supply pin for Ch2 PWM signal Please connect a capacitor.	
16	BSP2N	O	Boot-strap pin of Ch2 negative PWM signal Please connect a capacitor.	
17	OUT2N	O	Output pin of Ch2 negative PWM signal Please connect to output LPF.	
18	GNDP2	-	GND pin for Ch2 PWM signal	
19	OUT2P	O	Output pin of Ch2 positive PWM signal Please connect to output LPF.	
20	BSP2P	O	Boot-strap pin of Ch2 positive PWM signal Please connect a capacitor.	
21	BSP1N	O	Boot-strap pin of Ch1 negative PWM signal Please connect a capacitor.	
22	OUT1N	O	Output pin of Ch1 negative PWM signal Please connect to output LPF.	
23	GNDP1	-	GND pin for Ch1 PWM signal	
24	OUT1P	O	Output pin of Ch1 positive PWM signal Please connect to output LPF.	
25	BSP1P	O	Boot-strap pin of Ch1 positive PWM signal Please connect a capacitor.	
26	VCCP1	-	Power supply pin for Ch1 PWM signal Please connect a capacitor.	
27	VCCA	-	Power supply pin for Analog signal Please connect a capacitor.	
28	NC	-	Non connection	
29	NC	-	Non connection	
30	TEST	I	Test pin Please connect to GND.	

Pin Description – continued

31	PDX	I	Power down setting pin H: Active L: Standby	
32	ERROR	O	Error flag pin Please connect to pull-up resistor. H: Normal L: Error detected *An error flag is outputted when Output Short Protection, DC Voltage Protection, and High Temperature Protection are operated. This flag shows IC condition during operation.	

The numerical value of internal equivalent circuit is typical value, not guaranteed value.

Block Diagram

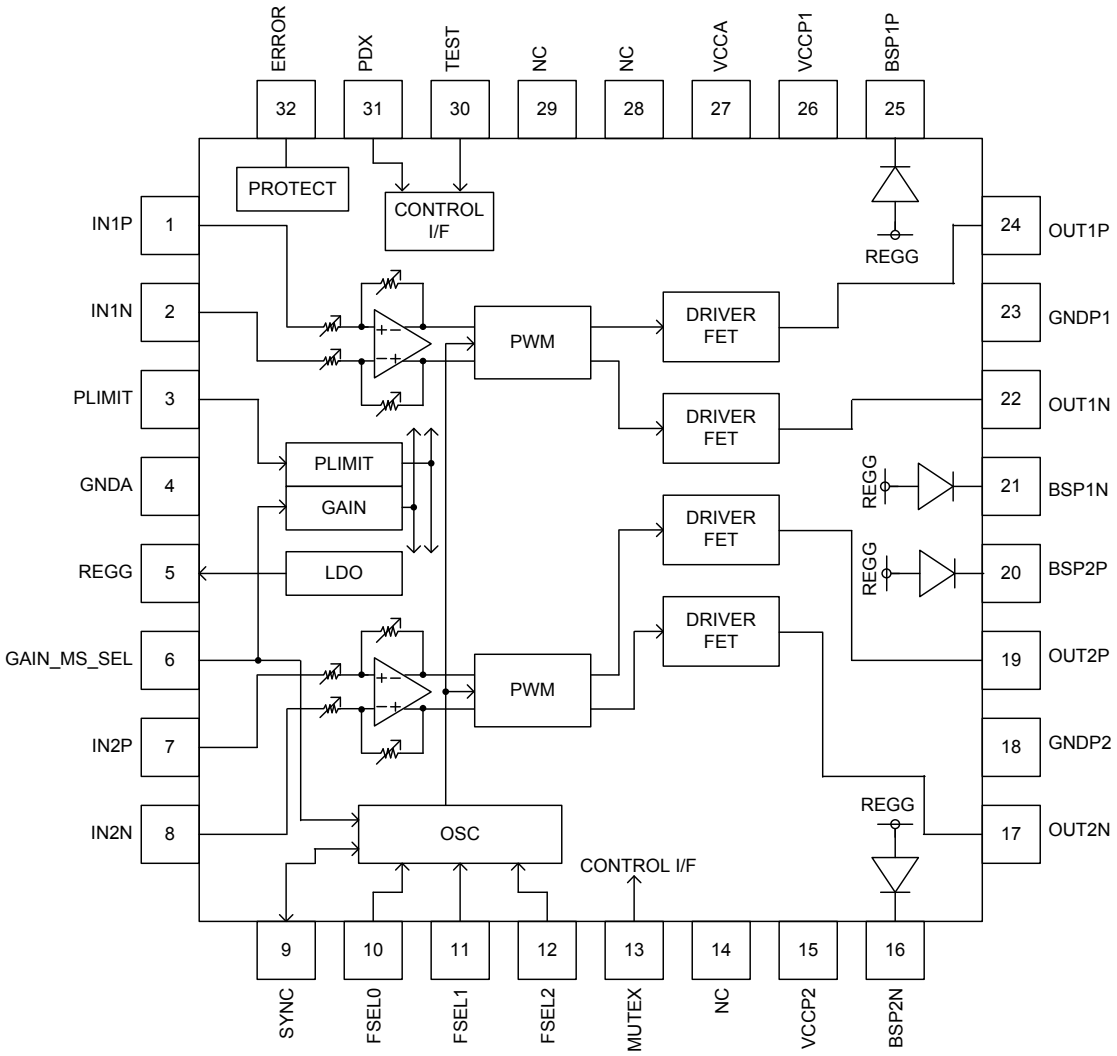


Figure 3. Block Diagram

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit	Applied pins and Conditions
Supply Voltage(Note 1)	V_{CCMAX}	-0.3 to +15.5	V	VCCA,VCCP1,VCCP2
Power Dissipation(Note 2)	Pd	3.26(Note 3)	W	Please refer to Power Dissipation for details.
		4.56(Note 4)	W	
Input Voltage1(Note 1)	V_{IN}	-0.3 to +V_{REGG}	V	IN1P, IN1N, IN2P, IN2N, PLIMIT, GAIN_MS_SEL, PLIMIT, SYNC(Note 5), FSEL0, FSEL1, FSEL2, PDX, MUTEX
Input Voltage2(Note 1)	V_{ERR}	-0.3 to +7	V	ERROR
Pin Voltage1(Note 1) (Note 6)	V_{PIN1}	-0.3 to +V_{CCMAX}	V	OUT1P, OUT1N, OUT2P, OUT2N
Operating Temperature	Topr	-25 to +85	°C	
Storage Temperature	Tstg	-55 to +150	°C	
Junction Temperature	Tjmax	+150	°C	

(Note 1) The voltage that can be applied reference to GND (Pin4, 18, 23).
(Note 2) Do not exceed Pd and Tjmax=150°C.
(Note 3) Derate by 26.1mW/°C for operating above Ta=25°C when mounted on 74.2mm × 74.2mm × 1.6mm, FR4, 4-layer glass epoxy board (Top and bottom layer back copper foil size: 20.2mm^2, 2nd and 3rd layer back copper foil size: 5505mm^2). There are thermal vias on the board.
(Note 4) Derate by 36.5mW/°C for operating above Ta=25°C when mounted on 74.2mm × 74.2mm × 1.6mm, FR4, 4-layer glass epoxy board (Copper area: 5505mm^2). There are thermal vias on the board.
(Note 5) SYNC pin is I/O pin. It is specified for input mode.
(Note 6) Please use under this rating including the AC peak waveform (overshoot) for all conditions.
Only undershoot is allowed at condition of ≦ 15.5V by the VCC reference and ≦ 10nsec (cf. Figure 4)

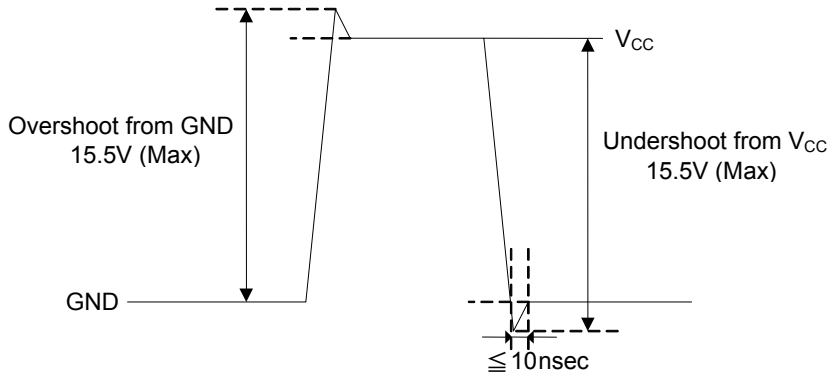


Figure 4. Overshoot and Undershoot

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= -25°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Applied pins and Conditions
Supply Voltage	V_{IN}	4.5	-	13	V	VCCA, VCCP1, VCCP2
Minimum Load Impedance(Note 7)	R_{L1}	5.4	-	-	Ω	BTL
	R_{L2}	3.2	-	-	Ω	PBTL
High Level Input Voltage	V_{IH}	2.0	-	-	V	FSEL0, FSEL1, FSEL2, MUTEX, PDX
Low Level Input Voltage	V_{IL}	0	-	0.8	V	FSEL0, FSEL1, FSEL2, MUTEX, PDX
Low Level Output Voltage	V_{OL}	-	-	0.8	V	ERROR, I_{OL}=0.5mA

(Note 7) Pd should not be exceeded.

Electrical Characteristics

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, R_L=8Ω, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

Parameter	Symbol	Min	Typ	Max	Unit	Applied pins and Conditions
Quiescent Standby Current	I_{CC1}	-	0.1	25	μA	No load or filter, PDX=L, MUTEX=L
Quiescent Mute Current	I_{CC2}	-	10	20	mA	No load or filter, PDX=H, MUTEX=L
Quiescent Operating Current	I_{CC3}	-	16	32	mA	No load or filter, No signal, PDX=H, MUTEX=H
Regulator Output Voltage	V_{REGG}	4.45	5.55	6.05	V	PDX=H, MUTEX=H
Input Pull Down Impedance 1	R_{IN1}	70	100	130	kΩ	MUTEX, PDX, FSEL0, FSEL1, FSEL2, SYNC(Slave mode only),
Input Pull Down Impedance 2	R_{IN2}	140	200	260	kΩ	PLIMIT
Output Power(Note 8)	P_{O1}	-	9	-	W	V_{CC}=12V, THD+N=10%
Gain 1(Note 8)	G_{V1}	19	20	21	dB	Po=1W, GAIN_MS_SEL= 0V
Gain 2(Note 8)	G_{V2}	25	26	27	dB	P_O=1W , GAIN_MS_SEL= 2/9 × V_{REGG}
Gain 3(Note 8)	G_{V3}	31	32	33	dB	P_O=1W, GAIN_MS_SEL= 3/9 × V_{REGG}
Gain 4(Note 8)	G_{V4}	35	36	37	dB	P_O=1W, GAIN_MS_SEL= 4/9 × V_{REGG}
Total Harmonic Distortion(Note 8)	THD	-	0.03	-	%	Po=1W, BW=20 to 20kHz (AES17)
Crosstalk(Note 8)	CT	60	100	-	dB	Po=1W, 1kHz BPF
PSRR(Note 8)	PSRR	-	55	-	dB	V_{ripple}=0.2 V_{P-P}, f=1kHz
Output Noise Level(Note 8)	V_{NO}	-	-80	-70	dBV	Po=0W, BW=IHF-A
PWM (Pulse Width Modulation) Frequency	f_{PWM1}	564	600	636	kHz	FSEL2=H, FSEL1=L, FSEL0=H
	f_{PWM2}	470	500	530	kHz	FSEL2=H, FSEL1=L, FSEL0=L
	f_{PWM3}	376	400	424	kHz	FSEL2=L, FSEL1=H, FSEL0=H

(Note 8) The value is specified as typical application. Actual value depends on PCB layout and external components.

Typical Performance Curves

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, R_L=8Ω, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

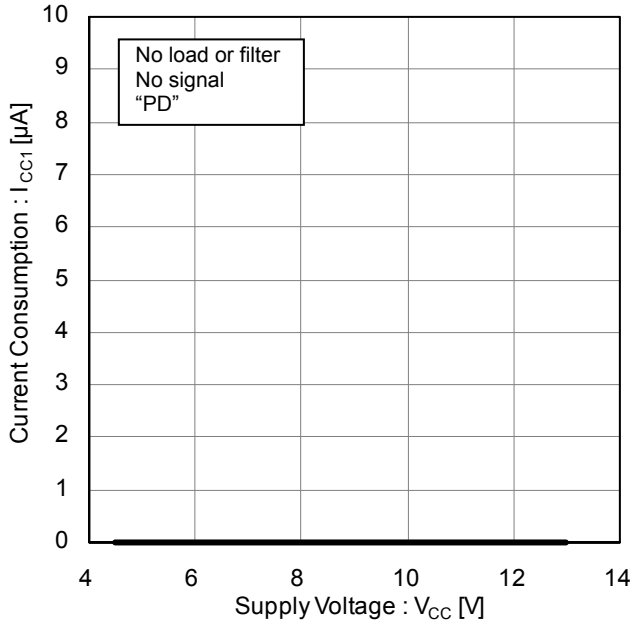


Figure 5. Circuit Current vs Supply Voltage (PD)

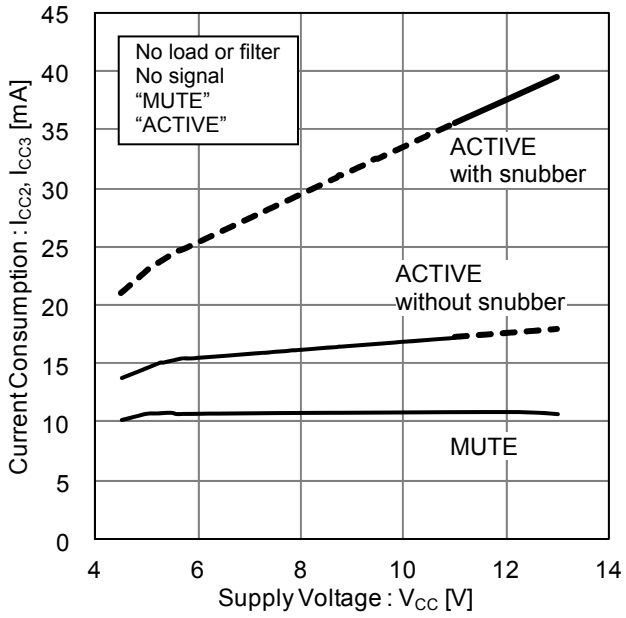


Figure 6. Circuit Current vs Supply Voltage (MUTE, ACTIVE)

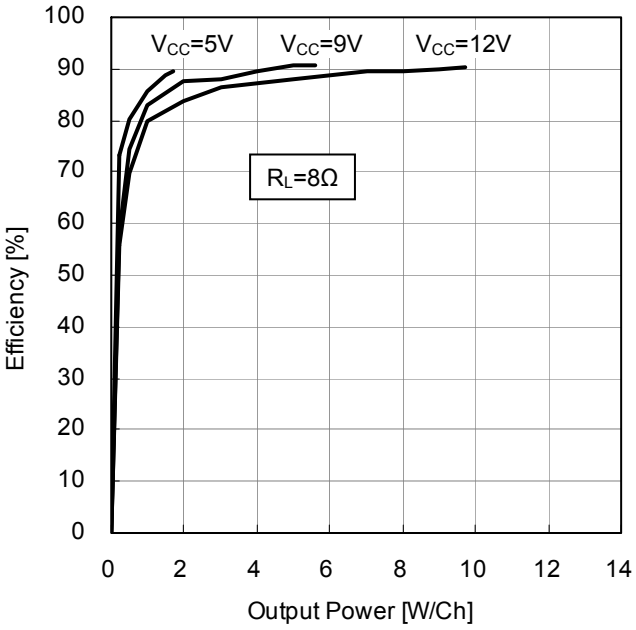


Figure 7. Efficiency vs Output Power (R_L=8Ω)

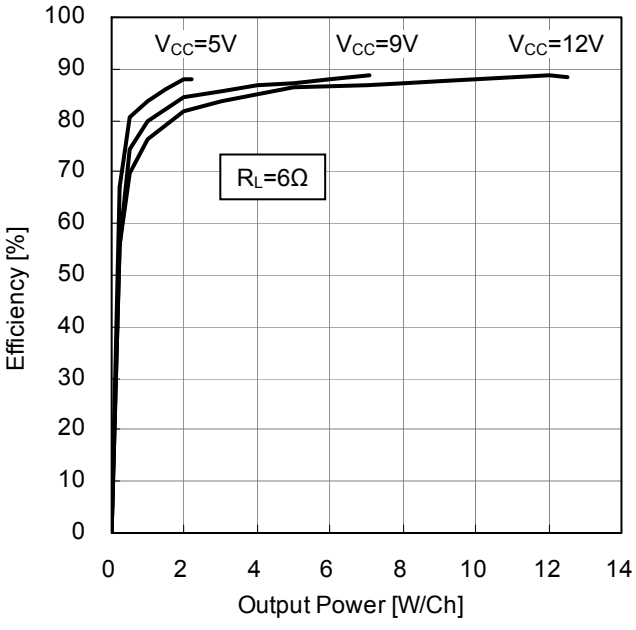


Figure 8. Efficiency vs Output Power (R_L=6Ω)

Typical Performance Curves

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, R_L=8Ω, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

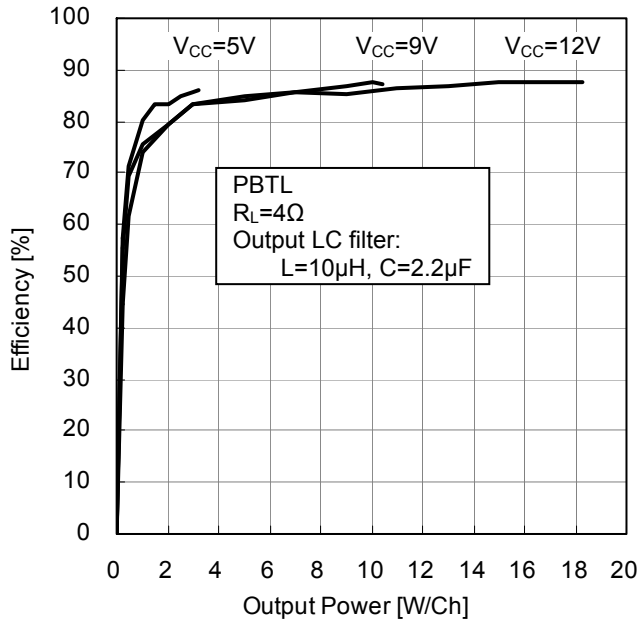


Figure 9. Efficiency vs Output Power
(PBTL, R_L=4Ω)

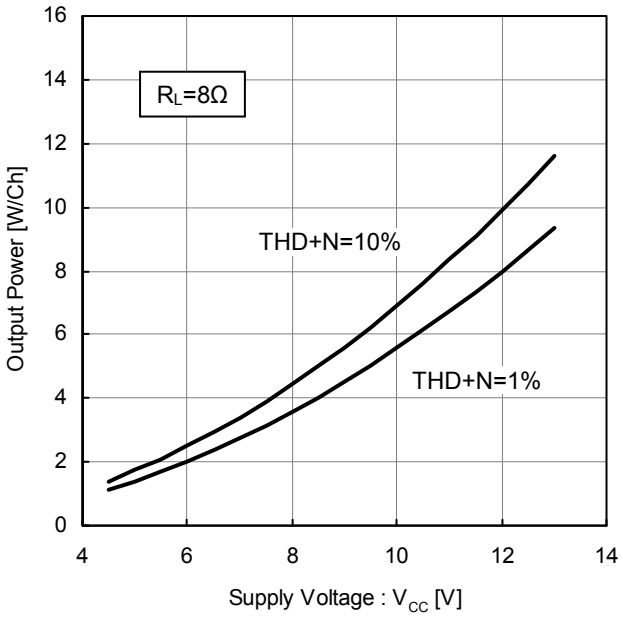


Figure 10. Output Power vs Supply Voltage
(R_L=8Ω)

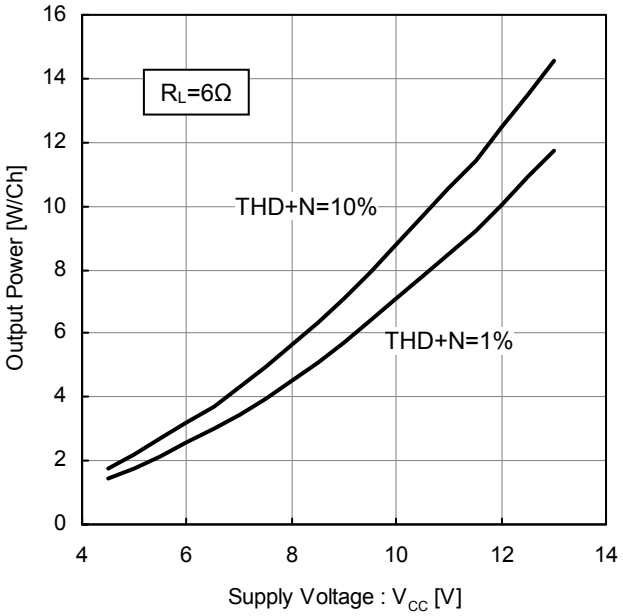


Figure 11. Output Power vs Supply Voltage
(R_L=6Ω)

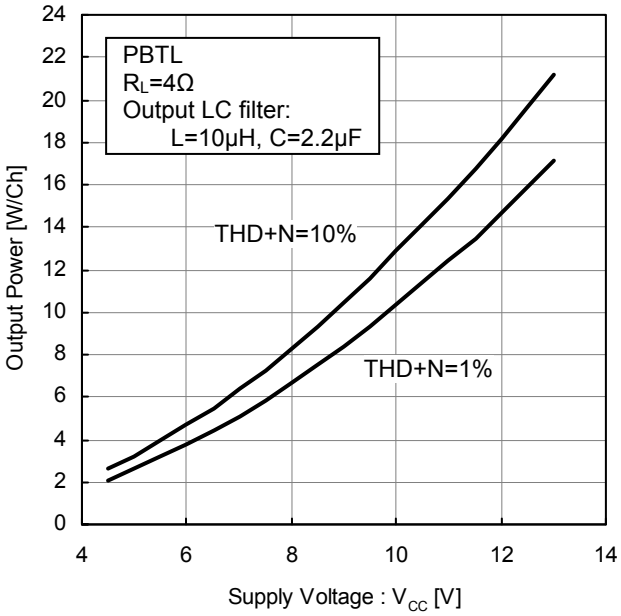


Figure 12. Output Power vs Supply Voltage
(PBTL, R_L=4Ω)

Typical Performance Curves

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, R_L=8Ω, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

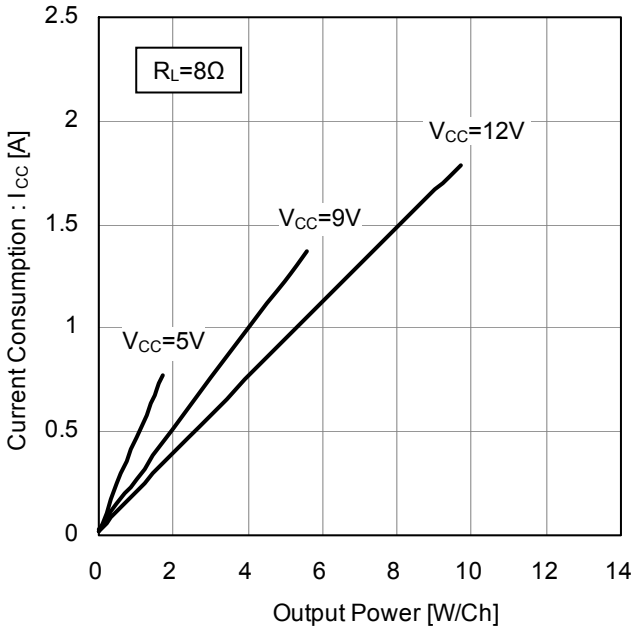


Figure 13. Circuit Current vs Output Power (R_L=8Ω)

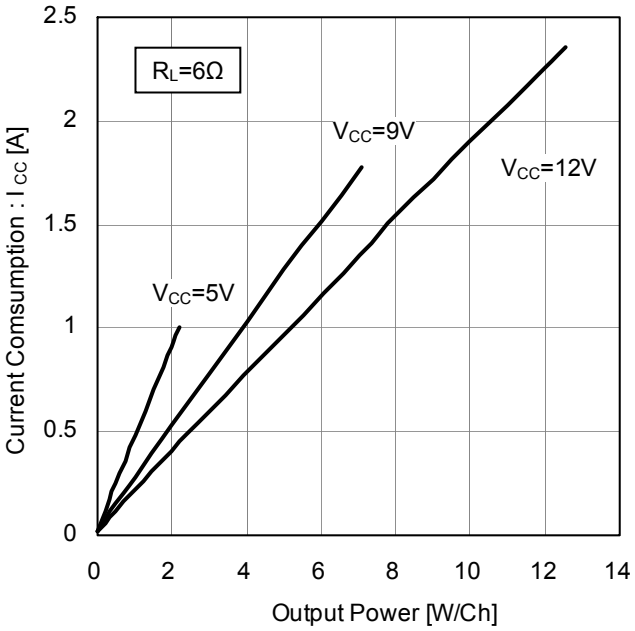


Figure 14. Circuit Current vs Output Power (R_L=6Ω)

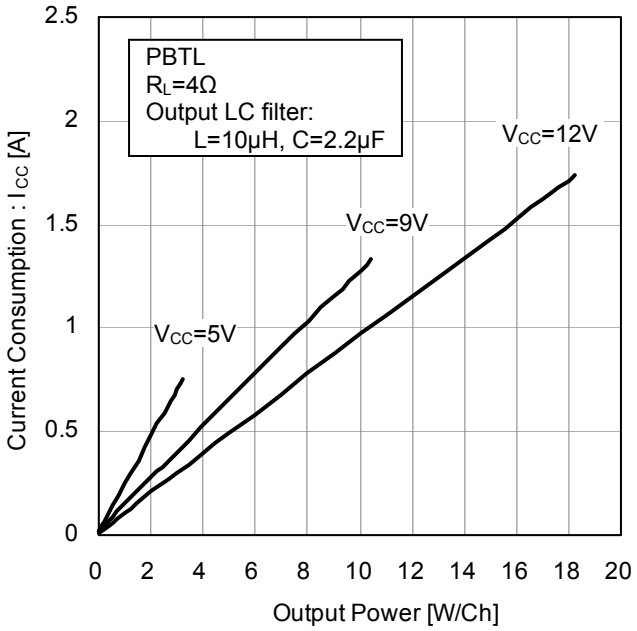


Figure 15. Circuit Current vs Output Power (PBTL, R_L=4Ω)

Typical Performance Curves

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, R_L=8Ω, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

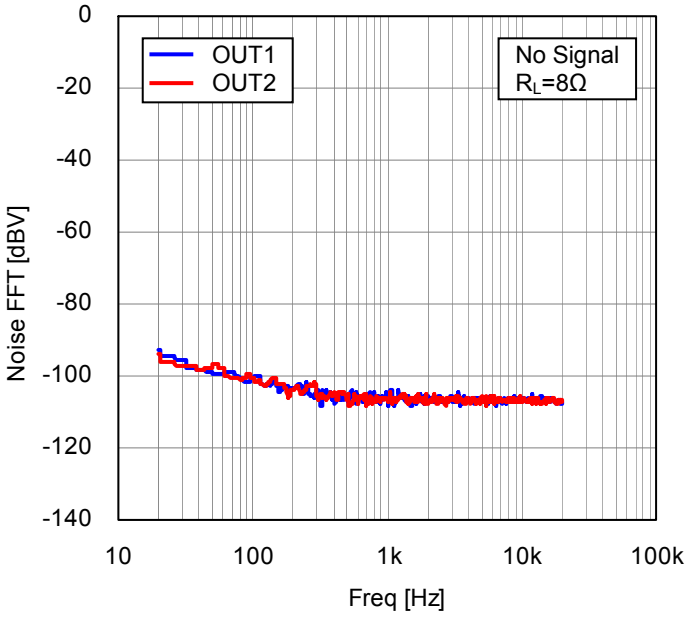


Figure 16. FFT of Output Noise Voltage
(R_L=8Ω)

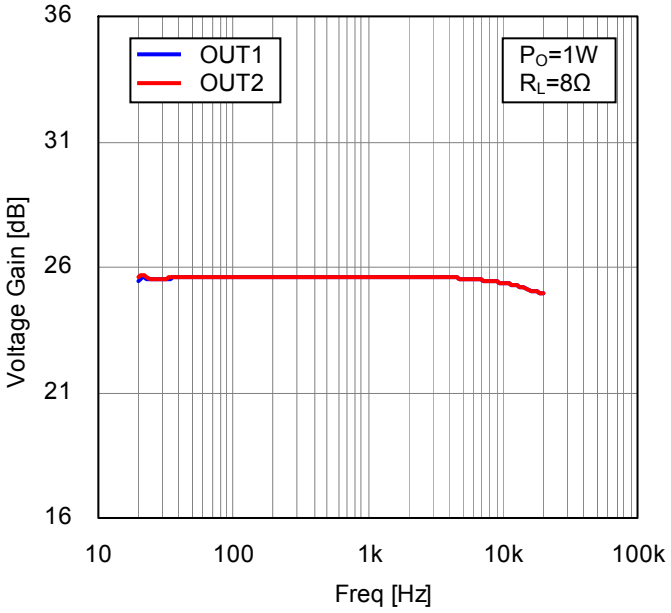


Figure 17. Voltage Gain vs Freq.
(R_L=8Ω)

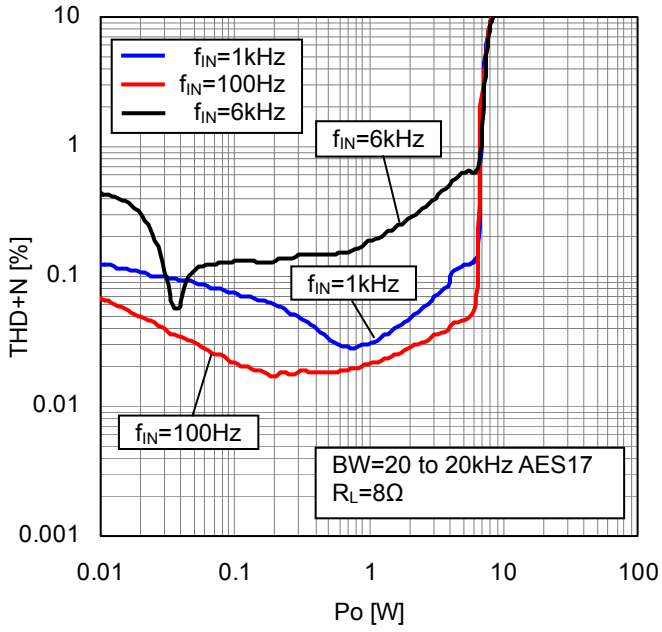


Figure 18. THD+N vs Output Power
(R_L=8Ω)

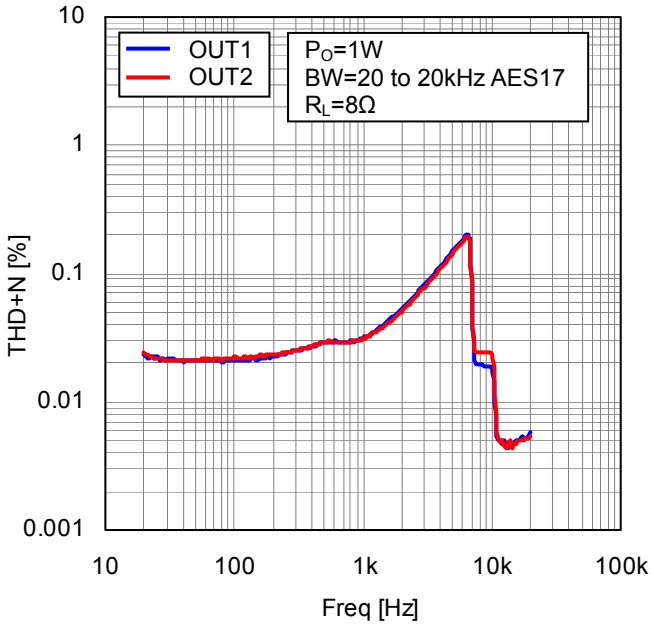


Figure 19. THD+N vs Freq.
(R_L=8Ω)

Typical Performance Curves

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, R_L=8Ω, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

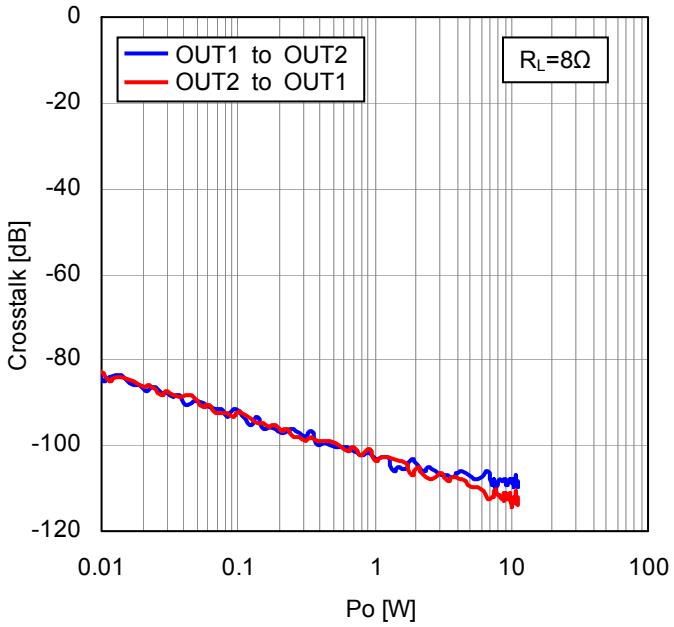


Figure 20. Crosstalk vs Output Power
(R_L=8Ω)

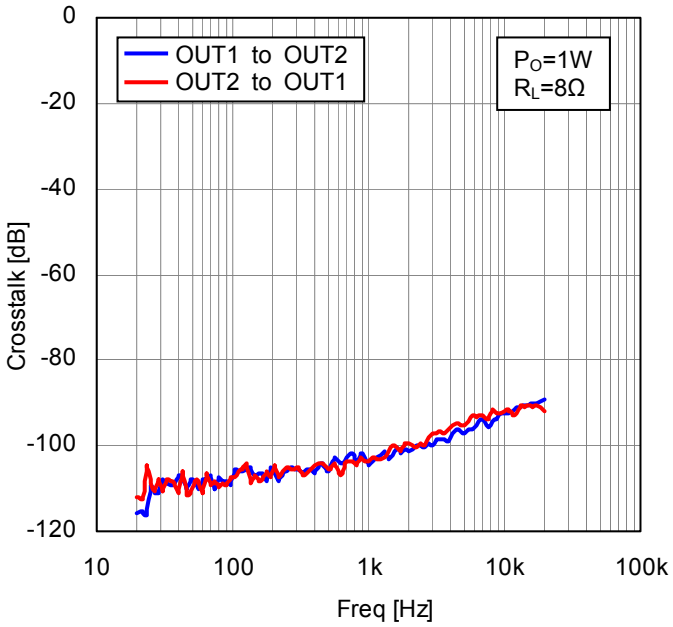


Figure 21. Crosstalk vs Freq.
(R_L=8Ω)

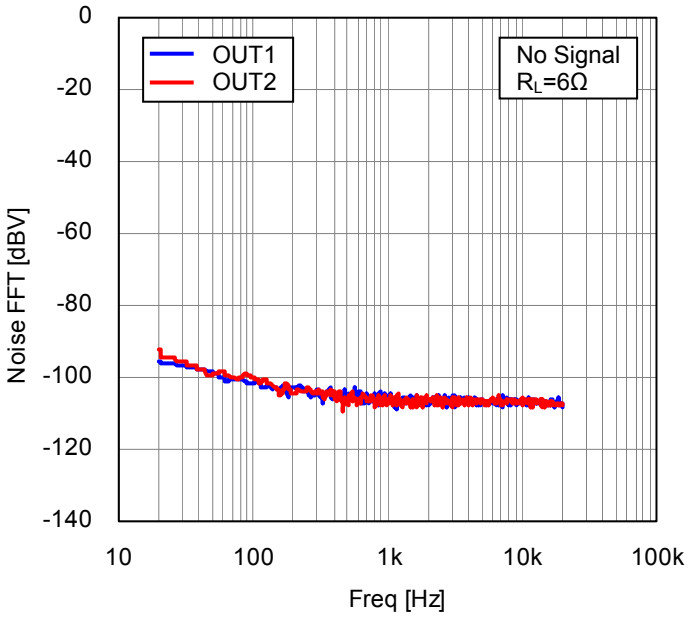


Figure 22. FFT of Output Noise Voltage
(R_L=6Ω)

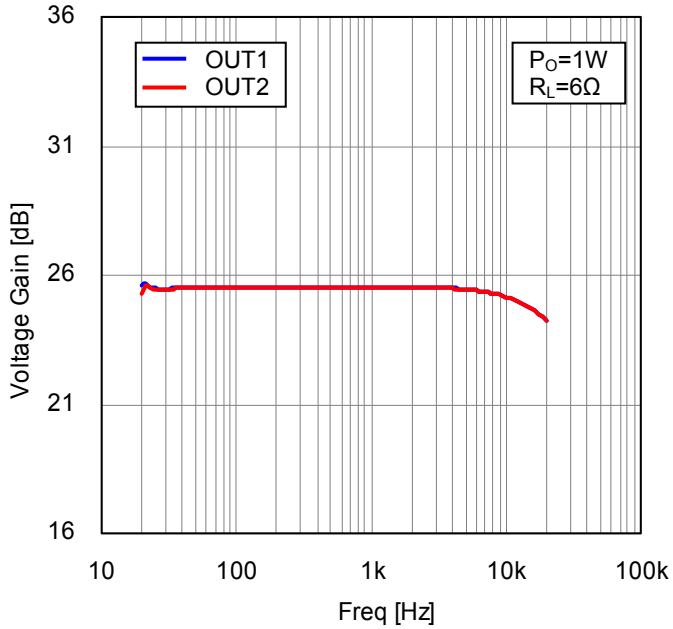


Figure 23. Voltage Gain vs Freq.
(R_L=6Ω)

Typical Performance Curves

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, R_L=8Ω, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

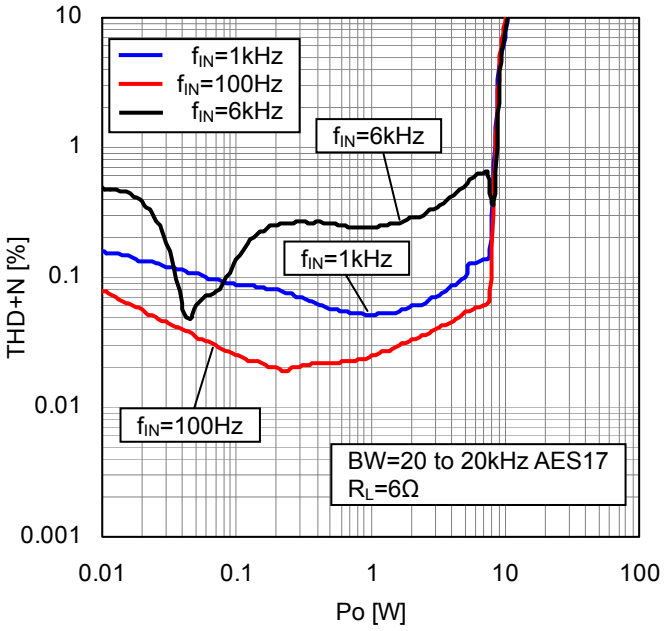


Figure 24. THD+N vs Output Power
(R_L=6Ω)

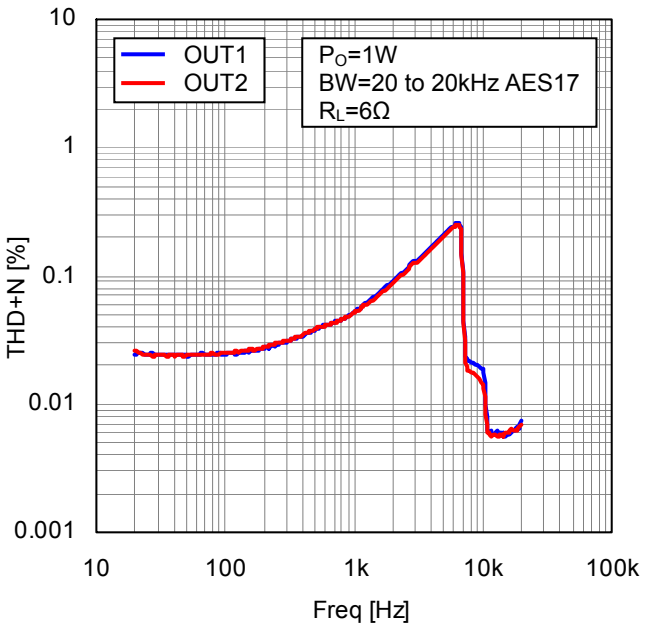


Figure 25. THD+N vs Freq.
(R_L=6Ω)

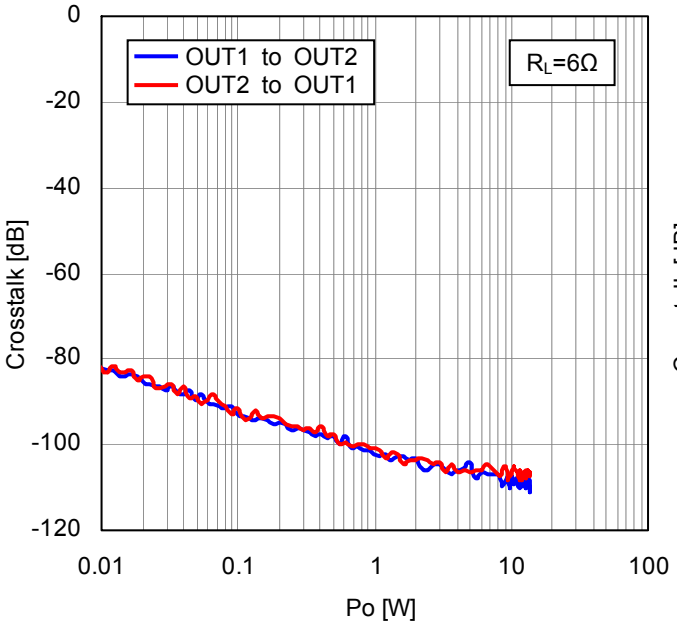


Figure 26. Crosstalk vs Output Power
(R_L=6Ω)

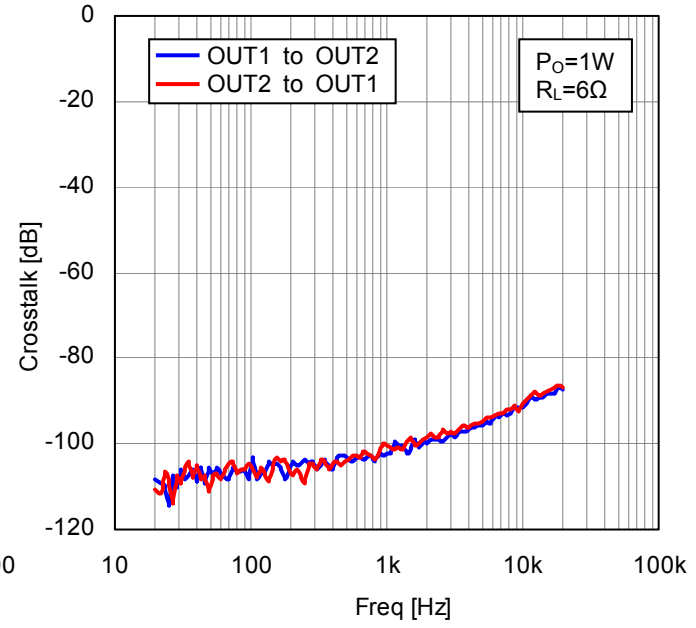


Figure 27. Crosstalk vs Freq.
(R_L=6Ω)

Typical Performance Curves

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, R_L=8Ω, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

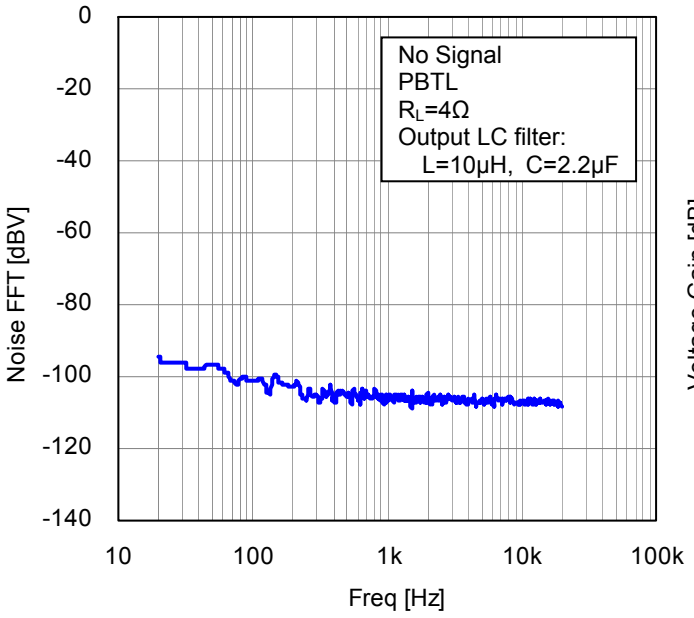


Figure 28. FFT of Output Noise Voltage
(PBTL, R_L=4Ω)

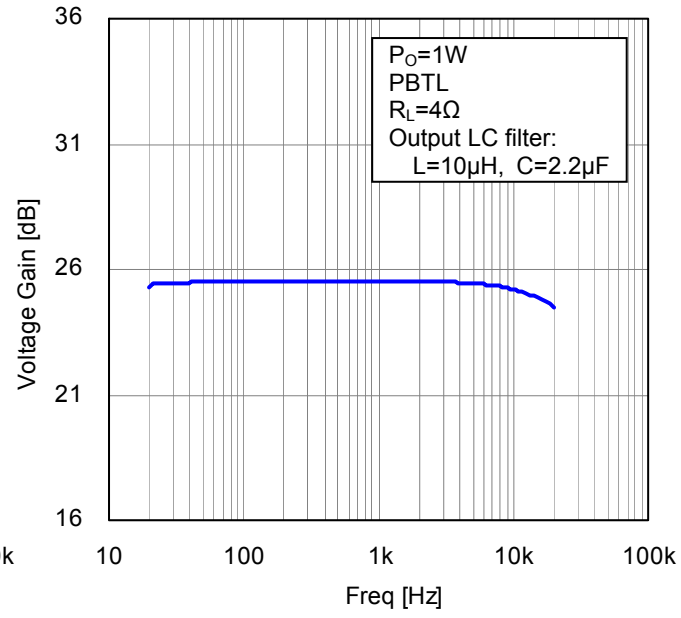


Figure 29. Voltage Gain vs Freq.
(PBTL, R_L=4Ω)

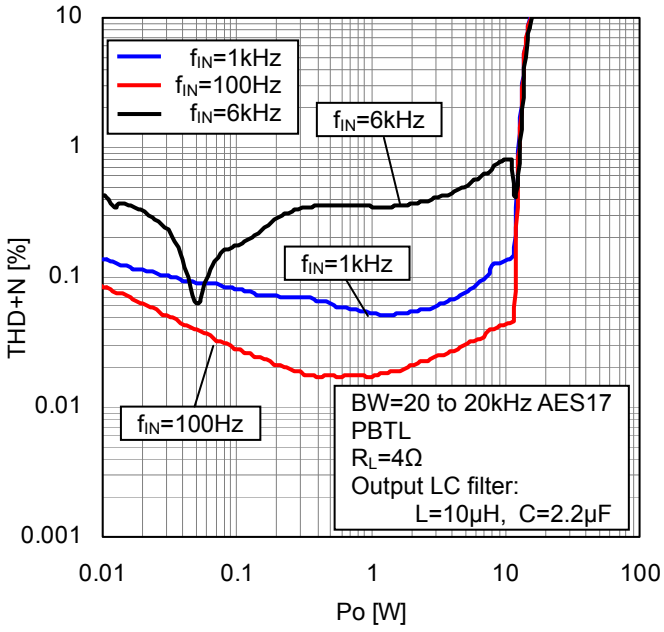


Figure 30. THD+N vs Output Power
(PBTL, R_L=4Ω)

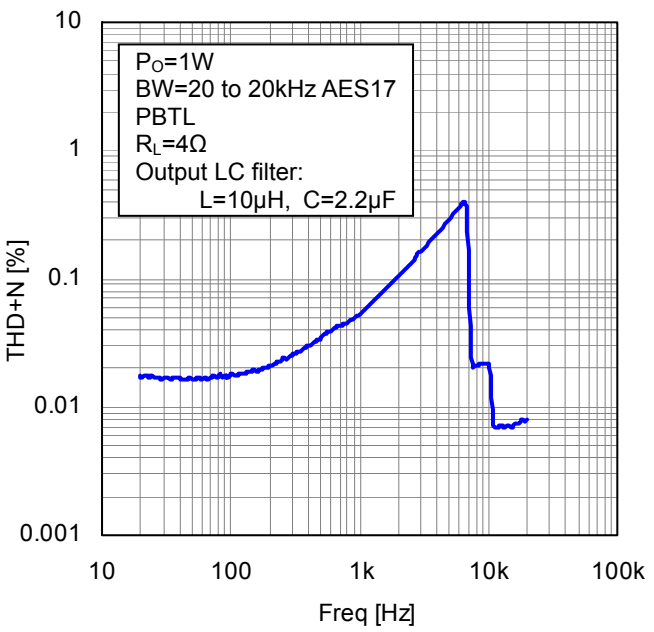


Figure 31. THD+N vs Freq.
(PBTL, R_L=4Ω)

Typical Performance Curves

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, R_L=8Ω, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

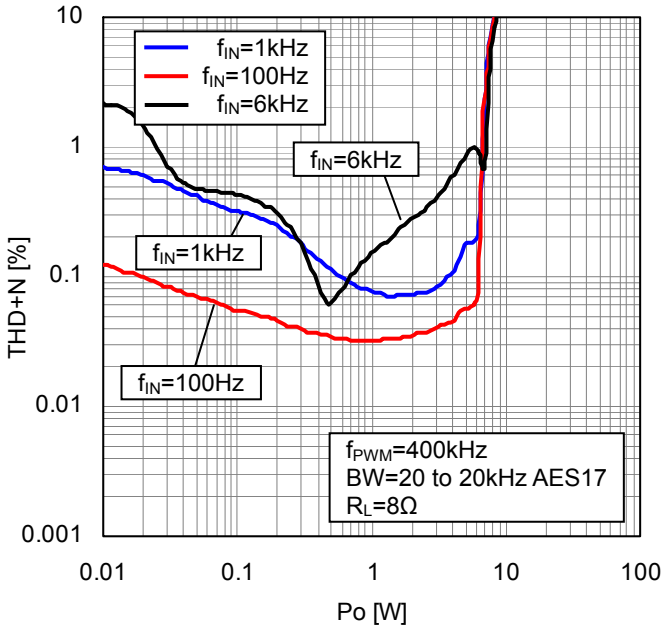


Figure 32. THD+N vs Output Power
(f_{PWM}=400kHz, R_L=8Ω)

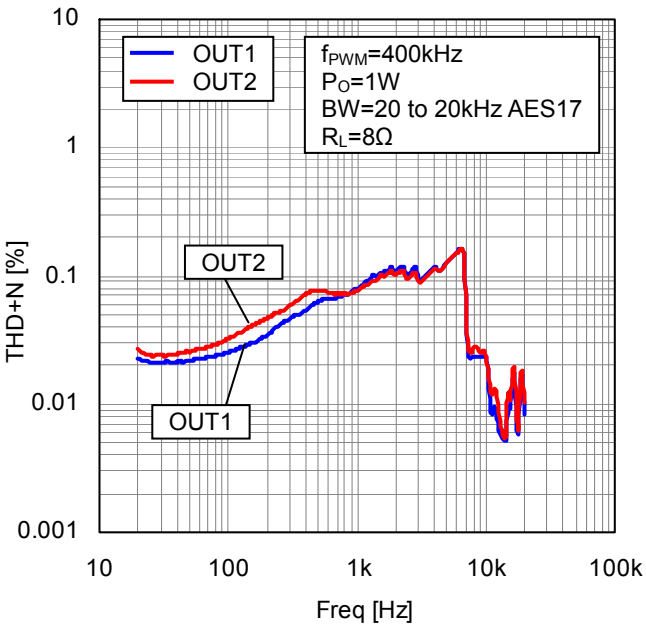


Figure 33. THD+N vs Freq.
(f_{PWM}=400kHz, R_L=8Ω)

Power up / down sequence

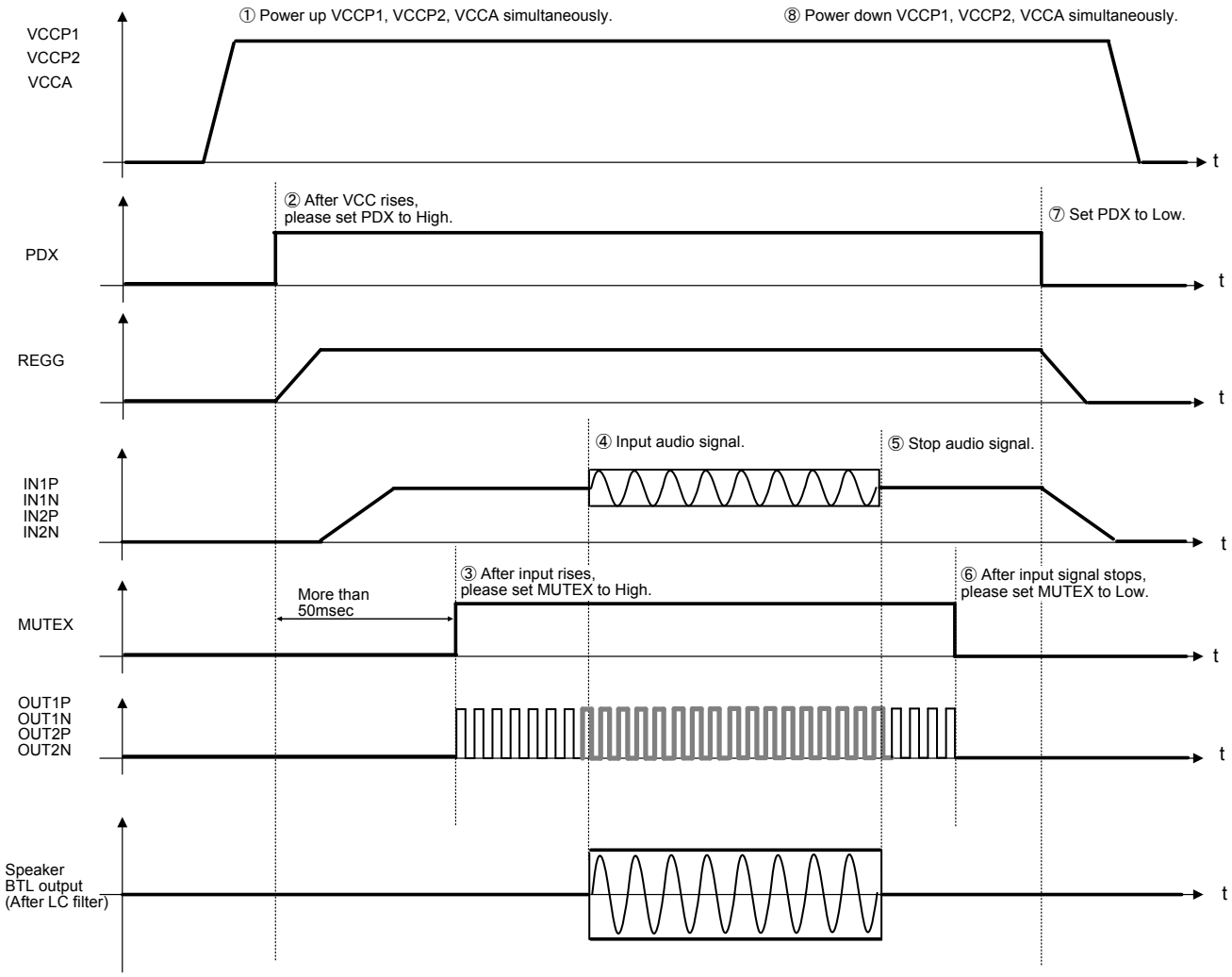


Figure 34. Power Up / Down Sequence

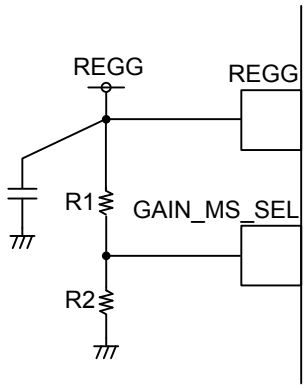
Function Description

(1) Power down and Mute setting

PDX	MUTEX	Normal		ERROR Detection	
		PWM output OUT1P, 1N, 2P, 2N	ERROR(Note 10)	PWM output OUT1P, 1N, 2P, 2N	ERROR(Note 10)
L	L/H	High-Z_Low(Note 9) (Power down)	H	High-Z_Low(Note 9) (Power down)	H
H	L	High-Z_Low(Note 9) (MUTE_ON)	H	High-Z_Low(Note 9) (MUTE_ON)	L
H	H	Active (MUTE_OFF)	H	High-Z_Low(Note 9) (MUTE_ON)	L

(Note 9) All power transistors are OFF and output terminals are pulled down by 40kΩ (Typ).
(Note 10) ERROR pin is pulled up by 10kΩ resistor.

(2) Gain and Master/Slave setting
Master/slave and gain are set by GAIN_MS_SEL pin voltage.



R1(Note 11) (to REGG)	R2(Note 11) (to GND)	Master/Slave	Gain	Input Impedance
18kΩ	Open	Slave	36dB	30kΩ
18kΩ	68kΩ	Slave	32dB	45.1kΩ
33kΩ	68kΩ	Slave	26dB	79.3kΩ
51kΩ	68kΩ	Slave	20dB	127.9kΩ
68kΩ	51kΩ	Master	36dB	30kΩ
68kΩ	33kΩ	Master	32dB	45.1kΩ
68kΩ	18kΩ	Master	26dB	79.3kΩ
open	18kΩ	Master	20dB	127.9kΩ

(Note 11) Please use 1% tolerance resistor.

Figure 35. GAIN_MS_SEL Pin Setting

Setting cannot be changed when IC is active, but it can be set by rebooting (PDX=H to L to H).

Master/Slave Function

This IC has master and slave mode, and it can be synchronized by PWM frequency between two ICs. In master mode, SYNC pin becomes output pin for synchronization and in slave mode it becomes input pin, so please connect each SYNC pins. Please set FSEL2/FSEL1/FSEL0 pins to be same each other.

(3) Parallel BTL Function
Parallel BTL mode can be set by connecting IN2P and IN2N pins to GND.
Please short OUT1P – OUT2P, OUT1N – OUT2N near the IC as much as possible.
Parallel BTL mode cannot be set by connecting IN1P and IN1N pins to GND.

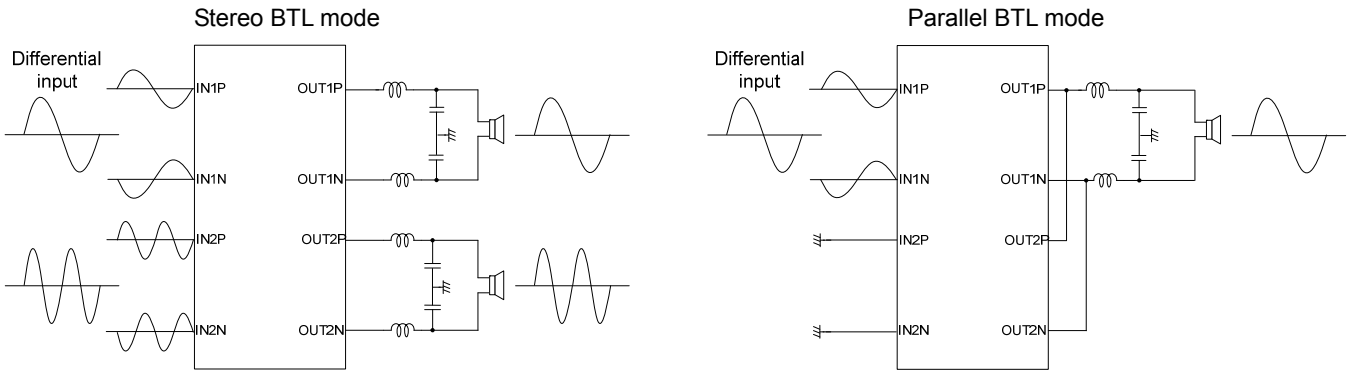


Figure 36. Parallel BTL mode

(4) Power Limit Function
It is possible to limit the maximum output voltage by PLIMIT pin.

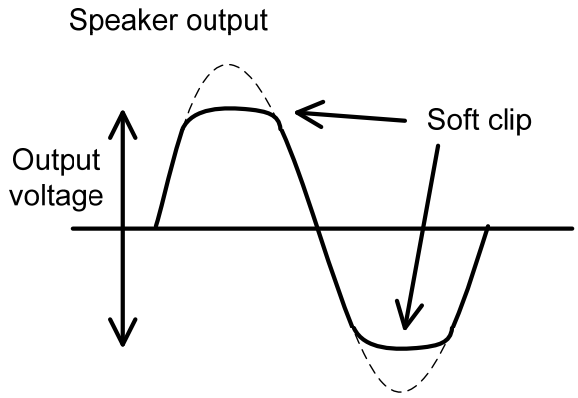


Figure 37. Power Limit

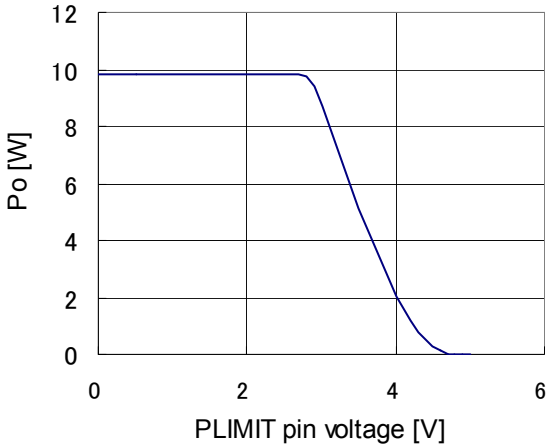


Figure 38. Power Limit Function [V_{CC}=12V, R_L=8Ω] (Typ)

Ex.) If PLIMIT is set by R3A=12kΩ and R3B=20kΩ in “Application Information”, output power is limited to about 6.4W.

If power limit function is not needed, connect PLIMIT pin to GND.

(5) FSEL2 / FSEL1 / FSEL0 (AM avoidance function)

FSEL2 / FSEL1 / FSEL0 pins are used for PWM frequency setting. PWM frequency is near to AM radio frequency band therefore this makes interference during AM radio is used, and may negatively affects reception of AM radio wave. This interference can be reduced by shift of PWM frequency. Below are the recommended settings. For example, receiving AM radio wave of 1269kHz in Asia / Europe please set PWM frequency to 500kHz.

AM frequency [kHz]		Recommended PWM frequency setting		
Americas	Asia / Europe	f_{PWM}=400kHz FSEL2=L FSEL1=H FSEL0=H	f_{PWM}=500kHz FSEL2=H FSEL1=L FSEL0=L	f_{PWM}=600kHz FSEL2=H FSEL1=L FSEL0=H
	522 – 540	○	-	○
540 – 917	540 – 914	-	○	-
917 – 1125	914 – 1122	○	-	○
1125 – 1375	1122 – 1373	-	○	-
1375 – 1547	1373 – 1548	○	-	○
1547 – 1700	1548 – 1701	○	-	○

Do not set following conditions:
FSEL2=FSEL1=FSEL0=H
FSEL2=H, FSEL1=H, FSEL0=L
FSEL2=L, FSEL1=H, FSEL0=L
FSEL2=L, FSEL1=L, FSEL0=H
FSEL2=FSEL1=FSEL0=L

Application Information

(1) Application Circuit Example 1 (Stereo BTL, V_{CC}=4.5 to 11V)
Overshoot of output PWM differs according to the board, and etc. Please check to ensure that it is lower than absolute maximum ratings. If it exceeds the absolute maximum ratings, snubber circuit need to be added, the circuit example is shown on the next page.

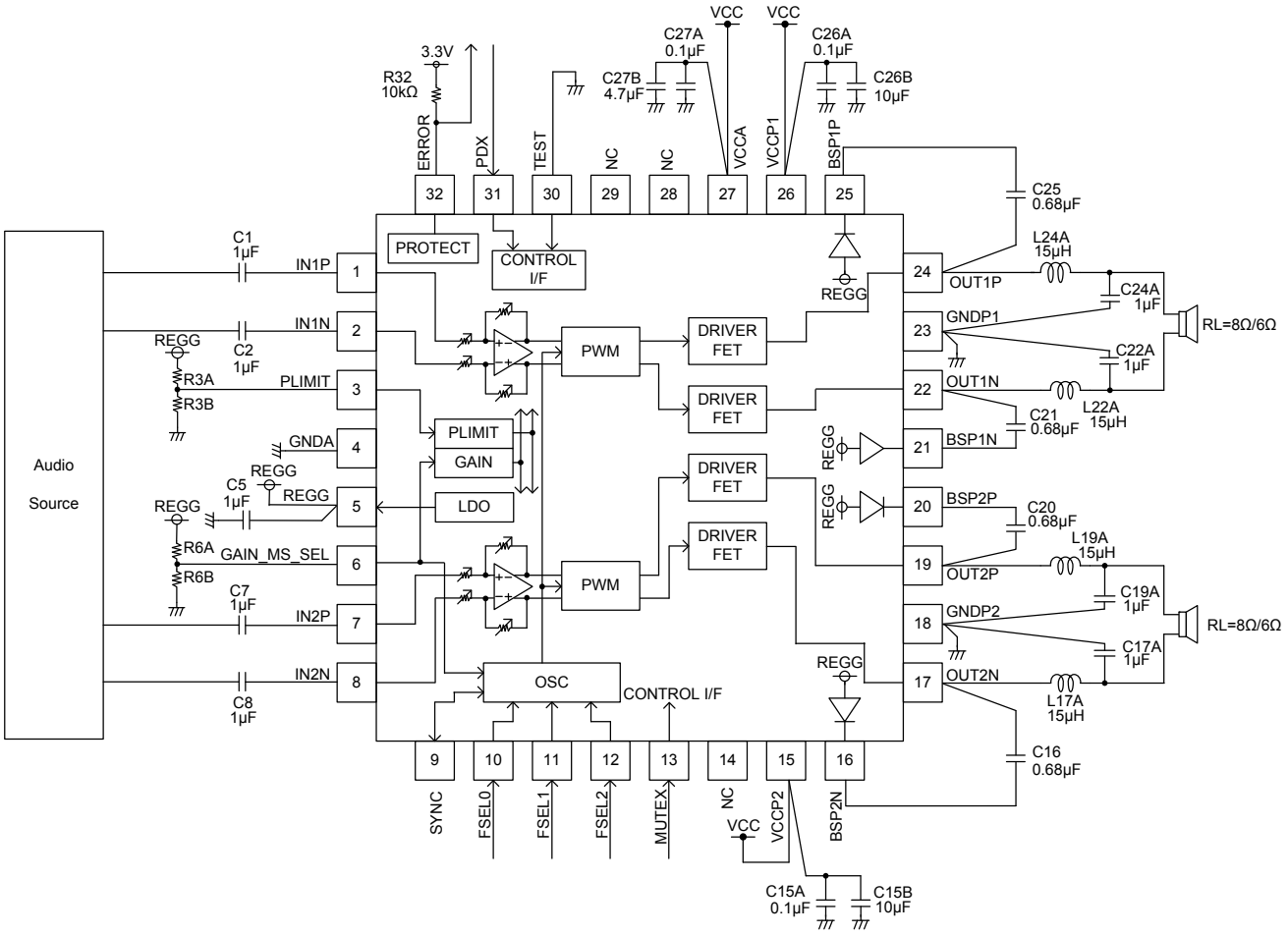


Figure 39. Application Circuit 1

BOM 1 (Stereo BTL, V_{CC}=4.5 to 11V)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description (4)Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description (2)Gain and Master/Slave setting
	1	R6B	
	1	R32	100kΩ, 1/16W, J(±5%)
Capacitor	4	C1, C2, C7, C8	1µF, 16V, B(±10%)
	1	C5(Note 12)	1µF, 16V, B(±10%)
	3	C15A, C26A, C27A(Note 12)	0.1µF, 25V, B(±10%)
	2	C15B, C26B(Note 12)	10µF, 25V, B(±10%)
	4	C16, C20, C21, C25(Note 12)	0.68µF, 16V, B(±10%)
	4	C17A, C19A, C22A, C24A	1µF, 25V, B(±10%)
	1	C27B(Note 12)	4.7µF, 25V, B(±10%)
Inductor	4	L17A, L19A, L22A, L24A	15µH, 2.1A, ±20%

(Note 12) Please place it near pin as much as possible.

(2) Application Circuit Example 2 (Stereo BTL, V_{CC}=11 to 13V)
Please add the snubber circuit at OUT pin when V_{CC}=11 to 13V.

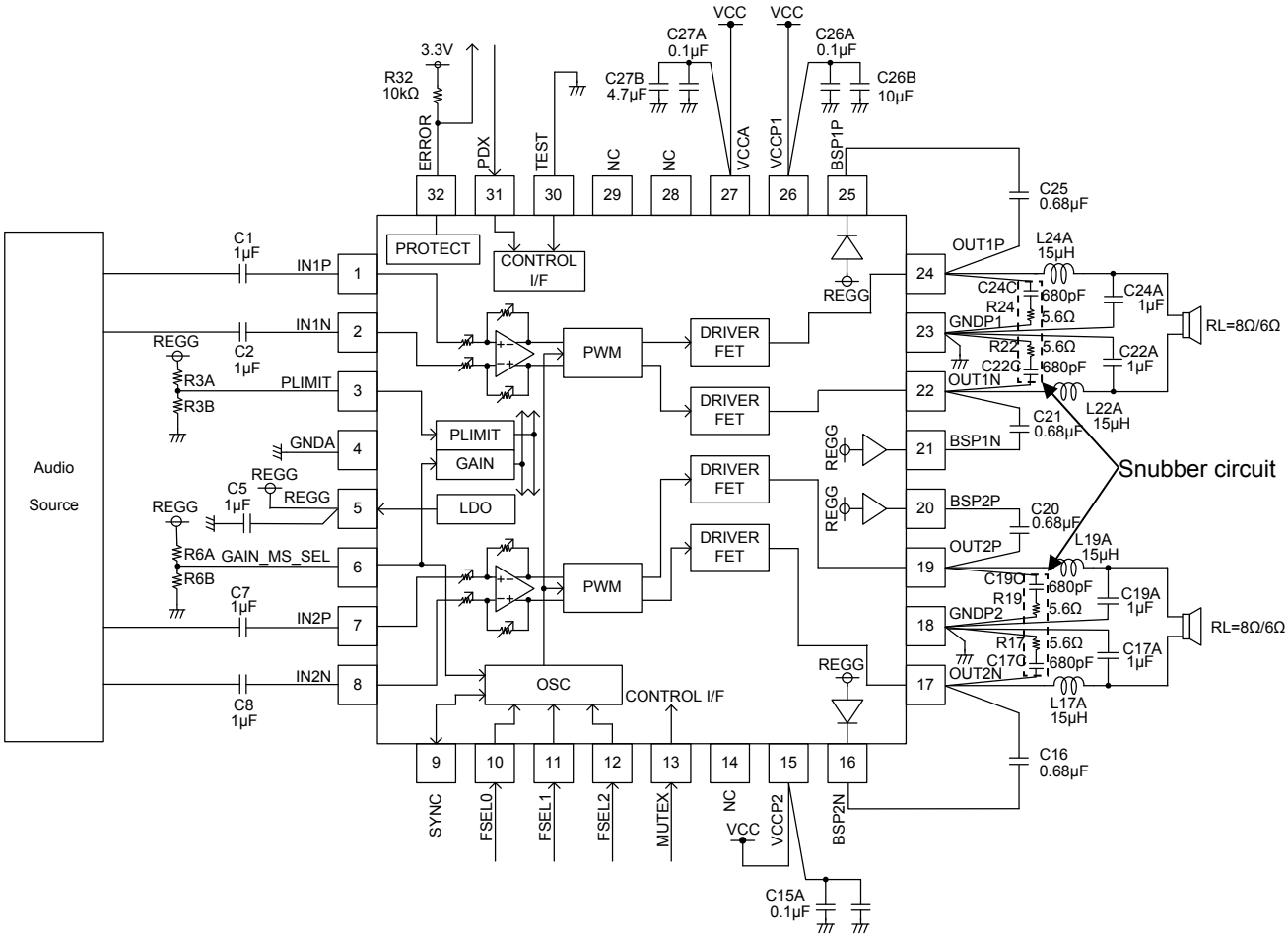


Figure 40. Application Circuit 2

BOM 2 (Stereo BTL, V_{CC}=11to 13V)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description (4)Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description (2)Gain and Master/Slave setting
	1	R6B	
	1	R32	100kΩ, 1/16W, J(±5%)
	4	R17, R19, R22, R24	5.6Ω, 1/10W, J(±5%)
Capacitor	4	C1, C2, C7, C8	1µF, 16V, B(±10%)
	1	C5(Note 13)	1µF, 16V, B(±10%)
	3	C15A, C26A, C27A(Note 13)	0.1µF, 25V, B(±10%)
	2	C15B, C26B(Note 13)	10µF, 25V, B(±10%)
	4	C16, C20, C21, C25(Note 13)	0.68µF, 16V, B(±10%)
	4	C17A, C19A, C22A, C24A	1µF, 25V, B(±10%)
	4	C17C, C19C, C22C, C24C(Note 13)	680pF, 25V, B(±10%)
	1	C27B(Note 13)	4.7µF, 25V, B(±10%)
Inductor	4	L17A, L19A, L22A, L24A	15µH, 2.1A, ±20%

(Note 13) Please place it near pin as much as possible.

(3) Application Circuit Example 3 (Monaural PBTL, V_{CC}=4.5 to 11V)
Overshoot of output PWM differs according to the board, and etc. Please check to ensure that it is lower than absolute maximum ratings. If it exceeds the absolute maximum ratings, snubber circuit need to be added, the circuit example is shown on the next page.

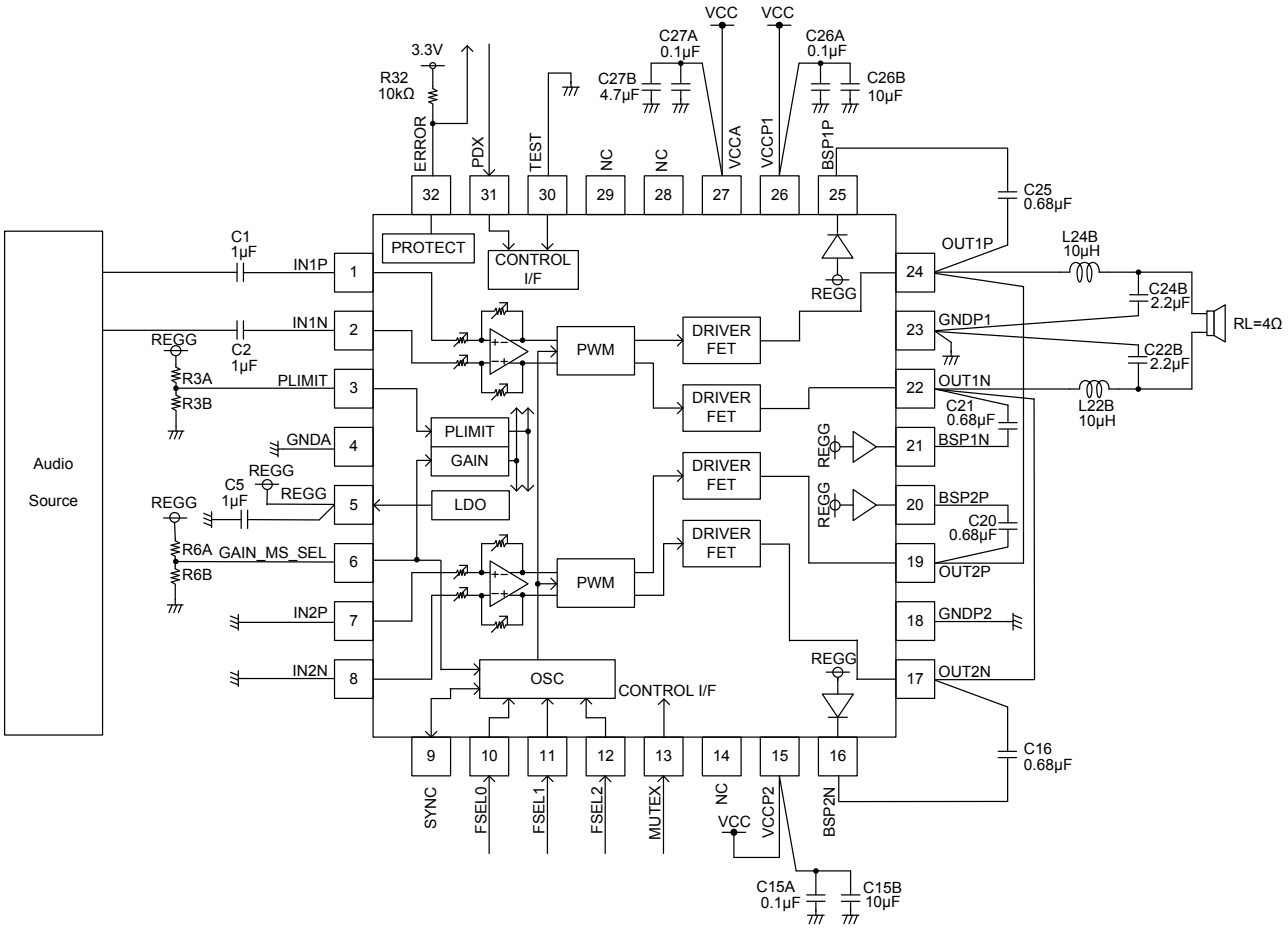


Figure 41. Application Circuit 3

BOM 3 (Monaural PBTL, V_{CC}=4.5 to 11V)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description (4)Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description (2)Gain and Master/Slave setting
	1	R6B	
	1	R32	100kΩ, 1/16W, J(±5%)
Capacitor	4	C1, C2, C7, C8	1µF, 16V, B(±10%)
	1	C5(Note 14)	1µF, 16V, B(±10%)
	3	C15A, C26A, C27A(Note 14)	0.1µF, 25V, B(±10%)
	2	C15B, C26B(Note 14)	10µF, 25V, B(±10%)
	4	C16, C20, C21, C25	0.68µF, 16V, B(±10%)
	2	C22B, C24B(Note 14)	2.2µF, 25V, B(±10%)
	1	C27B	4.7µF, 25V, B(±10%)
Inductor	2	L22B, L24B	10µH, 2.6A, ±20%

(Note 14) Please place it near pin as much as possible.

(4) Application Circuit Example 4 (Monaural PBTL, V_{CC}=11 to 13V)
Please add the snubber circuit at OUT pin when V_{CC}=11 to 13V.

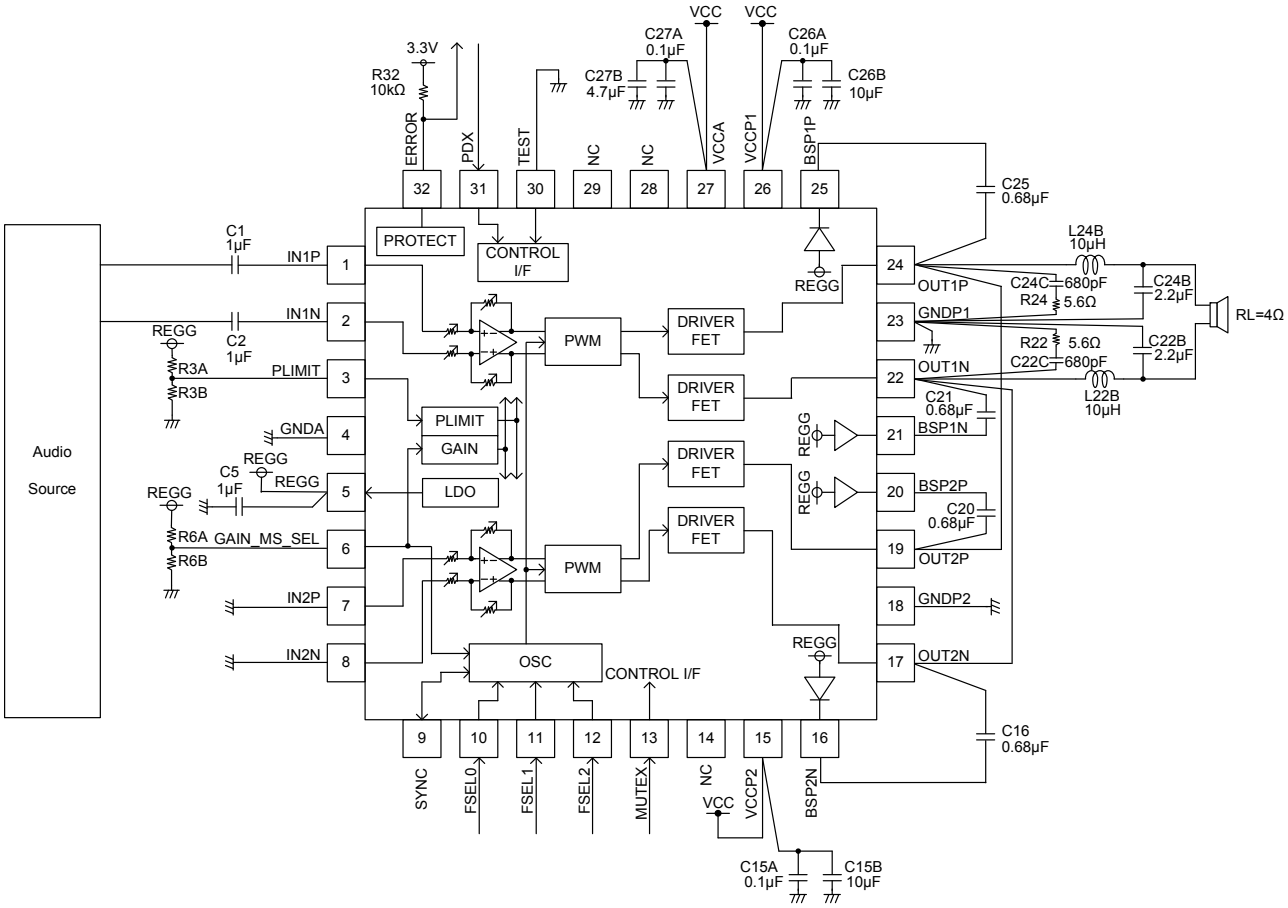


Figure 42. Application Circuit 4

BOM 4 (Monaural PBTL, V_{CC}=11 to 13V)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description (4)Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description (2)Gain and Master/Slave setting
	1	R6B	
	1	R32	100kΩ, 1/16W, J(±5%)
	2	R22, R24 (Note 15)	5.6Ω, 1/10W, J(±5%)
Capacitor	4	C1, C2, C7, C8	1µF, 16V, B(±10%)
	1	C5 (Note 15)	1µF, 16V, B(±10%)
	3	C15A, C26A, C27A (Note 15)	0.1µF, 25V, B(±10%)
	2	C15B, C26B (Note 15)	10µF, 25V, B(±10%)
	4	C16, C20, C21, C25 (Note 15)	0.68µF, 16V, B(±10%)
	2	C22B, C24B	2.2µF, 25V, B(±10%)
	2	C22C, C24C (Note 15)	680pF, 25V, B(±10%)
	1	C27B (Note 15)	4.7µF, 25V, B(±10%)
Inductor	2	L22B, L24B	10µH, 2.6A, ±20%

(Note 15) Please place it near pin as much as possible.

(5) Application Example 5 (MASTER/SLAVE mode, V_{CC}=4.5 to 11V)

This GAIN_MS_SEL setting is one example, so another Gain setting can be used.

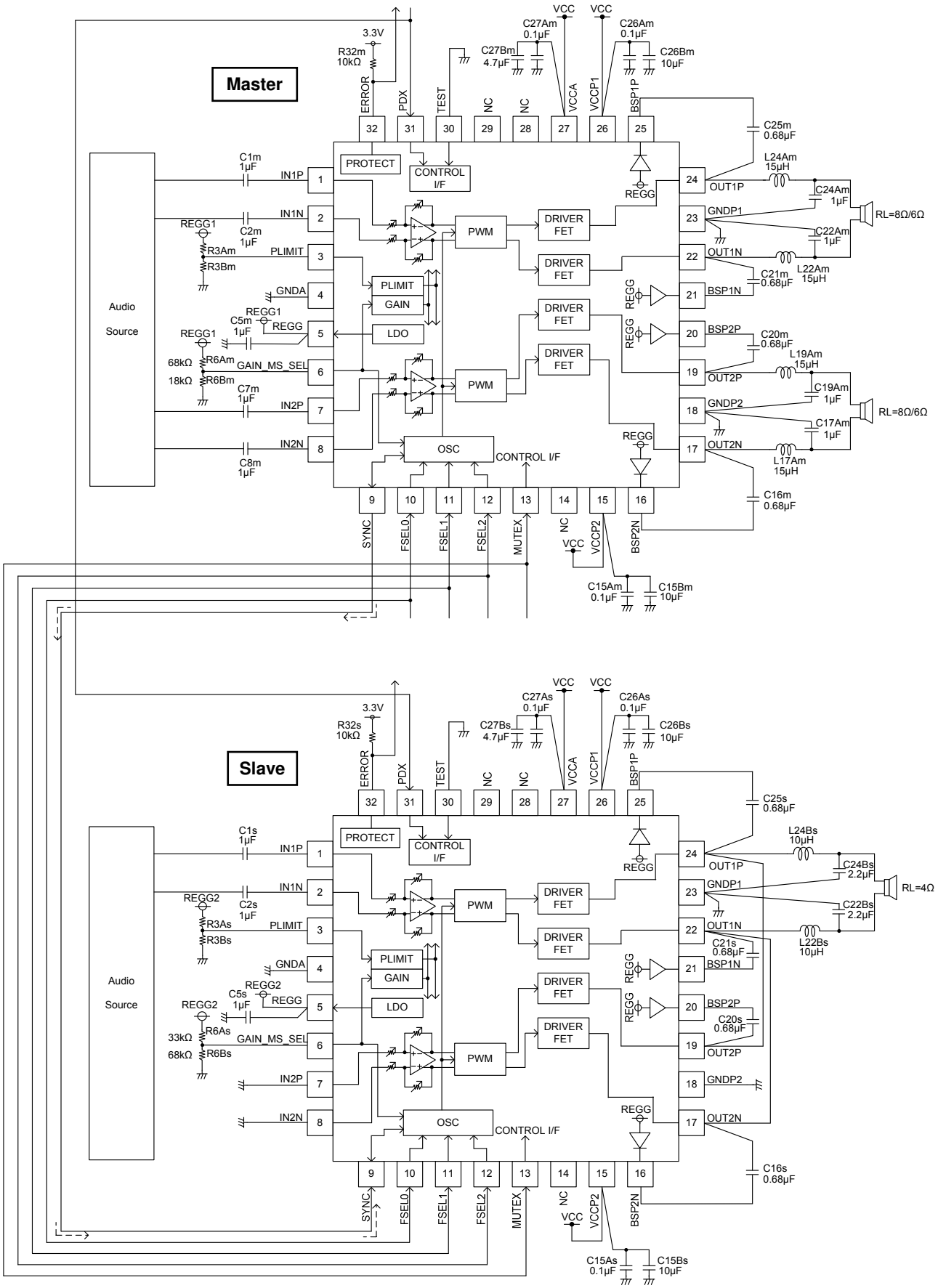


Figure 43. Application Circuit 5

About the Protection Function

Protection Function	Detecting & Releasing Condition		PWM Output OUT1P, 1N, 2P, 2N	ERROR(Note 16)
Output short protection	Detecting condition	Detecting current = 8A (Typ)	High-Z_Low (Latch)(Note17)	L (Latch) (Note17)
DC voltage protection	Detecting condition	DC voltage is over 3.5V for a period of 0.33sec to 0.66sec at speaker output	High-Z_Low (Latch) (Note17)	L (Latch) (Note17)
Overheat protection	Detecting condition	Chip temperature to be over 150°C (Typ)	High-Z_Low	L
	Releasing condition	Chip temperature to be below 120°C (Typ)	Normal operation	
Under voltage protection	Detecting condition	Power supply voltage to be below 4.0V (Typ)	High-Z_Low	H
	Releasing condition	Power supply voltage to be above 4.1V (Typ)	Normal operation	

(Note 16) ERROR pin is pulled up by 10kΩ resistor.
(Note 17) Once an IC is latched, the circuit is not released automatically even after an abnormal status is gone.
The following procedures ① or ② is available for recovery.
① After turning MUTEX terminal to Low (holding time to Low = 10msec (Min)) turn back to High again.
② Restore power supply after dropping to power supply voltage V_{CC} < 3V (10msec (Min) holding) which internal power on reset circuit activates.