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Low Power Consumption Class D Amplifier

9W+9W Analog Input Class D Speaker Amplifier

BD28412MUV

General Description

BD28412MUV is a 9W+9W stereo (or 18W monaural) class D amplifier, developed for battery equipped speaker systems such as wireless speakers. This IC is incorporated with a precise oscillator to generate multiple switching frequencies that can avoid the AM radio interference. In addition, 2.1Ch audio system can be realized by master and slave operation without beat noise caused by interference between two ICs. Furthermore, this IC achieves lower power consumption that eliminates the need for an external heat sink.

Features

- Analog Differential Input
- Low Standby Current
- Output Feedback Circuitry Prevents Sound Quality Degradation Caused by Power Supply Voltage Fluctuation, Achieves Low Noise and Low Distortion, Eliminates the Need of Large Electrolytic-Capacitors for Decoupling
- Power Limit Function (Linearly-programmable)
- Selectable Switching Frequency (AM Avoidance Function)
- Synchronization Control is Supported (Selectable Master and Slave Operation)
- Parallel BTL (PBTL) is Supported
- Wide Voltage Range (V_{CC}=4.5V to 13V)
- High Efficiency and Low-heat-generation Make the System Smaller, Thinner, and More Power-saving
- Pop Noise Prevention During Power Supply ON/OFF
- High Reliability Design by Built-in Protection Circuits
  - Overheat Protection
  - Under Voltage Protection
  - Output Short Protection
  - Output DC Voltage Protection
- Small Package (VQFN032V5050) Achieves Mount Area Reduction

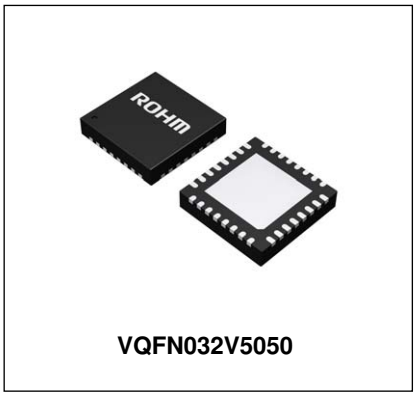
Applications

- Wireless Speakers, Small Active Speakers, Portable Audio Equipments, etc.

Key Specifications

- Supply Voltage Range: 4.5V to 13V
- Speaker Output Power: 9W+9W (Typ)
  (V_{CC}=12V, R_L=8Ω, PLIMIT=0V)
- Speaker Output Power(PBTL): 18W (Typ)
  (V_{CC}=12V, R_L=4Ω, PLIMIT=0V)
- Total Harmonic Distortion Ratio:
  0.03% (Typ) @Po=1W
  (V_{CC}=11V, R_L=8Ω, PLIMIT=0V)
- Crosstalk: 100dB (Typ)
- PSRR: 55dB (Typ)
- Output Noise Voltage: -80dBV (Typ)
- Standby Current: 0.1μA (Typ)
- Operating Current: 16mA (Typ)
  (No load or filter, No signal)
- Operating Temperature Range: -25°C to +85°C

Package	W(Typ) x D(Typ) x H(Max)
VQFN032V5050	5.00mm x 5.00mm x 1.00mm



Typical Application Circuit

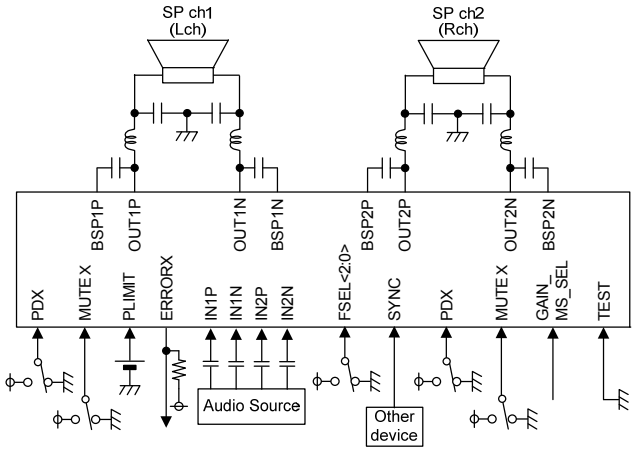


Figure 1. Typical Application Circuit

Pin Configuration

(TOP VIEW)

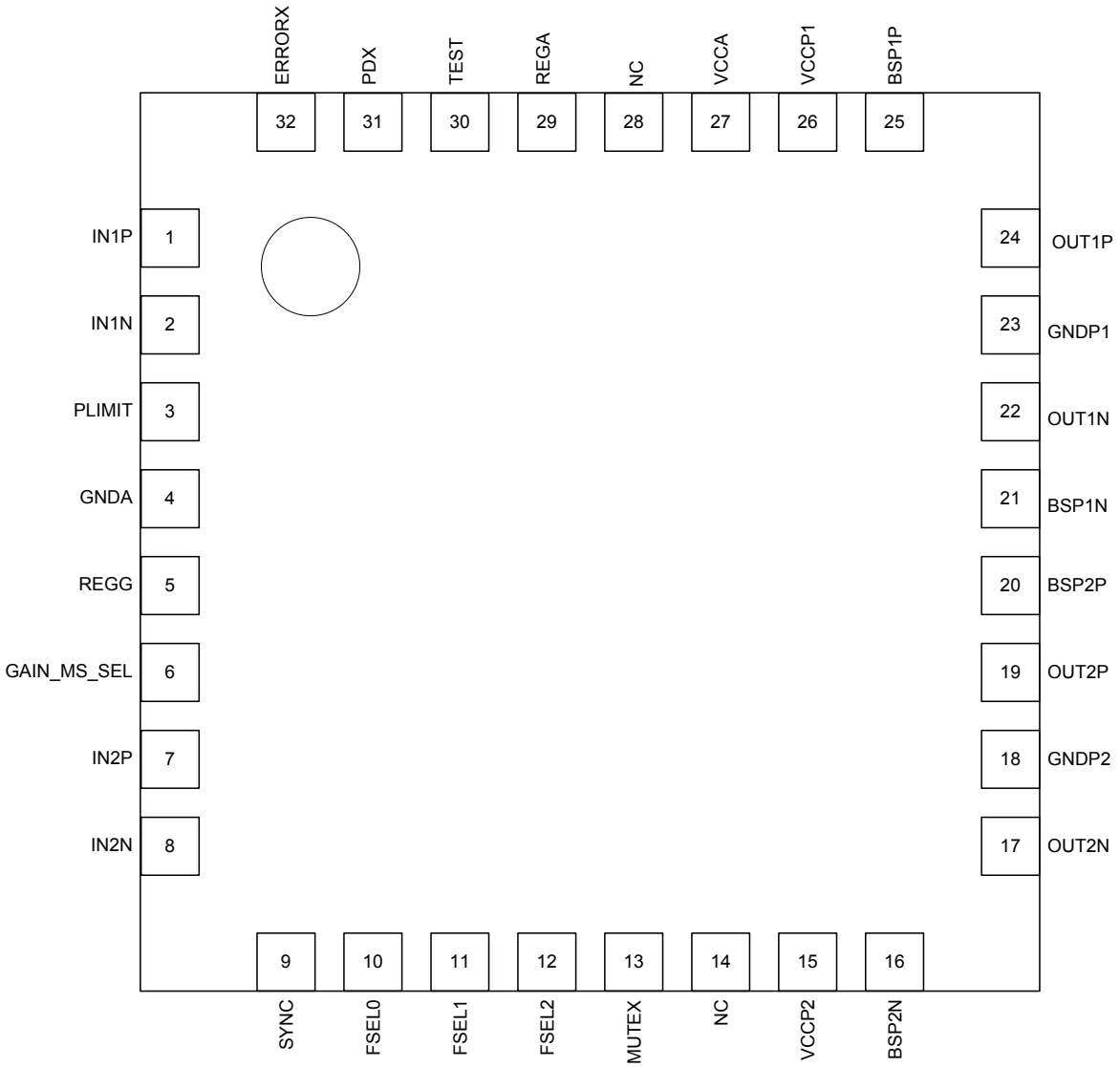
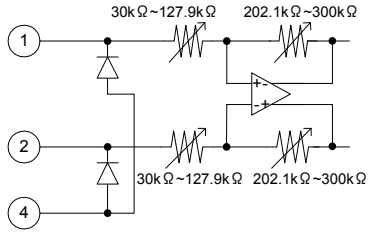
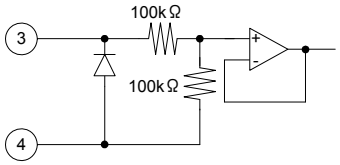
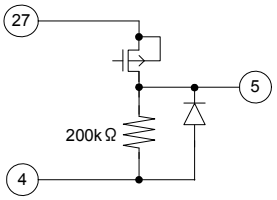
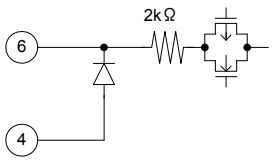
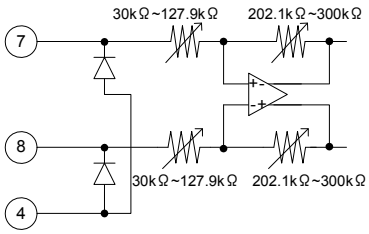
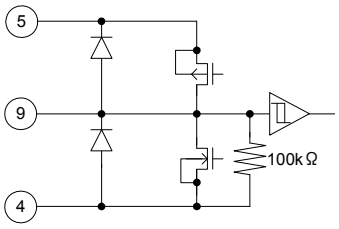
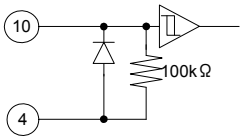
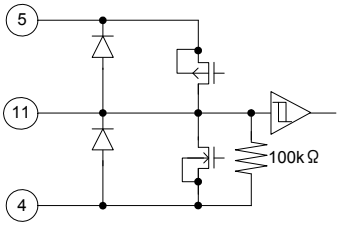
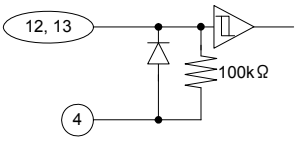
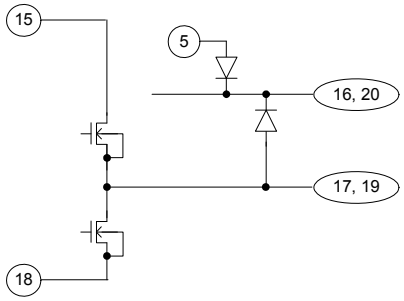
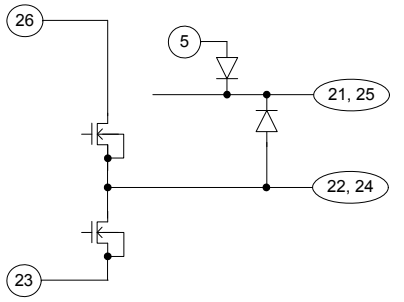
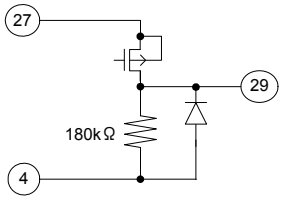
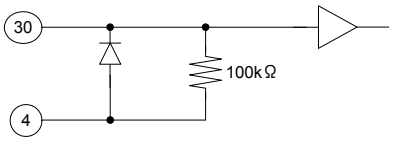


Figure 2. Pin Configuration

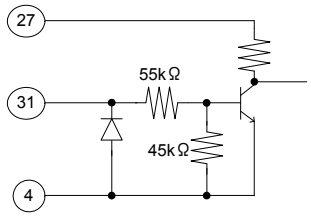
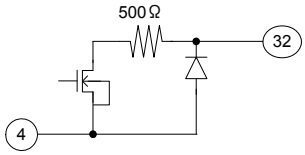
Pin Description

Pin No.	Pin Name	IO	Function	Internal Equivalent Circuit
1	IN1P	I	Positive input pin for Ch1	
2	IN1N	I	Negative input pin for Ch1	
3	PLIMIT	I	Power limit level setting pin	
4	GNDA	-	GND pin for Analog signal	
5	REGG	O	Internal power supply pin for Gate driver Please connect a capacitor. The REGG terminal of BD28412MUV should not be used as external supply. Therefore, do not connect anything except the capacitor for stabilization and the resistors for setting of GAIN_MS_SEL and PLIMIT.	
6	GAIN_MS_SEL	I	Gain and Master/Slave mode Setting pin	
7	IN2P	I	Positive input pin for Ch2	
8	IN2N	I	Negative input pin for Ch2	
9	SYNC	I/O	Clock input/output pin to synchronize multiple class D amplifiers	

Pin Description – continued

10	FSEL0	I	PWM frequency setting pin 0	
11	FSEL1	I	PWM frequency setting pin 1	
12	FSEL2	I	PWM frequency setting pin 2	
13	MUTEX	I	Speaker output mute control pin H: Mute OFF L: Mute ON	
14	NC	-	Non connection	
15	VCCP2	-	Power supply pin for Ch2 PWM signal Please connect a capacitor.	
16	BSP2N	O	Boot-strap pin of Ch2 negative PWM signal Please connect a capacitor.	
17	OUT2N	O	Output pin of Ch2 negative PWM signal Please connect to output LPF.	
18	GNDP2	-	GND pin for Ch2 PWM signal	
19	OUT2P	O	Output pin of Ch2 positive PWM signal Please connect to output LPF.	
20	BSP2P	O	Boot-strap pin of Ch2 positive PWM signal Please connect a capacitor.	
21	BSP1N	O	Boot-strap pin of Ch1 negative PWM signal Please connect a capacitor.	
22	OUT1N	O	Output pin of Ch1 negative PWM signal Please connect to output LPF.	
23	GNDP1	-	GND pin for Ch1 PWM signal	
24	OUT1P	O	Output pin of Ch1 positive PWM signal Please connect to output LPF.	
25	BSP1P	O	Boot-strap pin of Ch1 positive PWM signal Please connect a capacitor.	
26	VCCP1	-	Power supply pin for Ch1 PWM signal Please connect a capacitor.	
27	VCCA	-	Power supply pin for Analog signal Please connect a capacitor.	
28	NC	-	Non connection	
29	REGA	O	Internal power supply pin for Gate driver Please connect a capacitor. The REGA terminal of BD28412MUV should not be used as external supply. Therefore, do not connect anything except the capacitor for stabilization.	
30	TEST	I	Test pin Please connect to GND.	

Pin Description – continued

31	PDX	I	Power down setting pin H: Active L: Standby	
32	ERRORX	O	Error flag pin Please connect to pull-up resistor. H: Normal L: Error detected An error flag occurs when Output Short Protection, DC Voltage Protection, or High Temperature Protection is activated. This flag shows IC condition during operation.	

The numerical value of internal equivalent circuit is typical value, not guaranteed value.

Block Diagram

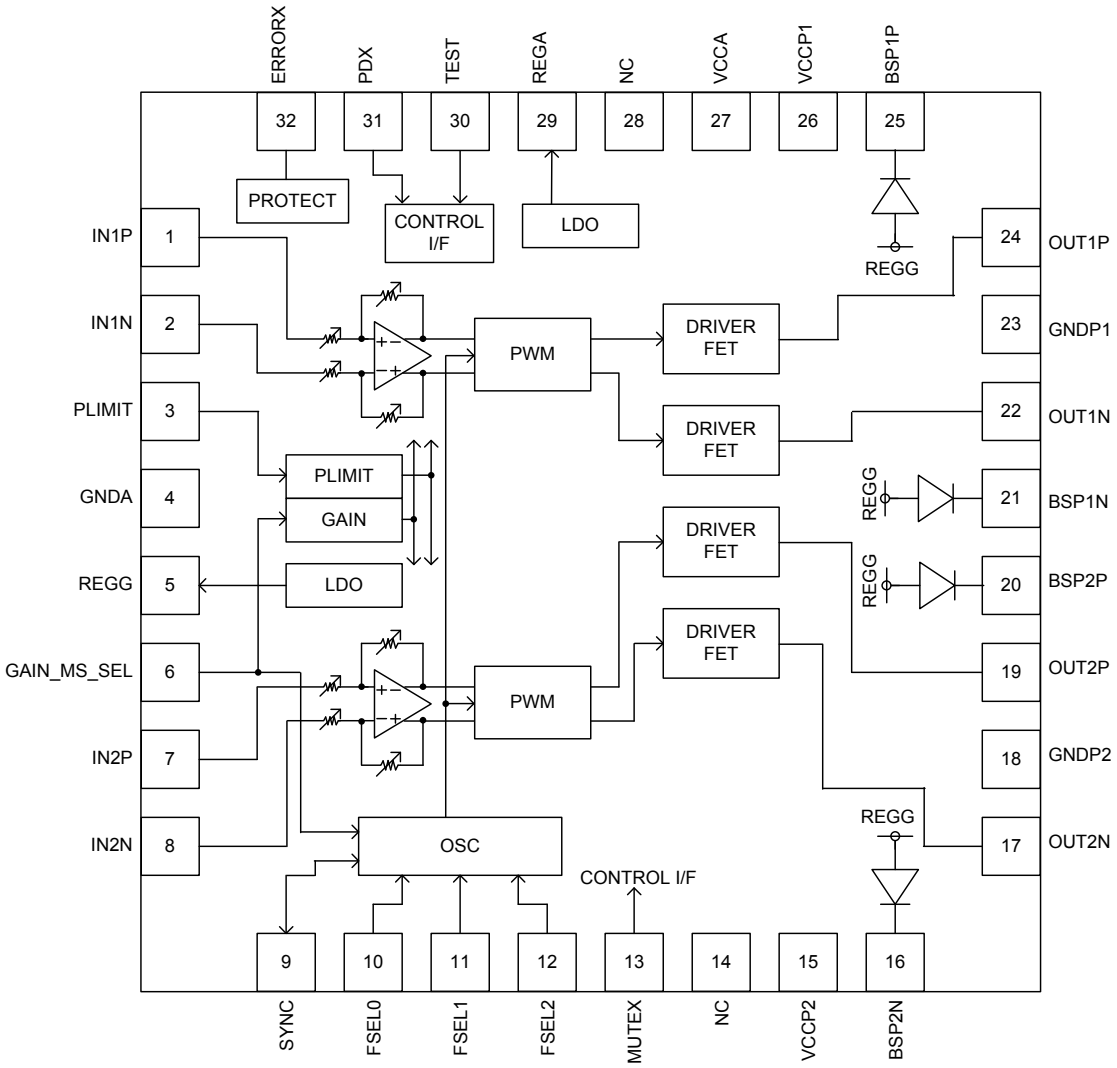


Figure 3. Block Diagram

Absolute Maximum Ratings (Tj = 25°C)

Parameter	Symbol	Rating	Unit	Conditions
Supply Voltage(Note 1)	V_{CCMAX}	-0.3 to +15.5	V	VCCA,VCCP1,VCCP2
Input Voltage1(Note 1)	V_{IN}	-0.3 to +7	V	IN1P, IN1N, IN2P, IN2N, PLIMIT, GAIN_MS_SEL, PLIMIT, SYNC(Note 2), FSEL0, FSEL1, FSEL2, PDX, MUTEX
Input Voltage2(Note 1)	V_{ERR}	-0.3 to +7	V	ERRORX
Pin Voltage1(Note 1) (Note 3)	V_{PIN1}	-0.3 to +V_{CCMAX}	V	OUT1P, OUT1N, OUT2P, OUT2N
Operating Temperature Range	Topr	-25 to +85	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	
Junction Temperature Range	Tj	-40 to +150	°C	

(Note 1) The voltage that can be applied reference to GND (Pin4, 18, 23).
(Note 2) SYNC pin is I/O pin. It is specified for input mode.
(Note 3) Please use under this rating including the AC peak waveform (overshoot) for all conditions.
Only undershoot is allowed at condition of ≤15.5V by the VCC reference and ≤10nsec (cf. Figure 4)

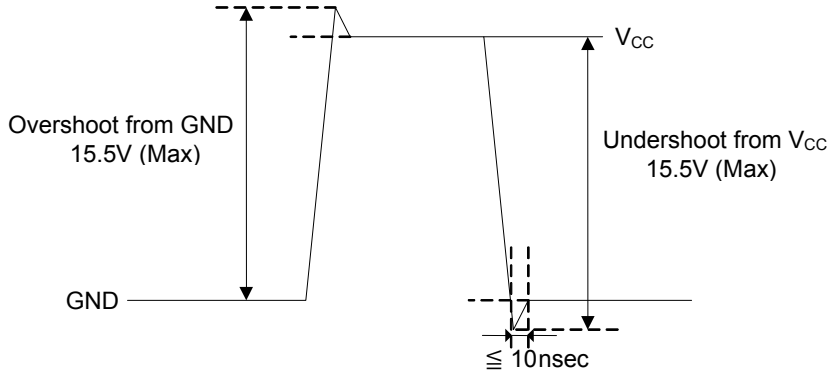


Figure 1. Overshoot and Undershoot

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance (Note 4)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 6)	2s2p(Note 7)	
VQFN032V5050				
Junction to Ambient	θ_{JA}	138.9	39.1	°C/W
Junction to Top Characterization Parameter(Note 5)	Ψ_{JT}	11	5	°C/W

(Note 4) Based on JESD51-2A(Still-Air)
(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 6) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mm

Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 7) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 8)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mm	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 8) This thermal via connects with the copper pattern of all layers..

Use a thermal design that allows for a sufficient margin in consideration of power dissipation under actual operating conditions. This IC exposes its frame at the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.

Recommended Operating Conditions (Ta= -25°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply Voltage	V_{IN}	4.5	-	13	V	VCCA, VCCP1, VCCP2
Load Impedance (Note 9)	R_{L1}	5.4	-	-	Ω	BTL
	R_{L2}	3.2	-	-	Ω	PBTL
High Level Input Voltage	V_{IH}	2.0	-	3.3	V	FSEL0, FSEL1, FSEL2, MUTEX, PDX
Low Level Input Voltage	V_{IL}	0	-	0.8	V	FSEL0, FSEL1, FSEL2, MUTEX, PDX
Low Level Output Voltage	V_{OL}	-	-	0.8	V	ERRORX, I_{OL}=0.5mA

(Note 9) Tj<150°C

Electrical Characteristics

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, R_L=8Ω, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent Standby Current	I_{CC1}	-	0.1	25	μA	No load or filter, PDX=L, MUTEX=L
Quiescent Mute Current	I_{CC2}	-	10	20	mA	No load or filter, PDX=H, MUTEX=L
Quiescent Operating Current	I_{CC3}	-	16	32	mA	No load or filter, No signal, PDX=H, MUTEX=H
Regulator Output Voltage	V_{REGG}	4.45	5.55	6.05	V	PDX=H, MUTEX=H
Input Impedance 1	R_{IN1}	50	-	-	kΩ	MUTEX, PDX, FSEL0, FSEL1, FSEL2, SYNC(Slave mode only),
Input Impedance 2	R_{IN2}	140	200	260	kΩ	PLIMIT
Output Power(Note 10)	P_{O1}	-	9	-	W	V_{CC}=12V, THD+N=10%
Gain 1(Note 10)	G_{V1}	19	20	21	dB	Po=1W, GAIN_MS_SEL= 0V
Gain 2(Note 10)	G_{V2}	25	26	27	dB	P_O=1W , GAIN_MS_SEL= 2/9 × V_{REGG}
Gain 3(Note 10)	G_{V3}	31	32	33	dB	P_O=1W, GAIN_MS_SEL= 3/9 × V_{REGG}
Gain 4(Note 10)	G_{V4}	35	36	37	dB	P_O=1W, GAIN_MS_SEL= 4/9 × V_{REGG}
Total Harmonic Distortion(Note 10)	THD	-	0.03	-	%	Po=1W, BW=AES17
Crosstalk(Note 10)	CT	60	100	-	dB	Po=1W, 1kHz BPF
PSRR(Note 10)	PSRR	-	55	-	dB	V_{RIPPLE}=0.2 V_{P-P}, f=1kHz
Output Noise Voltage(Note 10)	V_{NO}	-	-80	-70	dBV	Po=0W, BW=A-Weight
PWM (Pulse Width Modulation) Frequency	f_{PWM1}	1128	1200	1272	kHz	FSEL2=H, FSEL1=H, FSEL0=H
	f_{PWM2}	940	1000	1060	kHz	FSEL2=H, FSEL1=H, FSEL0=L
	f_{PWM3}	564	600	636	kHz	FSEL2=H, FSEL1=L, FSEL0=H
	f_{PWM4}	470	500	530	kHz	FSEL2=H, FSEL1=L, FSEL0=L
	f_{PWM5}	376	400	424	kHz	FSEL2=L, FSEL1=H, FSEL0=H

(Note 10) The value is specified as typical application. Actual value depends on PCB layout and external components.

Typical Performance Curves

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15µH, C=1µF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

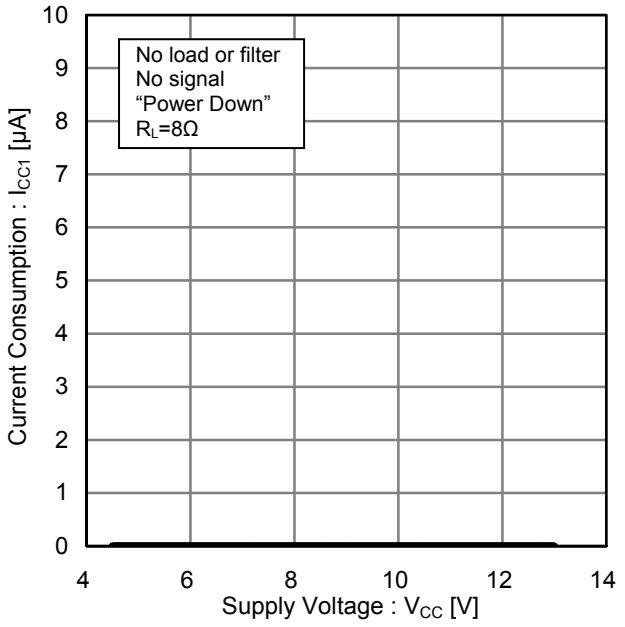


Figure 5. Current Consumption vs Supply Voltage (Power Down)

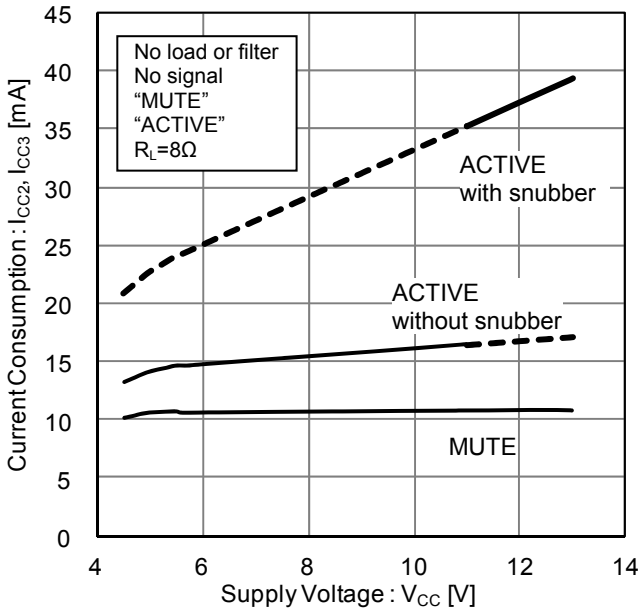


Figure 6. Current Consumption vs Supply Voltage (MUTE, ACTIVE)

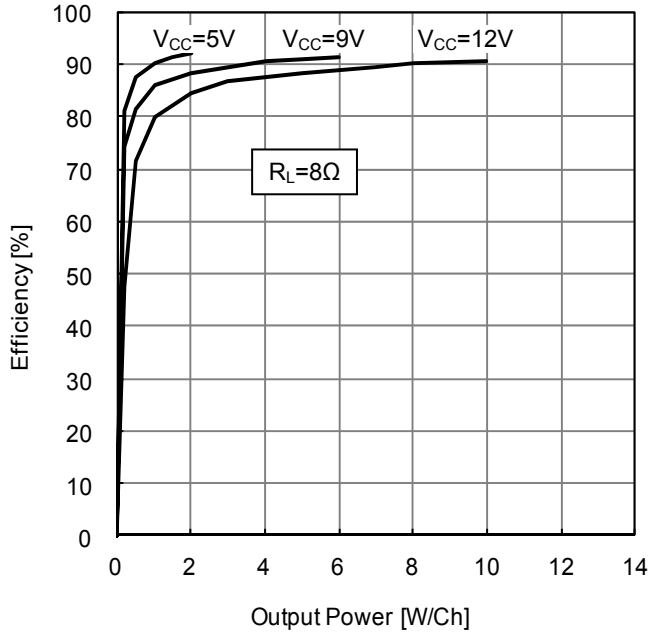


Figure 7. Efficiency vs Output Power (R_L=8Ω)

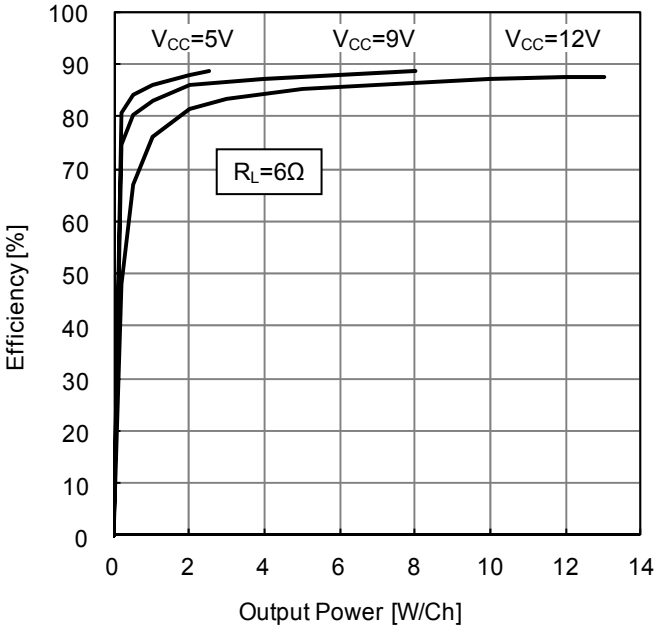


Figure 8. Efficiency vs Output Power (R_L=6Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15µH, C=1µF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

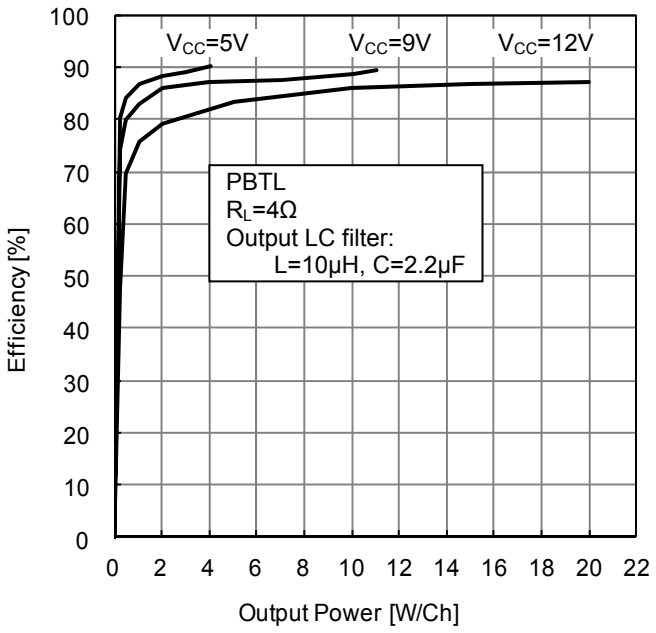


Figure 9. Efficiency vs Output Power (PBTL, R_L=4Ω)

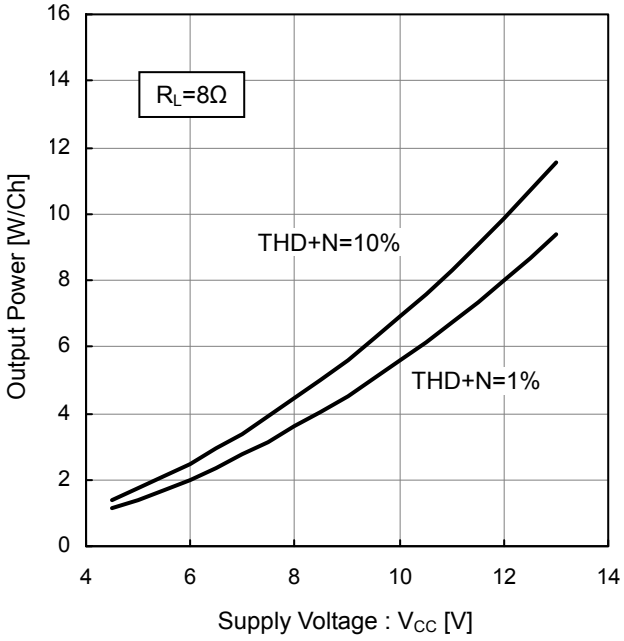


Figure 10. Output Power vs Supply Voltage (R_L=8Ω)

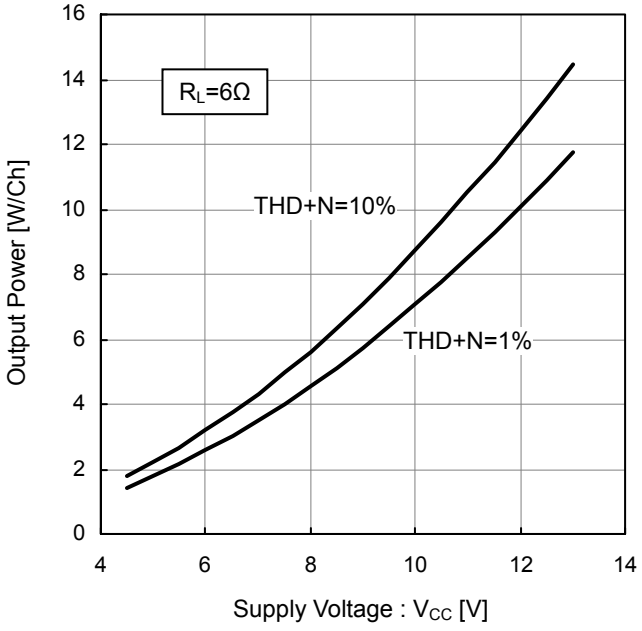


Figure 11. Output Power vs Supply Voltage (R_L=6Ω)

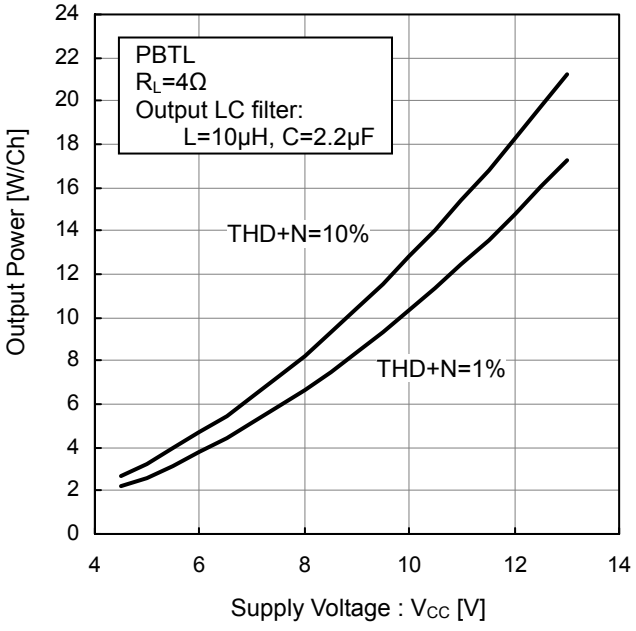


Figure 12. Output Power vs Supply Voltage (PBTL, R_L=4Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15µH, C=1µF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

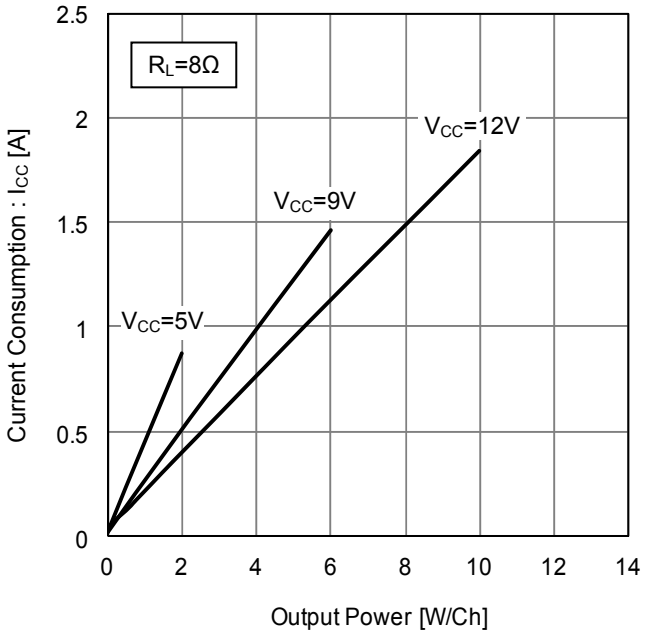


Figure 13. Current Consumption vs Output Power (R_L=8Ω)

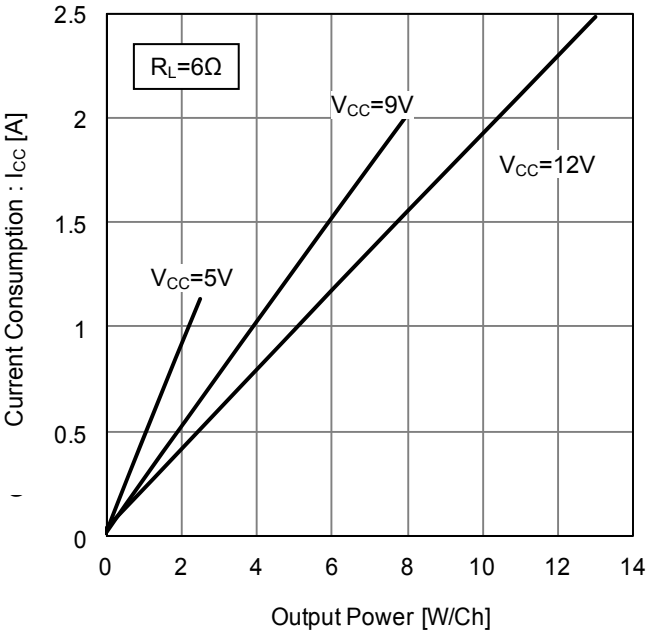


Figure14. Current Consumption vs Output Power (R_L=6Ω)

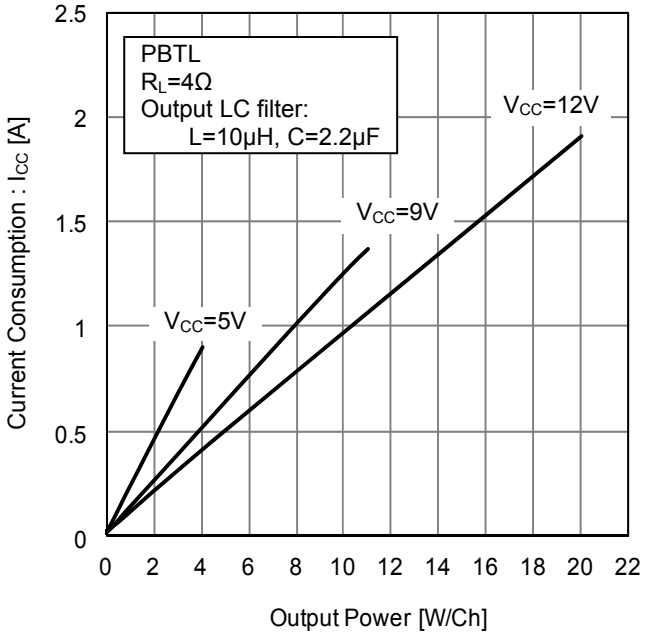


Figure15. Current Consumption vs Output Power (PBTL, R_L=4Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

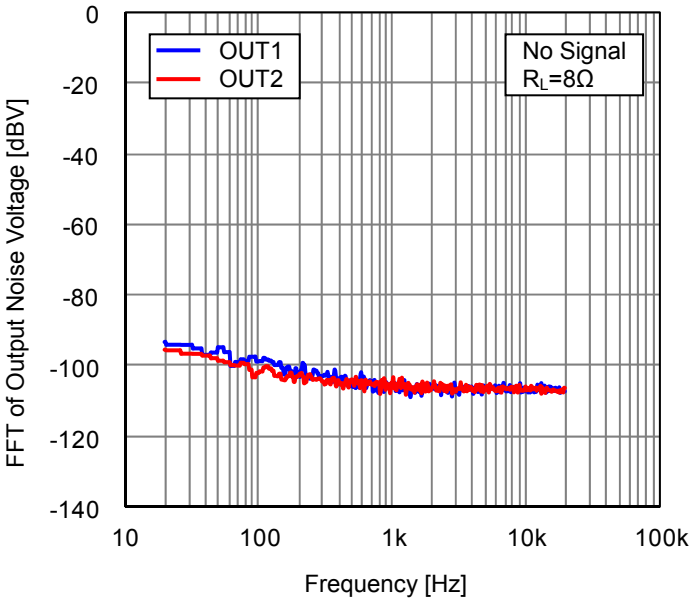


Figure16. FFT of Output Noise Voltage vs Frequency
(R_L=8Ω)

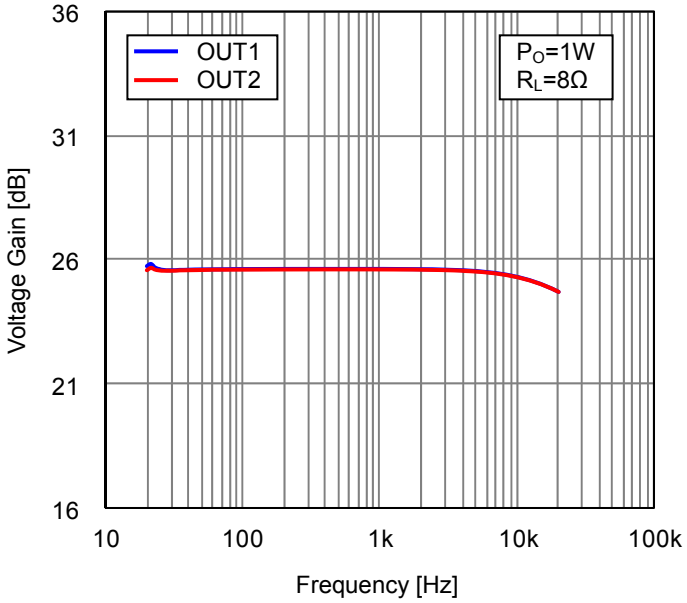


Figure17. Voltage Gain vs Frequency
(R_L=8Ω)

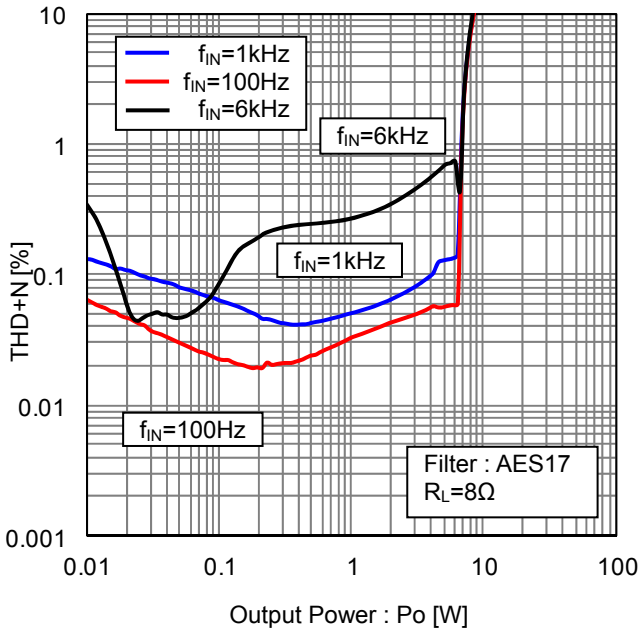


Figure18. THD+N vs Output Power
(R_L=8Ω)

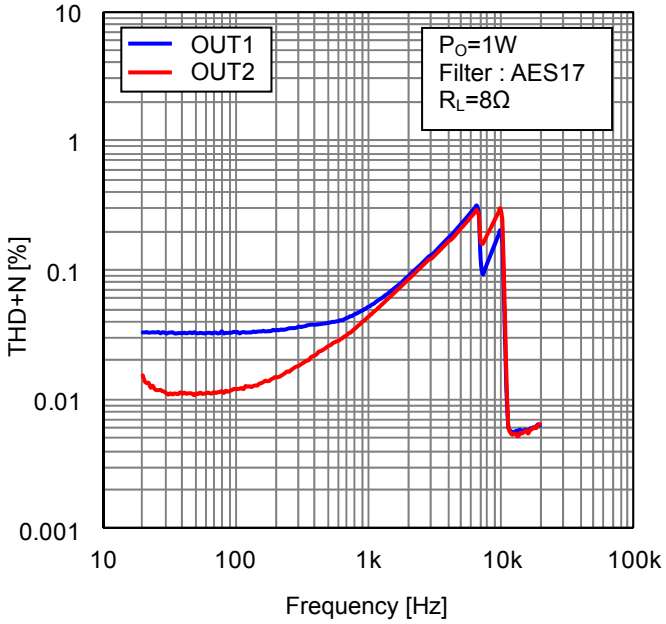


Figure19. THD+N vs Frequency
(R_L=8Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

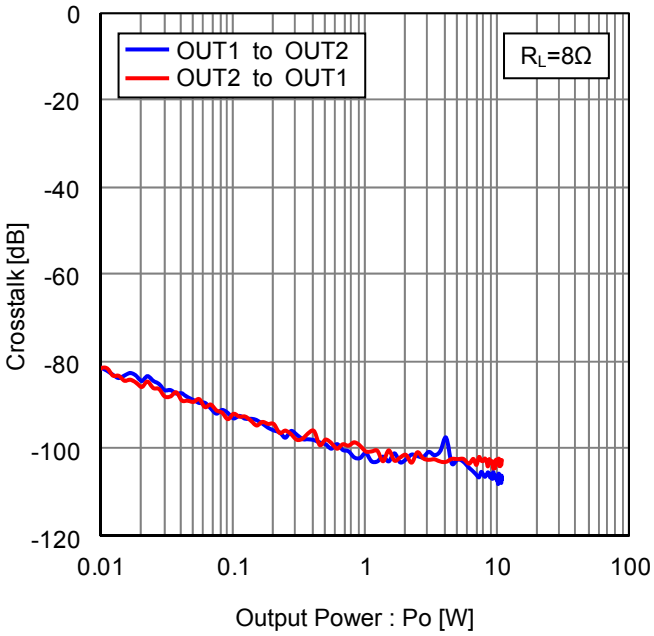


Figure 20. Crosstalk vs Output Power
(R_L=8Ω)

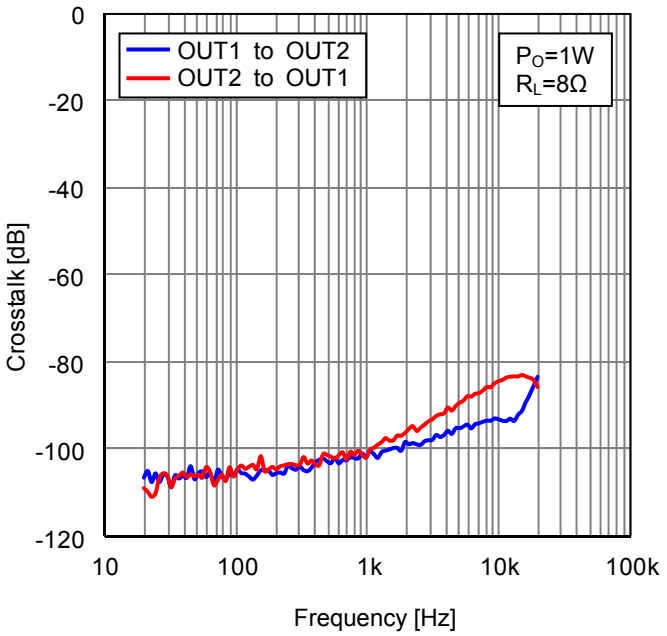


Figure 21. Crosstalk vs Frequency
(R_L=8Ω)

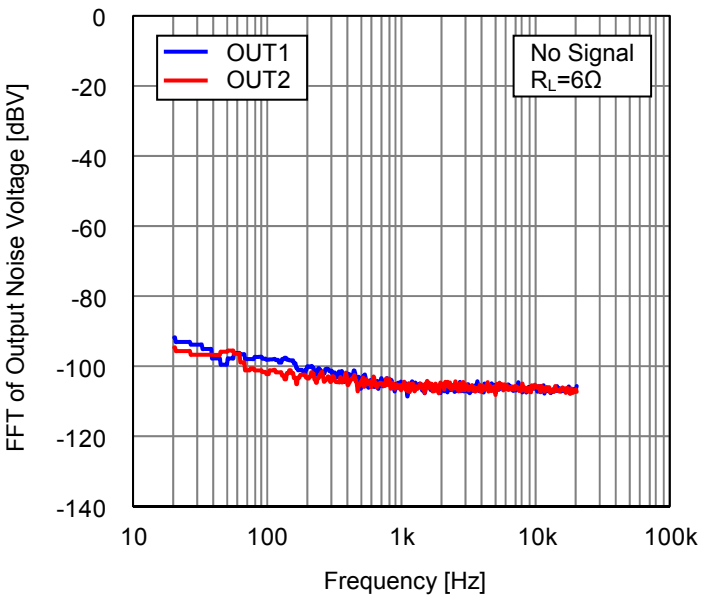


Figure 22. FFT of Output Noise Voltage vs Frequency
(R_L=6Ω)

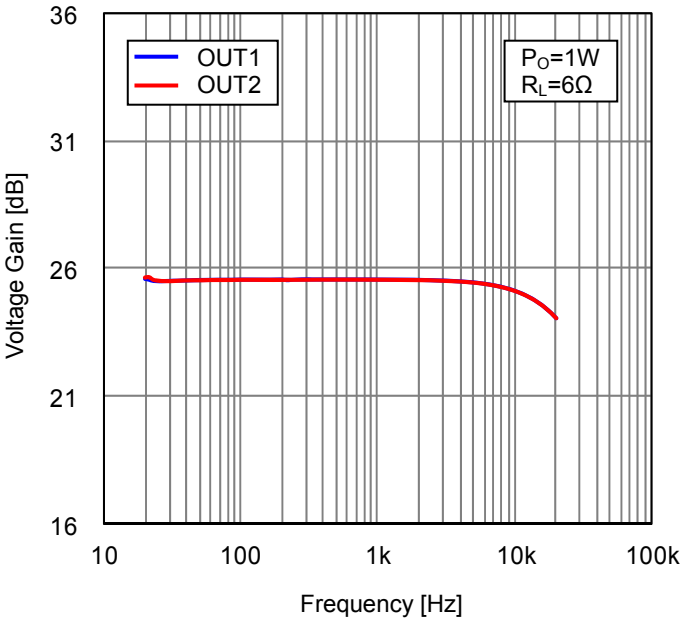


Figure 23. Voltage Gain vs Frequency
(R_L=6Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

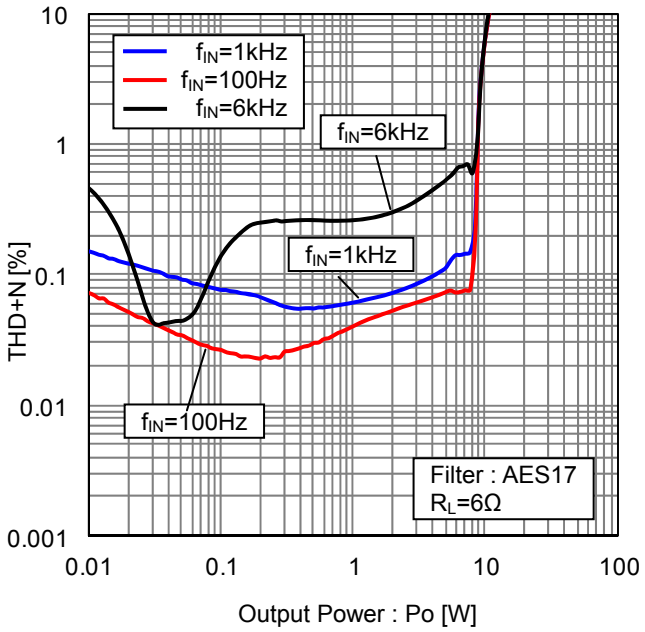


Figure 24. THD+N vs Output Power
(R_L=6Ω)

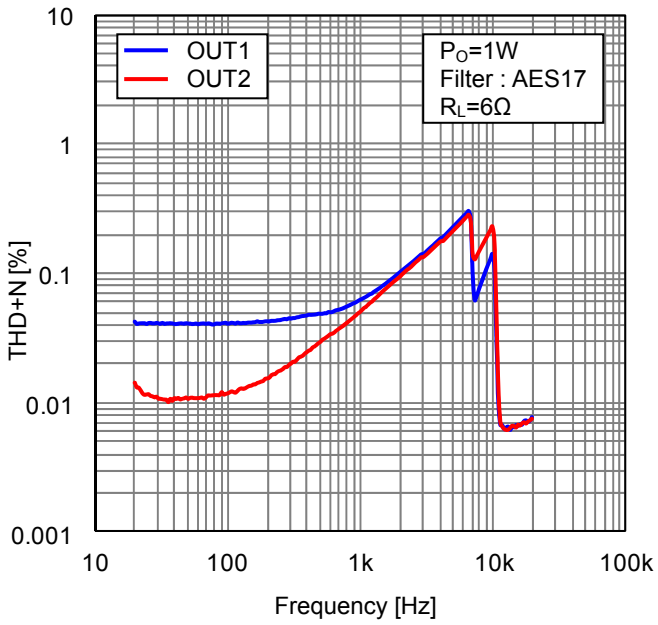


Figure 25. THD+N vs Frequency
(R_L=6Ω)

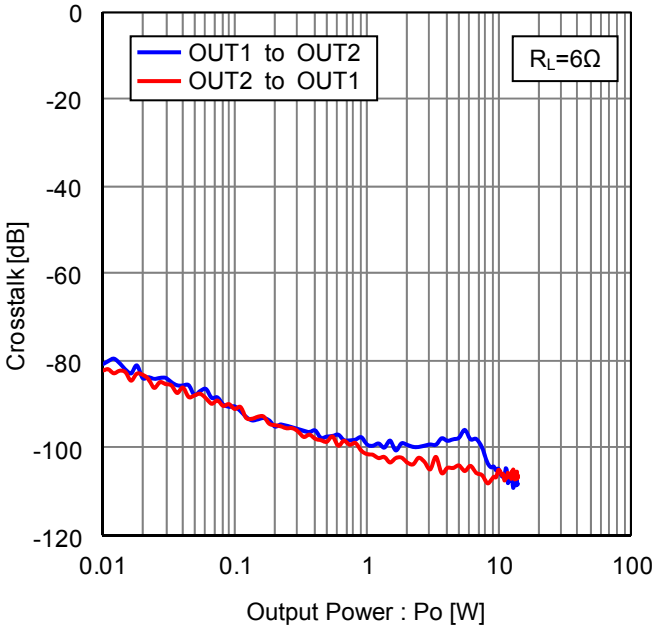


Figure 26. Crosstalk vs Output Power
(R_L=6Ω)

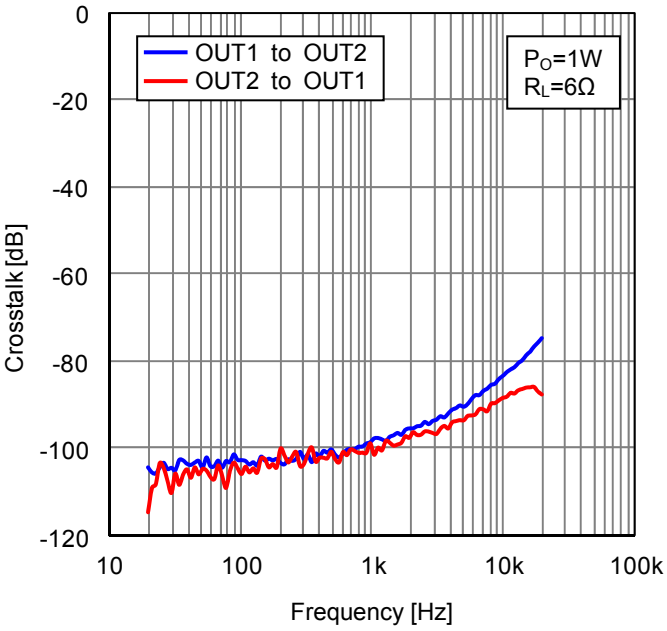


Figure 27. Crosstalk vs Frequency
(R_L=6Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{PWM}=600kHz, f_{IN}=1kHz, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=10μH, C=2.2μF
when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

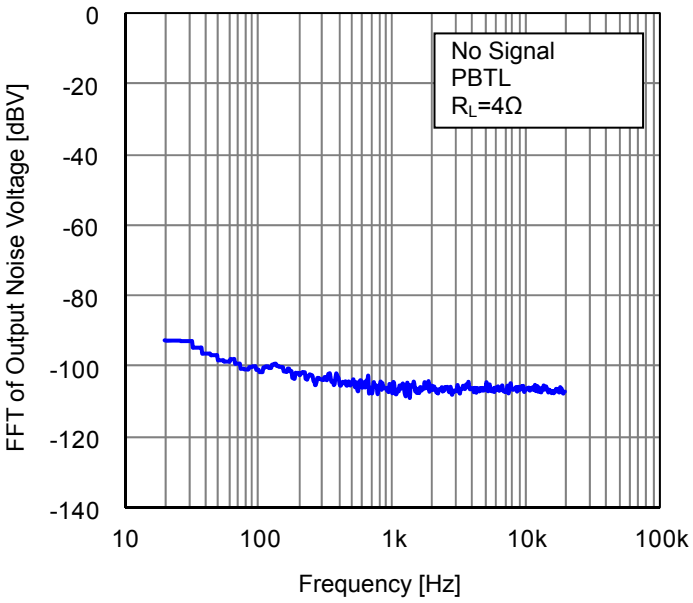


Figure 28. FFT of Output Noise Voltage vs Frequency (PBTL, R_L=4Ω)

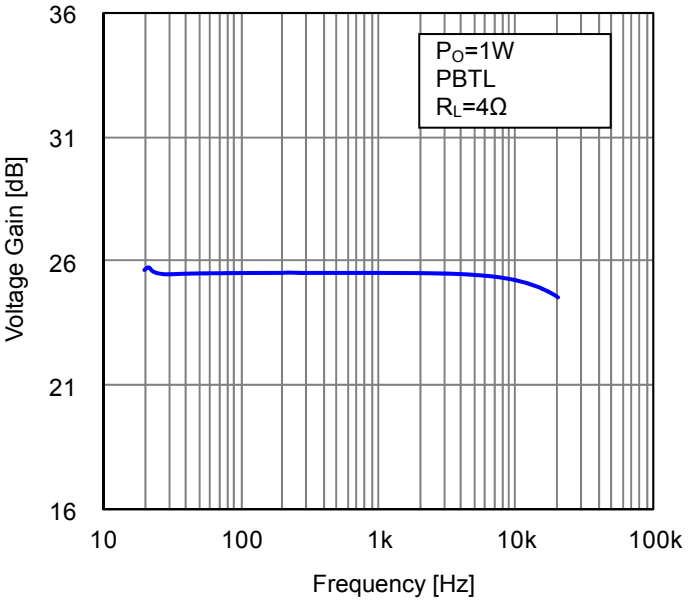


Figure 29. Voltage Gain vs Frequency (PBTL, R_L=4Ω)

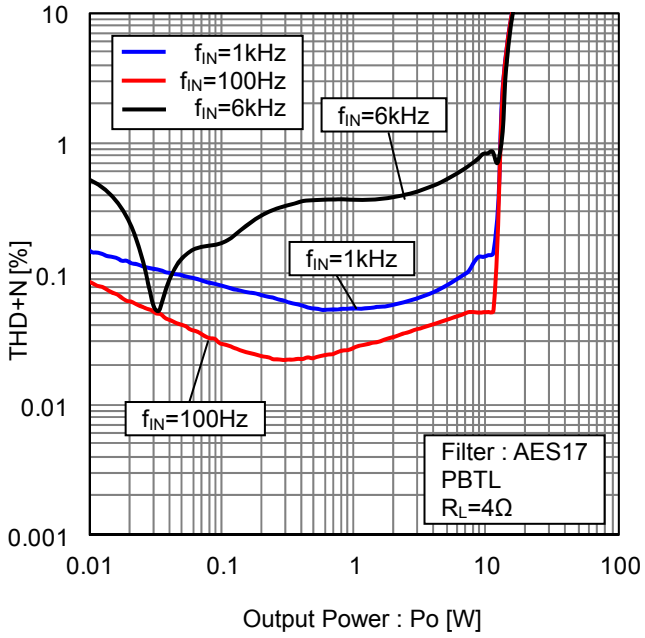


Figure 30. THD+N vs Output Power (PBTL, R_L=4Ω)

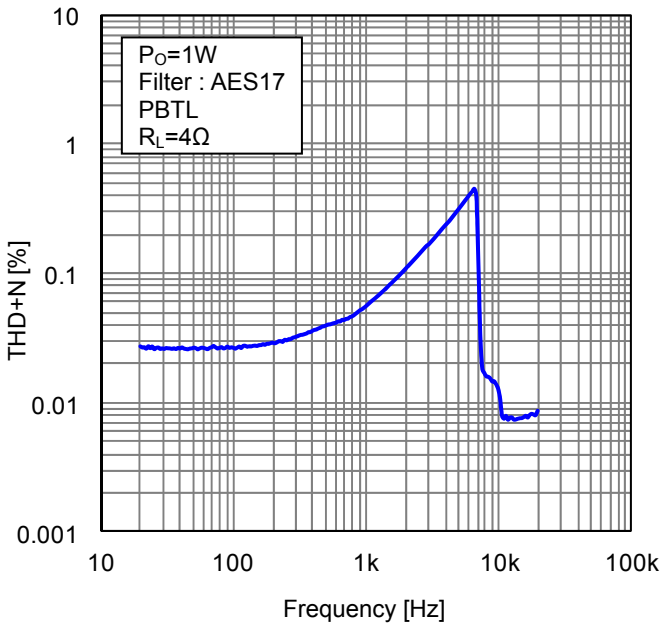


Figure 31. THD+N vs Frequency (PBTL, R_L=4Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{IN}=1kHz, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

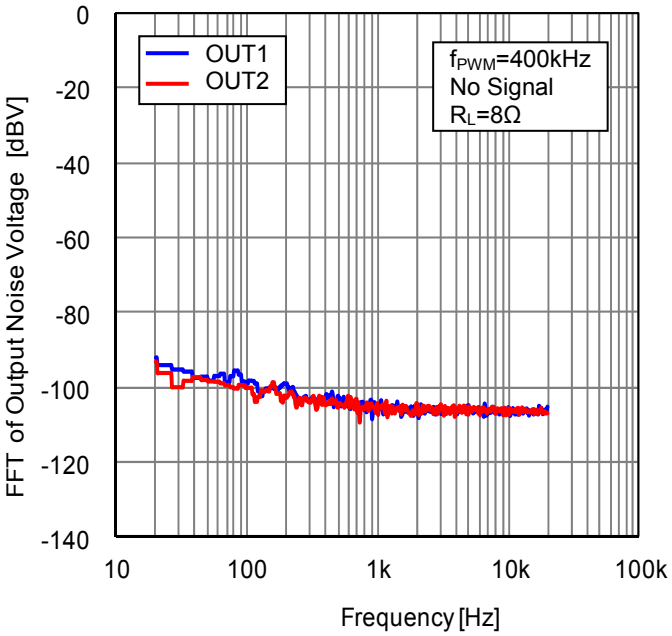


Figure 32. FFT of Output Noise Voltage vs Frequency (f_{PWM}=400kHz, R_L=8Ω)

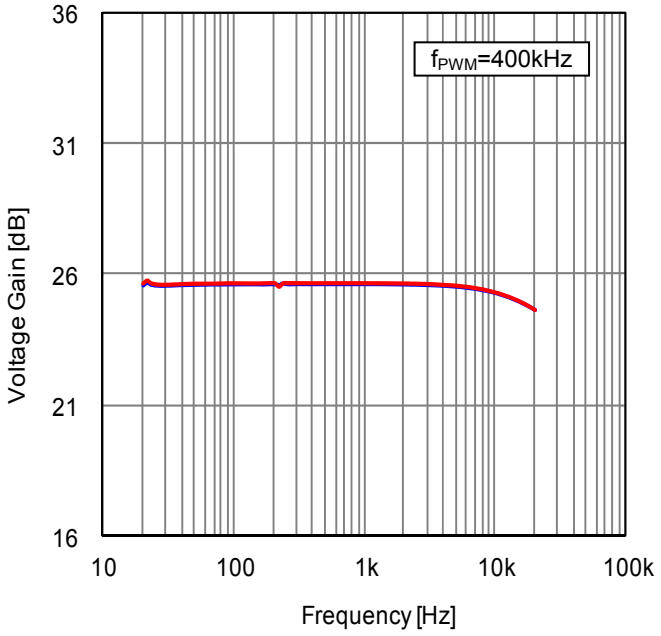


Figure 33. Voltage Gain vs Frequency (f_{PWM}=400kHz, R_L=8Ω)

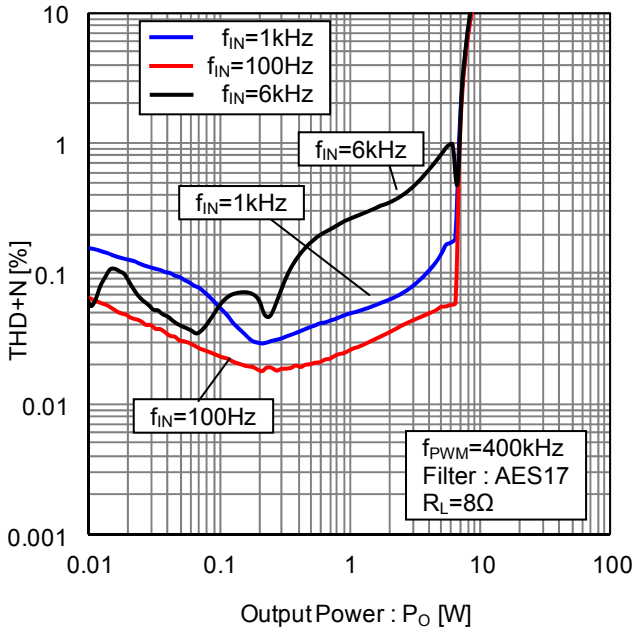


Figure 34. THD+N vs Output Power (f_{PWM}=400kHz, R_L=8Ω)

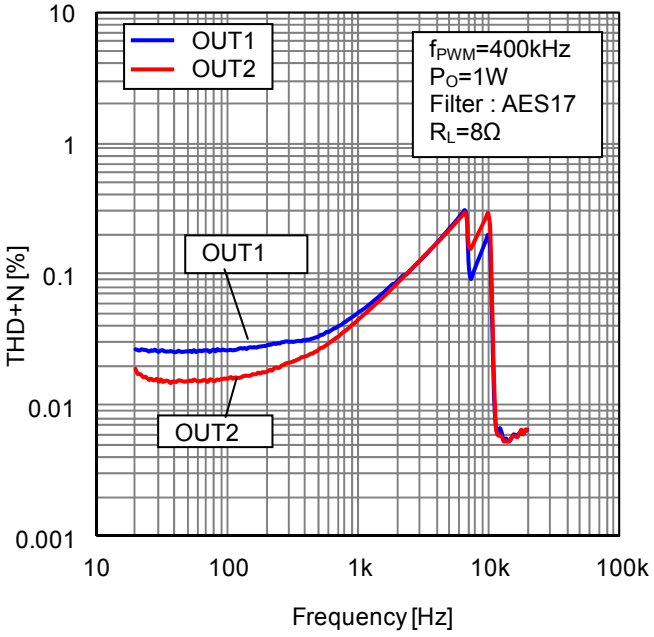


Figure 35. THD+N vs Frequency (f_{PWM}=400kHz, R_L=8Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta=25°C, V_{CC}=11V, f_{IN}=1kHz, PDX=3.3V, MUTEX=3.3V, PLIMT=0V, Gain=26dB, Output LC filter: L=15μH, C=1μF when V_{CC}>11V, snubber circuit is added: C=680pF, R=5.6Ω)

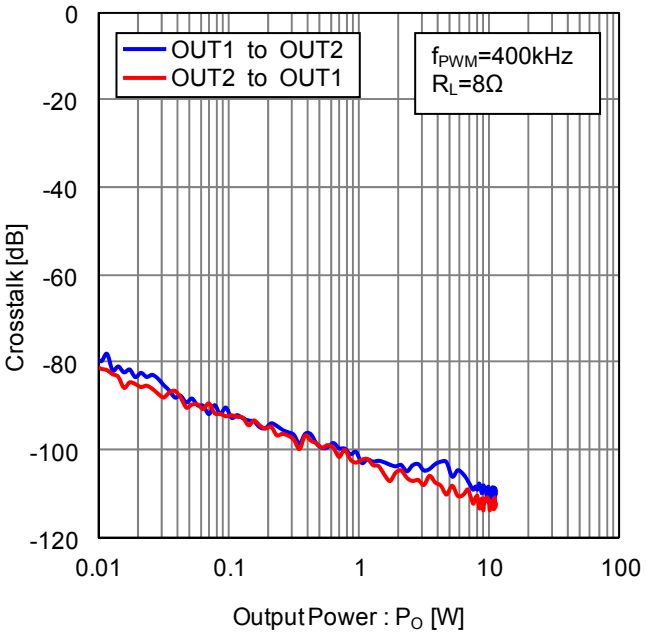


Figure 36. Crosstalk vs Output Power
(f_{PWM}=400kHz, R_L=8Ω)

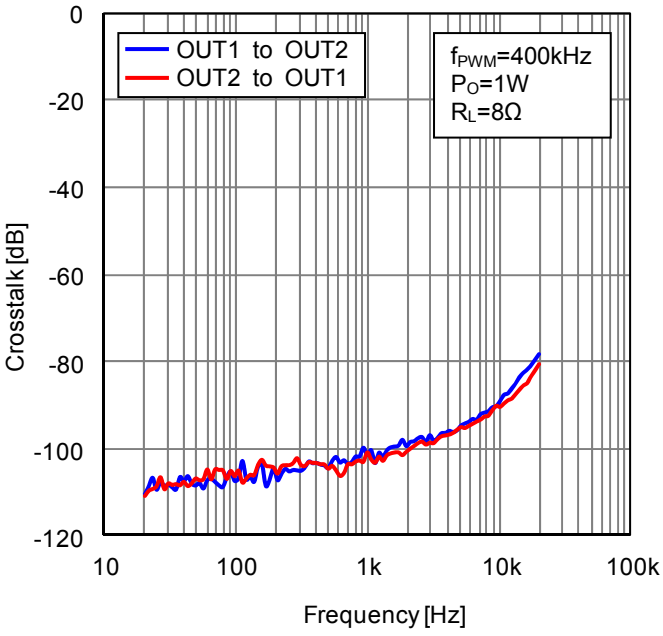


Figure 37. Crosstalk vs Frequency
(f_{PWM}=400kHz, R_L=8Ω)

Application Information

1. Power Up / Down Sequence

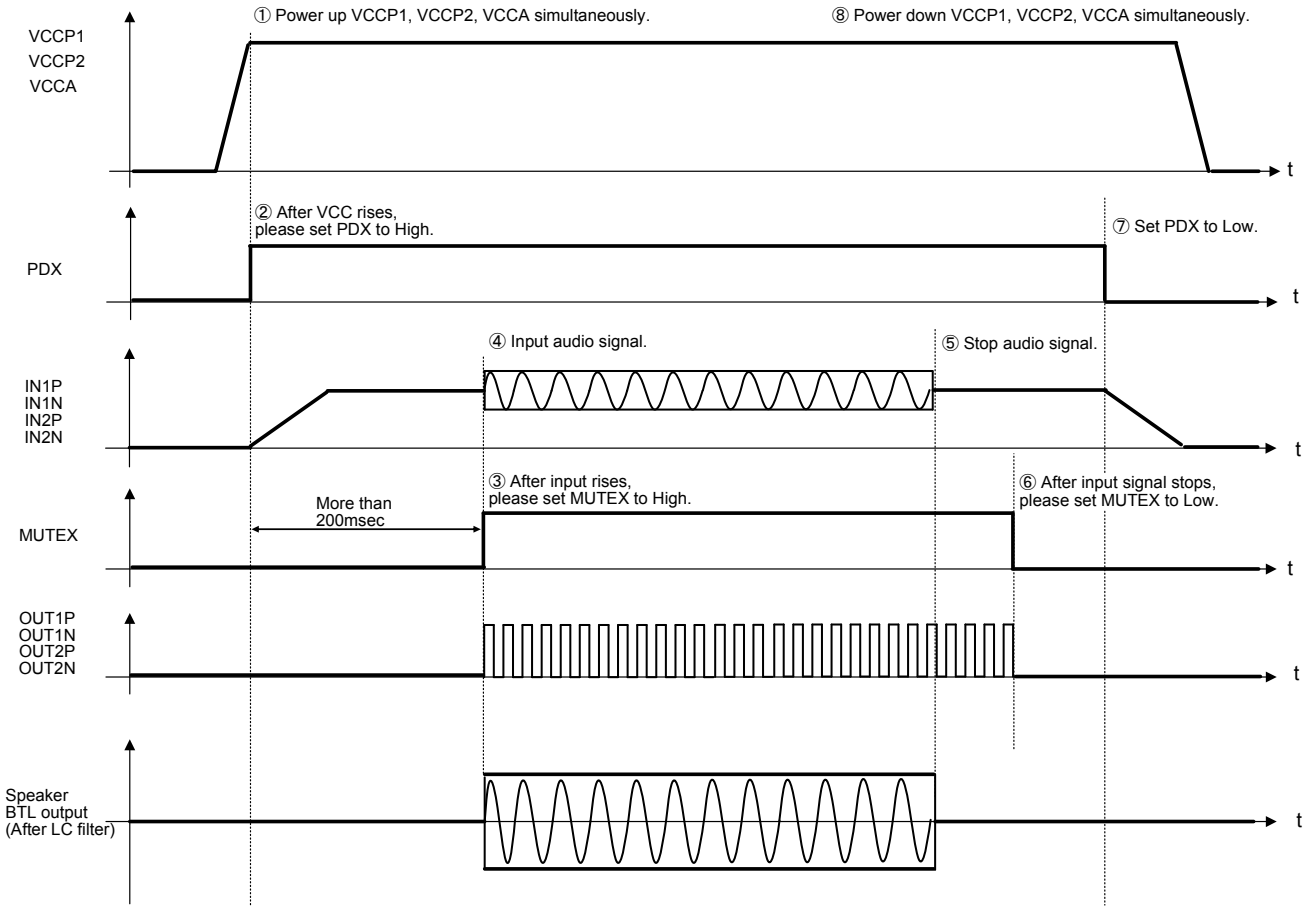


Figure 38. Power Up / Down Sequence

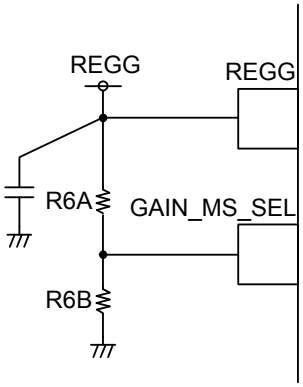
2. Function Description

(1) Power Down and Mute Setting

PDX	MUTEX	Normal		ERROR Detection	
		PWM output OUT1P, 1N, 2P, 2N	ERRORX(Note 12)	PWM output OUT1P, 1N, 2P, 2N	ERRORX(Note 12)
L	L/H	High-Z_Low(Note 11) (Power down)	H	High-Z_Low(Note 11) (Power down)	H
H	L	High-Z_Low(Note 11) (MUTE_ON)	H	High-Z_Low(Note 11) (MUTE_ON)	L
H	H	Active (MUTE_OFF)	H	High-Z_Low(Note 11) (MUTE_ON)	L

(Note 11) All power transistors are OFF and output terminals are pulled down by 40kΩ (Typ).
(Note 12) ERRORX pin is pulled up by 10kΩ resistor.

(2) Gain and Master/Slave Setting
Master/slave and gain are set by GAIN_MS_SEL pin voltage.



R6A(Note 13) (to REGG)	R6B(Note 13) (to GND)	Master/Slave	Gain	Input Impedance (IN1P,IN1N,IN2P,IN2N)
18kΩ	Open	Slave	36dB	30kΩ (Typ)
18kΩ	68kΩ	Slave	32dB	45.1kΩ (Typ)
33kΩ	68kΩ	Slave	26dB	79.3kΩ (Typ)
51kΩ	68kΩ	Slave	20dB	127.9kΩ (Typ)
68kΩ	51kΩ	Master	36dB	30kΩ (Typ)
68kΩ	33kΩ	Master	32dB	45.1kΩ (Typ)
68kΩ	18kΩ	Master	26dB	79.3kΩ (Typ)
open	18kΩ	Master	20dB	127.9kΩ (Typ)

(Note 13) Please use 1% tolerance resistor.

Figure 39. GAIN_MS_SEL Pin Setting

Setting cannot be changed when IC is active, but it can be set by rebooting (PDX=H to L to H).

Master/Slave Function
This IC has master and slave mode, and it can be synchronized by PWM frequency between two ICs. In master mode, SYNC pin becomes output pin for synchronization and in slave mode it becomes input pin, thus ensure that each SYNC pins are connected. Also, same setting for FSEL2/FSEL1/FSEL0 pins must be secured.

(3) Parallel BTL Function
Parallel BTL mode can be set by connecting IN2P and IN2N pins to GND.
Please short OUT1P – OUT2P, OUT1N – OUT2N near the IC as much as possible.
Parallel BTL mode cannot be set by connecting IN1P and IN1N pins to GND.

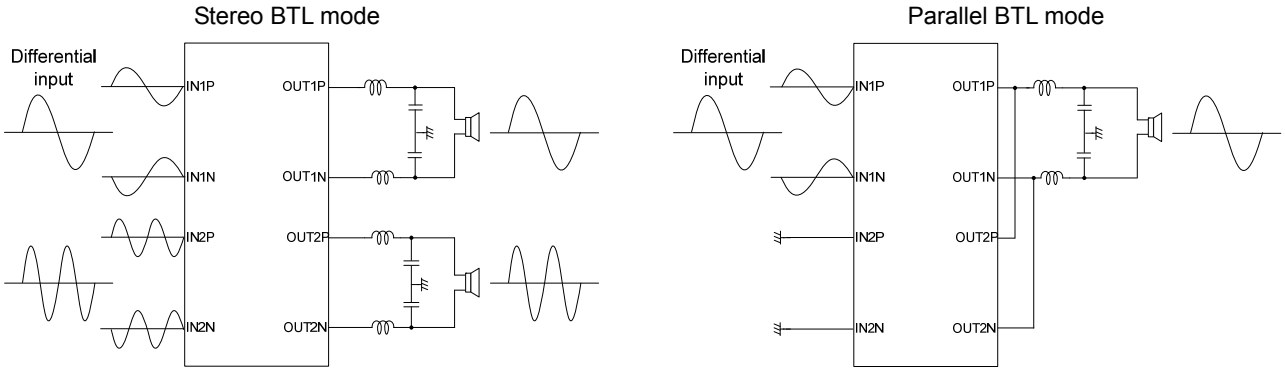


Figure 40. Parallel BTL Mode

(4) Power Limit Function

It is possible to limit the maximum output voltage by PLIMIT pin for protection of speaker.

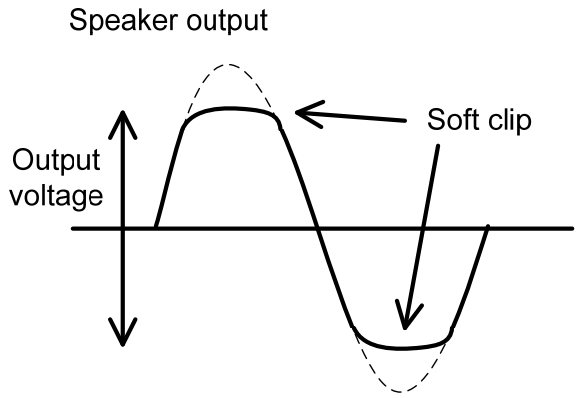


Figure 41. Power Limit

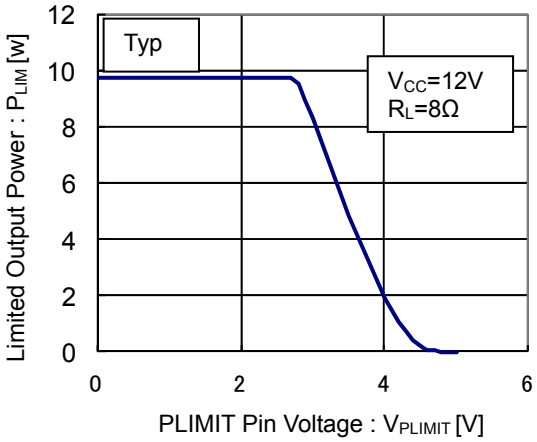


Figure 42. Limited Output Power vs PLIMIT Pin Voltage

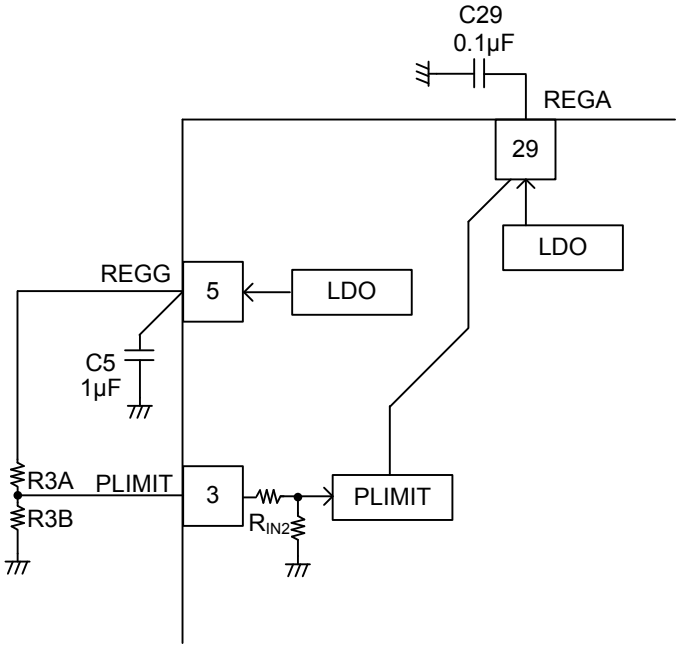


Figure 43. PLIMIT Pin Setting

Output wave is clipped like Figure 37. by applying the DC voltage to 3PIN (PLIMIT), and output power is limited. Figure 41 shows the relation between limited output power P_{LIM} and 3PIN (PLIMIT) pin voltage V_{PLIMIT}. V_{PLIMIT} is set by using external resistance R3A and R3B. Setting examples of R3A and R3B is showed below. If you don't use the power limit function, connect 3PIN (PLIMIT) to GND.

R3A [Ω]	R3B [Ω]	Max output power P_{LIM} [W] (R_L=8Ω)		
		Min	Typ	Max
OPEN	Short to GND	-	(unlimited)	-
12k	20k	3.4	6.8	13.6
10k	20k	2.5	5	10
8.2k	20k	1.7	3.4	6.8

When you use the power limit function in the setting except the table, P_{LIM} is

$$P_{LIM} = \frac{(V_{REGA} - V_{PLIMIT})^2 \times 39.8}{2R_L}$$

$$V_{PLIMIT} = \frac{1}{R_{3A}\left(\frac{1}{R_{3A}} + \frac{1}{R_{3B}} + \frac{1}{R_{IN2}}\right)} V_{REGG}$$

Where:
V_{REGA} is the voltage of 29PIN (REGA), 5V(Typ)
V_{REGG} is the voltage of 5PIN (REGG), 5.55V(Typ)
R_{IN2} is pull-down resistance of 3PIN (PLIMIT), 200kΩ(Typ)

Set the R3A and R3B to become the limited power.

(5) FSEL2 / FSEL1 / FSEL0 (AM avoidance function)
FSEL2 / FSEL1 / FSEL0 pins are used for PWM frequency setting. They can change the PWM frequency like below.

FSEL2	FSEL1	FSEL0	PWM frequency
H	H	H	1200kHz (Typ)
H	H	L	1000kHz (Typ)
H	L	H	600kHz (Typ)
H	L	L	500kHz (Typ)
L	H	H	400kHz (Typ)

Do not set following conditions to become un-recommended frequency:
FSEL2=L, FSEL1=H, FSEL0=L
FSEL2=L, FSEL1=L, FSEL0=H
FSEL2=FSEL1=FSEL0=L

(6) AM avoidance function
PWM frequency is near to AM radio frequency band therefore this makes interference during AM radio is used, and may negatively affects reception of AM radio wave. This interference can be reduced by adjusting PWM frequency. Below are the recommended settings. Example, for receiving AM radio wave of 1269kHz in Asia / Europe, PWM frequency must be set to 500kHz.

AM frequency [kHz]		Recommended PWM frequency setting				
Americas	Asia / Europe	f_{PWM}=400kHz FSEL2=L FSEL1=H FSEL0=H	f_{PWM}=500kHz FSEL2=H FSEL1=L FSEL0=L	f_{PWM}=600kHz FSEL2=H FSEL1=L FSEL0=H	f_{PWM}=1000kHz FSEL2=H FSEL1=H FSEL0=L	f_{PWM}=1200kHz FSEL2=H FSEL1=H FSEL0=H
	522 – 540	○	-	○	○	○
540 – 917	540 – 914	-	○	-	○	○
917 – 1125	914 – 1122	○	-	○	-	○
1125 – 1375	1122 – 1373	-	○	-	○	-
1375 – 1547	1373 – 1548	○	-	○	○	○
1547 – 1700	1548 – 1701	○	-	○	○	○

3. Application Information

(1) Application Circuit Example 1 (Stereo BTL, V_{CC}=4.5V to 11V)
Overshoot of output PWM differs depending on the board, etc. Ensure that it is lower than absolute maximum ratings. If it exceeds the absolute maximum ratings, snubber circuit need to be added, the circuit example is shown on the next page.

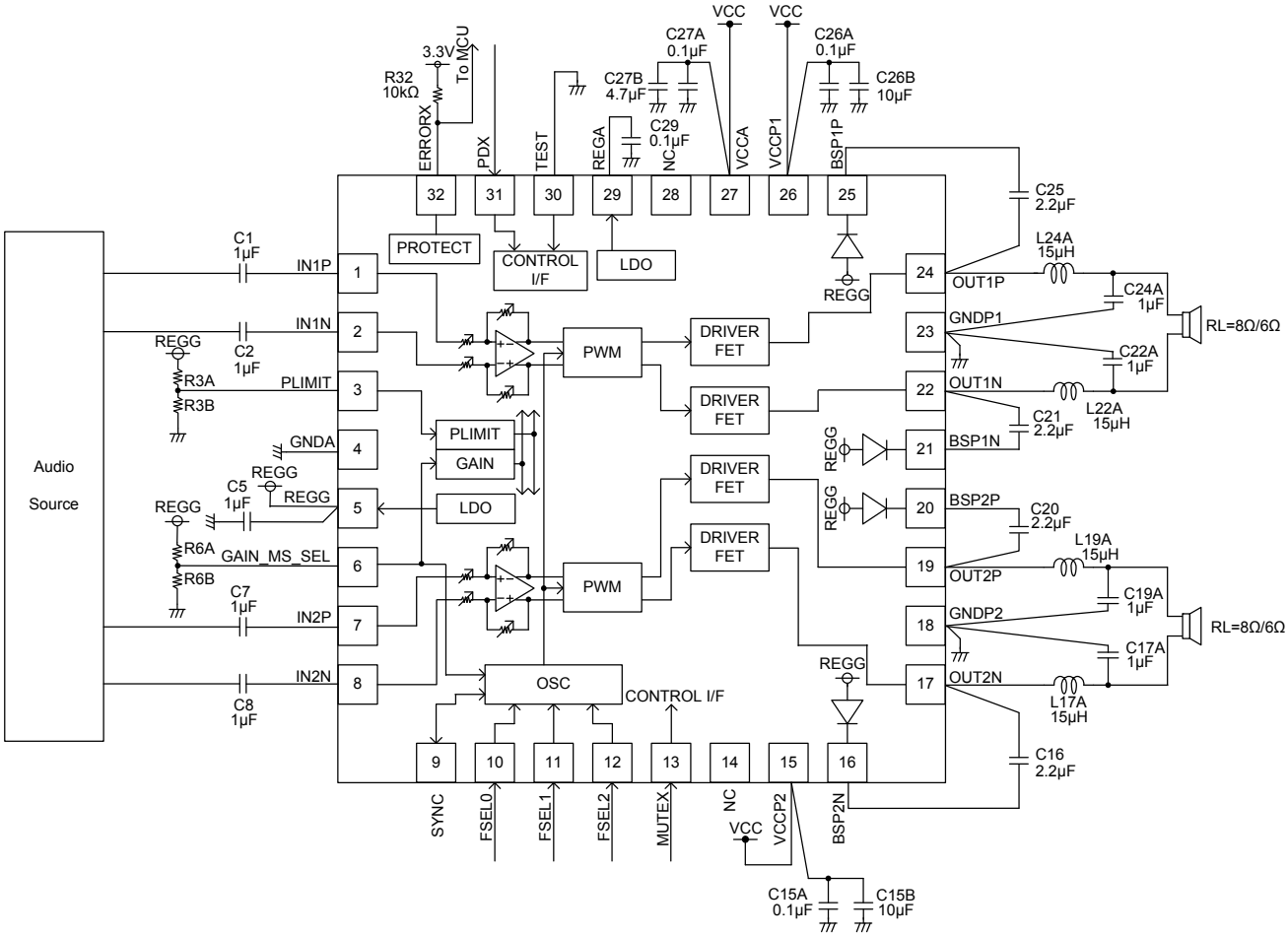


Figure 44. Application Circuit 1

BOM 1 (Stereo BTL, V_{CC}=4.5V to 11V)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description (4)Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description (2)Gain and Master/Slave setting
	1	R6B	
	1	R32	10kΩ, 1/16W, J(±5%)
Capacitor	4	C1, C2, C7, C8	1µF, 16V, B(±10%)
	1	C5(Note 14)	1µF, 16V, B(±10%)
	3	C15A, C26A, C27A(Note 14)	0.1µF, 25V, B(±10%)
	2	C15B, C26B(Note 14)	10µF, 25V, B(±10%)
	4	C16, C20, C21, C25(Note 14)	2.2µF, 16V, B(±10%)
	4	C17A, C19A, C22A, C24A	1µF, 25V, B(±10%)
	1	C27B(Note 14)	4.7µF, 25V, B(±10%)
	1	C29(Note 14)	0.1µF, 16V, B(±10%)
Inductor	4	L17A, L19A, L22A, L24A	15µH, 2.1A, ±20%

(Note 14) Please place it near pin as much as possible.

(2) Application Circuit Example 2 (Stereo BTL, V_{CC}=11V to 13V)
Please add the snubber circuit at OUT pin when V_{CC}=11V to 13V.

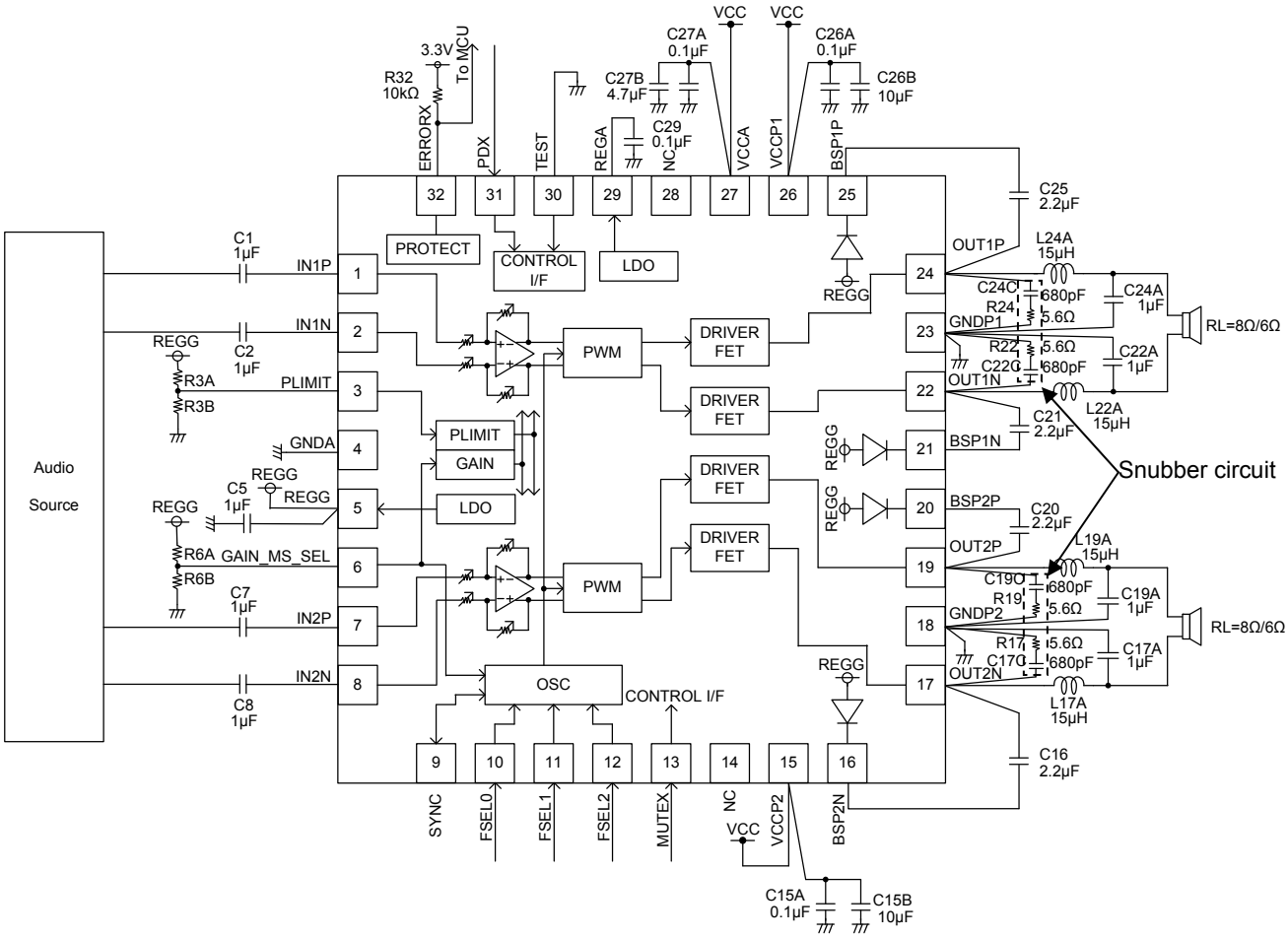


Figure 45. Application Circuit 2

BOM 2 (Stereo BTL, V_{CC}=11V to 13V)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description (4)Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description (2)Gain and Master/Slave setting
	1	R6B	
	1	R32	10kΩ, 1/16W, J(±5%)
	4	R17, R19, R22, R24	5.6Ω, 1/10W, J(±5%)
Capacitor	4	C1, C2, C7, C8	1μF, 16V, B(±10%)
	1	C5(Note 15)	1μF, 16V, B(±10%)
	3	C15A, C26A, C27A(Note 15)	0.1μF, 25V, B(±10%)
	2	C15B, C26B(Note 15)	10μF, 25V, B(±10%)
	4	C16, C20, C21, C25(Note 15)	2.2μF, 16V, B(±10%)
	4	C17A, C19A, C22A, C24A	1μF, 25V, B(±10%)
	4	C17C, C19C, C22C, C24C(Note 15)	680pF, 25V, B(±10%)
	1	C27B(Note 15)	4.7μF, 25V, B(±10%)
	1	C29(Note 15)	0.1μF, 16V, B(±10%)
Inductor	4	L17A, L19A, L22A, L24A	15μH, 2.1A, ±20%

(Note 15) Please place it near pin as much as possible.

(3) Application Circuit Example 3 (Monaural PBTL, V_{CC}=4.5V to 11V)
Overshoot of output PWM differs depending on the board, etc. Ensure that it is lower than absolute maximum ratings. If it exceeds the absolute maximum ratings, snubber circuit need to be added, the circuit example is shown on the next page.

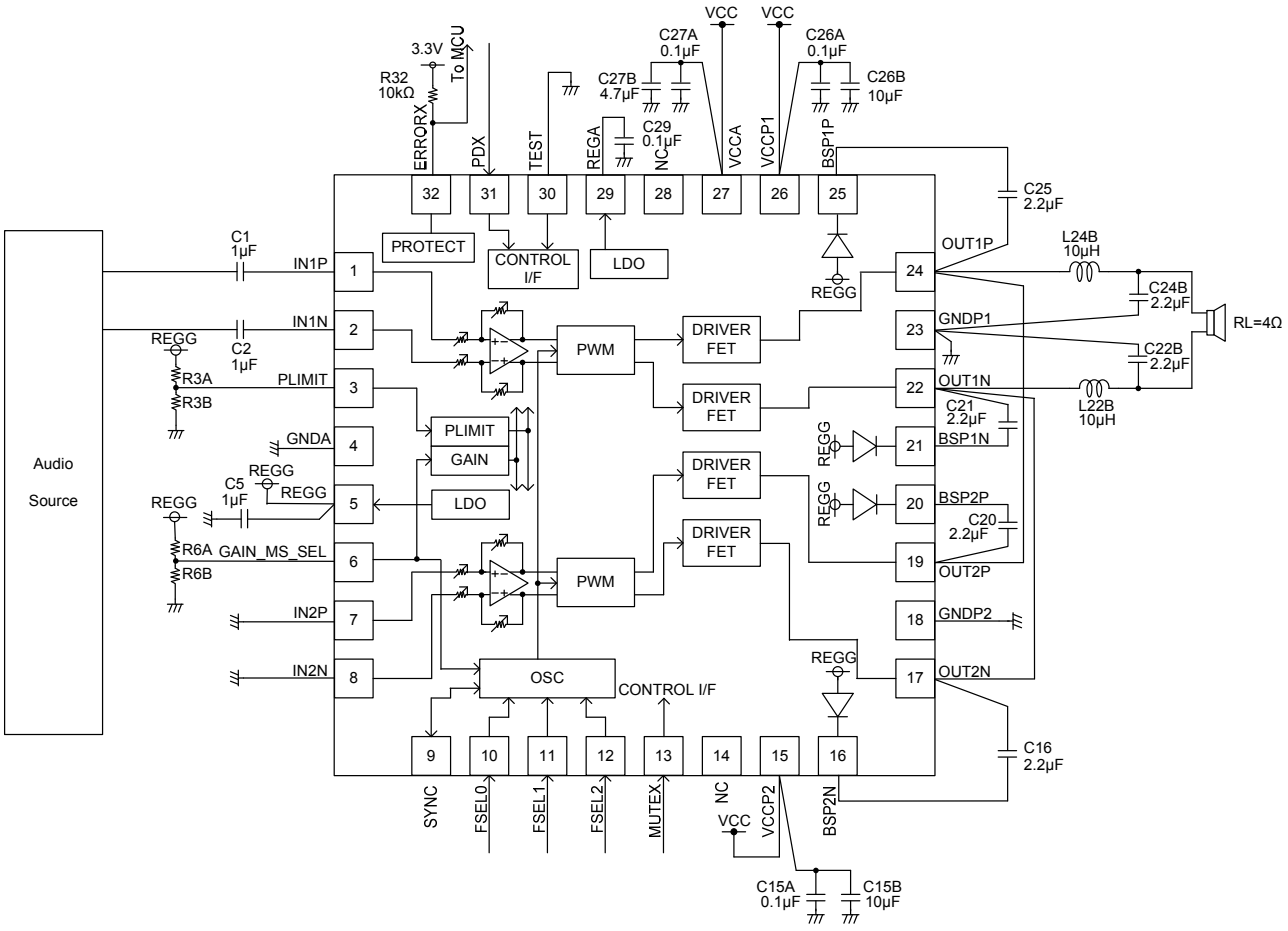


Figure 46. Application Circuit 3

BOM 3 (Monaural PBTL, V_{CC}=4.5V to 11V)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description (4)Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description (2)Gain and Master/Slave setting
	1	R6B	
	1	R32	10kΩ, 1/16W, J(±5%)
Capacitor	2	C1, C2	1µF, 16V, B(±10%)
	1	C5(Note 16)	1µF, 16V, B(±10%)
	3	C15A, C26A, C27A(Note 16)	0.1µF, 25V, B(±10%)
	2	C15B, C26B(Note 16)	10µF, 25V, B(±10%)
	4	C16, C20, C21, C25	2.2µF, 16V, B(±10%)
	2	C22B, C24B(Note 16)	2.2µF, 25V, B(±10%)
	1	C27B	4.7µF, 25V, B(±10%)
	1	C29(Note 16)	0.1µF, 16V, B(±10%)
Inductor	2	L22B, L24B	10µH, 2.6A, ±20%

(Note 16) Please place it near pin as much as possible.