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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Middle Power Class-D Speaker Amplifier Series

17W+17W
Class D Speaker Amplifier for Digital Input

BD28623MUV

General Description

BD28623MUV is a Class D Speaker Amplifier designed for Flat-panel TVs in particular for space-saving and low-power consumption. This IC delivers an output power of 20W+20W. This IC employs state-of-the-art Bipolar, CMOS, and DMOS (BCD) process technology. With this technology, the IC can achieve high efficiency. In addition, the IC is packaged in a compact back-surface heat-sink type power package to achieve low power consumption and low heat generation and to eliminate need for external heat-sink. With this package, total output power is only 34W as compared to 40W total output power of package with external heat-sink This product satisfies all needs for drastic downsizing, low-profile structures and powerful high quality playback of sound systems.

Features

- 1 Digital Audio Interface
  I^2S format
  SDATA: 16 / 20 / 24bit
  LRCLK (f_S): 32 kHz/ 44.1kHz / 48kHz
  BCLK: $64f_S$ (fixed)
  MCLK: $256f_S$ / $512f_S$ Automatic Identification)
- Low supply current at RESET mode.
- Slew rate controller
  ; No need snubber circuit (Vcc≤22V)
- Output Feedback Circuitry which prevents decrease of sound quality caused by change of power supply voltage, achieves low noise and low distortion, So the large electrolytic-capacitors for Vcc bypass is able to be eliminated.
- Variable Gain (17dB / 20dB / 26dB)
- Wide power supply voltage range (8.5V to 24V)
- High efficiency, low heat
- Pop noise prevention at power supply on / off
- Soft Muting Technology
- High reliability design by built-in protection circuits
  - Overheat protection
  - Under voltage protection
  - Output short protection
  - Output DC voltage protection
  - Clock stop protection (MCLK, BCLK, LRCLK)
- Small package (VQFN024V4040)

Applications

- Flat Panel TVs (LCD, Plasma)
- Home Audio (Sound Bar)
- Amusement Equipment
- Electronic Music Equipment
- Desktop PC, etc.

Key Specifications

- Supply Voltage: 8.5V to 24V
- Speaker Output Power: 17W+17W (Typ)
  (V_{CC}=18V, R_L=8Ω, Gain=26dB)
- Total Harmonic Distortion: 0.08% (Typ) @P_O=1W
  (V_{CC}=12V, R_L=8Ω, Gain=20dB)
- Crosstalk: 90dB (Typ)
- PSRR: 60dB (Typ)
- Output Noise Voltage: 150μV_{rms} (Typ)
- Standby Current: 33μA (Typ)
- Operating Temperature Range: -25°C to +85°C

Package W(Typ) x D(Typ) x H(Max)
VQFN024V4040 4.00mm x 4.00mm x 1.00mm

VQFN024V4040

Typical Application Circuit

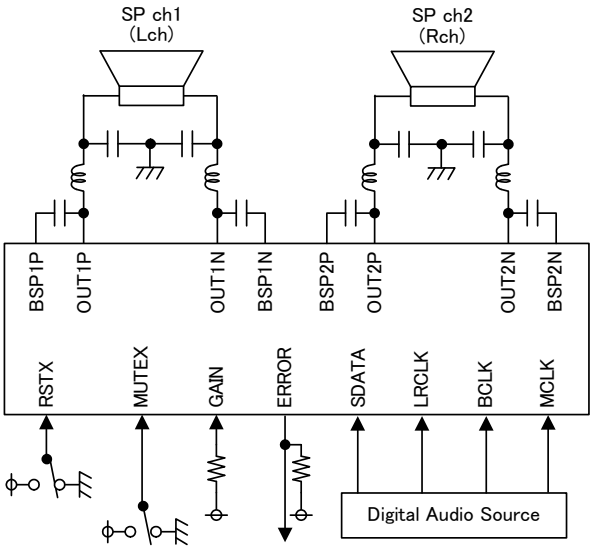


Figure 1. Typical Application Circuit

Pin Configuration

(TOP VIEW)

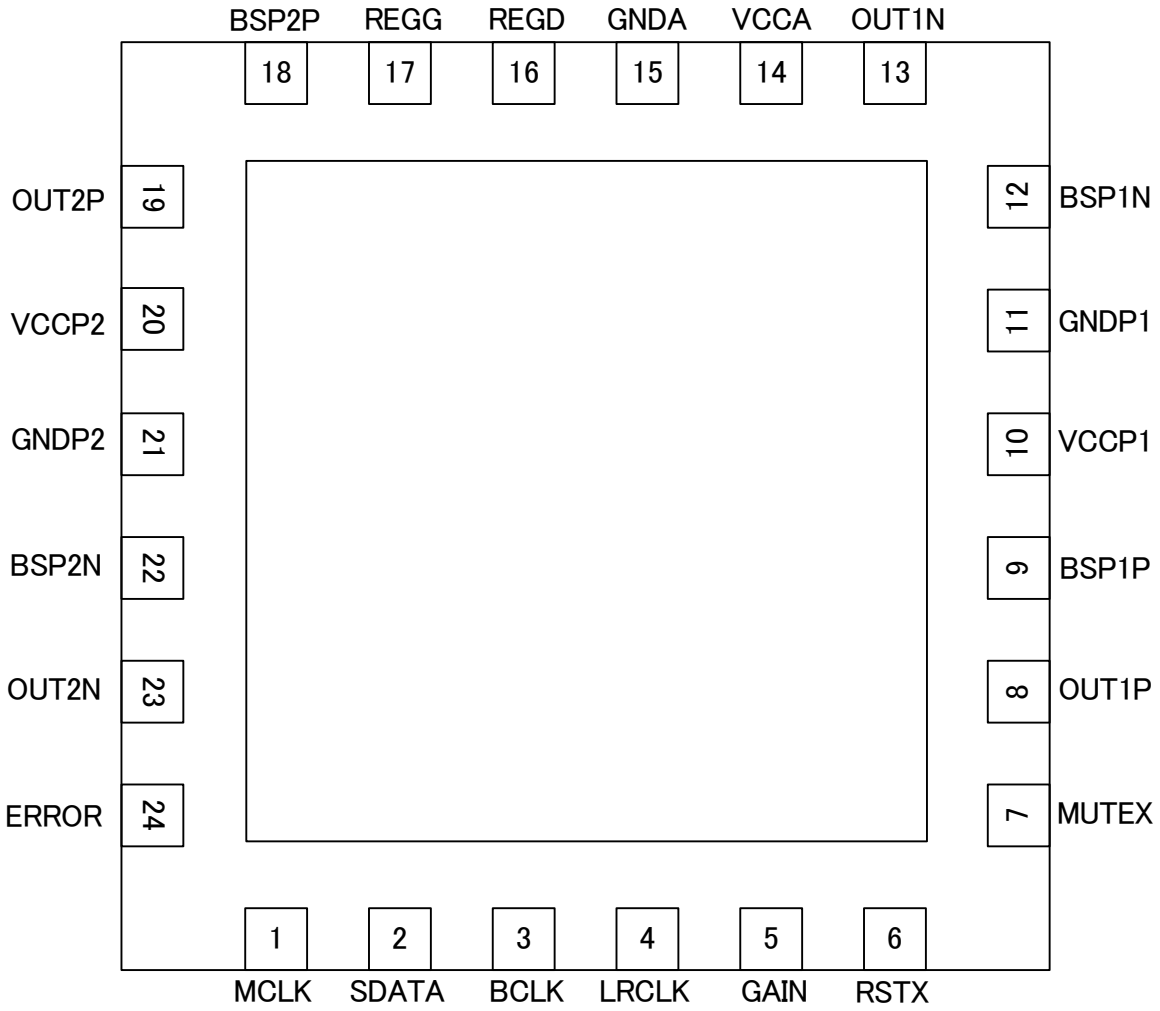
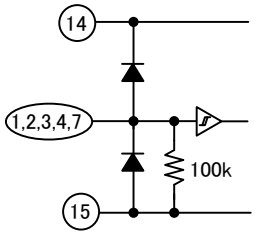
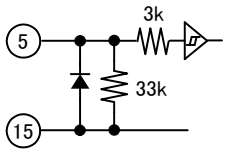
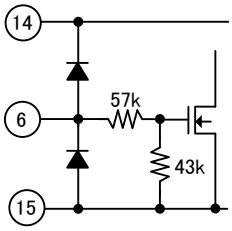
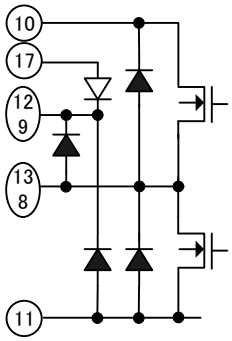
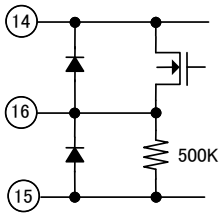
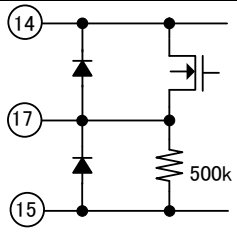
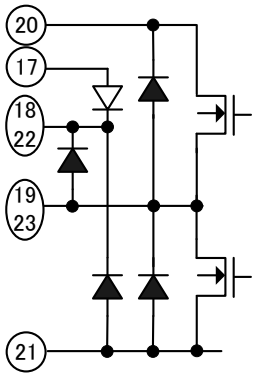
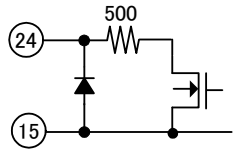


Figure 2. Pin Configuration

Pin Descriptions, I/O Equivalent Circuits (Provided pin voltages are typical values)

Pin No.	Pin Name	Pin Voltage	Pin Descriptions	Internal Equivalent Circuit
1 2 3 4	MCLK SDATA BCLK LRCLK	0V	Digital sound signal input pin	
7	MUTEX		Speaker output mute control pin H: Mute OFF L: Mute ON	
5	PLIMT	0V	Gain setting pin	
6	RSTX	0V	Reset pin H: Reset OFF L: Reset ON	
8	OUT1P	V_{CC} to 0V	Output pin of Ch1 positive PWM signal Please connect to output LPF. *If this pin is shorted to GND, the IC may be broken.	
9	BSP1P	-	Boot-strap pin of Ch1 positive PWM signal Please connect a capacitor to OUT1P.	
10	VCCP1	-	Power supply pin for Ch1 PWM signal Please connect a capacitor.	
11	GNDP1	0V	GND pin for Ch1 PWM signal	
12	BSP1N	-	Boot-strap pin of Ch1 negative PWM signal Please connect a capacitor to OUT1N.	
13	OUT1N	V_{CC} to 0V	Output pin of Ch1 negative PWM signal Please connect to output LPF. *If this pin is shorted to GND, the IC may be broken.	
14	VCCA	V_{CC}	Power supply pin for Analog signal Please connect a capacitor to GND.	–
15	GNDA	0V	GND pin for Analog signal	–
16	REGD	5.0V	Internal power supply pin for Digital circuit Please connect a capacitor to GND. *The REGD terminal of BD28623MUV should not be used as external supply. Therefore, don't connect anything except for the capacitor for stabilization.	

Pin Descriptions, I/O Equivalent Circuits – continued (Provided pin voltages are typical values)

Pin No.	Pin Name	Pin Voltage	Pint Descriptions	Internal Equivalent Circuit
17	REGG	5.7V	Internal power supply pin for Gate driver Please connect a capacitor to GND. *The REGG terminal of BD28623MUV should not be used as external supply. Therefore, don't connect anything except for the capacitor for stabilization.	
18	BSP2P	-	Boot-strap pin of Ch2 positive PWM signal Please connect a capacitor to OUT2P.	
19	OUT2P	V_{CC} to 0V	Output pin of Ch2 positive PWM signal Please connect to output LPF. *If this pin is shorted to GND, the IC may be broken.	
20	VCCP2	V_{CC}	Power supply pin for Ch2 PWM signal Please connect a capacitor to GND.	
21	GNDP2	0V	GND pin for Ch2 PWM signal	
22	BSP2N	-	Boot-strap pin of Ch2 negative PWM signal Please connect a capacitor to OUT2N.	
23	OUT2N	V_{CC} to 0V	Output pin of Ch2 negative PWM signal Please connect to output LPF. *If this pin is shorted to GND, the IC may be broken.	
24	ERROR	-	Error flag pin Please connect pull-up resistor. H: Normal L: Error *An error flag is outputted when Output Short Protection, DC Voltage Protection in the speaker, and High Temperature Protection are operated. This flag shows IC condition during operation.	

The numerical value of internal equivalent circuit is typical value, not guaranteed value.

Block Diagram

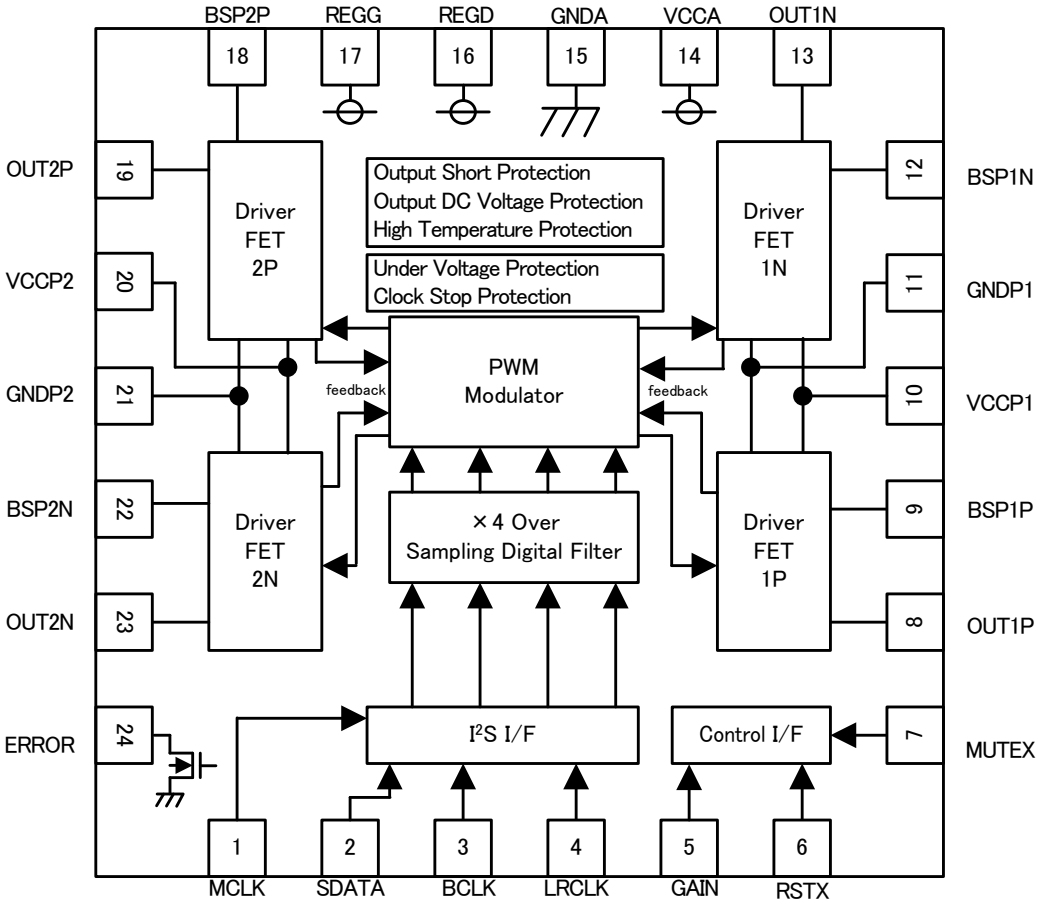


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit	Conditions
Supply Voltage (Note 1) (Note 2)	V_{CCMAX}	-0.3 to +30	V	Pin10, 14, 20
Power Dissipation	Pd	2.21 (Note 3)	W	Please refer to Power Dissipation for details.
		3.56 (Note 4)		
Input Voltage1 (Note 1)	V_{IN1}	-0.3 to +3.7	V	Pin1-7
Terminal Voltage 1 (Note 1)	V_{PIN1}	-0.3 to +7	V	Pin16, 17
Terminal Voltage 2 (Note 1) (Note 5-1)	V_{PIN2}	-0.3 to +V_{CC}	V	Pin8, 13, 19, 23
Terminal Voltage 3 (Note 1) (Note 5-2)	V_{PIN3}	-0.3 to OUTxx+7	V	Pin9, 12, 18, 22
Open-drain Terminal Voltage (Note 1)	V_{ERR}	-0.3 to +V_{CCMAX}	V	Pin24
Operating Temperature Range	Topr	-25 to +85	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	
Maximum Junction Temperature	Tjmax	+150	°C	

(Note 1) Voltage that can be applied with reference to GND (Pin11, 15, 21).
(Note 2) Pd and Tjmax=150°C must not be exceeded.
(Note 3) 74.2mm×74.2mm×1.6mm, FR4, 4-layer glass epoxy board
(Top and bottom layer back copper foil size: 20.2mm^2, 2nd and 3rd layer back copper foil size: 5505mm^2)
Derate by 17.7mW/°C when operating above Ta=25°C. The board is provided with thermal via.
(Note 4 74.2mm×74.2mm×1.6mm, FR4, 4-layer glass epoxy board
(Top and bottom layer back copper foil size: 5505mm^2)
Derate by 28.5mW/°C when operating above Ta=25°C. The board is provided with thermal via.
(Note 5-1) The chip should be used within AC peak limits at all conditions. Overshoot should be ≤30V with reference to GND.
Undershoot should be ≤10nsec and ≤30V with reference to V_{CC}. (Please refer to figure 4-1.)
(Note 5-2) The chip should be used within AC peak limits at all conditions. Overshoot should be ≤OUTxx+7V with reference to OUTxx.
Undershoot should be ≤10nsec and ≤OUTxx+7V with reference to OUTxx. (Please refer to figure 4-2.)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

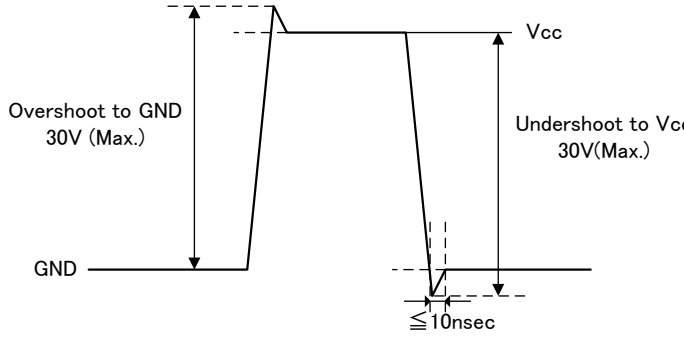


Figure 4-1

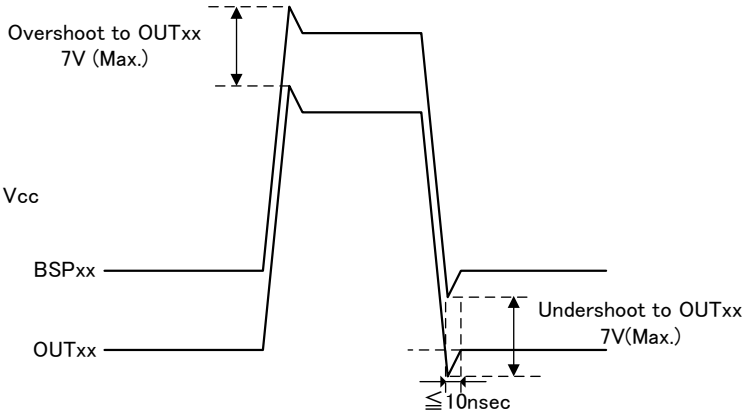


Figure 4-2

Recommended Operating Conditions

Parameter	Symbol	Limit	Unit	Conditions
Supply Voltage (Note 1) (Note 2)	V_{CC}	8.5 to 24	V	Pin10, 14, 20
Minimum Load Impedance (Note 6)	R_L	6.4	Ω	21V < V_{CC} ≤ 24V
		4.8		14V < V_{CC} ≤ 21V
		3.6		V_{CC} ≤14V

(Note 6) Pd should not be exceeded.

Electrical Characteristics

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω, RSTX=3.3V, MUTEX=3.3V, Gain= 20dB, f_S=48kHz, MCLK=256f_S, Output LC filter: L=10μH, C=0.68μF, Without Snubber circuit)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Total Circuit						
Circuit Current (Reset Mode)	I_{CC1}	-	33	200	μA	No load, RSTX=0V, MUTEX=0V
Circuit Current (Mute Mode)	I_{CC2}	-	15	25	mA	No load, RSTX=3.3V, MUTEX=0V
Circuit Current (Active Mode)	I_{CC3}	-	40	80	mA	No load, RSTX=3.3V, MUTEX=3.3V
Open-drain Terminal Low Level Voltage	V_{ERR}	-	-	0.8	V	I_O=0.5mA
Regulator Output Voltage 1	V_{REGG}	4.6	5.7	6.5	V	RSTX=3.3V, MUTEX=3.3V
Regulator Output Voltage 2	V_{REGD}	4.2	5.0	5.7	V	RSTX=3.3V, MUTEX=3.3V
High level Input Voltage 1	V_{IH1}	2.2	-	3.3	V	Pin1-4,6-7
Low level Input Voltage 1	V_{IL1}	0	-	0.8	V	Pin1-4,6-7
High level Input Voltage 2	V_{IH2}	2.6	-	3.3	V	Pin5
Low level Input Voltage 2	V_{IL2}	0	-	0.45	V	Pin5
Input Current1 (Input Pull-down Terminal)	I_{IH}	27.5	33	42	μA	V_{IN} = 3.3V, Pin1-4,6-7
]Input Current2 (Input Pull-down Terminal)	I_{IH2}	65	100	135	μA	V_{IN} = 3.3V, Pin5
Speaker Parts						
Maximum Output Power 1(Note 7)	P_{O1}	-	15	-	W	V_{CC}=16V, THD+N=10%, GAIN=26dB
Maximum Output Power 2(Note 7)	P_{O2}	10	12.5	-	W	V_{CC}=16V, THD+N<10%, GAIN=20dB
Maximum Output Power 3(Note 7)	P_{O3}	5	6.3	-	W	V_{CC}=16V, THD+N<10%, GAIN=17dB
Voltage Gain1(Note 7)	G_{V26}	25	26	27	dB	P_O=1W, GAIN=H
Voltage Gain2(Note 7)	G_{V20}	19	20	21	dB	P_O=1W , GAIN=Pull up(47kΩ)
Voltage Gain3(Note 7)	G_{V17}	16	17	18	dB	P_O=1W, GAIN=L
Total Harmonic Distortion1(Note 7)	THD_1	-	0.08	-	%	V_{CC}=12V, P_O=1W BW=20 to 20kHz (AES17) GAIN=20dB, With snubber circuit
Crosstalk (Note 7)	CT	60	90	-	dB	P_O=1W, 1kHz BPF, GAIN=20dB
PSRR (Note 7)	PSRR	-	60	-	dB	V_{ripple}=1V_{rms}, f=1kHz, GAIN=20dB
Output Noise Voltage (Note 7)	V_{NO}	-	150	250	μV_{rms}	Input=-∞dBFS, BW=IHF-A, GAIN=20dB
PWM (Pulse Width Modulation) Frequency	f_{PWM}	-	512	-	kHz	f_S=32kHz
		-	705.6	-	kHz	f_S=44.1kHz
		-	768	-	kHz	f_S=48kHz

(Note 7) The rated values of items above indicate average performances of the device, which largely depend on circuit layouts, components, and power supplies. The reference values are those applicable to the device and components directly installed on a board specified by ROHM during testing.

Typical Performance Curves (1/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, Gain=26dB, ROHM 4-layer Board)

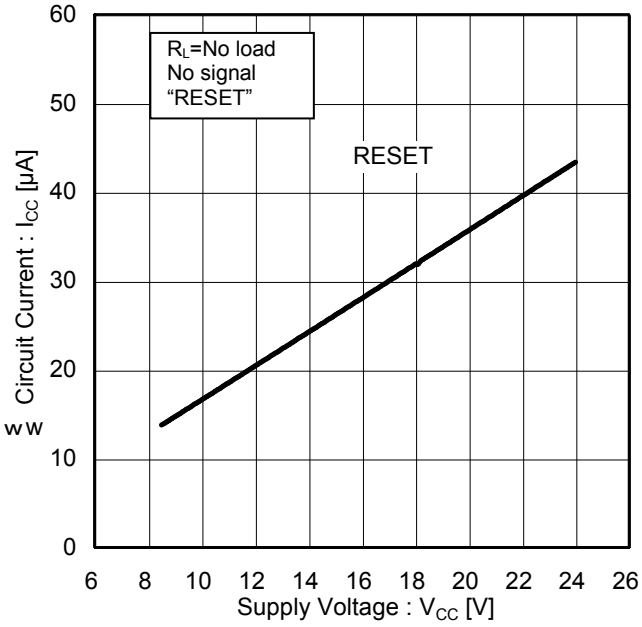


Figure 5. Circuit Current vs Supply Voltage (RESET)

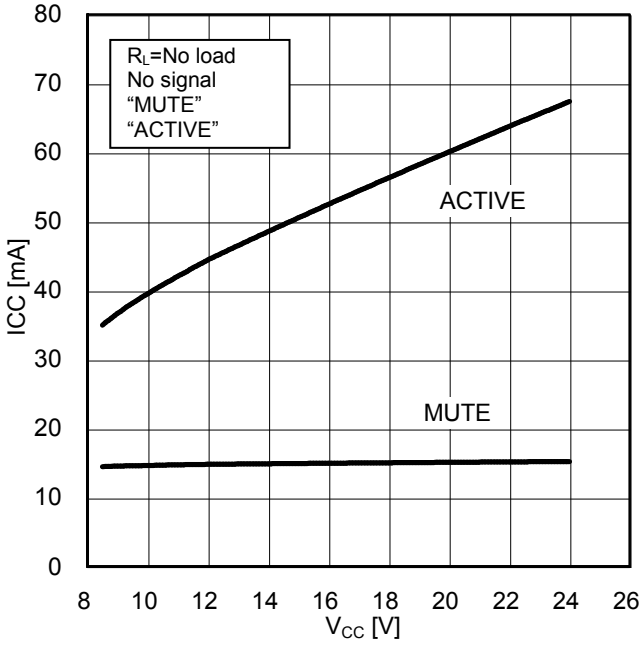


Figure 6. Circuit Current vs Supply Voltage (MUTE, ACTIVE)

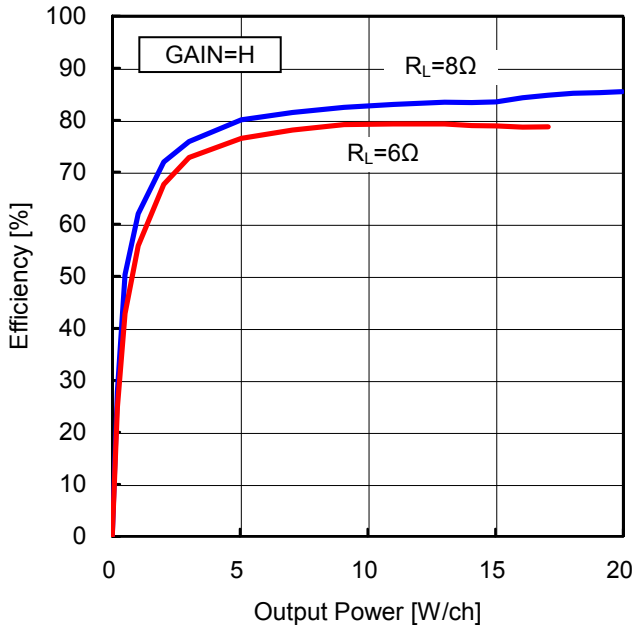


Figure 7. Efficiency vs Output Power (8Ω, 6Ω)

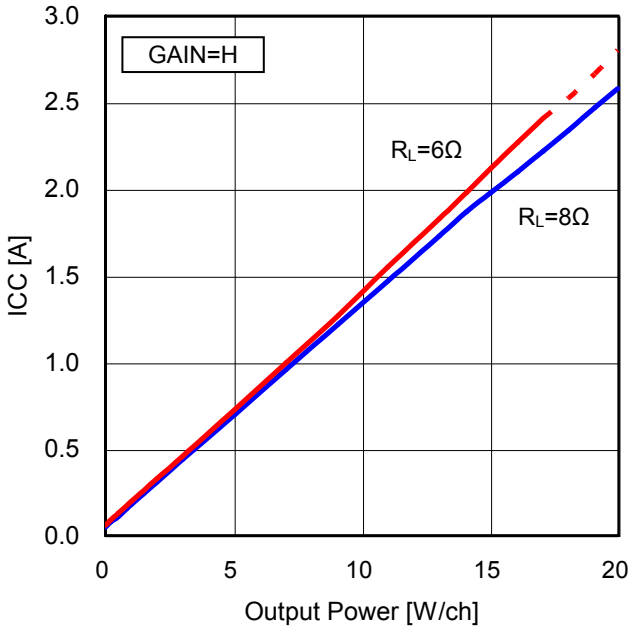


Figure 8. Circuit Current vs Output Power (8Ω, 6Ω)

※ Dotted line means power dissipation is exceeded.

Typical Performance Curves – continued (2/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, Gain=20dB, ROHM 4-layer Board)

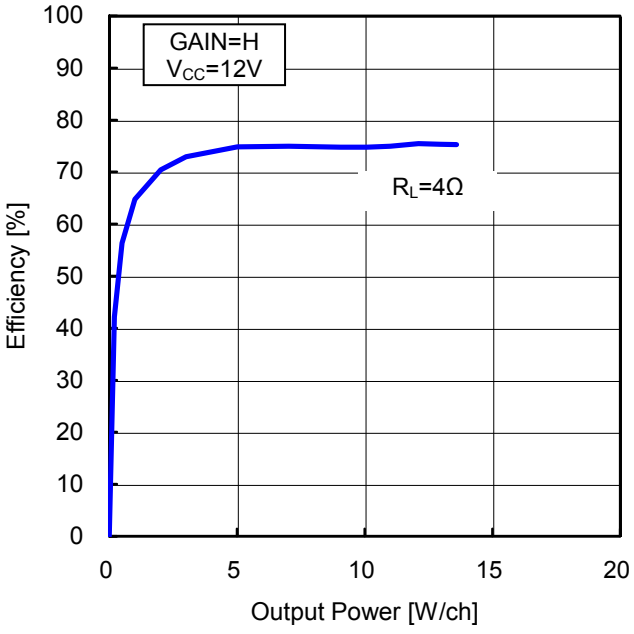


Figure 9. Efficiency vs Output Power (4Ω)

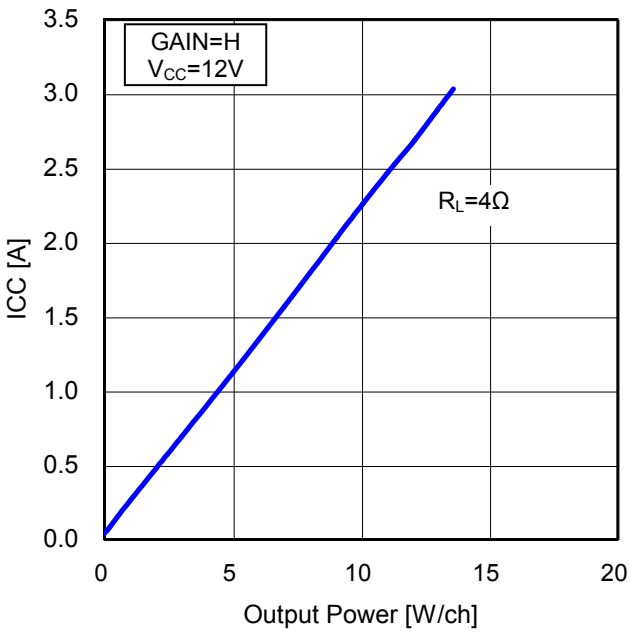


Figure 10. Circuit Current vs Output Power (4Ω)

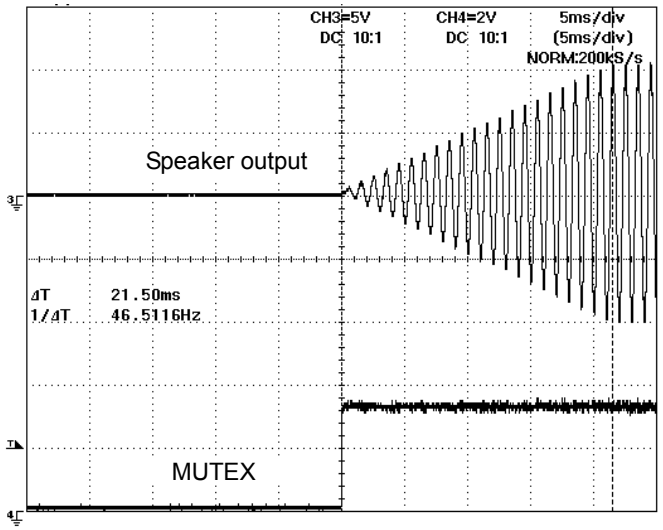


Figure 11. Waveform of Soft Start

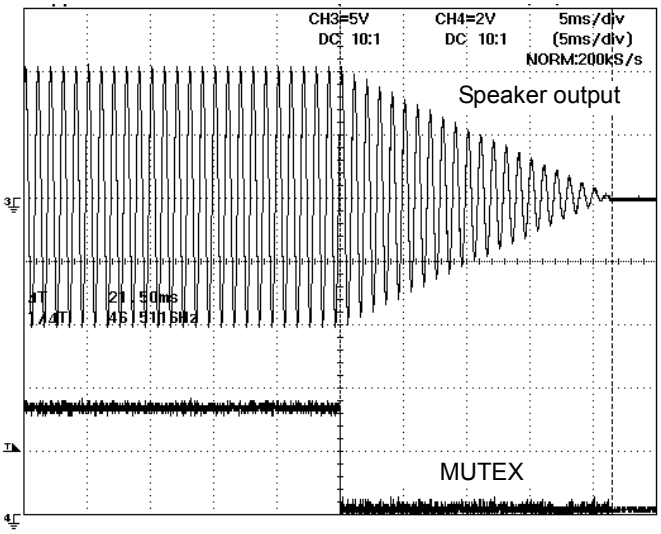


Figure 12. Waveform of Soft Mute

Typical Performance Curves - continued (3/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, Gain=26dB, ROHM 4-layer Board)

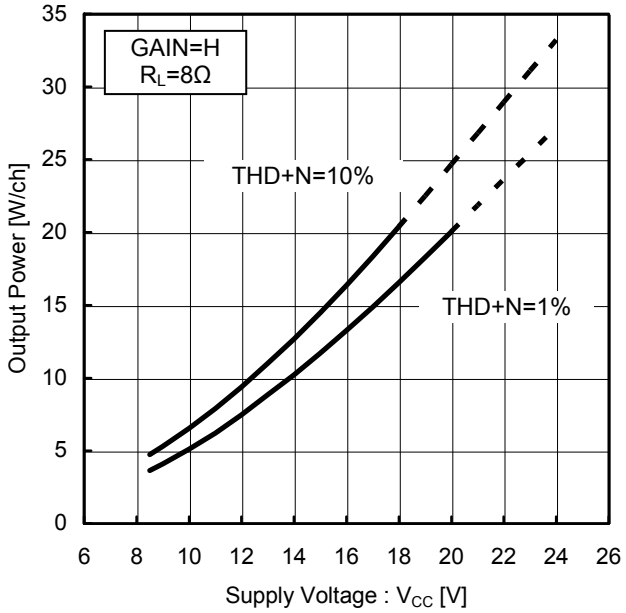


Figure 13. Output Power vs Supply Voltage (8Ω)

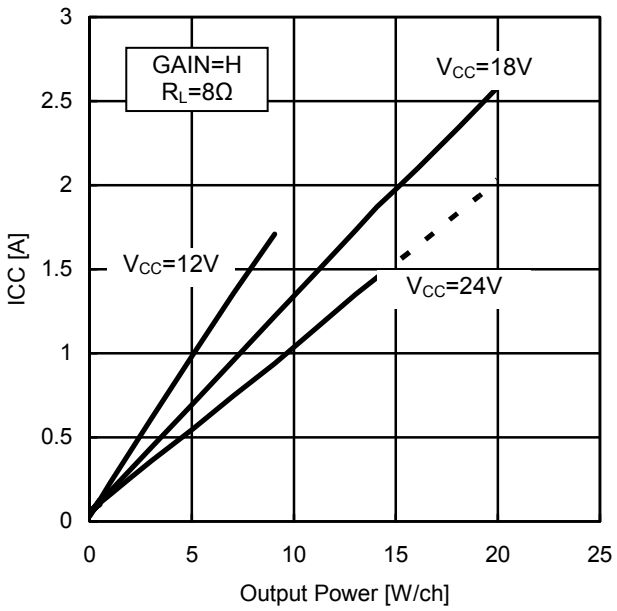


Figure 14. Circuit Current vs Output Power (8Ω)

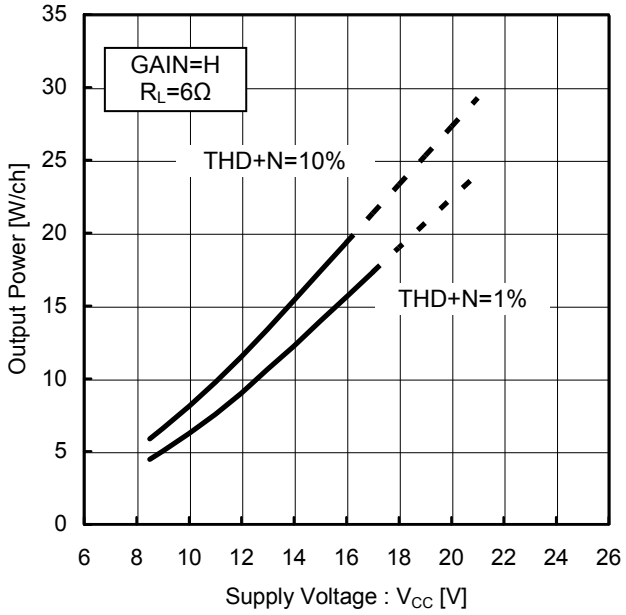


Figure 15. Output Power vs Supply Voltage (6Ω)

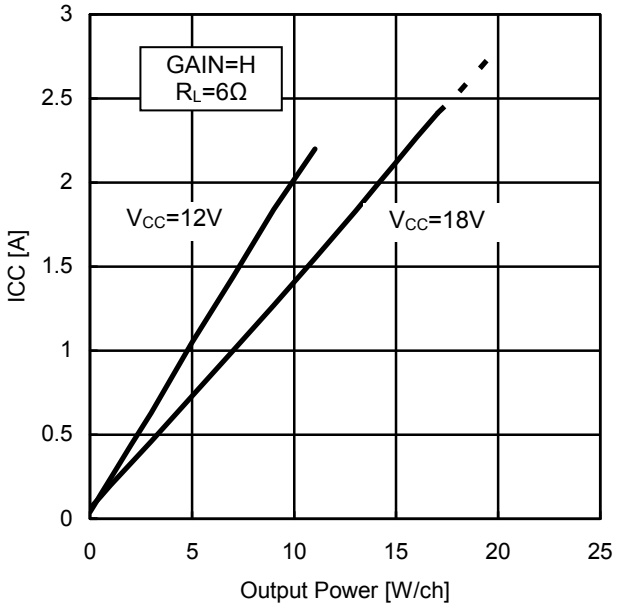


Figure 16. Circuit Current vs Output Power (6Ω)

※ Dotted line means power dissipation is exceeded.

Typical Performance Curves - continued (4/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, Gain=20dB, ROHM 4-layer Board)

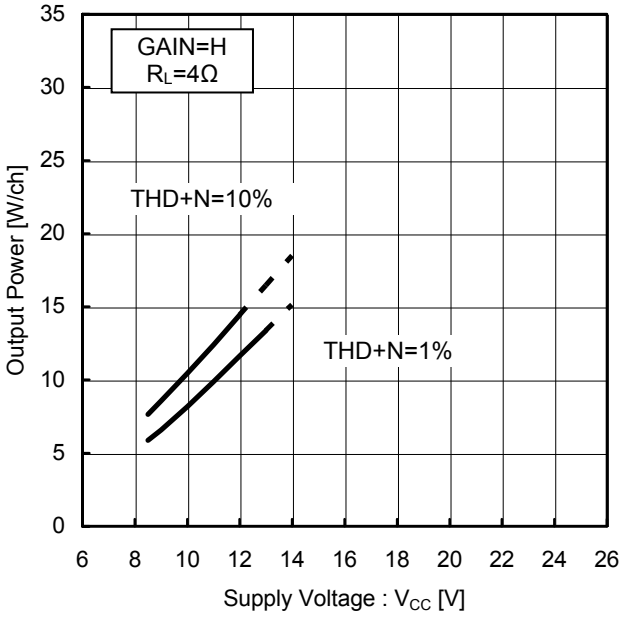


Figure 17. Output Power vs Supply Voltage (4Ω)

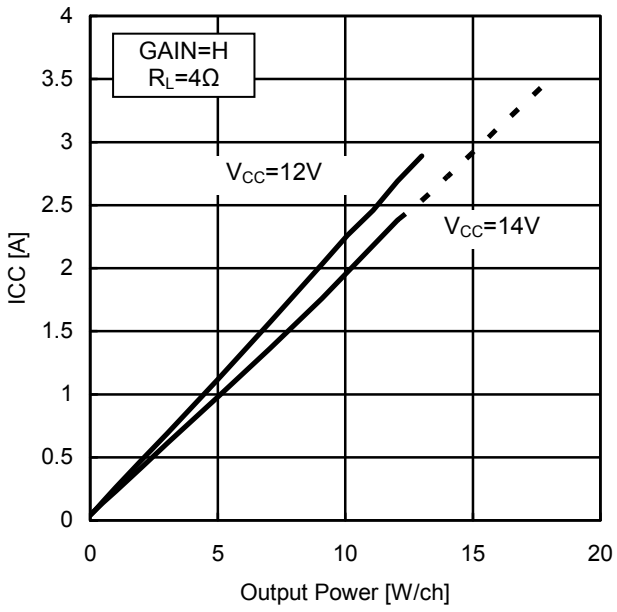


Figure 18. Circuit Current vs Output Power (4Ω)

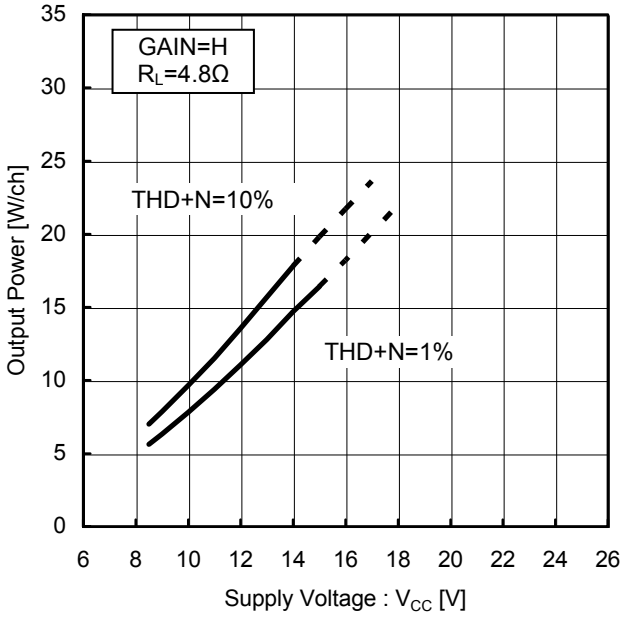


Figure 19. Output Power vs Supply Voltage (4.8Ω)

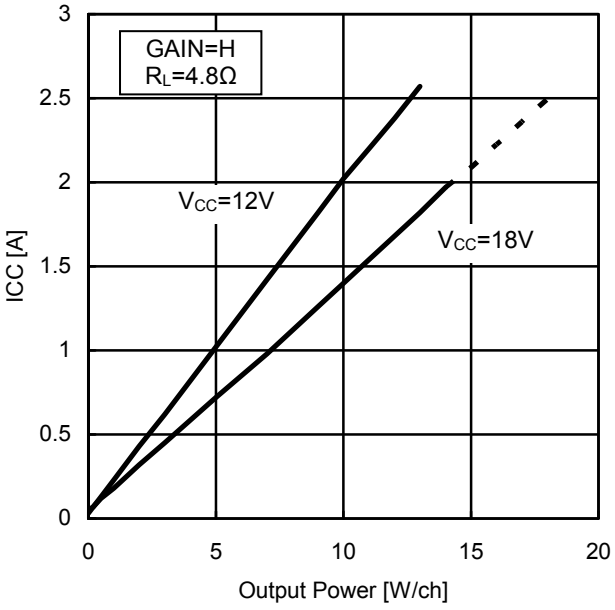


Figure 20. Circuit Current vs Output Power (4.8Ω)

※ Dotted line means power dissipation is exceeded.

Typical Performance Curves - continued (5/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, Gain=20dB, ROHM 4-layer Board)

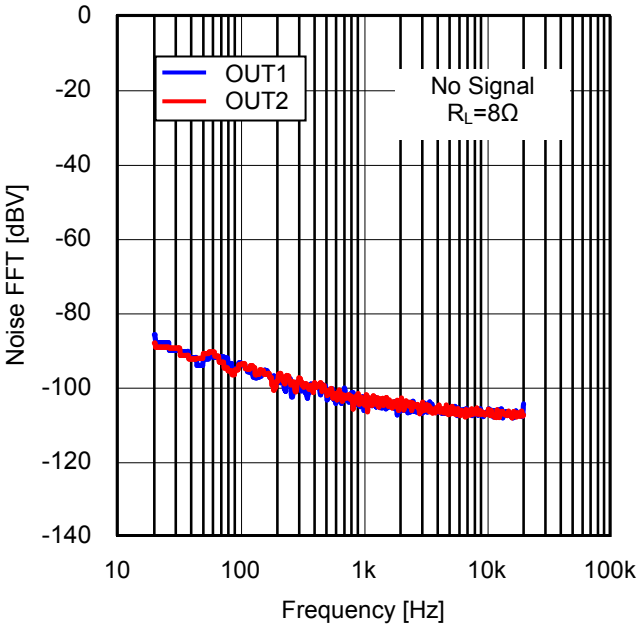


Figure 21. FFT of output noise voltage (8Ω)

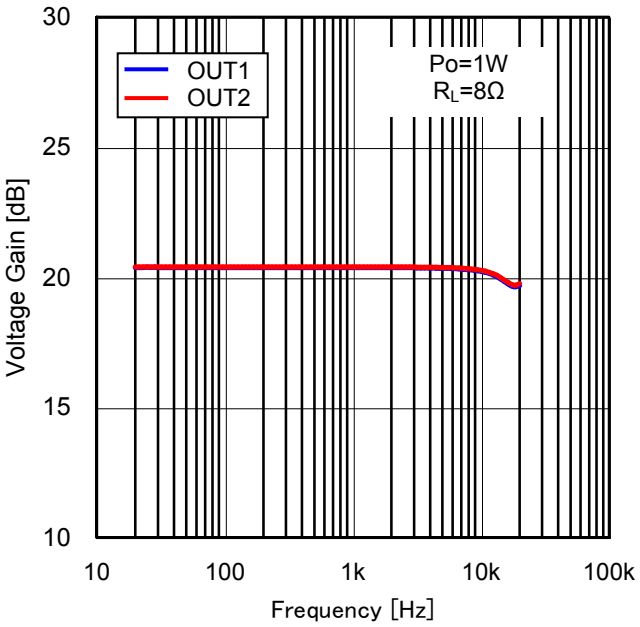


Figure 22. Voltage Gain vs Frequency (8Ω)

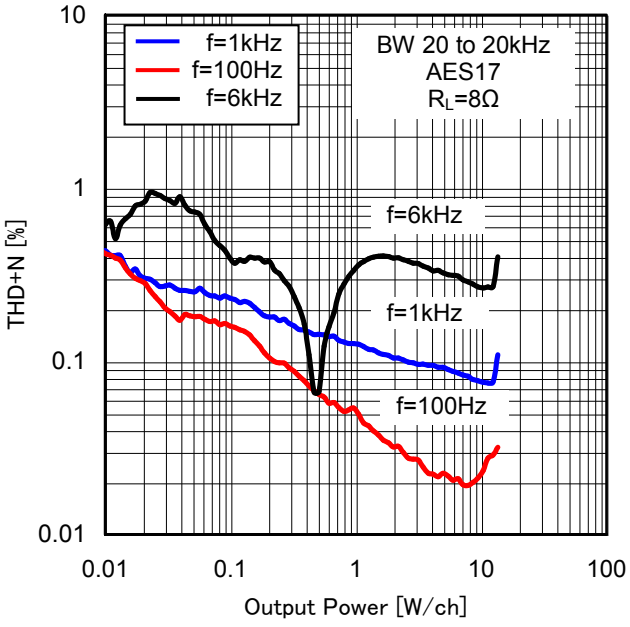


Figure 23. THD+N vs Output Power (8Ω)

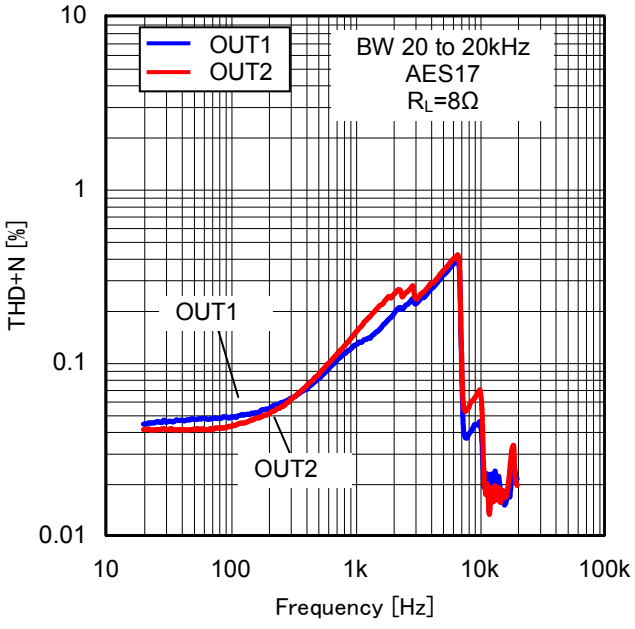


Figure 24. THD+N vs Frequency (8Ω)

Typical Performance Curves - continued (6/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L= 8Ω/6Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, Gain=20dB, ROHM 4-layer Board)

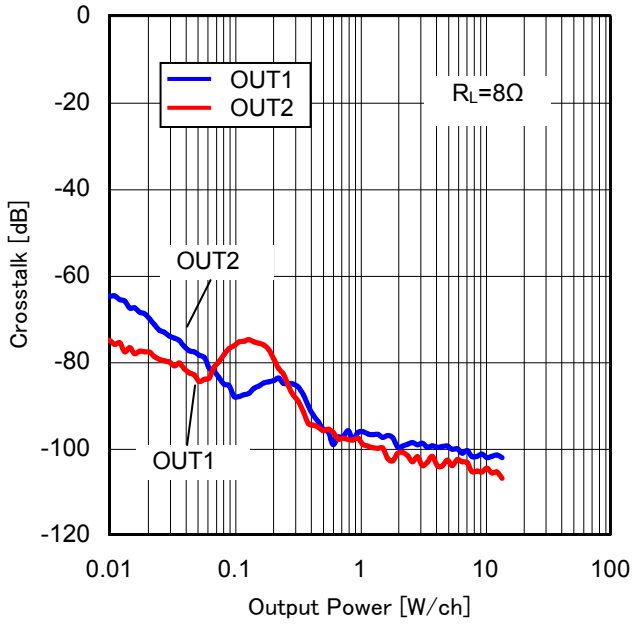


Figure 25. Crosstalk vs Output Power (8Ω)

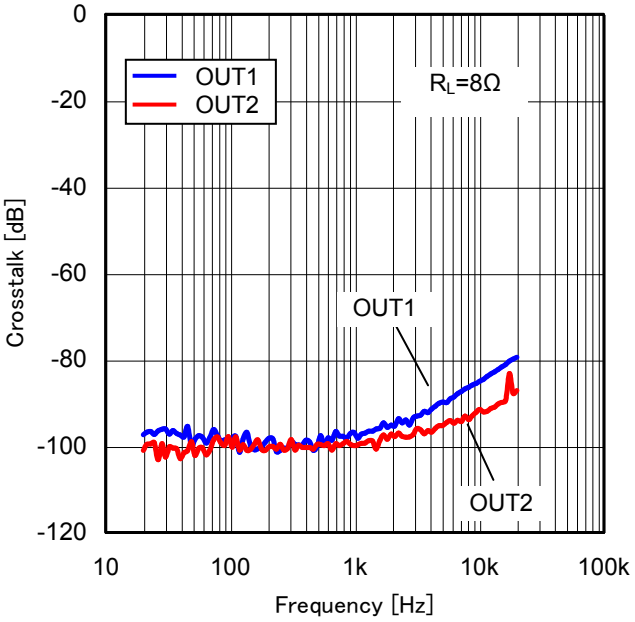


Figure 26. Crosstalk vs Frequency (8Ω)

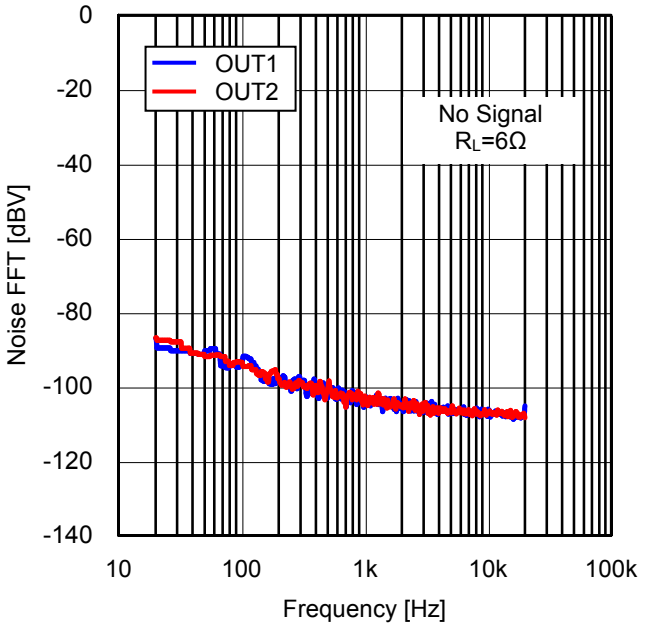


Figure 27. FFT of output noise voltage (6Ω)

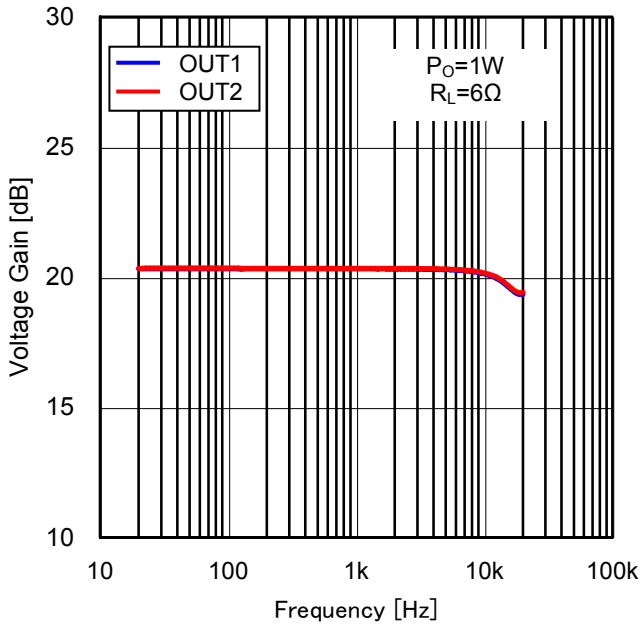


Figure 28. Voltage Gain vs Frequency (6Ω)

Typical Performance Curves – continued (7/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=6Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, Gain=20dB, ROHM 4-layer Board)

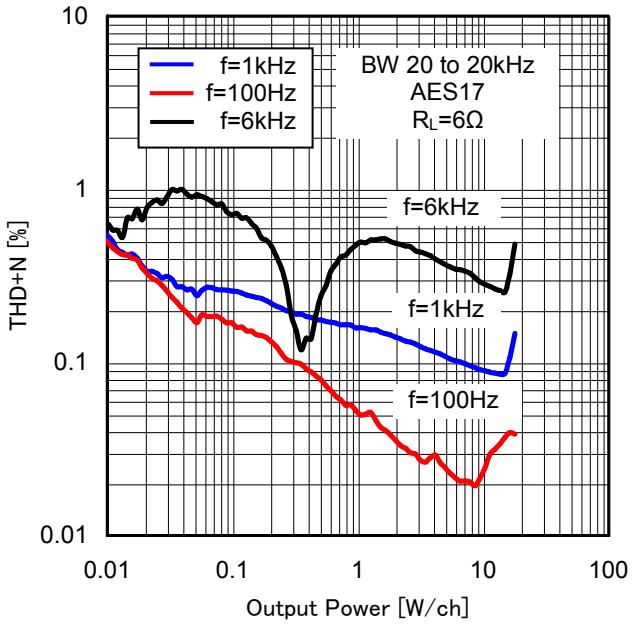


Figure 29. THD+N vs Output Power (6Ω)

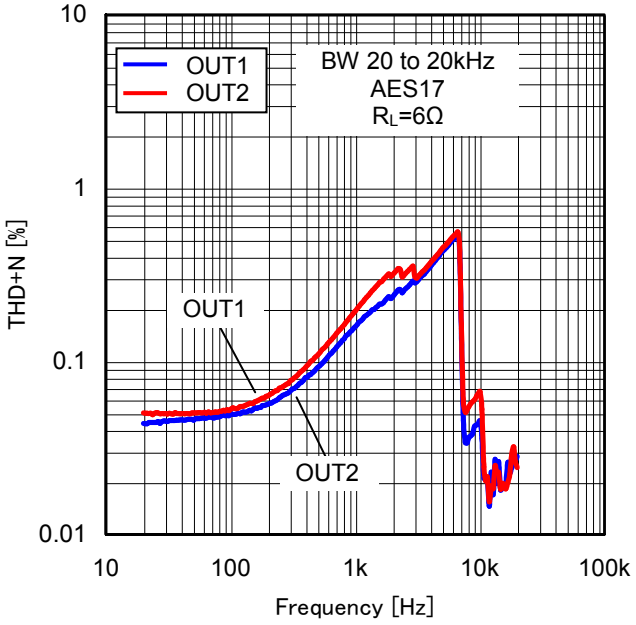


Figure 30. THD+N vs Frequency (6Ω)

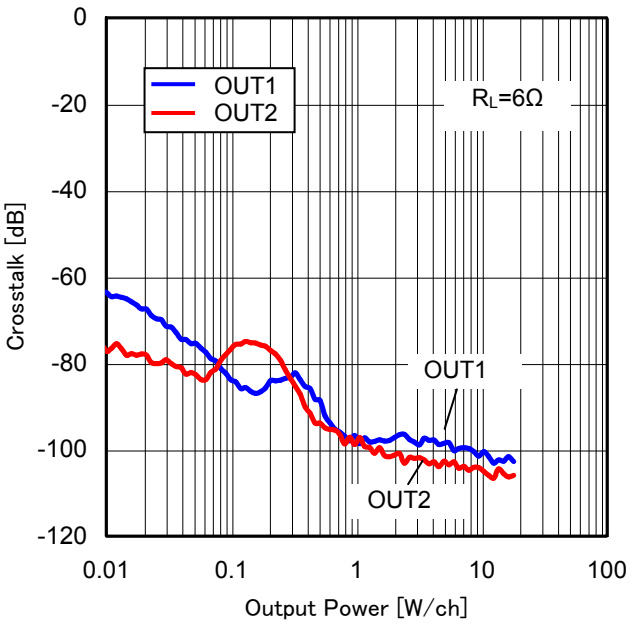


Figure 31. Crosstalk vs Output Power (6Ω)

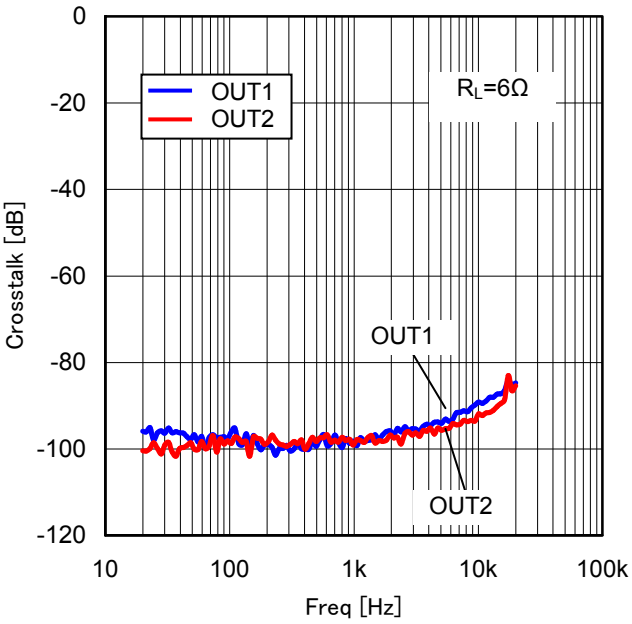


Figure 32. Crosstalk vs Frequency (6Ω)

Typical Performance Curves – continued (8/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=12V, f=1kHz, R_L=4Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, Gain=20dB, ROHM 4-layer Board)

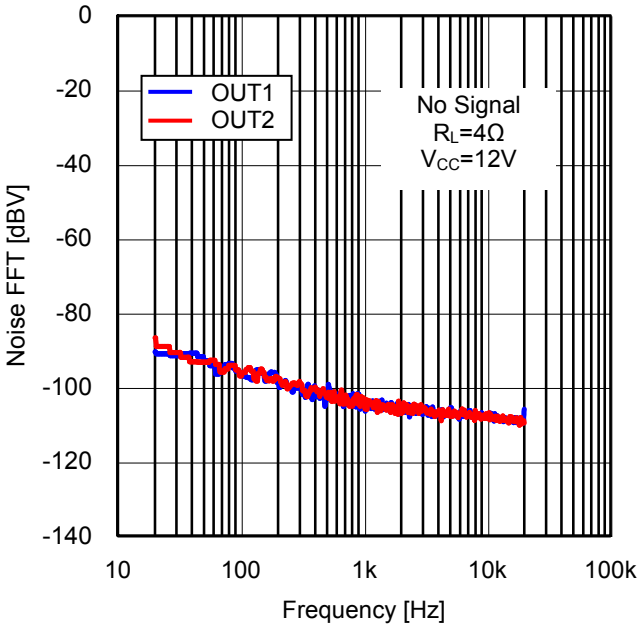


Figure 33. FFT of output noise voltage (4Ω)

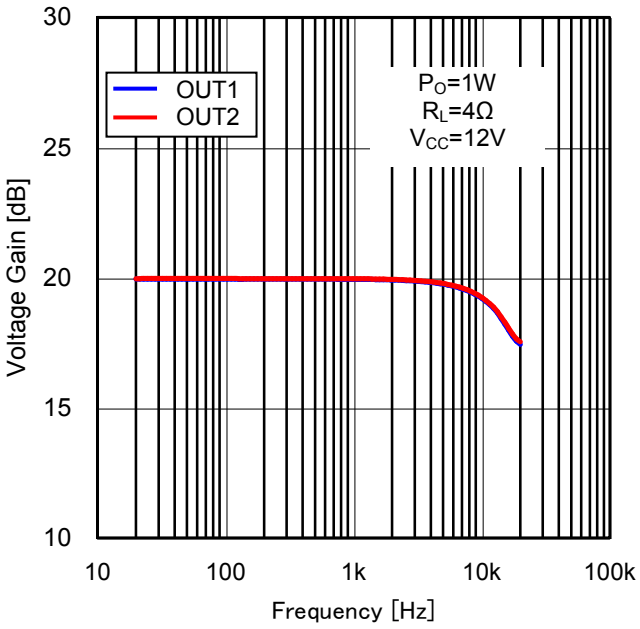


Figure 34. Voltage Gain vs Frequency (4Ω)

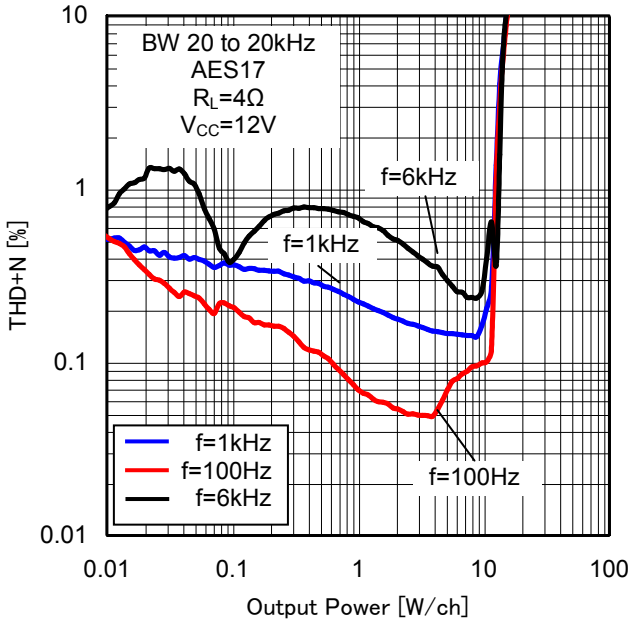


Figure 35. THD+N vs Output Power (4Ω)

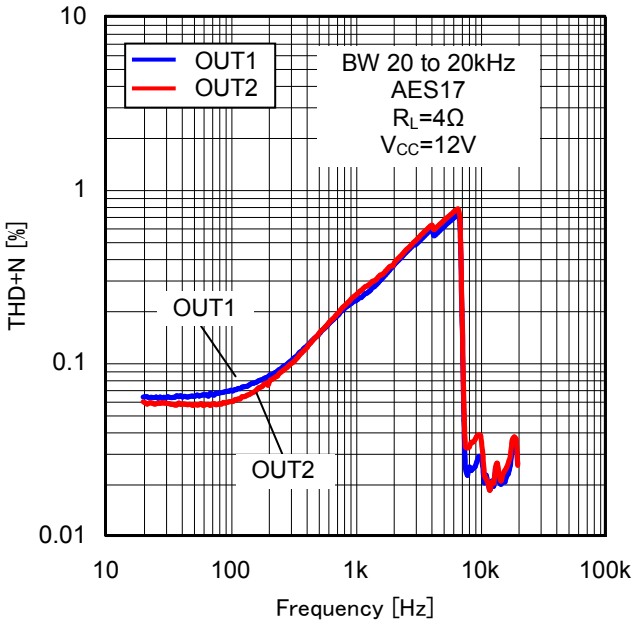


Figure 36. THD+N vs Frequency (4Ω)

Typical Performance Curves - continued (9/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L= 4Ω/4.8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, Gain=20dB, ROHM 4-layer Board)

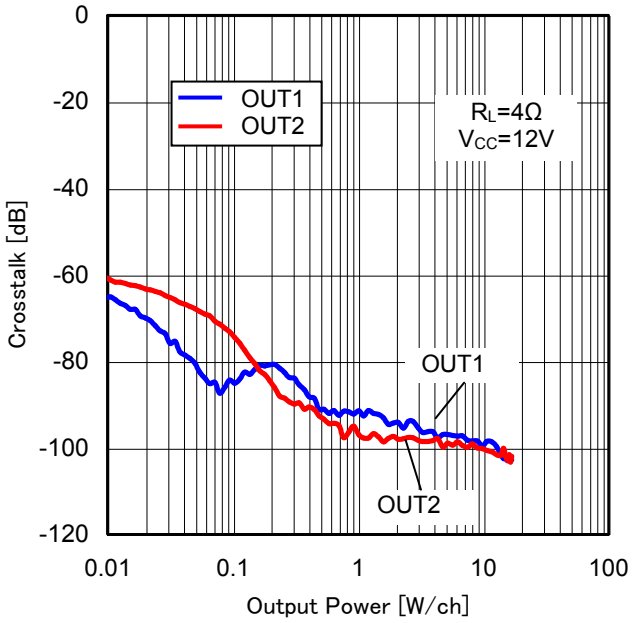


Figure 37. Crosstalk vs Output Power (4Ω)

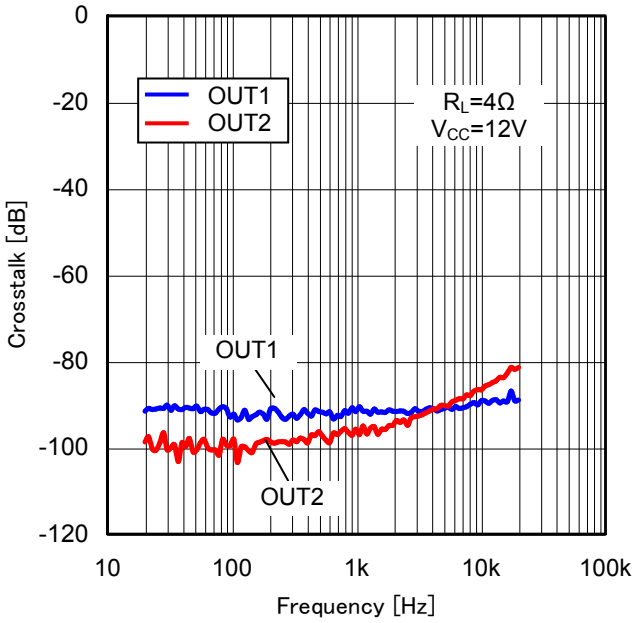


Figure 38. Crosstalk vs Frequency (4Ω)

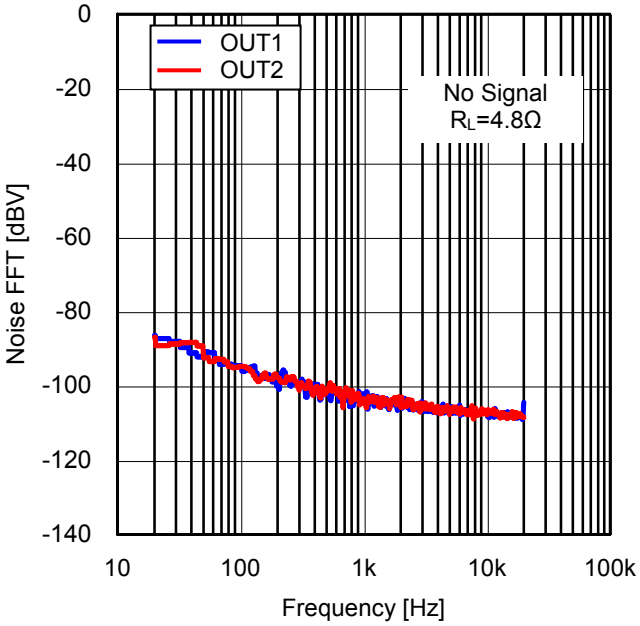


Figure 39. FFT of output noise voltage (4.8Ω)

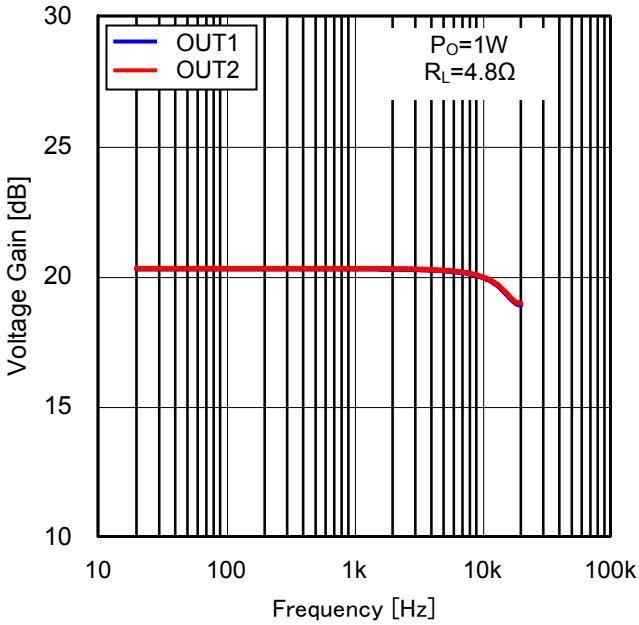


Figure 40. Voltage Gain vs Frequency (4.8Ω)

Typical Performance Curves – continued (10/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=4.8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, Gain=20dB, ROHM 4-layer Board)

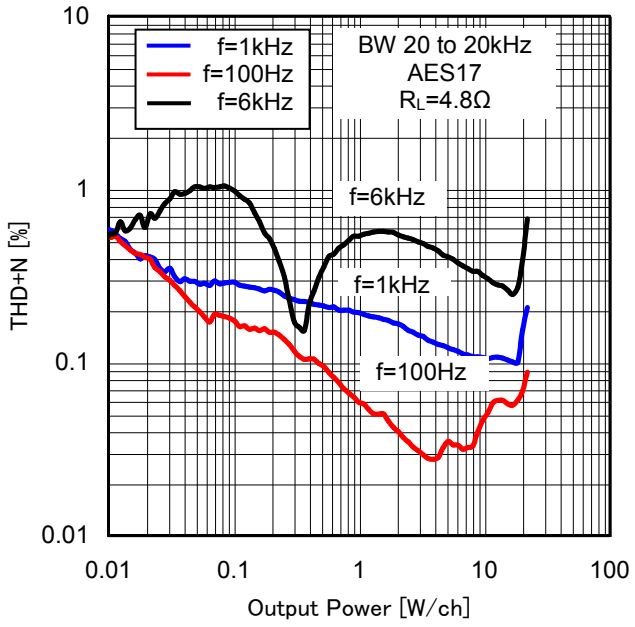


Figure 41. THD+N vs Output Power (4.8Ω)

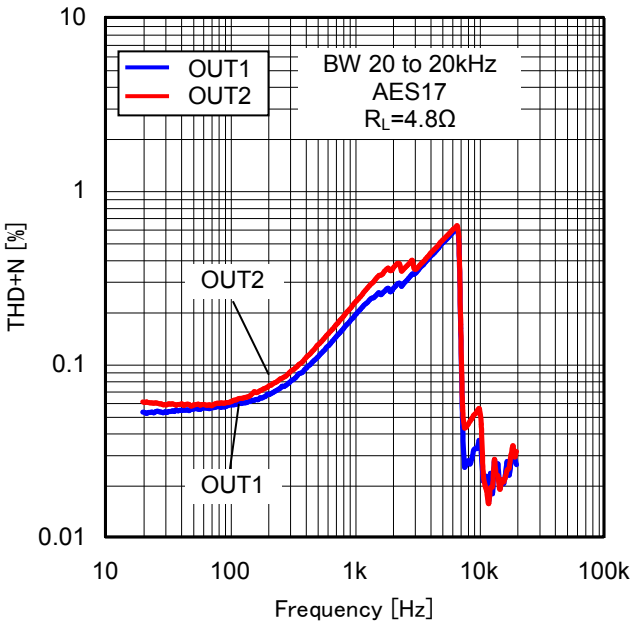


Figure 42. THD+N vs Frequency (4.8Ω)

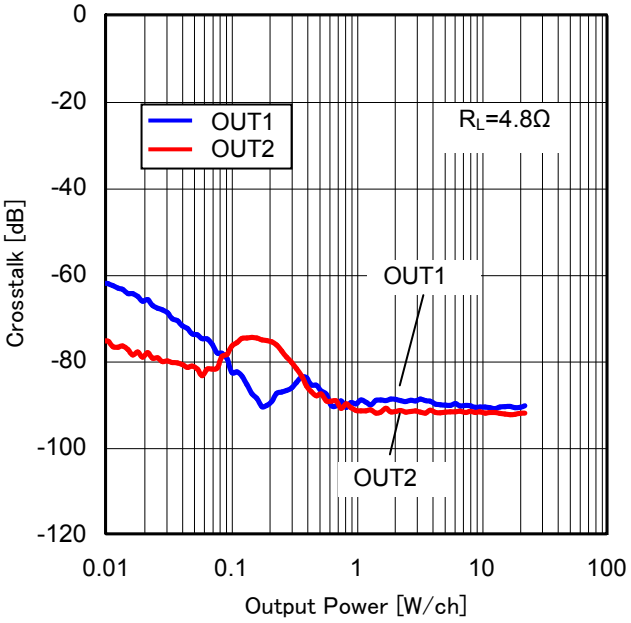


Figure 43. Crosstalk vs Output Power (4.8Ω)

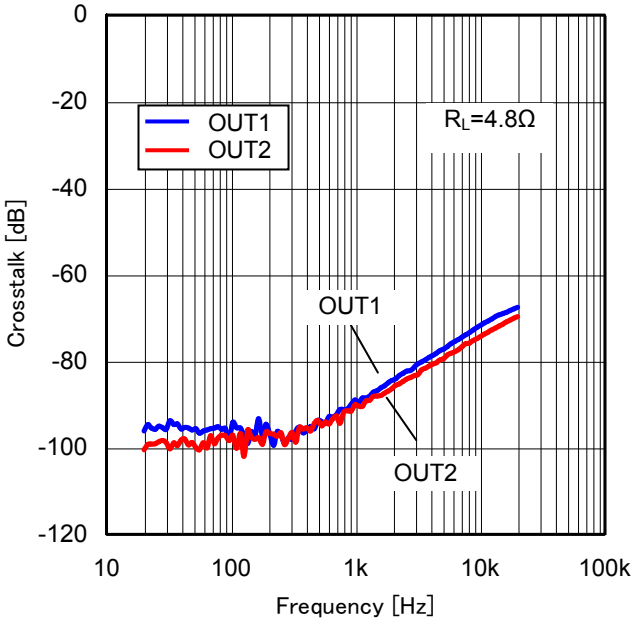


Figure 44. Crosstalk vs Frequency (4.8Ω)

Typical Performance Curves – continued (11/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω/6Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, ROHM 4-layer Board)

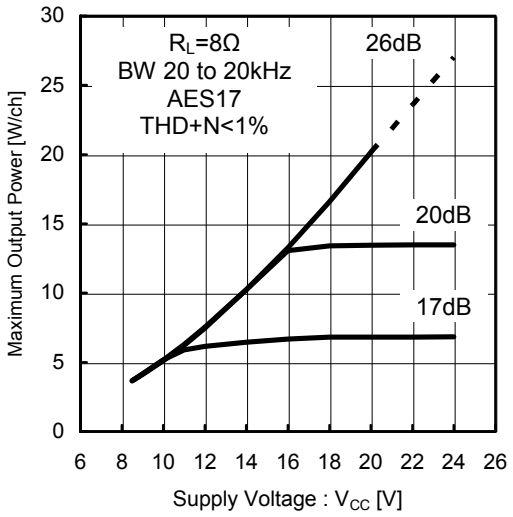


Figure 45. Supply Voltage vs Maximum Output Power (8Ω)

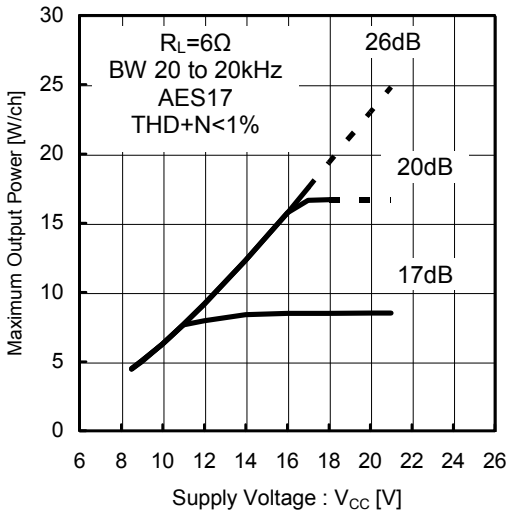


Figure 46. Supply Voltage vs Maximum Output Power (6Ω)

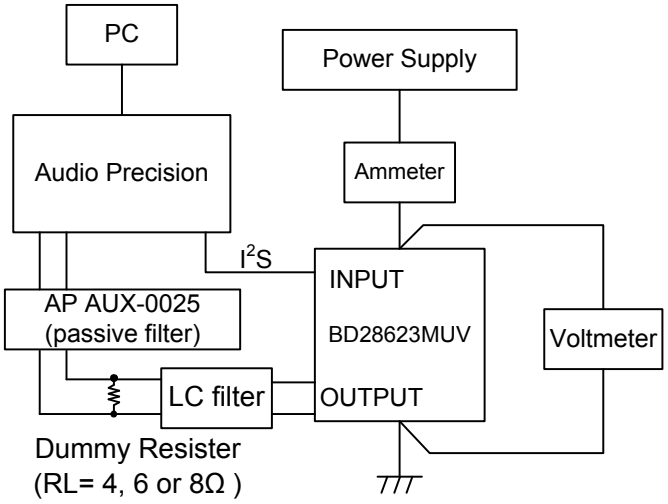


Figure 47. Audio Characteristics Measurement Environment

※ Dotted line means power dissipation is exceeded.

Timing Chart

1. Power Supply Start-up Sequence

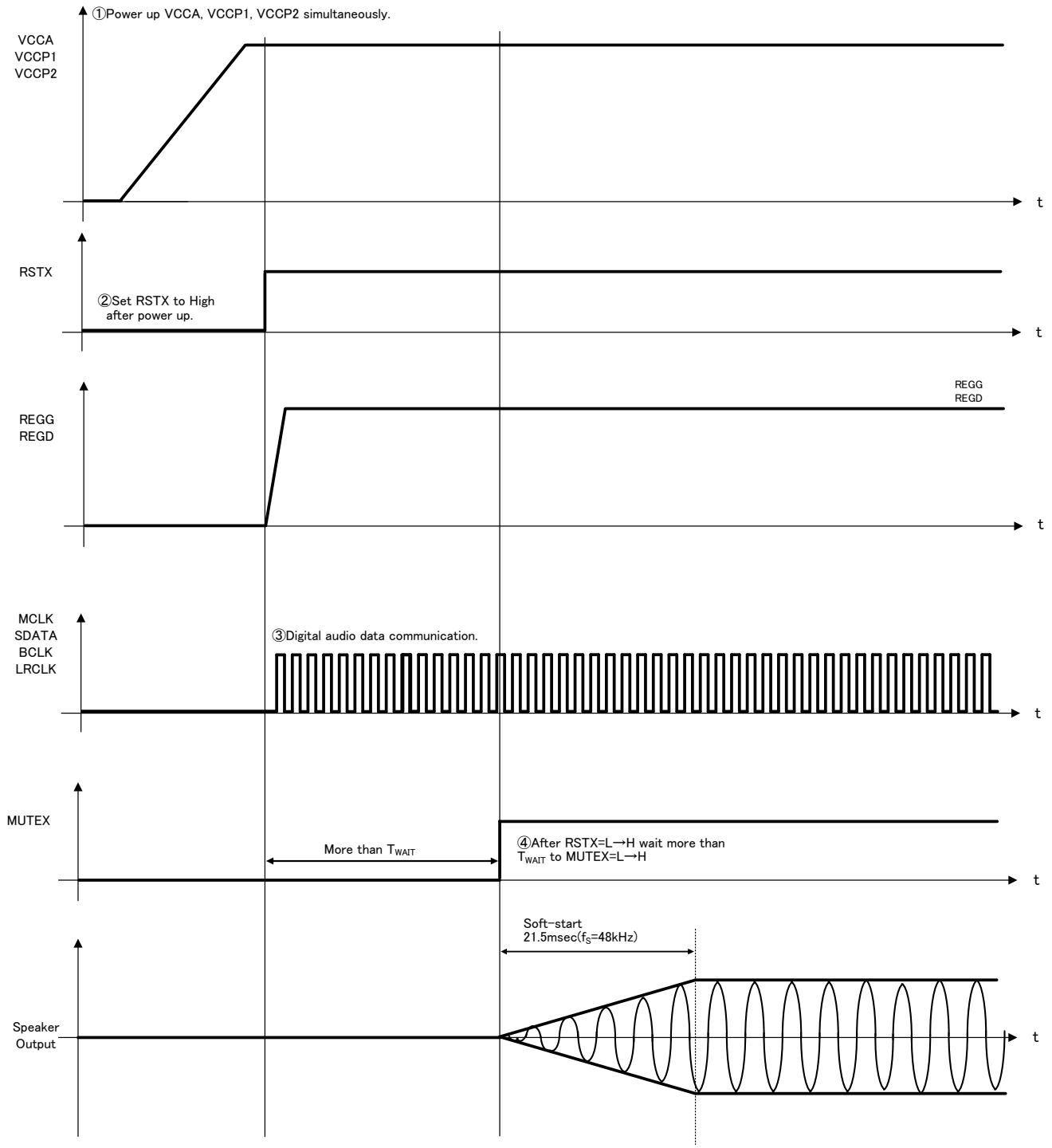


Figure 48. Power Supply Start-up Sequence

Caution: To eliminate pop noise when power supply is turned ON, RSTX and MUTEX should always be set Low. And also, all power supply terminals should start up together.
Order of ② and ③ can be interchange

BSP Capacitor Value (C9, C12, C19, C22)	Limit of T_{WAIT}			Unit
	Min	Typ	Max	
3.3μF	300	-	-	msec
4.7μF	400	-	-	msec

2. Power Supply Shutdown Sequence

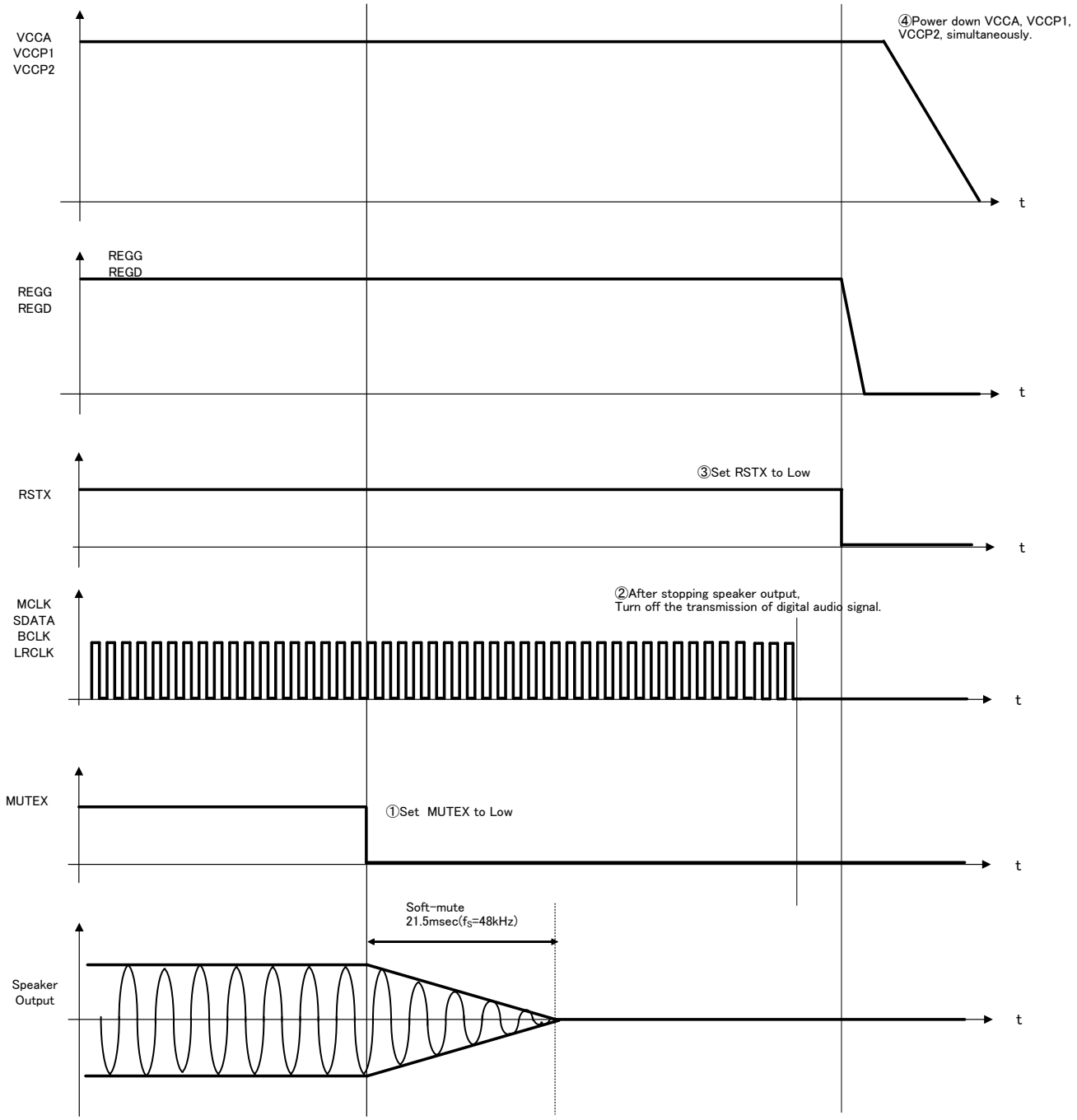


Figure 49. Power Supply Shutdown Sequence

Caution: To eliminate pop noise when power supply is turned OFF, RSTX and MUTEX should always be set Low first. And also, all power supply terminals should shut down together.

Order of ② and ③ can be interchanged

3. About Changing Audio Signal

Output PWM frequency is sixteen times the sampling frequency "f_S".
Therefore, output PWM frequency will also become unstable if MCLK becomes unstable when switching channel or switching input. During unstable period, LC resonance may occur and short protection function may work.

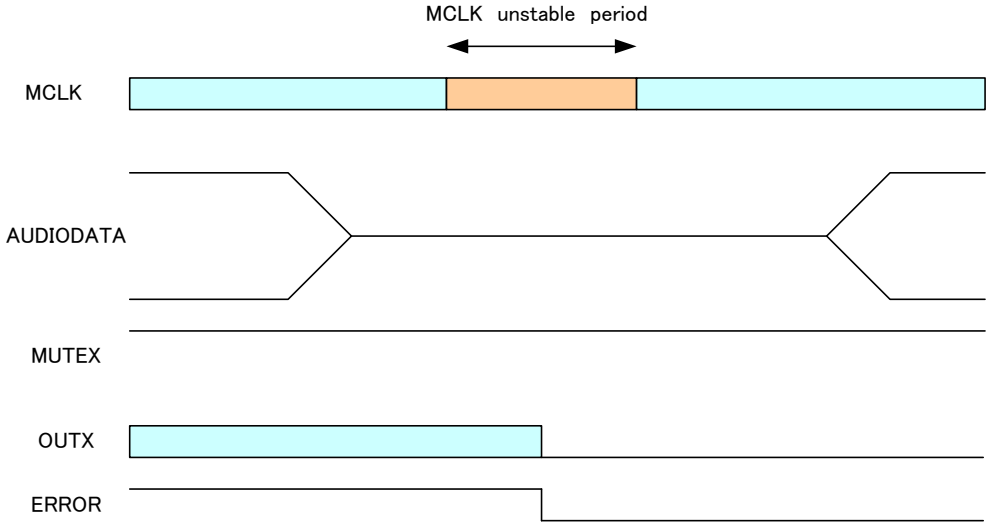
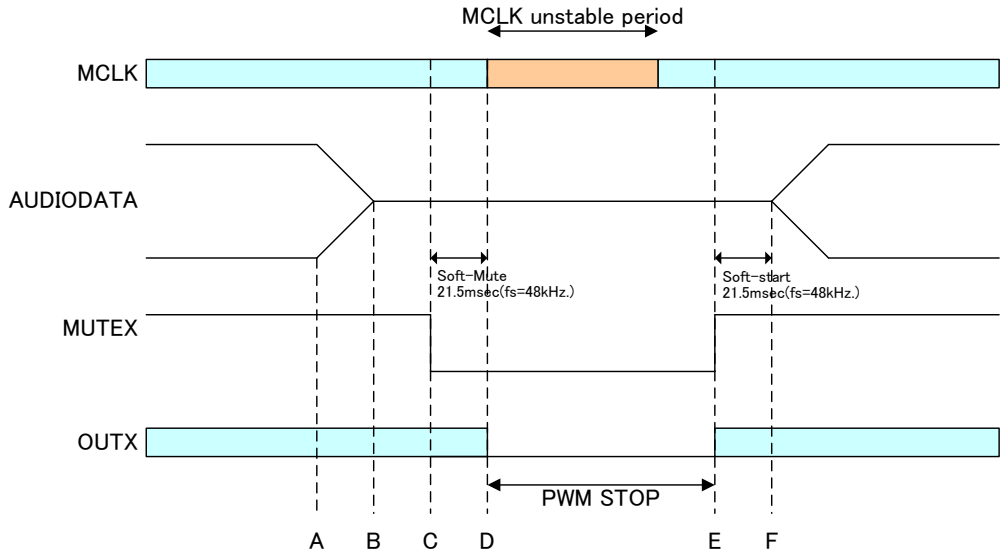


Figure 50. Action at MCLK Unstable 1

To prevent "MCLK unstable condition", please obey the following process.
(1) Mute "AUDIODATA" from scaler IC. (A)
(2) After muting "AUDIODATA" (B), set MUTEX=L (C).
(3) After MCLK goes to stable state, set MUTEX=H (D).
(4) Release mute "AUDIODATA" (E).



Order of E and F can be interchanged

Figure 51. Action at MCLK Unstable 2

Especially, if the “twice and more frequency compared with normality” is entered, for some timing, the incorrect data is set to the IC’s internal resistor and it generates noises continuously.
In case the “twice and more frequency compared with normality” is entered, please follow the timing chart bellow and add a reset sequence.
(Please release reset after MCLK (BCLK) becomes stable, then release mute of BD28623MUV.)

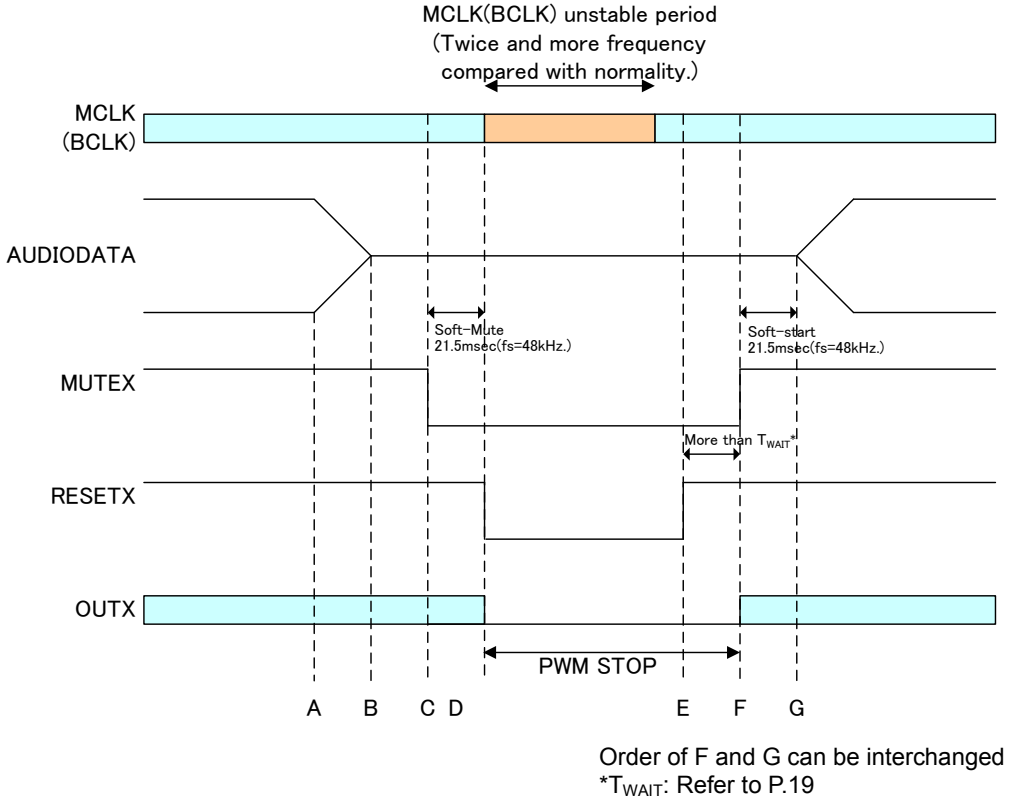


Figure 52. Action at MCLK Unstable 3

4. Recovery Sequence from the Instantaneous Power Supply Interruption

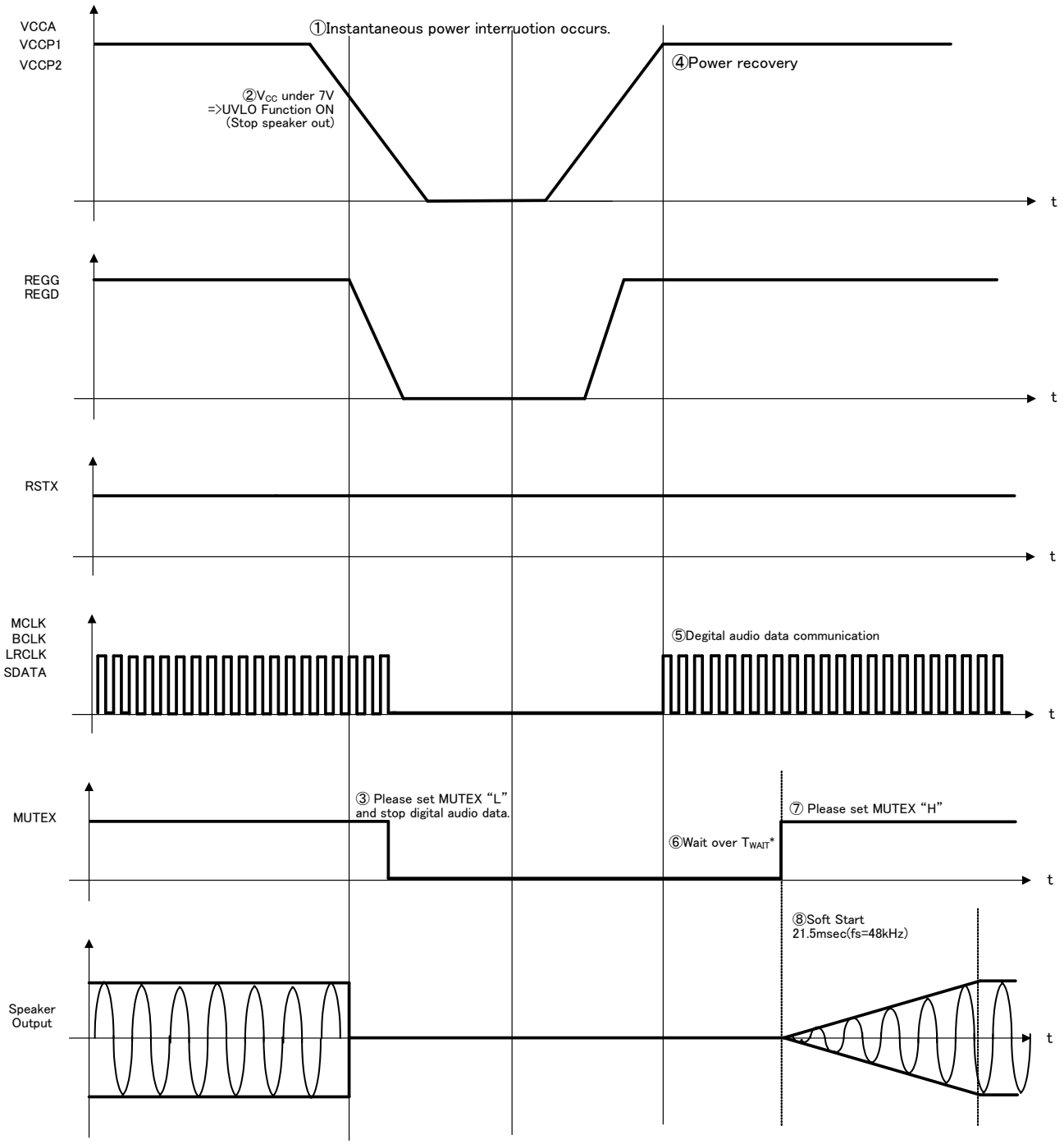


Figure 53. Instantaneous Power Interruption Recovery Sequence

*T_{WAIT}: Refer to P.19

Application Information

1. About digital audio input

(1) Input digital audio signal sampling frequency (f_S)

PWM frequency, Soft-start time, Soft-mute time, and the detection time of the DC voltage protection in the speaker depend on the sampling frequency (f_S) of the digital audio input.

Sampling Frequency of the Digital Audio Input (f_S)	PWM Frequency (f_{PWM})	Soft-start / Soft-mute Time	DC Voltage Protection in the Speaker Detection Time
32kHz	512kHz	32msec	1.02sec
44.1kHz	705.6kHz	23msec	0.74sec
48kHz	768kHz	21.5msec	0.68sec

(2) Format of digital audio input

MCLK: System Clock input signal

It will input LRCLK, BCLK, SDATA that synchronizes with this clock. MCLK frequency is 256 times the sampling frequency (256f_S) or 512 times the sampling frequency (512f_S).

LRCLK: L/R Clock input signal

It corresponds to 32kHz/44.1kHz/48kHz clock (f_S) which are same to the sampling frequency (f_S). The audio data of left and right channel for one sample is input to this section.

BCLK: Bit Clock input signal

It is used to latch data per bit using 64 times the sampling frequency (64f_S).

SDATA: Data input signal

It is amplitude data. The data length is different according to the resolution of the input digital audio data. It corresponds to 16/ 20/ 24 bits.

(3) I^2S Data Format

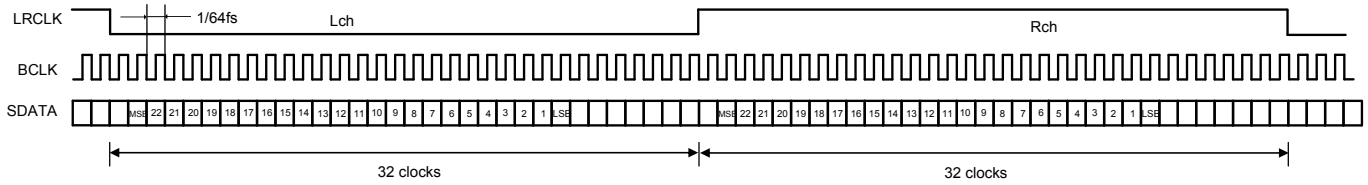


Figure 54. I2S Data Format 64fs, 24bit Data

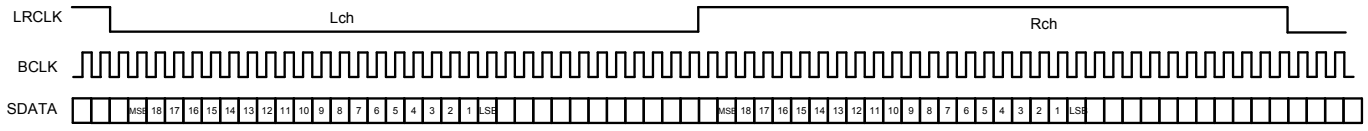


Figure 55. I2S Data Format 64fs, 20bit Data

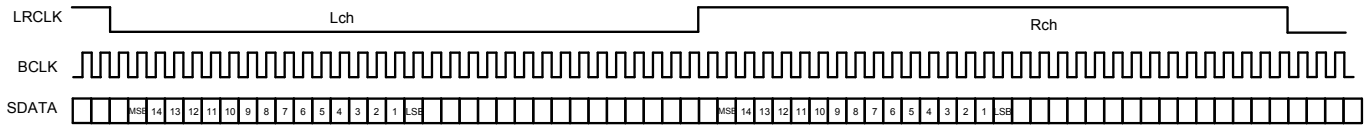


Figure 56. I2S Data Format 64fs, 16bit Data

The Low section of LRCLK becomes Lch and the High section of LRCLK becomes Rch.
After changing LRCLK, second bit becomes MSB.

(4) Audio Interface Format and Timing

Recommended timing and operating condition (MCLK, BCLK, LRCLK and SDATA)

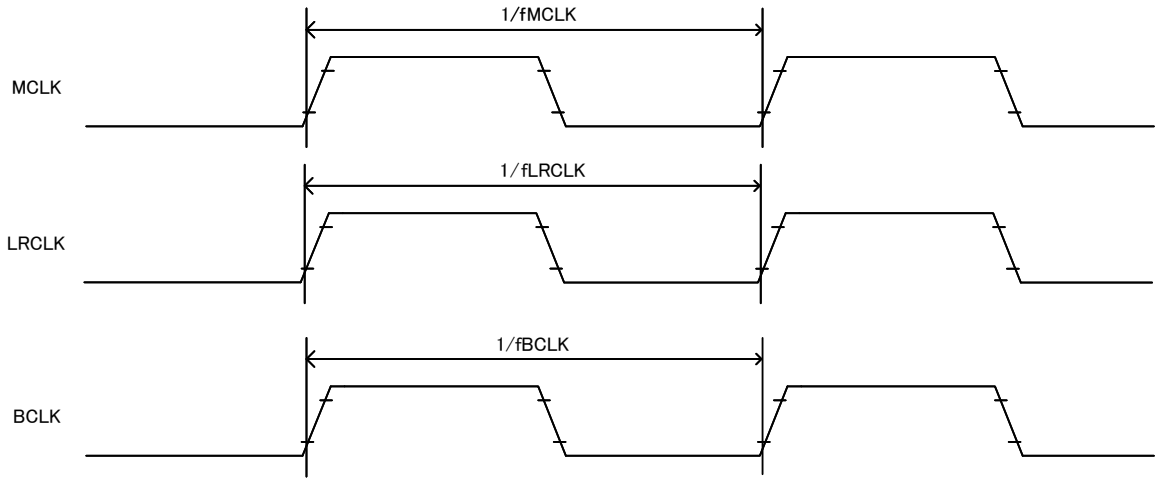


Figure 57. Clock Timing

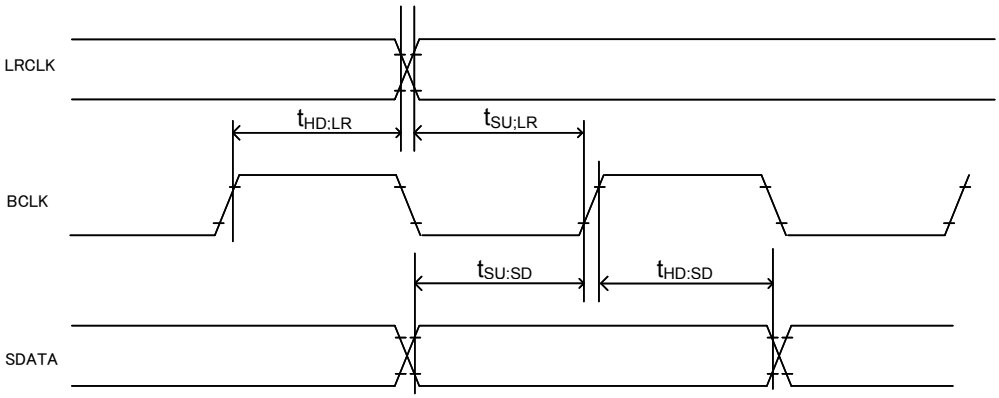


Figure 58. Audio Interface Timing

No.	Parameter	Symbol	Limit				Unit
			MCLK=256f_S		MCLK=512f_S		
			Min	Max	Min	Max	
1	MCLK Frequency(Note 8-1)	f_{MCLK}	8.192 ±10%	12.288 ±10%	16.384 ±10%	24.576 ±10%	MHz
2	LRCLK Frequency(Note 8-1)	f_{LRCLK}	32 ±10%	48 ±10%	32 ±10%	48 ±10%	kHz
3	BCLK Frequency(Note 8-1)	f_{BCLK}	2.048 ±10%	3.072 ±10%	2.048 ±10%	3.072 ±10%	MHz
4	Setup Time, LRCLK (Note 8-2)	$t_{SU;LR}$	20	−	20	−	ns
5	Hold Time, LRCLK (Note 8-2)	$t_{HD;LR}$	20	−	20	−	ns
6	Setup Time, SDATA	$t_{SU;SD}$	20	−	20	−	ns
7	Hold Time, SDATA	$t_{HD;SD}$	20	−	20	−	ns
8	MCLK, DUTY	d_{MCLK}	40	60	40	60	%
9	LRCLK, DUTY	d_{LRCLK}	40	60	40	60	%
10	BCLK, DUTY	d_{BCLK}	40	60	40	60	%

(Note 8-1) Must be synchronized with BCLK, LRCK

(Note 8-2) This regulation is to keep rising edge of LRCK and rising edge of BCLK from overlapping.