Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Multiple Input Switch Monitor LSI for Automotive

BD3376EFV-C

General Description

BD3376EFV-C is a 10-channel Multiple Input Switch Monitor IC that detects the opening and closing of mechanical switches. Once it senses a change in the status of a switch, it sends an interrupt signal to the MCU via a serial peripheral interface (SPI).

The 10 switch inputs have two types of power supply, VPUB and VPUA. The VPUB and the VPUA power supplies can either be from a battery or from another power supply system. VPUB is the supply for the INB inputs while VPUA is for the INZ and INA inputs.

BD3376EFV-C has two modes of operation, Normal and Sleep. In both modes, the internal registers can be set to make the device perform either intermittent or continuous monitoring of the switches.

In intermittent monitoring, the switch status is monitored at regular time intervals, allowing the IC to operate with low power consumption. Also, operation with reduced noise can be achieved by enabling uniform sequential monitoring of all switches or sequential monitoring by power supply system.

Application

- Engine Control Module

Key Specifications

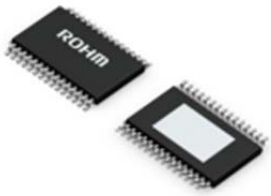
- Fully Operational Voltage Range: 8V to 26V
- Input Voltage on Switch Pin: -14V to +40V
- Selectable Wetting Current (Min): 1mA, 3mA, 5mA, 10mA, 15mA
- Low –voltage Operating Range: 3.9V to 8.0V

Specifications

- AEC-Q100 Qualified (Note 1)
- Uses 3.3/5.0V SPI Protocol in Communicating with the MCU
- Serial Communication Error Checking through 8bit-CRC
- Thermal Shutdown Protection (TSD)
- Power on Reset (POR)
- Selectable Source/Sink Current Levels through Register Settings
- Wetting Current Timer Capability
- 4 Source or Sink Input Terminals
- 6 Source Input Terminals
- Separable Power Supply
  VPUA: 7ch (INA&INZ), VPUB: 3ch (INB)
- Interrupt Notification upon Switch Status Change
- 1 to 10 Times Matched LPF that Eliminates Input Terminal Noise
- Low Current Consumption (Intermittent Monitoring)
- Status Display of Selected Terminal at DMUX Terminal

(Note 1) Grade 1

Package	W(Typ) x D(Typ) x H(Max)
HTSSOP-B30	10.00mm x 7.60mm x 1.00mm



Typical Application Circuit

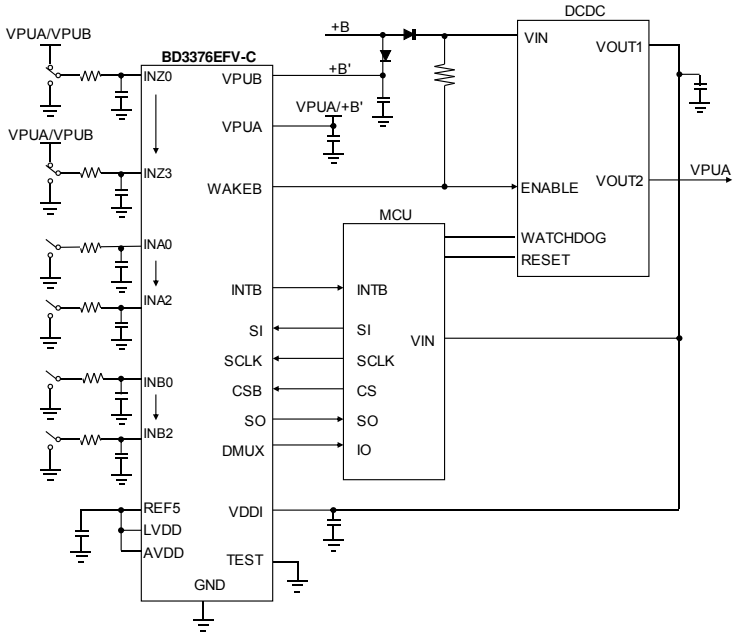


Figure 1. Typical Application Circuit

Pin Configuration

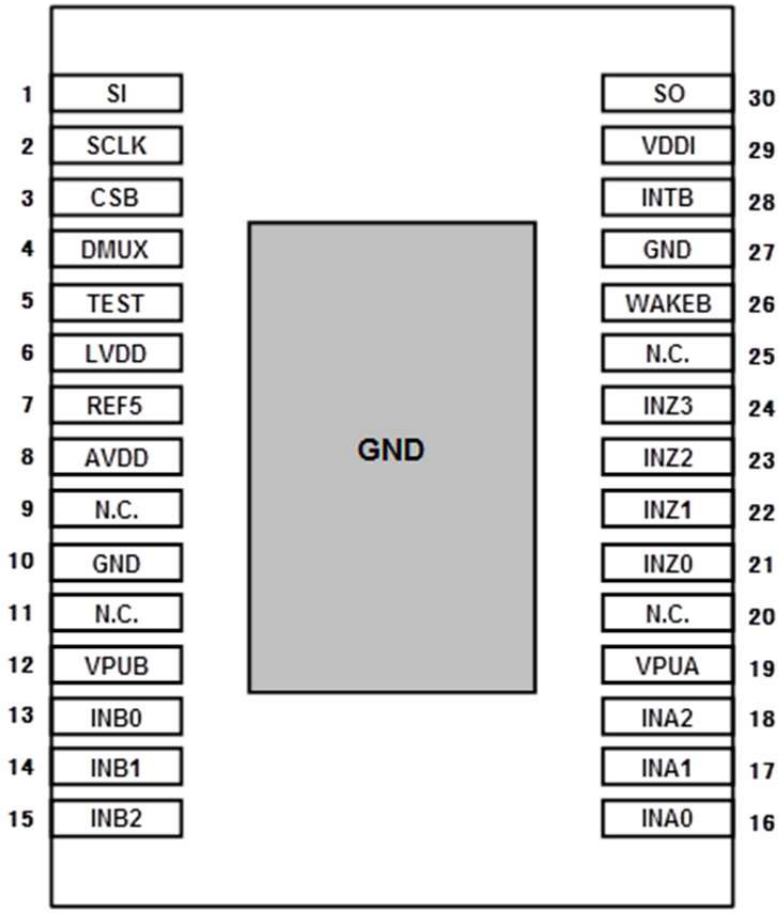


Figure 2. Pin Configuration (Top View)

Pin Description

Table 1. Pin Description

Pin No.	Pin Name	Function	Description	Equivalent Circuit Diagram (Note 2)
1	SI	Input	SPI control data input pin from the MCU (with an internal pull-down resistor)	A
2	SCLK	Input	SPI control clock input pin from the MCU (with an internal pull-down resistor)	A
3	CSB	Input	SPI control chip select input pin from the MCU (with an internal pull-up current source)	B
4	DMUX	Output	Digital multiplexer for switch input output pin	G
5	TEST	Input	Test mode control pin (Note 3) (with an internal pull-down resistor)	J
6	LVDD	Input	Power supply input pin for the logic block (Note 4)	--
7	REF5	Output	5V power supply output pin (Note 4)	I
8	AVDD	Input	Power supply input pin for the analog block (Note 4)	--
9	N.C.	-	No Connection	--
10	GND	Ground	Ground	--
11	N.C.	-	No Connection	--
12	VPUB	Input	Power supply input pin for the main system and INB switches	--
13	INB0	Input	Switch input pin 0 under VPUB power supply system (with an internal pull-up current source)	F
14	INB1	Input	Switch input pin 1 under VPUB power supply system (with an internal pull-up current source)	F
15	INB2	Input	Switch input pin 2 under VPUB power supply system (with an internal pull-up current source)	F
16	INA0	Input	Switch input pin 0 under VPUA power supply system (with an internal pull-up current source)	F
17	INA1	Input	Switch input pin 1 under VPUA power supply system (with an internal pull-up current source)	F
18	INA2	Input	Switch input pin 2 under VPUA power supply system (with an internal pull-up current source)	F
19	VPUA	Input	Power supply input pin for INA and INZ switches	--
20	N.C.	-	No Connection	--
21	INZ0	Input	Switch input pin 0 under VPUA power supply system (with an internal pull-up/down current source)	E
22	INZ1	Input	Switch input pin 1 under VPUA power supply system (with an internal pull-up/down current source)	E
23	INZ2	Input	Switch input pin 2 under VPUA power supply system (with an internal pull-up/down current source)	E
24	INZ3	Input	Switch input pin 3 under VPUA power supply system (with an internal pull-up/down current source)	E
25	N.C.	-	No Connection	--
26	WAKEB	Output	Open-drain output pin to monitor the mode of operation (Note 5)	D
27	GND	Ground	Ground pin	--
28	INTB	Output	Open-drain interrupt output pin to the MCU (with an internal pull-up resistor)	C
29	VDDI	Input	Power supply pin for CSB, SI, SCLK, SO, INTB and DMUX	--
30	SO	Output	SPI data output pin to the MCU	H

(Note 2) Ref. Page 65 I/O Equivalence Circuit
(Note 3) Short TEST pin to ground when mounted.
(Note 4) Short REF5 pin to AVDD pin and LVDD pin, and connect a 4.7μF(Min) capacitor between it and ground.
Do not use it as voltage source to another IC.
(Note 5) In the application circuit, WAKEB should be pulled-up by an external resistor.

Block Diagram

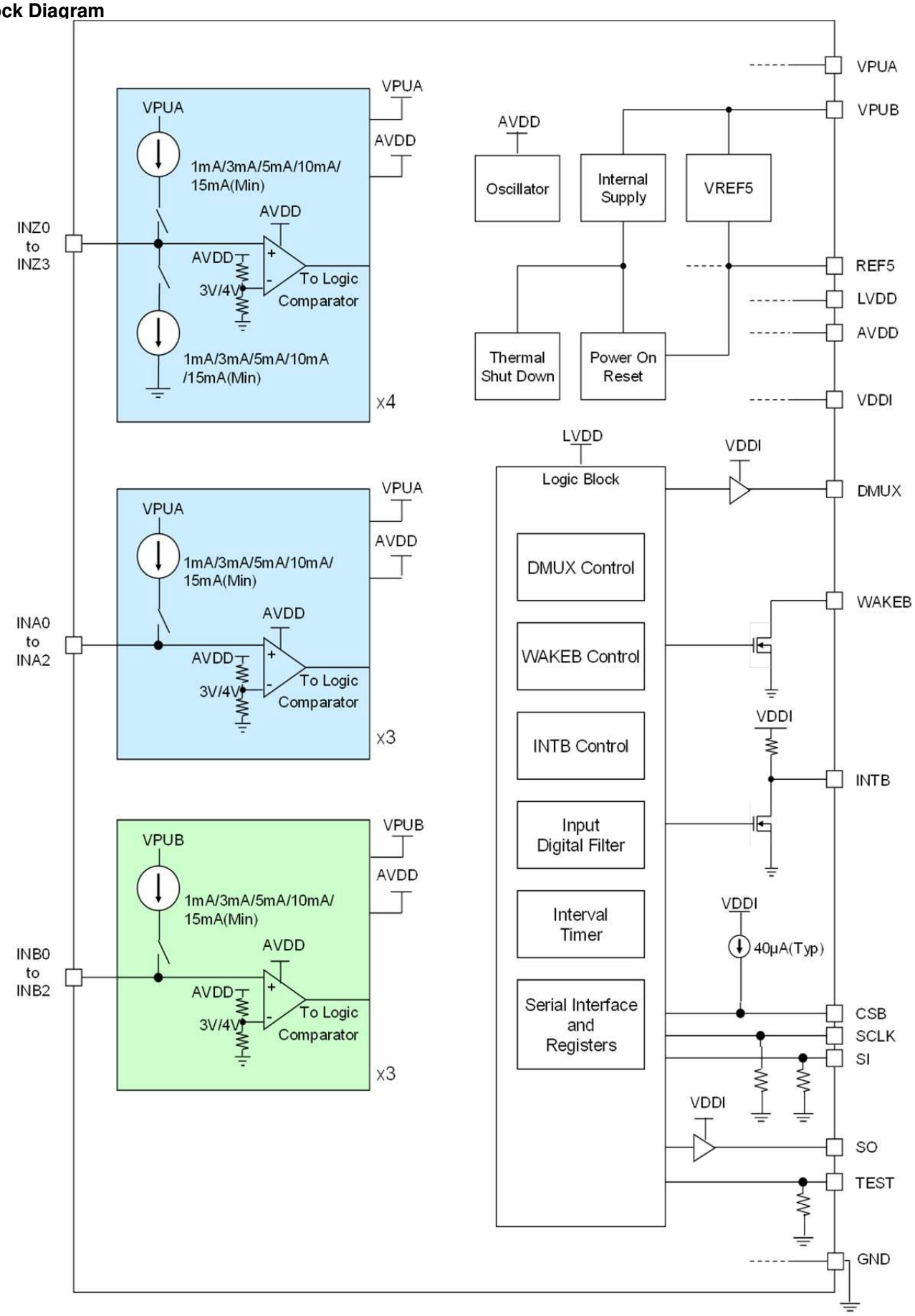


Figure 3. Block Diagram

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage Range on Pin VDDI, AVDD, LVDD Input Voltage Range on Pin CSB, SI, SCLK, TEST Output Voltage Range at Pin SO, INTB, DMUX, REF5	-	-0.3 to +7.0	V
Supply Voltage Range on Pin VPUA, VPUB Voltage Range on Pin WAKEB	-	-0.3 to +40	V
Input Current at Pin WAKEB	-	10	mA
Input Voltage on Switch Pin (INB0 to INB2, INA0 to INA2, INZ0 to INZ3)	-	-14 to +40	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tj	-40 to +150	°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance (Note 6)

Table 3. Thermal Resistance

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s (Note 8)	2s2p (Note 9)	
HTSSOP-B30				
Junction to Ambient	θ_{JA}	111.9	22.5	°C/W
Junction to Top Characterization Parameter (Note 7)	Ψ_{JT}	2	1	°C/W

(Note 6) Based on JESD51-2A (Still-Air)
(Note 7) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 8) Using a PCB board based on JESD51-3 (Table 4).
(Note 9) Using a PCB board based on JESD51-5, 7 (Table 5).

Table 4. 1s

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Table 5. 2s2p

Layer Number of Measurement Board	Material	Board Size	Thermal Via (Note 10)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 10) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Parameter	Symbol	Ratings		Unit
		Min	Max	
Operating Temperature	Topr	-40	+125	°C
VPUA/VPUB Supply Voltage	V_{VPUX}	8.0	26	V
VDDI Supply Voltage	V_{VDDI}	3.1	5.25	V
Capacitance for REF5 (Note 11)	C_{REF}	4.7	-	µF

(Note 11) Recommend a ceramic capacitance. Please consider variation of capacitance.

Electrical Characteristics

Spec conditions: 8.0V≤VPUA/VPUB≤26V, 3.1V≤VDDI≤5.25V, -40°C≤Topr≤+125°C
VPUA/VPUB/INZ/INA/INB terminal: resistors and capacitors are not connected
REF5 terminal: 4.7μF
Unless otherwise specified, the typical condition is VPUA/VPUB=13V, VDDI=5.00V, Topr=25°C.

Table 7. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
VPUA/VPUB Supply Voltage Low -voltage Operating Range (Note 12) Fully Operational Voltage Range High-voltage Operating Range (Note 13)	 $V_{VPUX(QFL)}$ $V_{VPUX(FO)}$ $V_{VPUX(QFH)}$	 3.9 8.0 26	 - - -	 8.0 26.0 40	V
POR(Power on Reset) Activation Voltage (Note 14)	$V_{POR(LOW)}$	3.9	4.2	4.5	V
POR(Power on Reset) Deactivation Voltage (Note 14)	$V_{POR(HIGH)}$	4.0	4.3	4.6	V
VPUA/VPUB Operating Current Continuous Monitoring Current source is invalid, “Hi-Z” Status	$I_{VPUX(OFF)}$	-	-	480	μA
VPUA/VPUB Average Operating Current Intermittent Monitoring Source/Sink Current Setting=1mA Monitoring Period=50ms, Strobe Time=125μs	$I_{VPUX(SS)}$	-	75	100	μA
VDDI Operating Current INTB=“H”, CSB=“H”	I_{VDDI}	-	5	10	μA
REF5 Output Voltage	V_{REF5}	4.75	5.00	5.25	V

(Note 12) Electrical characteristics are not guaranteed though functions are operating. POR is active between 3.9V and 4.5V.
(Note 13) Electrical characteristics are not guaranteed though functions are operating.
(Note 14) The POR circuit monitors the REF5 voltage.

Electrical Characteristics - continued

Table 8. Electrical Characteristics (Switch Input)

Parameter	Symbol	Min	Typ	Max	Unit
Source Current 1 (Internal Pull-up Current Source) 0V External Supply, VPUA/VPUB System (1mA Setting)	$I_{SOURCE1}$	1.0	1.4	1.8	mA
Sink Current 1 (Internal Pull-down Current Source) 8V External Supply, VPUA System (1mA Setting)	I_{SINK1}	1.0	1.4	1.8	mA
Source Current 2 (Internal Pull-up Current Source) 0V External Supply, VPUA/VPUB System (3mA Setting)	$I_{SOURCE3}$	3.0	4.2	5.4	mA
Sink Current 2 (Internal Pull-down Current Source) 8V External Supply, VPUA System (3mA Setting)	I_{SINK3}	3.0	4.2	5.4	mA
Source Current 3 (Internal Pull-up Current Source) 0V External Supply, VPUA/VPUB System (5mA Setting)	$I_{SOURCE5}$	5.0	7.0	9.0	mA
Sink Current 3 (Internal Pull-down Current Source) 8V External Supply, VPUA System (5mA Setting)	I_{SINK5}	5.0	7.0	9.0	mA
Source Current 4 (Internal Pull-up Current Source) 0V External Supply, VPUA/VPUB System (10mA Setting)	$I_{SOURCE10}$	10.0	14.0	18.0	mA
Sink Current 4 (Internal Pull-down Current Source) 8V External Supply, VPUA System (10mA Setting)	I_{SINK10}	10.0	14.0	18.0	mA
Source Current 5 (Internal Pull-up Current Source) 0V External supply, VPUA/VPUB System (15mA Setting)	$I_{SOURCE15}$	15.0	21.0	27.0	mA
Sink Current 5 (Internal Pull-down Current Source) 8V External Supply, VPUA System (15mA Setting)	I_{SINK15}	15.0	21.0	27.0	mA
Low to High Switch Detection Threshold Voltage (3.0V Setting)	$V_{TH3(HIGH)}$	2.7	3.0	3.3	V
High to Low Switch Detection Threshold Voltage (3.0V Setting)	$V_{TH3(LOW)}$	2.6	2.9	3.2	V
Low to High Switch Detection Threshold Voltage (4.0V Setting)	$V_{TH4(HIGH)}$	3.7	4.0	4.3	V
High to Low Switch Detection Threshold Voltage (4.0V Setting)	$V_{TH4(LOW)}$	3.6	3.9	4.2	V

Electrical Characteristics - continued

Table 9. Electrical Characteristics (Static Electrical Characteristics)

Parameter	Symbol	Min	Typ	Max	Unit
Serial Interface Threshold Voltage (Note 15)	$V_{INLOGIC}$	0.8	-	2.2	V
CSB Input Current CSB=VDDI	$I_{CSB(HIGH)}$	-10	-	+10	µA
CSB Pull-up Current CSB=0V	$I_{CSB(LOW)}$	30	40	85	µA
SI, SCLK Pull-down Resistor	R_{SI}, R_{SCLK}	50	100	150	kΩ
SI, SCLK Input Current SI, SCLK=0V	$I_{SI(LOW)}$, $I_{SCLK(LOW)}$	-10	-	+10	µA
SO “H” Level Output Voltage I_{SOURCE}=200µA	$V_{SO(HIGH)}$	V_{VDDI}-0.8	-	V_{VDDI}	V
SO “L” Level Output Voltage I_{SINK}=1.6mA	$V_{SO(LOW)}$	-	-	0.4	V
SO(Set to “Hi-Z”) Input Current 0V to VDDI	$I_{SO(TRI)}$	-10	-	+10	µA
DMUX “H” Level Output Voltage I_{SOURCE}=200µA	$V_{DMUX(HIGH)}$	V_{VDDI}-0.8	-	V_{VDDI}	V
DMUX “L” Level Output Voltage I_{SINK}=1.6mA	$V_{DMUX(LOW)}$	-	-	0.4	V
INTB Internal Pull-up Current	$I_{INTB(PU)}$	15	53	85	µA
INTB “H” Level Output Voltage INTB=OPEN	$V_{INTB(HIGH)}$	V_{VDDI}-0.5	-	V_{VDDI}	V
INTB “L” Level Output Voltage I_{SINK}=1.0mA	$V_{INTB(LOW)}$	-	0.2	0.4	V
WAKEB “L” Level Output Voltage WAKEB=1.0mA	$V_{WAKEB(LOW)}$	-	0.2	0.4	V
WAKEB (Set to “Hi-Z”) Input Current 0V to VPUB	$I_{WAKEB(TRI)}$	-10	-	+10	µA

(Note 15) Applicable to SCLK, SI, CSB

Electrical Characteristics - continued

Table 10. Electrical Characteristics (Dynamic Electrical Characteristics)

Parameter	Symbol	Min	Typ	Max	Unit
Wetting Current Timer Counting starts after n-times detection of matched LPF	t_{WCT}	13	-	22	ms
Interrupt Delay Time 1 Time from switch status change to INTB output change in continuous monitoring	t_{INTB_DLY1}	-	-	1	ms
Interrupt Delay Time 2 Time from switch status change to INTB output change in intermittent monitoring n: Setting time of LPF matched n-times	t_{INTB_DLY2}	-	-	[Monitor cycle] x n+1	ms
Interrupt Clear Time Time from CSB rising edge to INTB output change	t_{INTB_CLR}	-	-	150	µs
Command Set Time Time from CSB rising edge to setting of register	t_{REG_EN}	-	-	150	µs
Transition Time to Normal Mode Time from CSB rising edge to WAKEB output change	t_{WAKEB_DLY1}	-	-	1	ms
Transition Time to Sleep Mode Time from CSB rising edge to WAKEB output change	t_{WAKEB_DLY2}	-	-	1	ms
Switch Strobe Time (93.75µs Setting) (Note 16)	t_{SCAN_94}	84.375	93.750	103.125	µs
Switch Strobe Time (125µs Setting) (Note 16)	t_{SCAN_125}	112.5	125.0	137.5	µs
Switch Strobe Time (187.5µs Setting) (Note 16)	t_{SCAN_188}	168.75	187.50	206.25	µs
Switch Strobe Time (250µs Setting) (Note 16)	t_{SCAN_250}	225	250	275	µs
Source/Sink Current Rise Time FSQ="0", FSQZ/A/B="0", 10mA Setting Load Resistance 100Ω	t_{SR_R}	-	20 (Note 17)	-	µs
Source/Sink Current Fall Time FSQ="0", FSQZ/A/B="0", 10mA Setting Load Resistance 100Ω	t_{SR_F}	-	15 (Note 17)	-	µs
Internal Clock Accuracy	t_{TIMER}	-10	-	+10	%

(Note 16) "H" width of internal signal (Ref. Page 12 Figure 6).
(Note 17) Reference value.

Electrical Characteristics - continued

Table 11. Electrical Characteristics (Digital Interface Characteristics)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SCLK}	-	-	4.4	MHz
Setup Time from CSB Fall to SCLK Rise	t_{LEAD}	100	-	1000	ns
Setup Time from SCLK Fall to CSB Rise	t_{LAG}	50	-	500	ns
Setup Time from SI to SCLK Fall	$t_{SI(SU)}$	16	-	-	ns
Hold Time from SCLK Fall to SI	$t_{SI(HOLD)}$	20	-	-	ns
SI, CSB, SCLK Rise Time	$t_{R(SI)}$	-	5.0 (Note 18)	-	ns
SI, CSB, SCLK Fall Time	$t_{F(SI)}$	-	5.0 (Note 18)	-	ns
Time from CSB Fall to SO Output Low Impedance	$t_{SO(EN)}$	-	-	55	ns
Time from CSB Rising to SO Output High Impedance	$t_{SO(DIS)}$	-	-	55	ns
SCLK “H” Level Width	t_{SCLKH}	75	-	-	ns
SCLK “L” Level Width	t_{SCLKL}	75	-	-	ns
Time from SCLK Rise to Stable SO Data Output SO C_L=20pF	t_{VALID}	-	25	55	ns
CSB “H” Level Time	t_{CSBH}	150	-	-	µs

(Note 18) Reference value.

Timing Chart

·Serial Access Timing

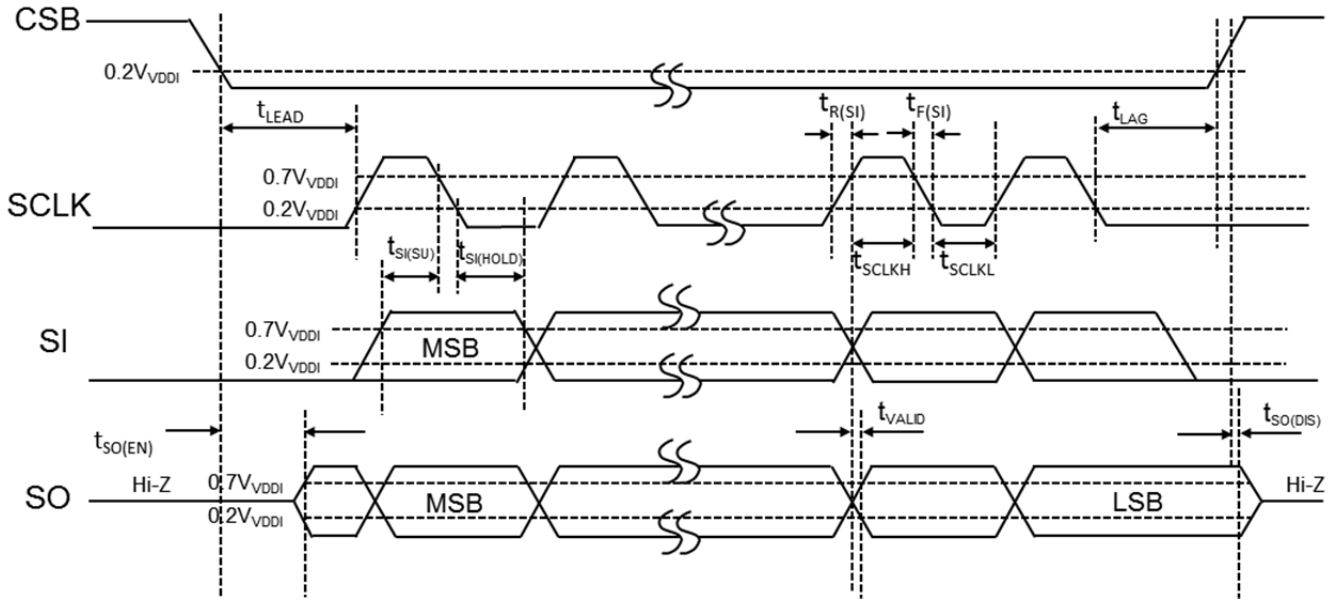


Figure 4. Serial Access Timing

Timing Chart - continued

·Power Supply Rising/Falling Sequence

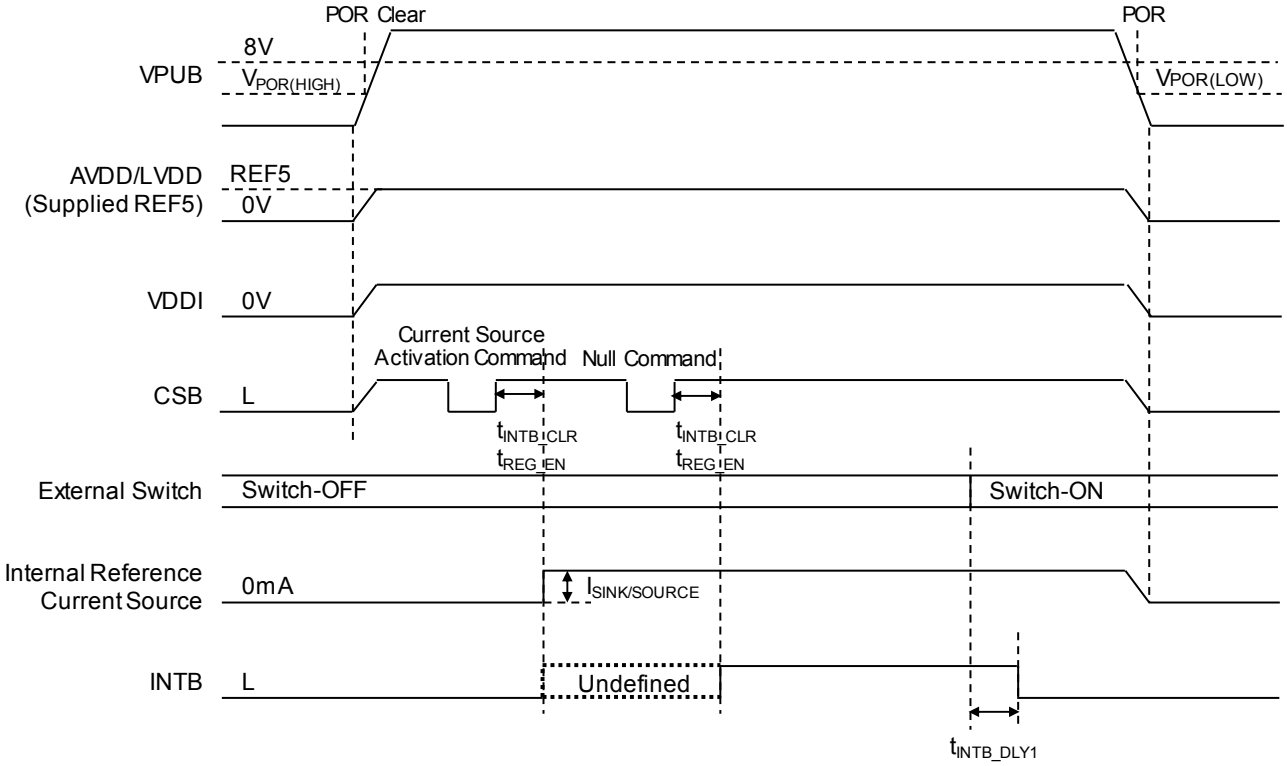


Figure 5. Power Supply Rising/Falling Sequence

·Source/Sink Current Rise and Fall Time

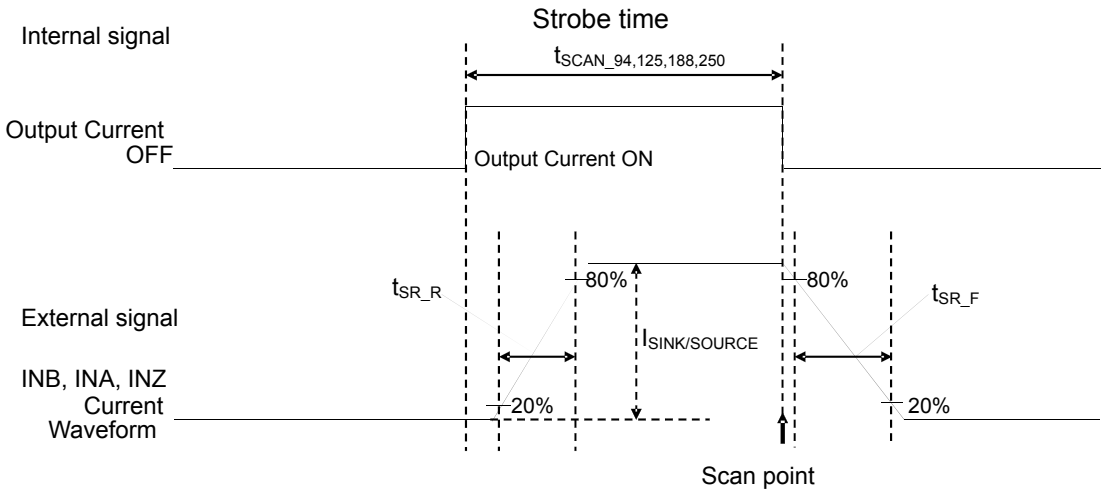


Figure 6. Intermittent Monitoring Enabled (FSQ=0, FSQZ/A/B=0, CMB/A/Z=1), Source/Sink Current Rise and Fall Time

Basic Operations

[Basic Operation 1] Detection of Switch Status Change (Continuous Monitoring)

Upon detection of a change in switch status, interrupt (INTB="H"→"L") occurs and the IC requests serial communication with the MCU.

< Example of Recommended Operation Sequence >

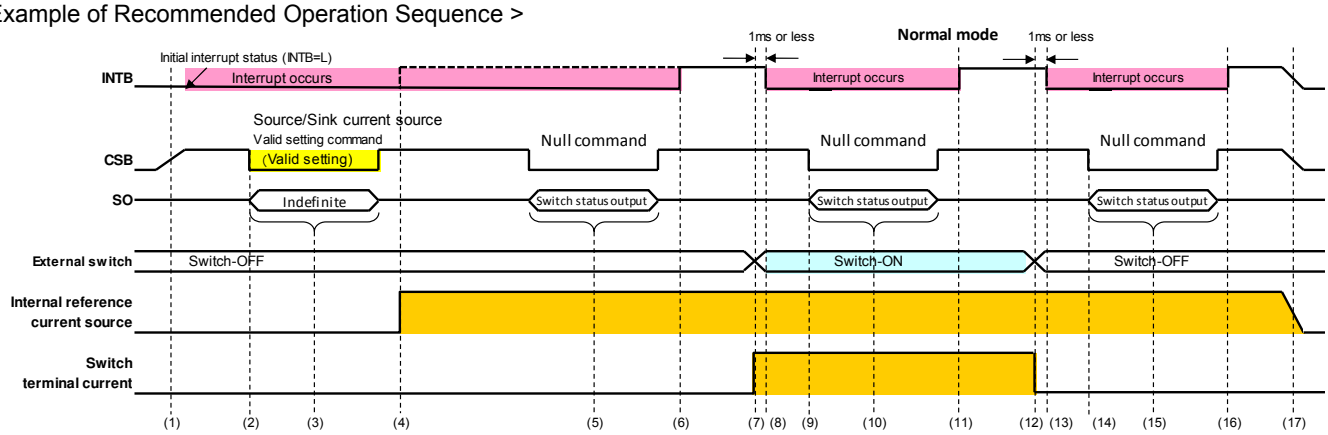


Figure 7. Basic Operation 1

(1) After power is turned on, interrupt (INTB="L") occurs.
(2) By serial communication, the switch status is obtained by the MCU at CSB falling edge.
(3) Since the current source is OFF, the switch terminal is "Hi-Z", and the output of SO is undefined.
(4) Internal reference current source is activated.
(5) Switch status is output by SO.
(6) Interrupt is cleared (INTB="L"→ "H") by CSB rising edge and prepares for switch change.
(7) Switch change occurs (OFF→ON) and IC detects switch status change.
(8) Interrupt (INTB="H"→"L") is notified to MCU, and serial communication is requested.
(9) By serial communication, the switch status is obtained by the MCU at CSB falling edge.
(10) Switch status is output by SO.
(11) Interrupt is cleared (INTB="L"→ "H") by CSB rising edge and prepares for switch change.
(12) Switch change occurs (ON→OFF) and IC detects switch status change.
(13) Interrupt (INTB="H"→"L") is notified to MCU, and serial communication is requested.
(14) By serial communication, the switch status is obtained by the MCU at CSB falling edge.
(15) Switch status is output by SO.
(16) Interrupt is cleared (INTB="L"→ "H") by CSB rising edge and prepares for switch change.
(17) Power is turned off.

Basic Operations - continued

[Basic Operation 2] Detection of Switch Status Change (Intermittent Monitoring)

When Intermittent Monitoring is enabled, switch status is monitored by periodically turning the current source on and off. Intermittent monitoring allows low power consumption.

< Example of Recommended Operation Sequence >

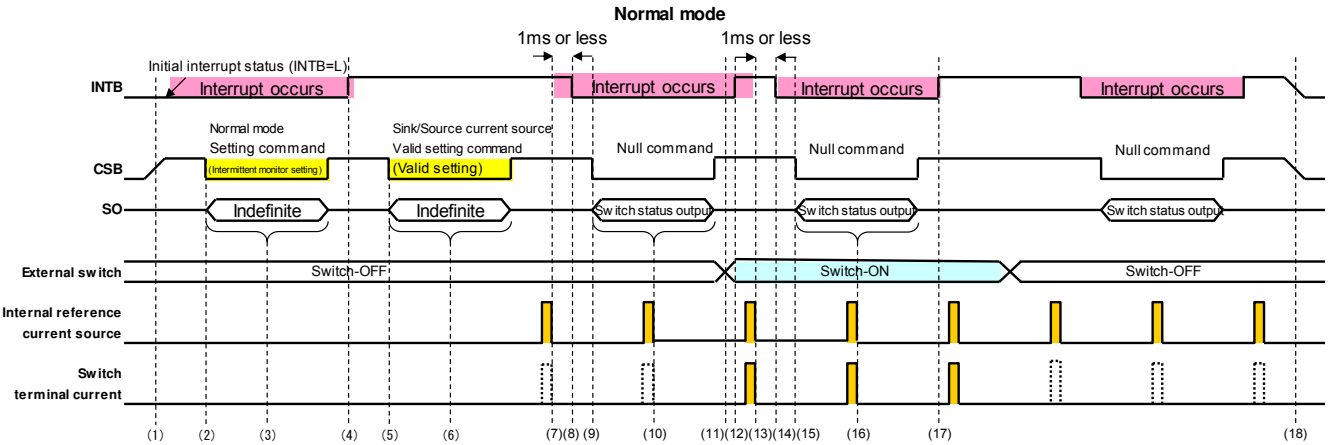


Figure 8. Basic Operation 2

(1) After power is turned on, interrupt (INTB="L") occurs.
(2) By serial communication, the switch status is obtained by the MCU at CSB falling edge.
(3) Since the current source is OFF, the switch terminal is "Hi-Z", and the output of SO is undefined.
(4) Interrupt is cleared (INTB="L"→ "H") by CSB rising edge and prepares for switch change.
(5) By serial communication, the switch status is obtained by the MCU at CSB falling edge.
(6) Since the current source is OFF, the switch terminal is "Hi-Z", and the output of SO is undefined.
(7) IC gets the switch status when the current source is ON.
(8) Interrupt (INTB="H"→"L") is notified to MCU, and serial communication is requested.
(9) By serial communication, switch status is obtained by the MCU at CSB falling edge.
(10) Switch status is output by SO.
(11) IC detects switch status change.
(12) Interrupt is cleared (INTB="L"→ "H") by CSB rising edge and prepares for switch change.
(13) IC detects switch status change.
(14) Interrupt (INTB="H"→"L") is notified to MCU, and serial communication is requested.
(15) By serial communication, switch status is obtained by the MCU at CSB falling edge.
(16) Switch status is output by SO.
(17) Interrupt is cleared (INTB="L"→ "H") by CSB rising edge and prepares for switch change.
(18) Power is turned off.

Basic Operations - continued

[Basic Operation 3] Sleep Mode Operation (Manual Transition)

When MDC register of Monitor Mode Transition Command is set to “1”, mode is changed to sleep.
When MDC register of Monitor Mode Transition Command is set to “0”, mode is changed to normal.
During sleep mode, WAKEB is in “Hi-Z” state and its voltage level is the level of the external pull-up.

< Example of Recommended Operation Sequence >

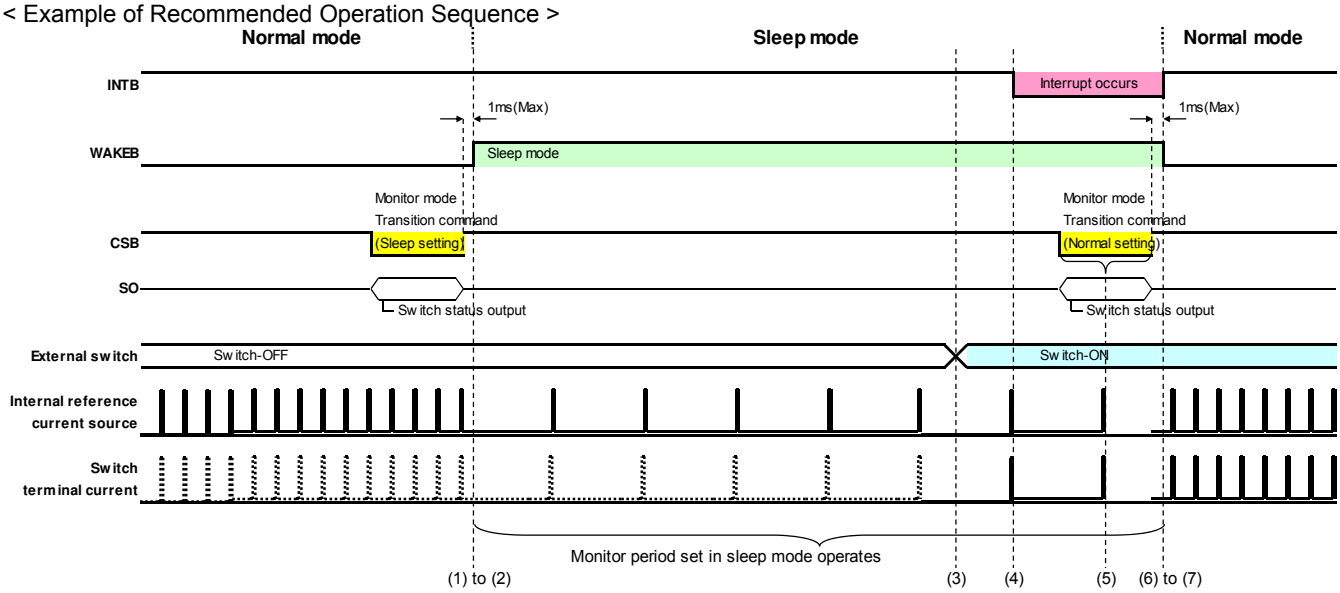


Figure 9. Basic Operation 3

(1) Monitor mode transition command (Sleep mode setting) is received from MCU.
(2) Transition to sleep mode.
(3) Switch change occurs (OFF→ON).
(4) IC detects switch status change.
(5) IC informs MCU the interrupt (INTB=“H”→“L”) and switch status is output by SO.
(6) Monitor mode transition command (Normal mode setting) is received from MCU.
(7) Transition to normal mode.

Basic Operations - continued

[Basic Operation 4] Sleep Mode Operation (Automatic Transition to Normal Mode)

Automatic transition from sleep mode to normal mode when a switch status changes is possible when the automatic mode transition setting is enabled.
During sleep mode, WAKEB is in “Hi-Z” state and its voltage level is the level of the external pull-up.

< Example of Recommended Operation Sequence >

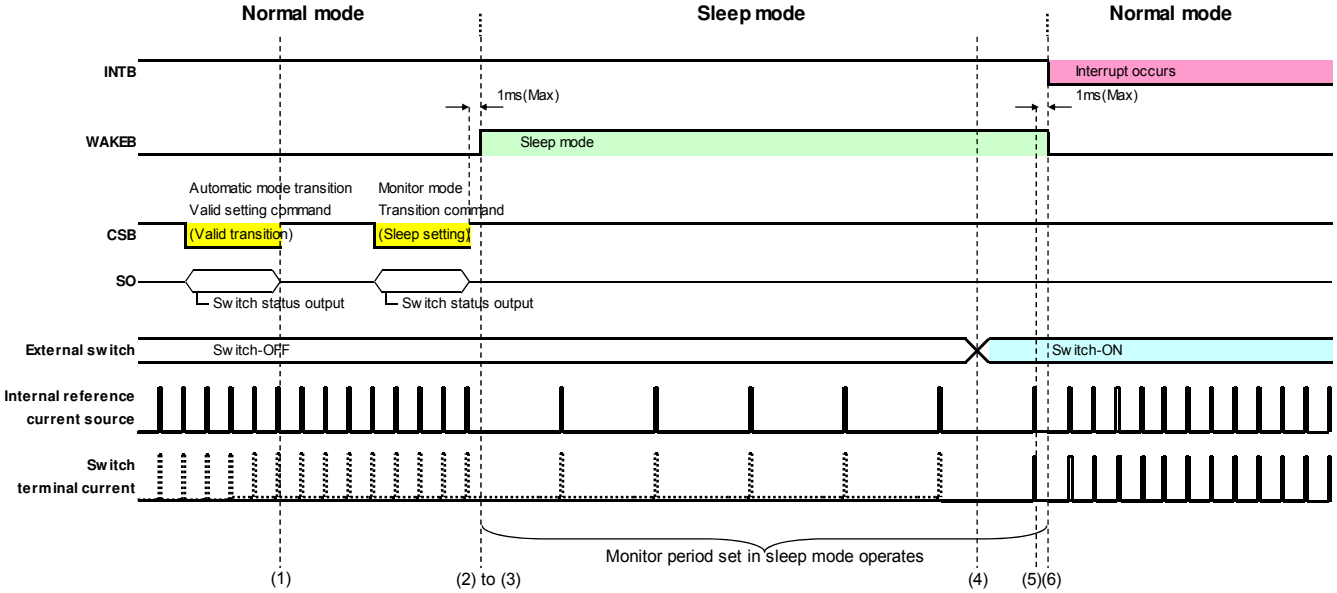


Figure 10. Basic Operation 4

(1) Automatic transition of mode is enable.
(2) Monitor mode transition command (sleep mode setting) is received from MCU.
(3) Transition to sleep mode.
(4) Switch change occurs (OFF→ON).
(5) IC detects switch status change.
(6) IC informs the interruption to MCU with INTB(“H” →“L”) and changes to Normal mode automatically.

Description of Functions

1. Power on Reset (POR)

Upon the application of an external voltage to VPUB, REF5 output is generated by the LDO inside the IC.
When REF5 ≤ 4.2(Typ), POR is activated.
When REF5 ≥ 4.3(Typ), POR is deactivated.

2. Serial Interface

Communication between BD3376EFV-C and the MCU uses terminals chip select bar input (CSB), serial clock input (SCLK), serial data input (SI), and serial data output (SO).
CSB is internally pulled-up to VDDI. When CSB status is “0”, SCLK and SI inputs are valid, and it is possible to read data from SO. When CSB status is “1”, SCLK and SI inputs are invalid, and SO status is “Hi-Z”.

・Communication Frame

The transmitted frame by the MCU is a 40-bit structure composed of the transmission and reception discrimination (2-bit), the address (6-bit), the data (24-bit), and the CRC (8-bit). The transmission and reception discrimination (2-bit) is intended to differentiate between the transmitted and the received frame. The command (6-bit) sets various settings such as the “valid interrupt setting command”. The CRC (8-bit) outputs the result of a 39 bit to 8 bit CRC calculation. If a CRC error occurs, either when the structure of the frame is not 40-bit or when the transmission and reception discrimination bit is an error (the 33-bit of the SO frame is “H”), communication error is output and data is not recognized. As for writing, SI data is latched by internal shift register at timing of SCLK falling.

Table 12. Serial Data Input (SI)

Communication frame	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
SI input bit	Register address								Setting data							

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
Setting data																CRC

The received frame by the MCU has two types of bit alignment, “switch status output” and “register value output”.

The switch status output bit alignment is a 40-bit structure composed of transmission and reception discrimination (2-bit), a fixed value (1-bit), interrupt factor output (5-bit), another fixed value (1-bit), mode status output (1-bit), switch status output (22-bit), and CRC (8-bit).
Transmission and reception discrimination (2-bit) is intended to discriminate transmit and receive frame. The interrupt factor is discussed on Page 19. When an interrupt factor occurs, the corresponding bit becomes “1”. Mode status (1-bit) is “0” when set to normal mode, and it is “1” when set to sleep mode. Switch status output (22-bit) is “1” when external switch is ON, and it is “0” when external switch is OFF. The CRC (8-bit) outputs the result of a 39 bit to 8 bit CRC calculation.
The switch status is latched to the timing of CSB falling edge. The then in order of interrupt factor output, mode status and switch status output are output from SO by SCLK rising.

Table 13. Serial Data Output (SO-Switch Status Output)

Output frame	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
SO output bit	1	0	0	Interrupt factor output					0	Mode	0	0	0	Switch INB2 to INB0 status output		

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
0	0	0	0	0	Switch INA2 to INA0 status output			0	0	0	0	Switch INZ3 to INZ0 status output				CRC

The register value output bit alignment is a 40-bit structure composed of transmission and reception discrimination (2-bit), a fixed value (1-bit), interrupt factor output (5-bit), register value output (24-bit), and CRC (8-bit).
The data is output by SO at SCLK's rising edge after the CSB falling edge of the command following the register value output command.
The bit alignment of the register value output is shown on Table 36. The sequence of register value output is shown in Figure 11 and Figure 12.

Table 14. Serial Data Output (SO-Register Value Output)

Output frame	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
SO output bit	1	0	0	Interrupt factor output					Register value output							

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
Register value output																CRC

Description of Functions - continued

The register value output command (Table 35 RIER to RMDR) is used to read-back the register value written by register write command (Table 35 IER to MDR).
Figure 11 describes the single read-back sequence. Figure 12 describes the continuous sequential read-back sequence.

<Single Read-back Sequence – Recommended Sequence>

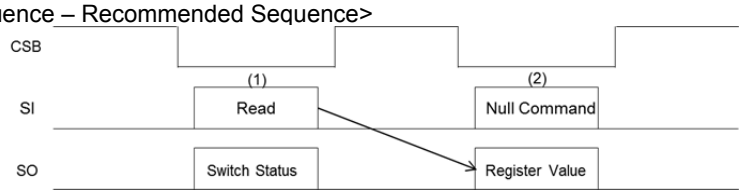


Figure 11. Single Read-back Sequence

(1) Send the register value output command.
The switch status is output by SO.
(2) Read the register value by sending the Null command.
The result of the register value output command (1) is output by SO.

<Continuous Sequential Read-back Sequence – Recommended Sequence>

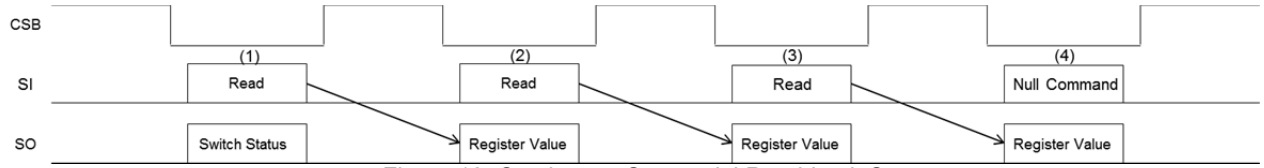


Figure 12. Continuous Sequential Read-back Sequence

(1) Send the register value output command.
The switch status is output by SO.
(2) Send the register value output command following (1). (The address of the register value output command does not need to be the next address.)
(3) Send the register value output command repeatedly as needed.
The SO output at each command is the result of the previous register value output command.
(4) Send the Null command in the end.
The register value of the previous register output command is output by SO.

3. Switch Status Output

Switch status can be sent through SO output.

Description of Functions - continued

4. Interrupt (INTB operation)

There are five interrupt factors that cause the INTB terminal to output “L”. The type of interrupt factor that occurred can be checked in the SO output when CSB is “L”.
INTB output will return to “H” once the interrupt factor is cleared by the rising edge of CSB. The INTB terminal is an open-drain output that is internally pulled-up to VDDI.

·Interrupt Factors

The interrupt factors are shown below:

Interrupt Factor	Interrupt flag (SO output)	Flag name
(1) Test detection	SO output bit [36]	: “test_flg”
(2) Thermal shutdown detection	SO output bit [35]	: “them_flg”
(3) Reset detection	SO output bit [34]	: “rst_flg”
(4) Communication error detection (CRC error, 40-bit frame error, or transmission and reception discrimination error)	SO output bit [33]	: “err_flg”
(5) Switch status change detection	SO output bit [32]	: “sw_flg”

(1) Test detection
The IC generates an interrupt after a transition to test mode. The TEST terminal should always be connected to ground.

(2) Thermal shutdown detection
Interrupt occurs when the thermal shutdown circuit detects a temperature higher than the allowable junction temperature inside IC.

(3) Reset detection
Interrupt occurs after the activation of Power on Reset (POR) or the transmission of the reset command. Upon POR activation, the SO output interrupt flag “rst_flg” is reflected instantly. With reset command transmission, “rst_flg” is reflected on the next command transmission.

(4) Communication error detection
Interrupt occurs due to either a CRC error, a 40-bit frame error, or a command transmission error. The interrupt flag “err_flg” is triggered by the following :
CRC error : when there is a Cyclic Redundancy Check error
40-bit frame error : when the command received is not 40-bit
Transmit and receive determination error : when the first two bits of the command received is not [39:38]=“01”

(5) Switch status change detection
Interrupt occurs when switch a status changes (switch-ON→OFF or switch-OFF→ON).

·Clearing of INTB output and interrupt factor

The INTB “L” output and the interrupt factor are both cleared by the CSB rising edge during command transmission. In case a new interrupt factor occurs during command transmission, the interrupt factor is not cleared. The new interrupt factor is reflected on the next command transmission.
The interrupt factor is not cleared by the register readout that follows the register value output command.

Description of Functions - continued

5. Operating Modes

BD3376EFV-C has two types of operating mode, the normal and the sleep mode. Transition between the two modes can be done by sending the correct “Monitor Mode Transition Command”. The current mode of operation can be checked through the WAKEB and the SO terminal outputs.

Monitor Mode Transition register address (0x4F): Bit [31]: 0=Normal mode, 1=Sleep mode

·Normal Mode

Normal mode operation can be set to continuous monitoring, wherein the switch status is checked by a continuously ON current source, or to intermittent monitoring, wherein the switch status is checked by a regularly ON/OFF current source.
The period of intermittent monitoring (Note 19) can be set according to power supply system while strobe time (Note 20) is common for all switch terminals.
At normal mode, WAKEB is “L” and the 30-bit of the SO output is “0”.

·Sleep Mode

Sleep mode operation, like in normal mode, can be set to continuous monitoring or intermittent monitoring.
The monitoring period (Note 19) of intermittent monitoring can be set according to power supply system.
The strobe time (Note 20) is common for all switch terminals and both modes.

The difference with normal mode is that, from sleep mode, it is possible to change to normal mode automatically when interrupt occurs. (Automatic mode transition function)
At sleep mode, WAKEB is in “Hi-Z” state and its voltage level is the level of the external pull-up. The 30-bit of SO output is “1” at sleep mode.

(Note 19) Monitor period is descripted in Figure.13.
(Note 20) Strobe time is descripted in Figure.13.

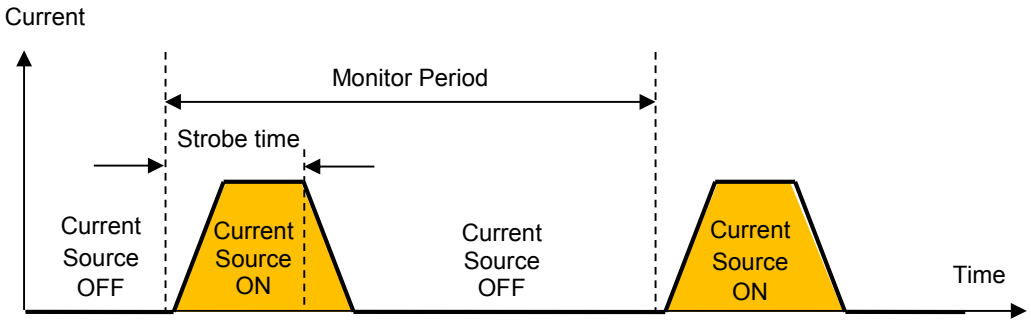


Figure 13. Intermittent Monitoring

6. Automatic Mode Transition Function

By sending the “Automatic Mode Transition Command” through setting the MIR register (0x4E) to “1”, automatic transition from sleep to normal mode is possible. The conditions for a change in mode from sleep to normal to occur for both enabled and disabled “Automatic Mode Transition Function” are shown below:

·Conditions for sleep to normal mode transition when “Automatic Mode Transition Function” is enabled:

1. Normal mode transition command is sent
2. POR occurs or reset command sent (Initialization)
3. A switch status changes (The “Switch Change Interrupt Setting” should be enabled)

·Conditions for sleep to normal mode transition when “Automatic Mode Transition Function” is disabled:

1. Normal mode transition command is sent
2. POR occurs or reset command sent (Initialization)

Description of Functions - continued

[Extension Function1: Intermittent Monitoring at the Same Time (with Current Slope)]

In intermittent monitoring, it is possible to detect the status of the all switches at the same time. When all inputs are set to detect the switch status by intermittent monitoring, the wetting current has a rising and falling slope.

Normal Mode Setting Register (0x4B) : 31 bit to 28 bit is “0000” and intermittent monitoring setting
Sleep Mode Setting Register (0x4C) : 31 bit to 28 bit is “0000” and intermittent monitoring setting

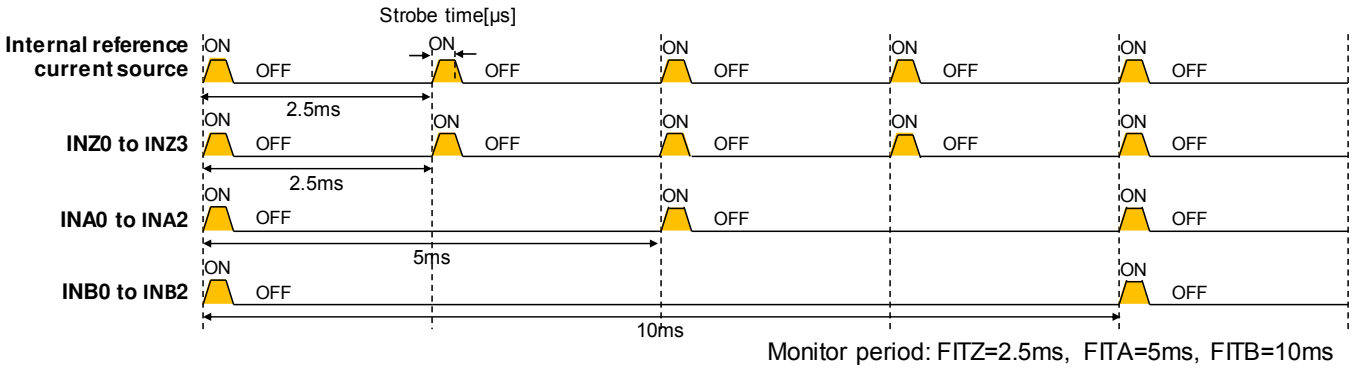


Figure 14. Intermittent Monitoring at the Same Time Example

[Extension Function 2: Sequential Monitoring by Power Supply System]

In this type of sequential monitoring, the status of the switches within a power supply system is monitored one at a time. This type has no slope. Since no two or more current sources in a power supply system are ON at the same time, radiation noise is reduced.

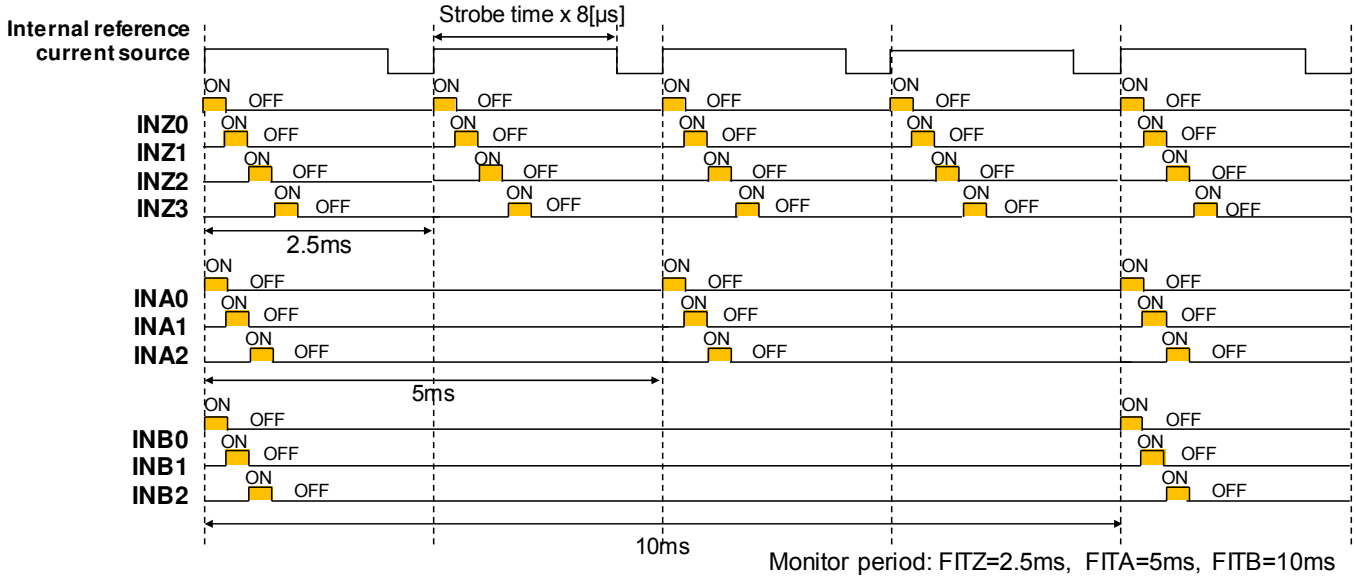


Figure 15. Sequential Monitoring by Power Supply System Example

Description of Functions - continued

[Extension Function 3: Sequential Monitoring of All Switch Terminals]

In this type of sequential monitoring, the status of all switches is monitored one at a time.
Since no two or more current sources are ON at the same time, radiation noise is reduced. This type has no slope.

The monitoring period for all switches increases by four times the monitoring period set for the INZ channels as shown in Figure 16. Uniform sequential monitoring and sequential monitoring by power supply should not be enabled at the same time. In case the two sequential monitoring methods are activated simultaneously, the method which prevails is uniform sequential monitoring.

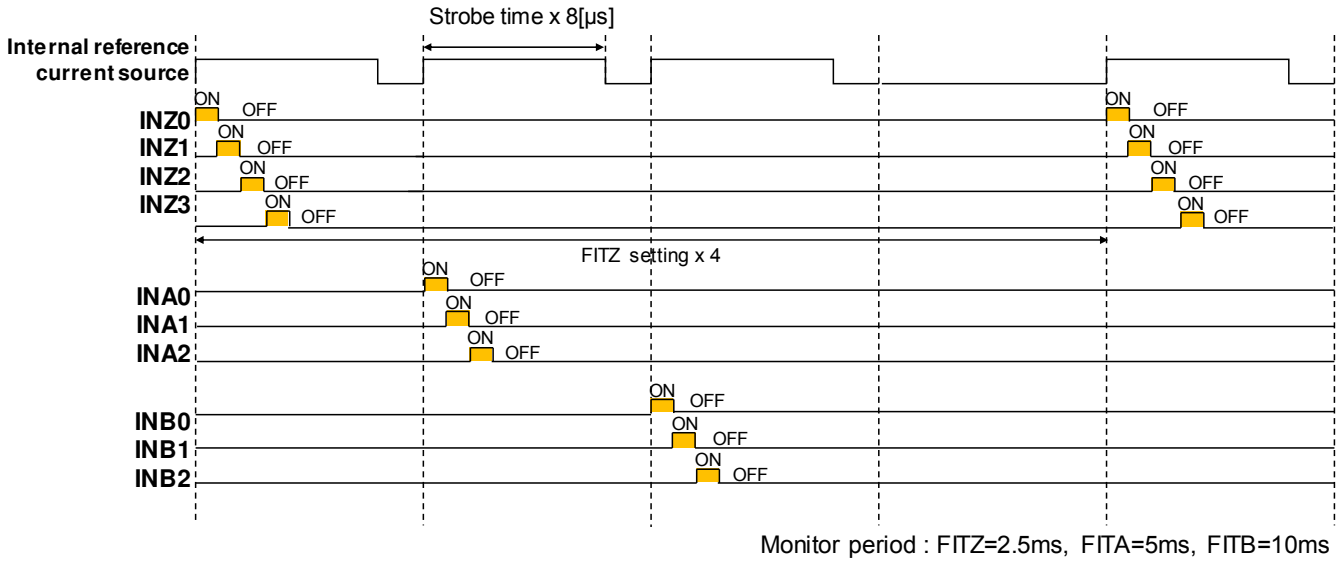


Figure 16. Sequential Monitoring of All Switch Terminals Example

Description of Functions - continued

7. WAKEB Terminal

WAKEB is an open drain output pin.
In normal mode, its output is “L”. In sleep mode, its output is “Hi-Z” and its voltage level is the level of the external pull-up.

8. Source/Sink Current Source for Switch Terminal

There are three types of switch terminal inputs with internal current source: INZ, INA, and INB. The current level can be set for each switch terminal.

·Current Source of INZ System (INZ0 to INZ3)

This current source is used to source or sink current to the external switch. The wetting current can be interchanged between pull-up and pull-down. VPUA is the power supply for the pull-up current source.

·Current Source of INA System (INA0 to INA2)

This current source is used to source current to the external switch. VPUA is the power supply

·Current Source of INB System (INB0 to INB2)

This current source is used to source current to the external switch. VPUB is the power supply.

The current source settings can be fixed by INZ current source/sink selection command, the current source setting command, and the holding current/wetting current value setting command.

Description of Functions - continued

9. Wetting Current Timer

The wetting current timer is 13ms to 22ms. This function can be enabled individually for each switch terminal. The timer starts after the switch has been detected as ON. After the 13ms to 22ms timer is finished, the wetting current (10mA/15mA) is switched to holding current (1mA/3mA/5mA). The timer is reset after the switch is turned OFF.

[Function operation1] Wetting Current Timer (Continuous Operation)

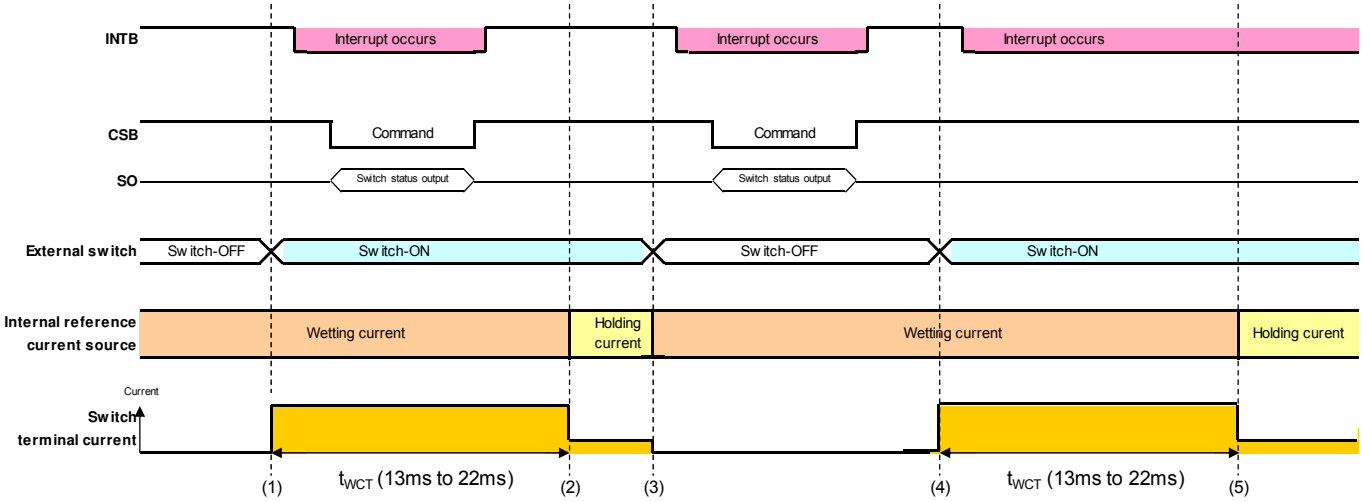


Figure 17. Wetting Current Timer (Continuous Operation)

(1) Switch change occurs (OFF→ON), IC detects switch status change.
(2) When ON state of the switch continues for more than 13ms to 22ms, the holding current is output.
(3) Switch change occurs (ON→OFF).
(4) Switch change occurs (OFF→ON), IC detects switch status change.
(5) When ON state of the switch continues for more than 13ms to 22ms, the holding current is output.

Description of Functions - continued

[Function operation2] Wetting Current Timer (Intermittent Monitoring)

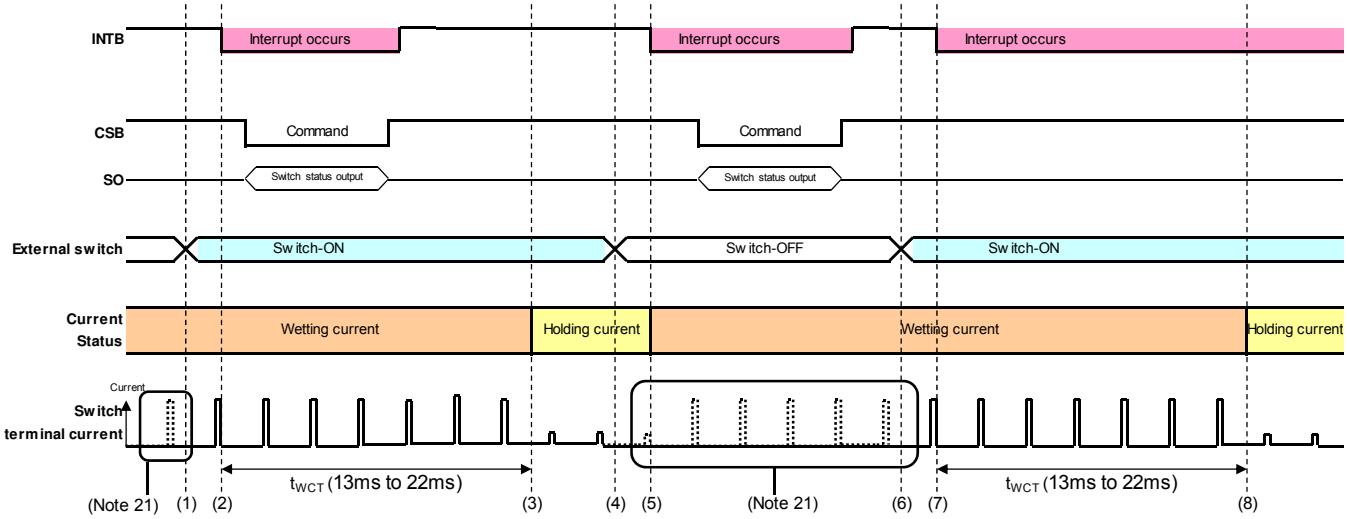


Figure 18. Wetting Current Timer (Intermittent Monitoring)

(1) Switch change occurs (OFF→ON)
(2) IC detects switch status change.
(3) When ON state of the switch continues for more than 13ms to 22ms, the holding current is output.
(4) Switch change occurs (ON→OFF).
(5) IC detects switch status change, switch current is switched from holding current to wetting current.
(6) Switch change occurs (OFF→ON).
(7) IC detects switch status change.
(8) When ON state of the switch continues for more than 13ms to 22ms, the holding current is output.

(Note 21)

The current does not flow for switch-off. This waveform shows a timing of Monitoring.