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Sound Processors for Car Audios

General-Purpose Electronic Volume with Built-in Advanced Switch

BD3460FS,BD3461FS,BD3464FV,BD3465FV

No.11085EBT09

●Description

BD3460FS, BD3461FS, BD3464FV, BD3465FV is 4ch / 6ch electronic volume which has audio efficiency of the industry best level. It has 『Outside sound mixing function (with volume)』(BD3461FS, BD3465FV) in favorite channel to mixing of the portable telephone and car navigation's guide sound. Also, which has 『Ground isolation amplifier』(BD3460FS, BD3461FS) when connecting with the outside voice inputs such as portable audio and car navigation. It is lineup and possible to be chosen to the use by it. Also, Rohm has the volume switching shock sound prevention technique "Advanced switch". Therefore, it supports the construct of the high quality car audio space by the simple control.

●Features

1) Reduce switching noise of volume by using advanced switch circuit. (Possible to control all steps)
2) Low distortion (0.0004% typ), Low noise (1.6μVrms)
3) Mixing for external sound monaural 3ch. It is possible that is mixed to front/Rear/Sub output (BD3461FS) Front/Rear output (BD3465FV) Lch/Rch independently.
4) Built-in 3ch ATT for external sound mixing that can be controlled independently. (BD3461FS, BD3465FV)
5) Built-in buffered stereo ground isolation amplifier inputs, ideal for external input. (BD3460FS, BD3461FS)
6) Bi-CMOS process is suitable for the design of low current and low energy. And it provides more quality for small scale regulator and heat in a set.
7) Package is SSOP-A24,SSOP-B20. Putting input-terminals together and output-terminals together can make PCB layout easier and can makes area of PCB smaller.
8) It is possible to control by 3.3V / 5V for I^2C BUS.

●Applications

It is the optimal for the car audio. Besides, it is possible to use for the car navigation, audio equipment of mini Compo, micro Compo, DVD, TV etc with all kinds.

●Line up matrix

Function	BD3460FS	BD3461FS	BD3464FV	BD3465FV
Volume	6ch	6ch	4ch	4ch
Input for external sound mixing	-	○	-	○
GND isolation amplifier	○	○	-	-
Package	SSOP-A24	SSOP-A24	SSOP-B20	SSOP-B20

●**Absolute maximum ratings** (Ta=25℃)

Parameter		Symbol	Ratings	Unit
Power supply Voltage		VCC	10.0V	V
Input voltage		VIN	VCC+0.3 ~ GND-0.3	V
Power Dissipation	BD3460FS BD3461FS	Pd	1000 ※1	mW
	BD3464FV BD3465FV		810 ※2	
Storage Temperature		Tastg	-55 ~ +150	℃

※1 This value decreases 8mW/℃ for Ta=25℃ or more. Thermal resistance θja=125.0 (℃/W)
※2 This value decreases 6.5mW/℃ for Ta=25℃ or more. Thermal resistance θja=153.8 (℃/W)
ROHM standard board shall be mounted.
ROHM Standard board Size：70×70×1.6(㎜)
material：FR4 grass epoxy board(3% or less of copper foil area)

●**Operating conditions**

Parameter	Symbol	Ratings			Unit
		Min.	Typ	Max.	
Power supply Voltage	VCC	7.0	-	9.5	V
Temperature	Topr	-40	-	+85	℃

●Electrical characteristics

Unless specified particularly, Ta=25℃, VCC=8.5V, f=1kHz, Vin=1Vrms, Rg=600Ω, R_L=10kΩ, INF1 input, Volume 0dB

BLOCK	Parameter	Symbol	Limit			Unit	Condition
			Min.	Typ.	Max.		
GENERAL	Current upon no signal	IQ	—	25	40	mA	No signal
	Voltage gain	GV	-1.5	0	1.5	dB	Gv=20log(VOUT/VIN)
	Channel balance	CB	-1.5	0	1.5	dB	CB=GV1-GV2
	Total harmonic distortion	THD	—	0.0004	0.05	%	VOUT=1Vrms BW=400-30kHz
	Output noise voltage ＊	VNO	—	1.9	10	μVrms	Rg=0Ω BW=IHF-A
	Residual output noise voltage ＊	VNOR	—	1.6	10	μVrms	Volume=-∞dB Rg=0Ω BW=IHF-A
	Cross-talk between channels ＊	CTC	—	-105	-90	dB	Rg=0Ω CTC=20log(VOUT/VIN) BW=IHF-A
	Ripple rejection	RR	—	-80	-40	THD	f=100Hz VRR=100mVrms RR=20log(VOUT/VCCIN)
DIFF (BD3460FS, BD3461FS)	Input impedance	$R_{IN\ D}$	70	100	130	kΩ	
	Common mode rejection ratio ＊	CMRR	50	65	—	dB	PIN and NIN input CMRR=20log10(VIN/VOUT) BW=IHF-A
VOLUME	Input impedance	$R_{IN\ V}$	70	100	130	kΩ	
	Maximum input voltage	V_{IM}	2	2.35	—	Vrms	VIM at THD+N(VOUT)=1% BW=400-30kHz
	Maximum gain	$G_{V\ BST}$	21	23	25	dB	Gain=23dB VIN=100mVrms G_V=20log(VOUT/VIN)
	Maximum attenuation ＊	$G_{V\ MIN}$	—	-109	-90	dB	Volume=-∞dB Gv=20log(VOUT/VIN) BW=IHF-A
	Step resolution	$G_{V\ STEP}$	—	1	—	dB	GAIN&ATT=+23～-79dB
	Gain set error	$G_{V\ ERR}$	-2	0	2	dB	Gain=+1～+23dB
	Attenuation set error 1	$G_{V\ ERR1}$	-2	0	2	dB	ATT=-1～-15dB
	Attenuation set error 2	$G_{V\ ERR2}$	-3	0	3	dB	ATT=-16～-47dB
	Attenuation set error 3	$G_{V\ ERR3}$	-4	0	4	dB	ATT=-48～-79dB
	Output impedance	R_{OUT}	-	—	50	Ω	Vin=100mVrms
	Maximum output voltage	VOM	2	2.35	—	Vrms	THD+N=1% BW=400-30kHz
MIXING ATT (BD3461FS, BD3465FS)	Input impedance	$R_{IN\ M}$	70	100	130	kΩ	
	Maximum attenuation ＊	$G_{M\ MIN}$	—	-90	—	dB	G_M=20log(VOUT/VIN) BW=IHF-A, ATT=-∞dB
	Step resolution 1	$G_{M\ STEP1}$	—	8	—	dB	ATT=0～-32dB
	Step resolution 2	$G_{M\ STEP2}$	—	16	—	dB	ATT=-32～-64dB

VP-9690A(Average value detection, effective value display) filter by Matsushita Communication is used for ＊ measurement.
Phase between input / output is same.

●Electrical characteristic curves (Reference data)

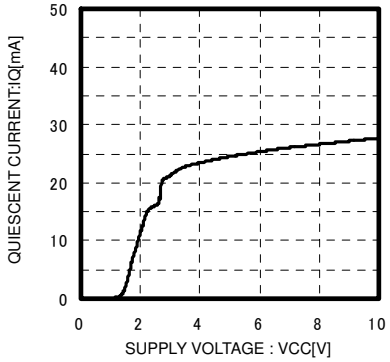


Fig.1 Iq vs Vcc

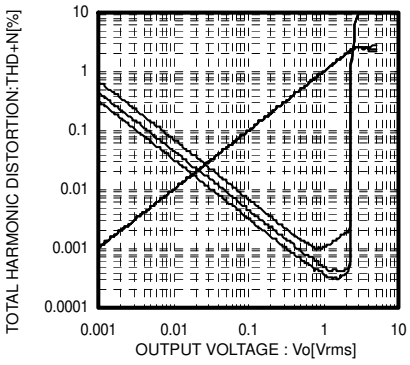


Fig.2 Thd vs Vo

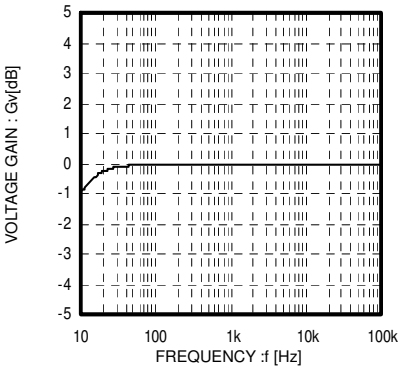


Fig.3 Gain vs Freq

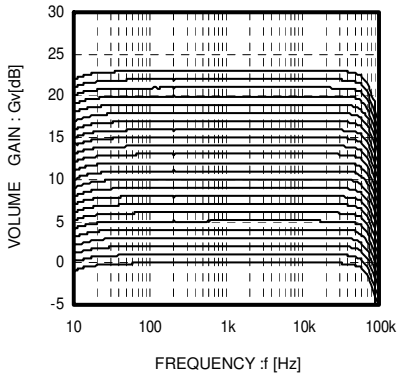


Fig.4 Volume Gain vs Freq
(0～+23dB)

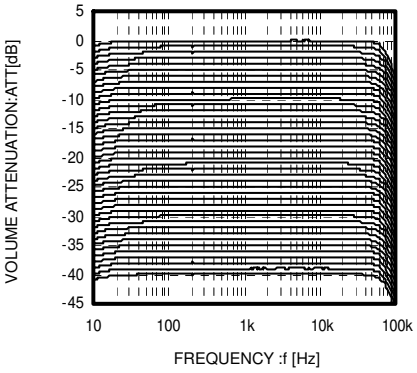


Fig.5 Volume Gain vs freq 1
(0～-40dB)

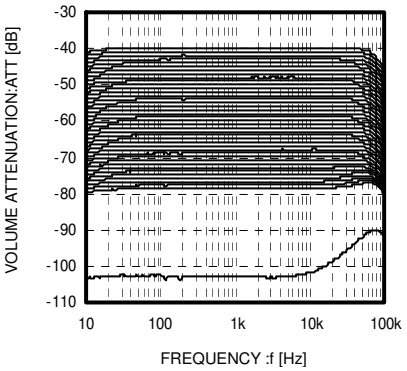


Fig.6 Volume Gain vs freq 2
(-41～-79dB)

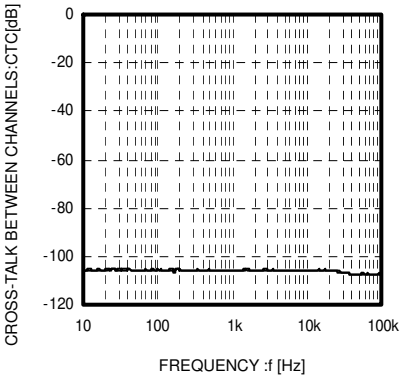


Fig.7 Cross-Talk vs Freq

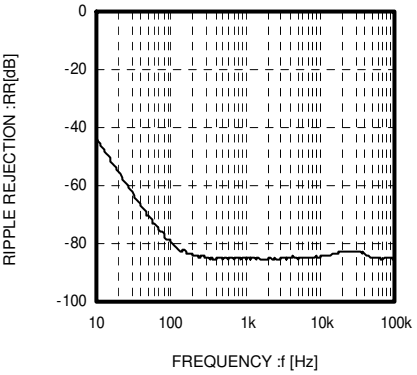


Fig.8 Ripple Rejection Ratio

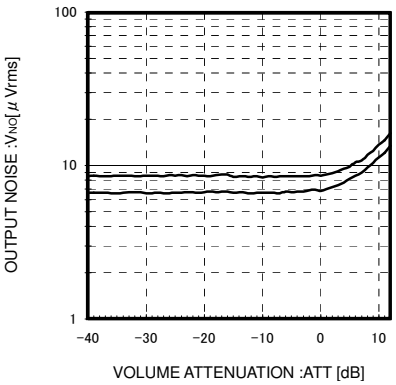


Fig.9 Volume Gain vs Noise

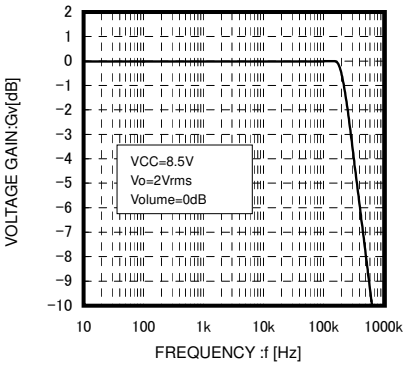


Fig.10 Volume gain of large
output level vs freq

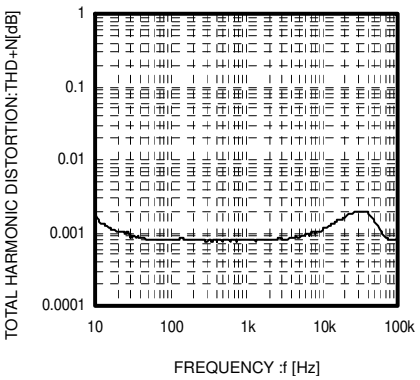


Fig.11 Thd vs freq

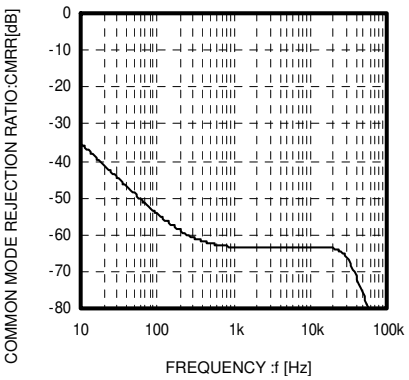


Fig.12 CMRR vs freq
(BD3460FS, BD3461FS)

●Electrical characteristic curves (Reference data) – Continued

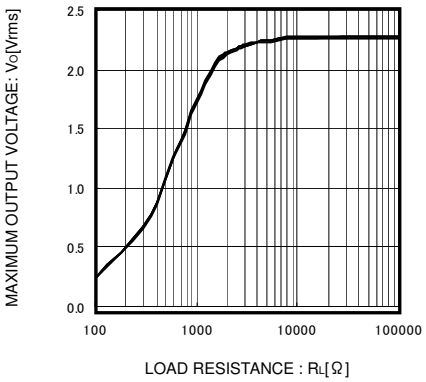


Fig.13 Rload vs Vo

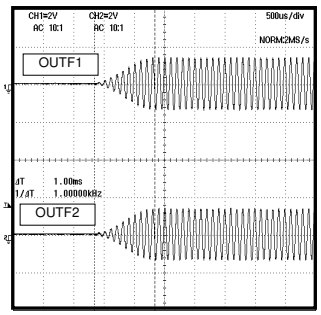


Fig.14 Advanced Switch 1

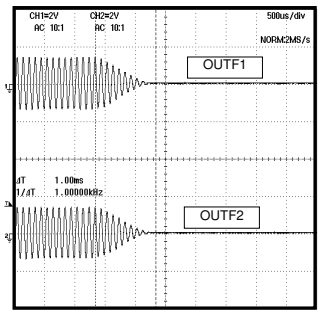


Fig.15 Advanced Switch 2

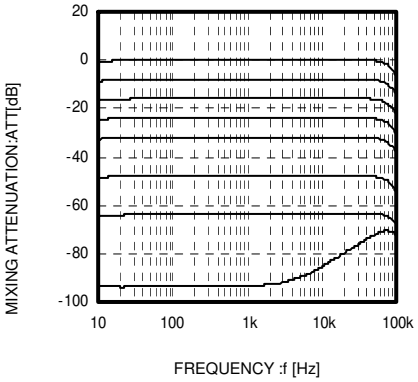


Fig.16 Mixing attenuation vs freq
(BD3461FS, BD3465FV)

●Block diagram and pin configuration

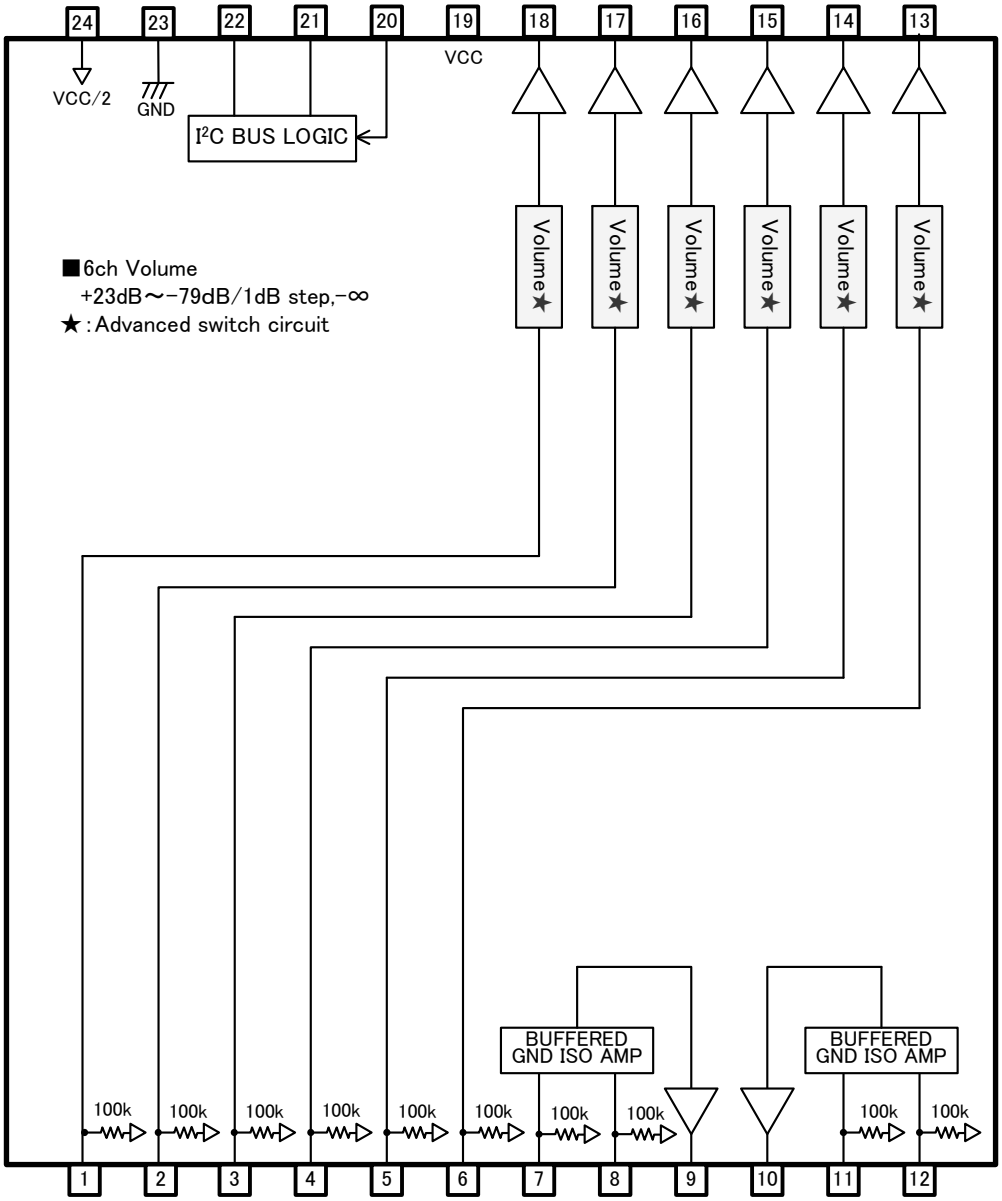


Fig.17 BD3460FS

Descriptions of terminal

Terminal No.	Terminal Name	Description	Terminal No.	Terminal Name	Description
1	INF1	Front input terminal of 1ch	13	OUTS2	Subwoofer output terminal of 2ch
2	INF2	Front input terminal of 2ch	14	OUTS1	Subwoofer output terminal of 1ch
3	INR1	Rear input terminal of 1ch	15	OUTR2	Rear output terminal of 2ch
4	INR2	Rear input terminal of 2ch	16	OUTR1	Rear output terminal of 1ch
5	INS1	Subwoofer input terminal of 1ch	17	OUTF2	Front output terminal of 2ch
6	INS2	Subwoofer input terminal of 2ch	18	OUTF1	Front output terminal of 1ch
7	PIN2	DIFF amp positive input terminal of 2ch	19	VCC	Power supply terminal
8	NIN2	DIFF amp negative input terminal of 2ch	20	CS	Chip select terminal
9	DIFFOUT2	DIFF amp output terminal of 2ch	21	SCL	I^2C Communication clock terminal
10	DIFFOUT1	DIFF amp output terminal of 1ch	22	SDA	I^2C Communication data terminal
11	NIN1	DIFF amp negative input terminal of 1ch	23	GND	GND terminal
12	PIN1	DIFF amp positive input terminal of 1ch	24	FIL	VCC/2 terminal

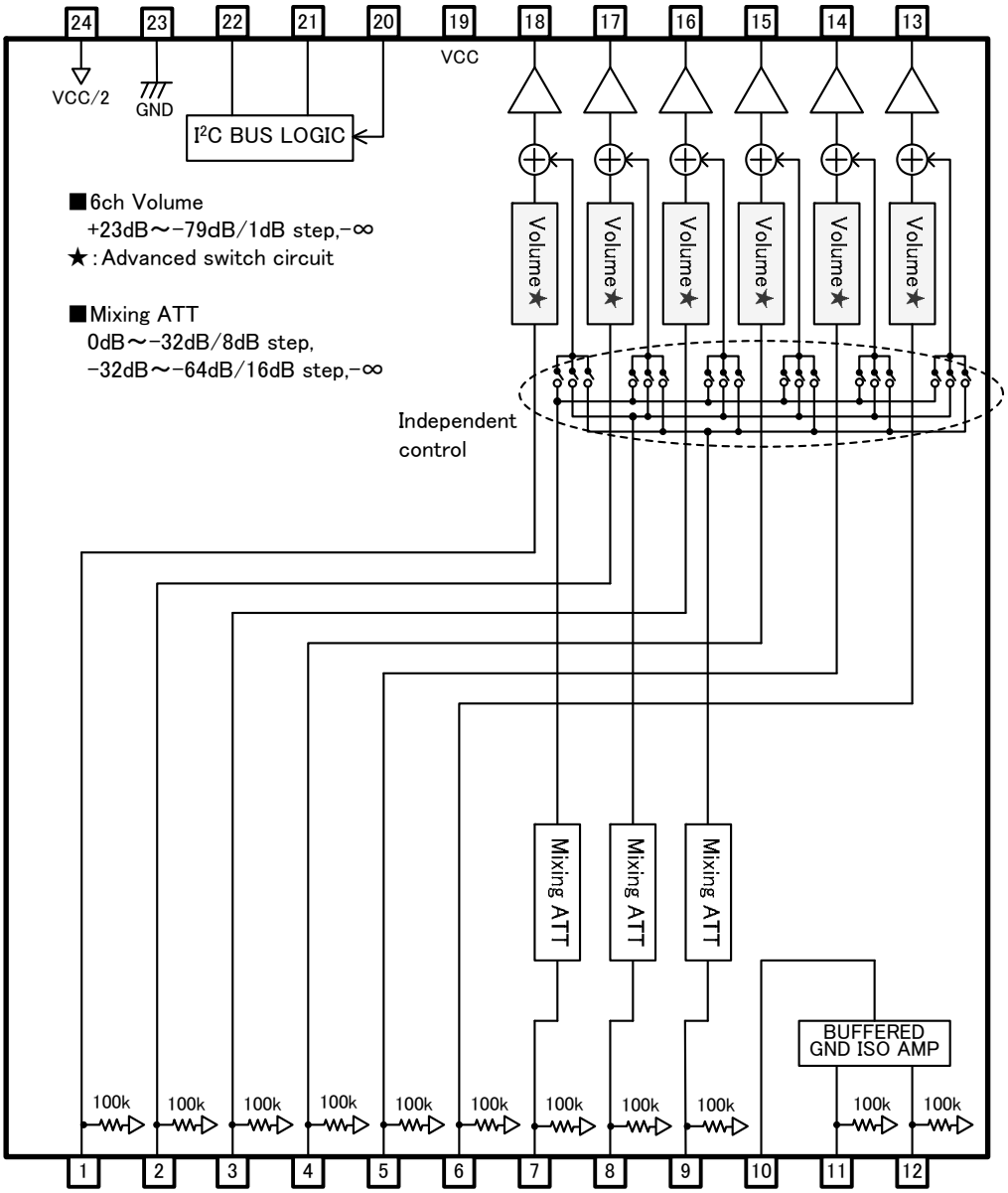


Fig.18 BD3461FS

Descriptions of terminal

Terminal No.	Terminal Name	Description	Terminal No.	Terminal Name	Description
1	INF1	Front input terminal of 1ch	13	OUTS2	Subwoofer output terminal of 2ch
2	INF2	Front input terminal of 2ch	14	OUTS1	Subwoofer output terminal of 1ch
3	INR1	Rear input terminal of 1ch	15	OUTR2	Rear output terminal of 2ch
4	INR2	Rear input terminal of 2ch	16	OUTR1	Rear output terminal of 1ch
5	INS1	Subwoofer input terminal of 1ch	17	OUTF2	Front output terminal of 2ch
6	INS2	Subwoofer input terminal of 2ch	18	OUTF1	Front output terminal of 1ch
7	EXT1	External input terminal of 1ch	19	VCC	Power supply terminal
8	EXT2	External input terminal of 2ch	20	CS	Chip select terminal
9	EXT3	External input terminal of 3ch	21	SCL	I^2C Communication clock terminal
10	DIFFOUT	DIFF amp output terminal	22	SDA	I^2C Communication data terminal
11	NIN	DIFF amp negative input terminal	23	GND	GND terminal
12	PIN	DIFF amp positive input terminal	24	FIL	VCC/2 terminal

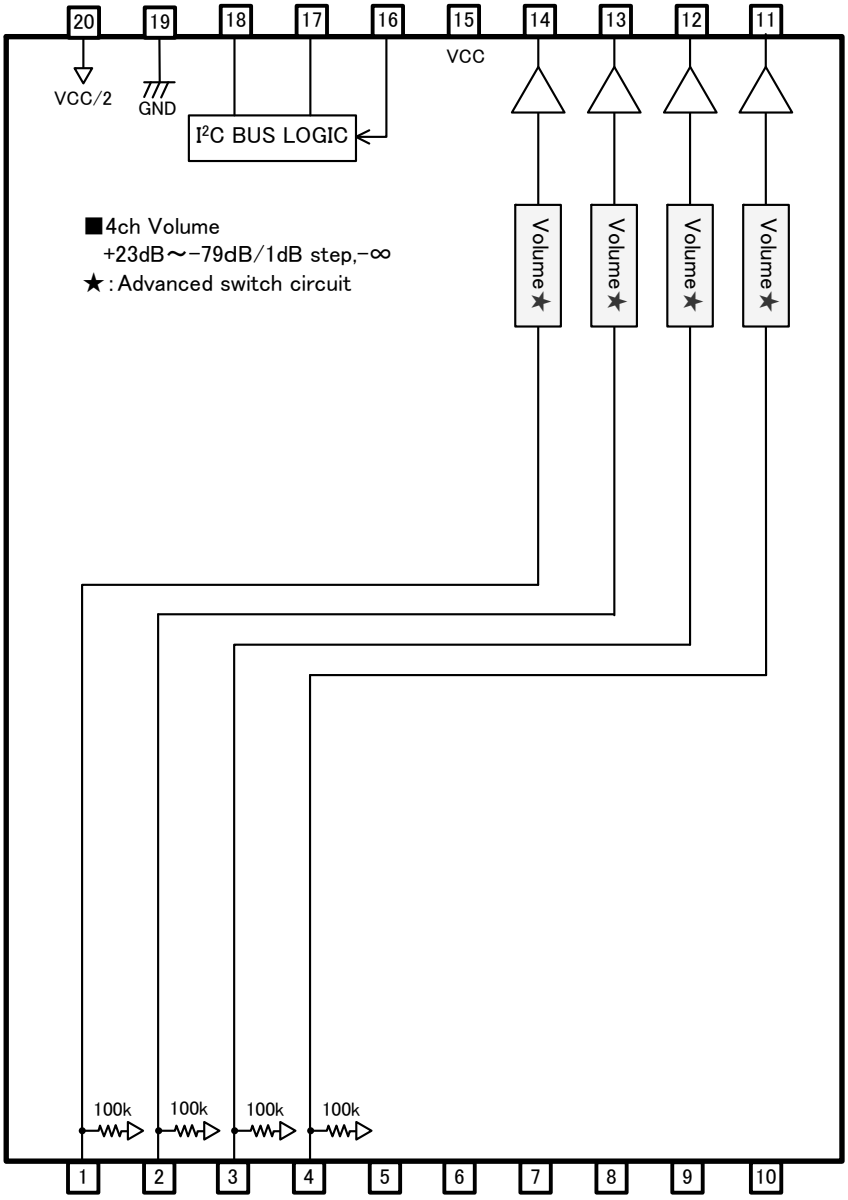


Fig.19 BD3464FV

Descriptions of terminal

Terminal No.	Terminal Name	Description	Terminal No.	Terminal Name	Description
1	INF1	Front input terminal of 1ch	11	OUTR2	Rear output terminal of 2ch
2	INF2	Front input terminal of 2ch	12	OUTR1	Rear output terminal of 1ch
3	INR1	Rear input terminal of 1ch	13	OUTF2	Front output terminal of 2ch
4	INR2	Rear input terminal of 2ch	14	OUTF1	Front output terminal of 1ch
5	NC		15	VCC	Power supply terminal
6	NC		16	CS	Chip select terminal
7	TEST1	Test Pin	17	SCL	I^2C Communication clock terminal
8	TEST2	Test Pin	18	SDA	I^2C Communication data terminal
9	TEST3	Test Pin	19	GND	GND terminal
10	NC		20	FIL	VCC/2 terminal

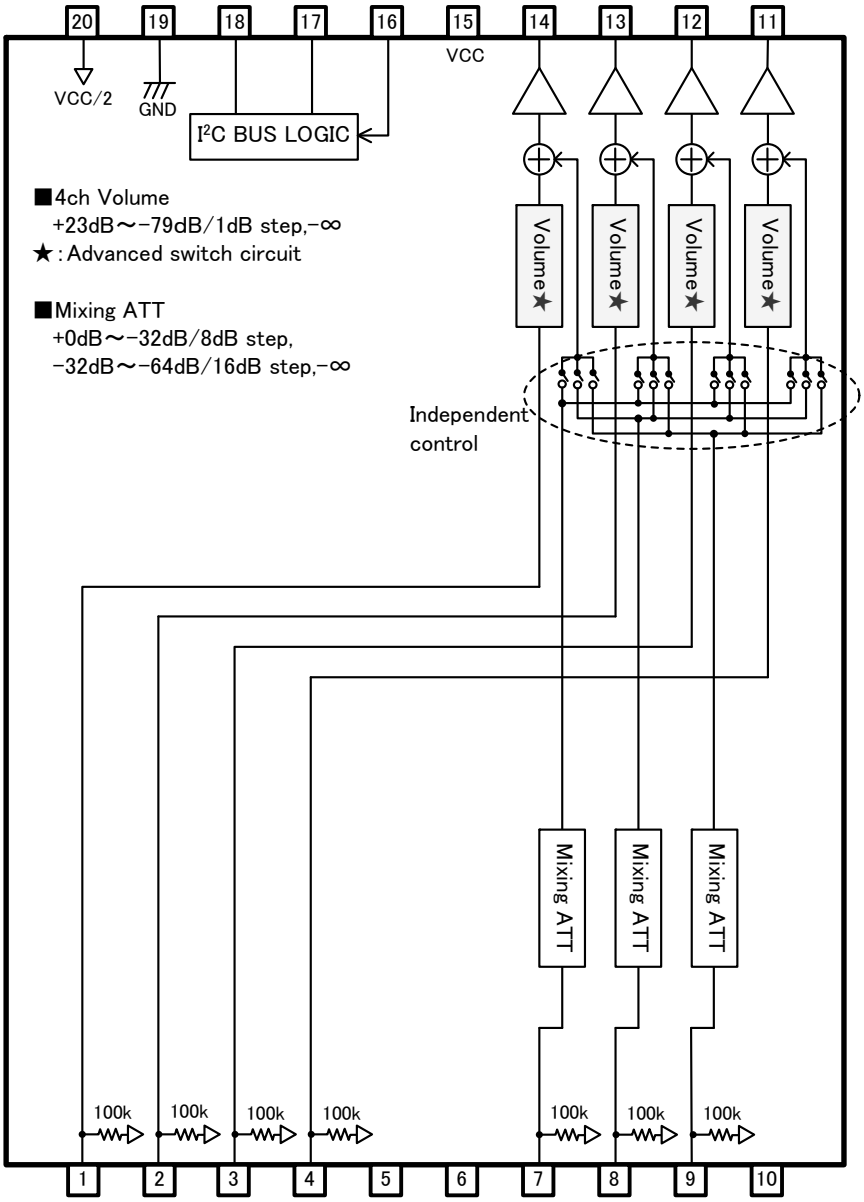


Fig.20 BD3465FV

Descriptions of terminal

Terminal No.	Terminal Name	Description	Terminal No.	Terminal Name	Description
1	INF1	Front input terminal of 1ch	11	OUTR2	Rear output terminal of 2ch
2	INF2	Front input terminal of 2ch	12	OUTR1	Rear output terminal of 1ch
3	INR1	Rear input terminal of 1ch	13	OUTF2	Front output terminal of 2ch
4	INR2	Rear input terminal of 2ch	14	OUTF1	Front output terminal of 1ch
5	NC		15	VCC	Power supply terminal
6	NC		16	CS	Chip select terminal
7	EXT1	External input terminal of 1ch	17	SCL	I^2C Communication clock terminal
8	EXT2	External input terminal of 2ch	18	SDA	I^2C Communication data terminal
9	EXT3	External input terminal of 3ch	19	GND	GND terminal
10	NC		20	FIL	VCC/2 terminal

●Timing Chart

CONTROL SIGNAL SPECIFICATION

(1) Electrical specifications and timing for bus lines and I/O stages

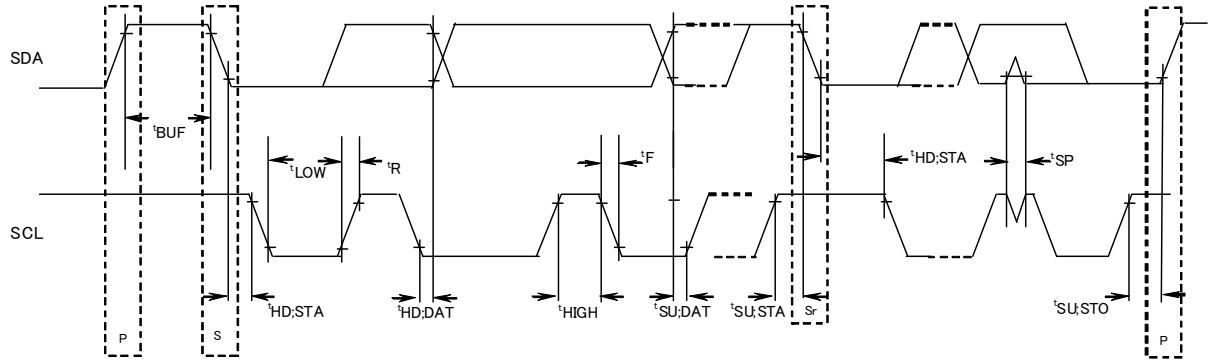


Fig.21 Definition of timing on the I²C-bus

Table 1 Characteristics of the SDA and SCL bus lines for I²C-bus devices
(Unless specified particularly, Ta=25℃, VCC=8.5V)

Parameter		Symbol	Fast-mode I²C-bus		Unit
			Min	Max	
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus free time between a STOP and START condition	tBUF	1.3	—	μS
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	0.6	—	μS
4	LOW period of the SCL clock	tLOW	1.3	—	μS
5	HIGH period of the SCL clock	tHIGH	0.6	—	μS
6	Set-up time for a repeated START condition	tSU;STA	0.6	—	μS
7	Data hold time	tHD;DAT	0*	—	μS
8	Data set-up time	tSU; DAT	100	—	ns
9	Set-up time for STOP condition	tSU;STO	0.6	—	μS

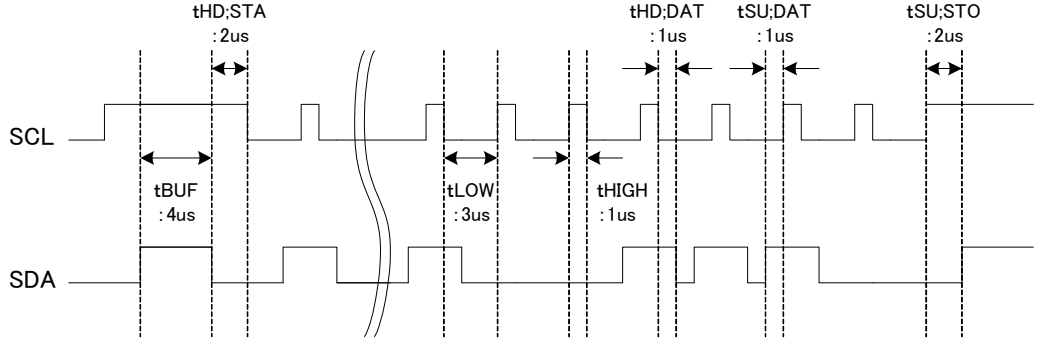
All values referred to VIH min. and VIL max. Levels (see Table 2).

* A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH min. of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

About 7(tHD;DAT), 8(tSU;DAT), make it the setup which a margin is fully in .

Table 2 Characteristics of the SDA and SCL I/O stages for I²C-bus devices

Parameter		Symbol	Fast-mode I²C-bus		Unit
			Min	Max	
10	LOW level input voltage	VIL	-0.5	1	V
11	HIGH level input voltage	VIH	2.3	—	V
12	Pulse width of spikes which must be suppressed by the input filter.	Tsp	0	50	ns
13	LOW level output voltage (open drain or open collector): at 3mA sink current	VOL1	0	0.4	V
14	Input current each I/O pin with an input voltage between 0.4V and 0.9 VDDmax.	Ii	-10	10	μA



SCL clock frequency: 250kHz

Fig.22 A command timing example in the I²C data transmission

(2)I²C BUS FORMAT

	MSB LSB		MSB LSB		MSB LSB			
S	Slave Address	A	Select Address	A	Data	A	P	
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit	

S = Start conditions (Recognition of start bit)
Slave Address = Recognition of slave address. 7 bits in upper order are voluntary. The least significant bit is "L" due to writing.
A = ACKNOWLEDGE bit (Recognition of acknowledgement)
Select Address = Select every of volume, bass and treble.
Data = Data on every volume and tone.
P = Stop condition (Recognition of stop bit)

(3)I²C BUS Interface Protocol

1)Basic form

S	Slave Address	A	Select Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

2)Automatic increment (Select Address increases (+1) according to the number of data.

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	····	DataN	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB			MSB LSB		

(Example) ①Data1 shall be set as data of address specified by Select Address.
②Data2 shall be set as data of address specified by Select Address +1.
③DataN shall be set as data of address specified by Select Address +N-1.

3)Configuration unavailable for transmission (In this case, only Select Address1 is set.

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

(Note)If any data is transmitted as Select Address 2 next to data, it is recognized as data, not as Select Address 2.

(4)Slave address

Because the slave address can be changed by the setting of CS, it is possible to use two chips at the same time on identical BUS.

	MSB → LSB							
SEL Voltage Condition	A6	A5	A4	A3	A2	A1	A0	R/W
GND ～ 0.2×VCC	1	0	0	0	0	0	0	0
0.8×VCC ～ VCC	1	0	0	0	0	1	0	0

80H
84H

Establish the voltage of CS in the condition to have been defined.

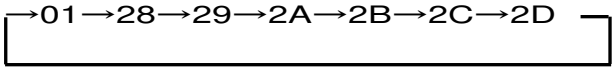
(5)Select Address & Data

BD3460FS, BD3464FV

Items to be set	Select Address (hex)	MSB	Data						LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Initial Setup 1	01	0	0	0	0	0	0	0	0
Volume 1ch Front	28	Volume Gain / Attenuation							
Volume 2ch Front	29	Volume Gain / Attenuation							
Volume 1ch Rear	2A	Volume Gain / Attenuation							
Volume 2ch Rear	2B	Volume Gain / Attenuation							
Volume 1ch Sub	2C	Volume Gain / Attenuation							
Volume 2ch Sub	2D	Volume Gain / Attenuation							
Test Mode	F0	0	0	0	0	0	0	0	0
System Reset	FE	1	0	0	0	0	0	0	1

Advanced switch

(Note)
1.In function changing of the hatching part, it works Advanced switch.
2.Select Address 2 C & 2 D can set only BD3460FS. Set all data of BD3464FV to "1".
3.Upon continuous data transfer, the Select Address is circulated by the automatic increment function, as shown below.

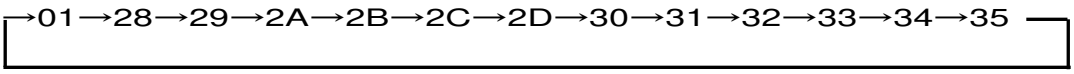


BD3461FS, BD3465FV

Items to be set	Select Address (hex)	MSB	Data						LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Initial Setup 1	01	0	0	0	0	0	1	0	0
Volume 1ch Front	28	Volume Gain / Attenuation							
Volume 2ch Front	29	Volume Gain / Attenuation							
Volume 1ch Rear	2A	Volume Gain / Attenuation							
Volume 2ch Rear	2B	Volume Gain / Attenuation							
Volume 1ch Sub	2C	Volume Gain / Attenuation							
Volume 2ch Sub	2D	Volume Gain / Attenuation							
EXT 1 ON/OFF	30	EXT1 S2	EXT1 S1	EXT1 R2	EXT1 R1	EXT1 F2	EXT1 F1	0	0
EXT 2 ON/OFF	31	EXT2 S2	EXT2 S1	EXT2 R2	EXT2 R1	EXT2 F2	EXT2 F1	0	0
EXT 3 ON/OFF	32	EXT3 S2	EXT3 S1	EXT3 R2	EXT3 R1	EXT3 F2	EXT3 F1	0	0
EXT 1 ATT	33	0	0	0	0	0	EXT1 Attenuation		
EXT 2 ATT	34	0	0	0	0	0	EXT2 Attenuation		
EXT 3 ATT	35	0	0	0	0	0	EXT3 Attenuation		
Test Mode	F0	0	0	0	0	0	0	0	0
System Reset	FE	1	0	0	0	0	0	0	1

Advanced switch

(Note)
1. In function changing of the hatching part, it works Advanced switch.
2. Select Address 2 C & 2 D can set only BD3461FS. Set all data of BD3465FV to "1".
3. Upon continuous data transfer, the Select Address is circulated by the automatic increment function, as shown below.



4. When changing “EXT = ON/OFF”, it is not corresponded for advance switch. Therefore, please do the measure that applies mute on the side of a set at the time of these setting changes

Select address 28, 29, 2A, 2B, 2C 2D(hex)

Gain & ATT	MSB	Volume Gain/Attenuation					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition ※	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
	0	1	1	0	1	0	0	0
23dB	0	1	1	0	1	0	0	1
22dB	0	1	1	0	1	0	1	0
21dB	0	1	1	0	1	0	1	1
:	:	:	:	:	:	:	:	:
-78dB	1	1	0	0	1	1	1	0
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
Prohibition ※	1	1	0	1	0	0	0	0
	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
−∞dB	1	1	1	1	1	1	1	1

※ Gain is set to “-∞dB” when sending “Prohibition data”.

※ Select Address 2 C & 2 D can set only BD3460FS, BD3461FS.
Set all data of BD3464FV & BD3465FV to "1".

Select address 30, 31, 32(hex)

MODE	MSB	EXT1 F1						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	EXT1 S2	EXT1 S1	EXT1 R2	EXT1 R1	EXT1 F2	0	0	0
ON						1		

MODE	MSB	EXT1 F2						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	EXT1 S2	EXT1 S1	EXT1 R2	EXT1 R1	0	EXT1 F1	0	0
ON					1			

MODE	MSB	EXT1 R1						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	EXT1 S2	EXT1 S1	EXT1 R2	0	EXT1 F2	EXT1 F1	0	0
ON				1				

MODE	MSB	EXT1 R2						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	EXT1 S2	EXT1 S1	0	EXT1 R1	EXT1 F2	EXT1 F1	0	0
ON			1					

MODE	MSB	EXT1 S1						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	EXT1 S2	0	EXT1 R2	EXT1 R1	EXT1 F2	EXT1 F1	0	0
ON		1						

MODE	MSB	EXT1 S2						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	EXT1 S1	EXT1 R2	EXT1 R1	EXT1 F2	EXT1 F1	0	0
ON	1							

:Initial condition

Select address 33, 34, 35(hex)

Gain	MSB	EXT Attenuation					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	0	0	0	0	0	0	0	0
-8dB						0	0	1
-16dB						0	1	0
-24dB						0	1	1
-32dB						1	0	0
-48dB						1	0	1
-64dB						1	1	0
−∞dB						1	1	1

※ Select Address 30, 31 32, 33, 34, 35 can set only BD3461FS & BD3465FV.

:Initial condition

(6)About power on reset

At one of supply voltage circuit made initialization inside IC is built-in. Please send data to all address as initial data at supply voltage on. And please supply mute at set side until this initial data is sent.

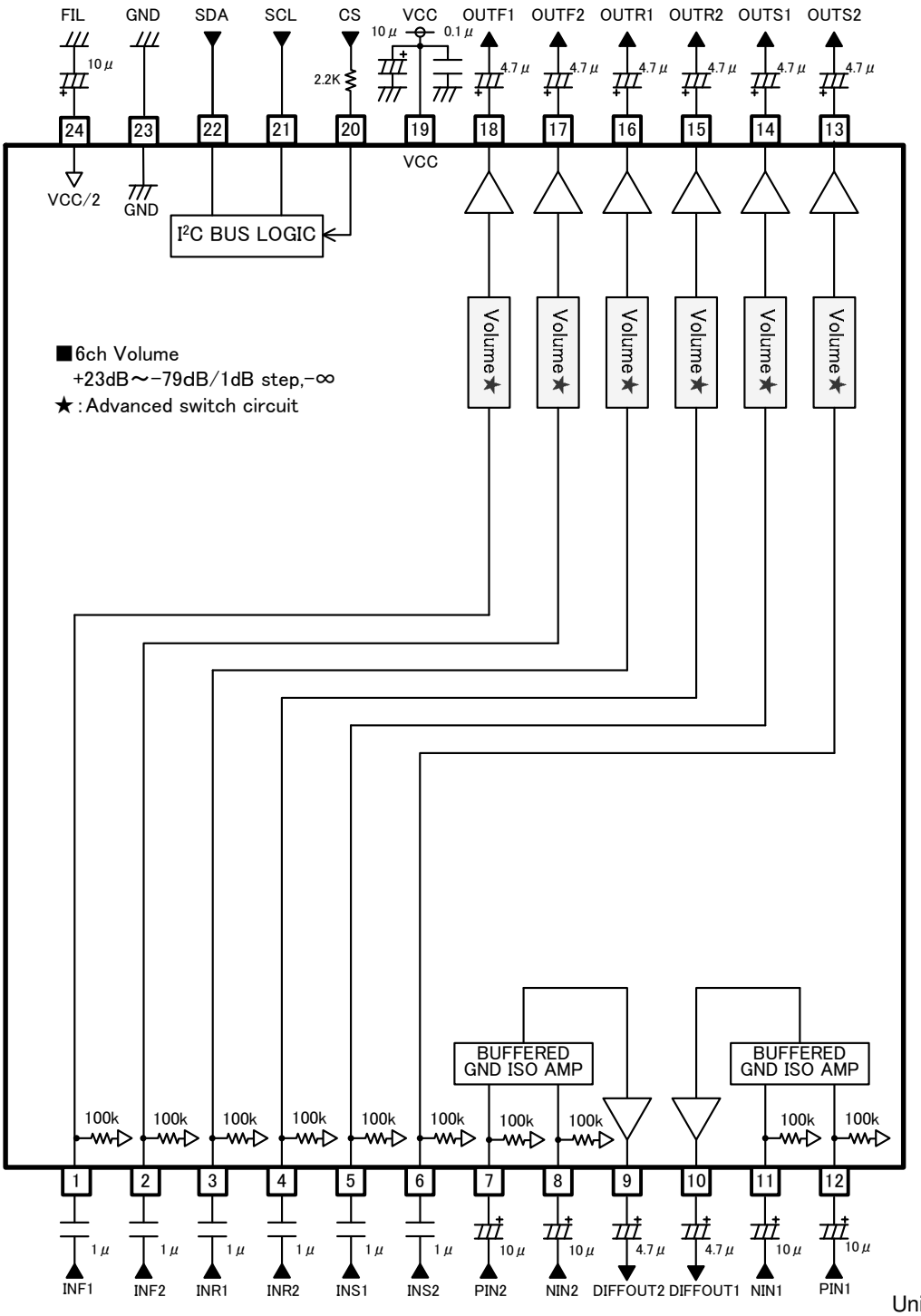
Item	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Rise time of VCC	Trise	20	—	—	μsec	VCC rise time from 0V to 3V
VCC voltage of release power on reset	Vpor	—	4.1	—	V	

Volume gain/attenuation of the details

(dB)	D7	D6	D5	D4	D3	D2	D1	D0		(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+23	0	1	1	0	1	0	0	1		-29	1	0	0	1	1	1	0	1
+22	0	1	1	0	1	0	1	0		-30	1	0	0	1	1	1	1	0
+21	0	1	1	0	1	0	1	1		-31	1	0	0	1	1	1	1	1
+20	0	1	1	0	1	1	0	0		-32	1	0	1	0	0	0	0	0
+19	0	1	1	0	1	1	0	1		-33	1	0	1	0	0	0	0	1
+18	0	1	1	0	1	1	1	0		-34	1	0	1	0	0	0	1	0
+17	0	1	1	0	1	1	1	1		-35	1	0	1	0	0	0	1	1
+16	0	1	1	1	0	0	0	0		-36	1	0	1	0	0	1	0	0
+15	0	1	1	1	0	0	0	1		-37	1	0	1	0	0	1	0	1
+14	0	1	1	1	0	0	1	0		-38	1	0	1	0	0	1	1	0
+13	0	1	1	1	0	0	1	1		-39	1	0	1	0	0	1	1	1
+12	0	1	1	1	0	1	0	0		-40	1	0	1	0	1	0	0	0
+11	0	1	1	1	0	1	0	1		-41	1	0	1	0	1	0	0	1
+10	0	1	1	1	0	1	1	0		-42	1	0	1	0	1	0	1	0
+9	0	1	1	1	0	1	1	1		-43	1	0	1	0	1	0	1	1
+8	0	1	1	1	1	0	0	0		-44	1	0	1	0	1	1	0	0
+7	0	1	1	1	1	0	0	1		-45	1	0	1	0	1	1	0	1
+6	0	1	1	1	1	0	1	0		-46	1	0	1	0	1	1	1	0
+5	0	1	1	1	1	0	1	1		-47	1	0	1	0	1	1	1	1
+4	0	1	1	1	1	1	0	0		-48	1	0	1	1	0	0	0	0
+3	0	1	1	1	1	1	0	1		-49	1	0	1	1	0	0	0	1
+2	0	1	1	1	1	1	1	0		-50	1	0	1	1	0	0	1	0
+1	0	1	1	1	1	1	1	1		-51	1	0	1	1	0	0	1	1
0	1	0	0	0	0	0	0	0		-52	1	0	1	1	0	1	0	0
-1	1	0	0	0	0	0	0	1		-53	1	0	1	1	0	1	0	1
-2	1	0	0	0	0	0	1	0		-54	1	0	1	1	0	1	1	0
-3	1	0	0	0	0	0	1	1		-55	1	0	1	1	0	1	1	1
-4	1	0	0	0	0	1	0	0		-56	1	0	1	1	1	0	0	0
-5	1	0	0	0	0	1	0	1		-57	1	0	1	1	1	0	0	1
-6	1	0	0	0	0	1	1	0		-58	1	0	1	1	1	0	1	0
-7	1	0	0	0	0	1	1	1		-59	1	0	1	1	1	0	1	1
-8	1	0	0	0	1	0	0	0		-60	1	0	1	1	1	1	0	0
-9	1	0	0	0	1	0	0	1		-61	1	0	1	1	1	1	0	1
-10	1	0	0	0	1	0	1	0		-62	1	0	1	1	1	1	1	0
-11	1	0	0	0	1	0	1	1		-63	1	0	1	1	1	1	1	1
-12	1	0	0	0	1	1	0	0		-64	1	1	0	0	0	0	0	0
-13	1	0	0	0	1	1	0	1		-65	1	1	0	0	0	0	0	1
-14	1	0	0	0	1	1	1	0		-66	1	1	0	0	0	0	1	0
-15	1	0	0	0	1	1	1	1		-67	1	1	0	0	0	0	1	1
-16	1	0	0	1	0	0	0	0		-68	1	1	0	0	0	1	0	0
-17	1	0	0	1	0	0	0	1		-69	1	1	0	0	0	1	0	1
-18	1	0	0	1	0	0	1	0		-70	1	1	0	0	0	1	1	0
-19	1	0	0	1	0	0	1	1		-71	1	1	0	0	0	1	1	1
-20	1	0	0	1	0	1	0	0		-72	1	1	0	0	1	0	0	0
-21	1	0	0	1	0	1	0	1		-73	1	1	0	0	1	0	0	1
-22	1	0	0	1	0	1	1	0		-74	1	1	0	0	1	0	1	0
-23	1	0	0	1	0	1	1	1		-75	1	1	0	0	1	0	1	1
-24	1	0	0	1	1	0	0	0		-76	1	1	0	0	1	1	0	0
-25	1	0	0	1	1	0	0	1		-77	1	1	0	0	1	1	0	1
-26	1	0	0	1	1	0	1	0		-78	1	1	0	0	1	1	1	0
-27	1	0	0	1	1	0	1	1		-79	1	1	0	0	1	1	1	1
-28	1	0	0	1	1	1	0	0		−∞	1	1	1	1	1	1	1	1

: Initial condition

●Application Circuit Diagram



Unit
R : [Ω]
C : [F]

Fig.23 BD3460FS

Notes on wiring

① Please connect the decoupling capacitor of a power supply in the shortest distance as much as possible to GND.
② Lines of GND shall be one-point connected.
③ Wiring pattern of Digital shall be away from that of analog unit and cross-talk shall not be acceptable.
④ Lines of SCL and SDA of I^2C BUS shall not be parallel if possible.
The lines shall be shielded, if they are adjacent to each other.
⑤ Lines of analog input shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.

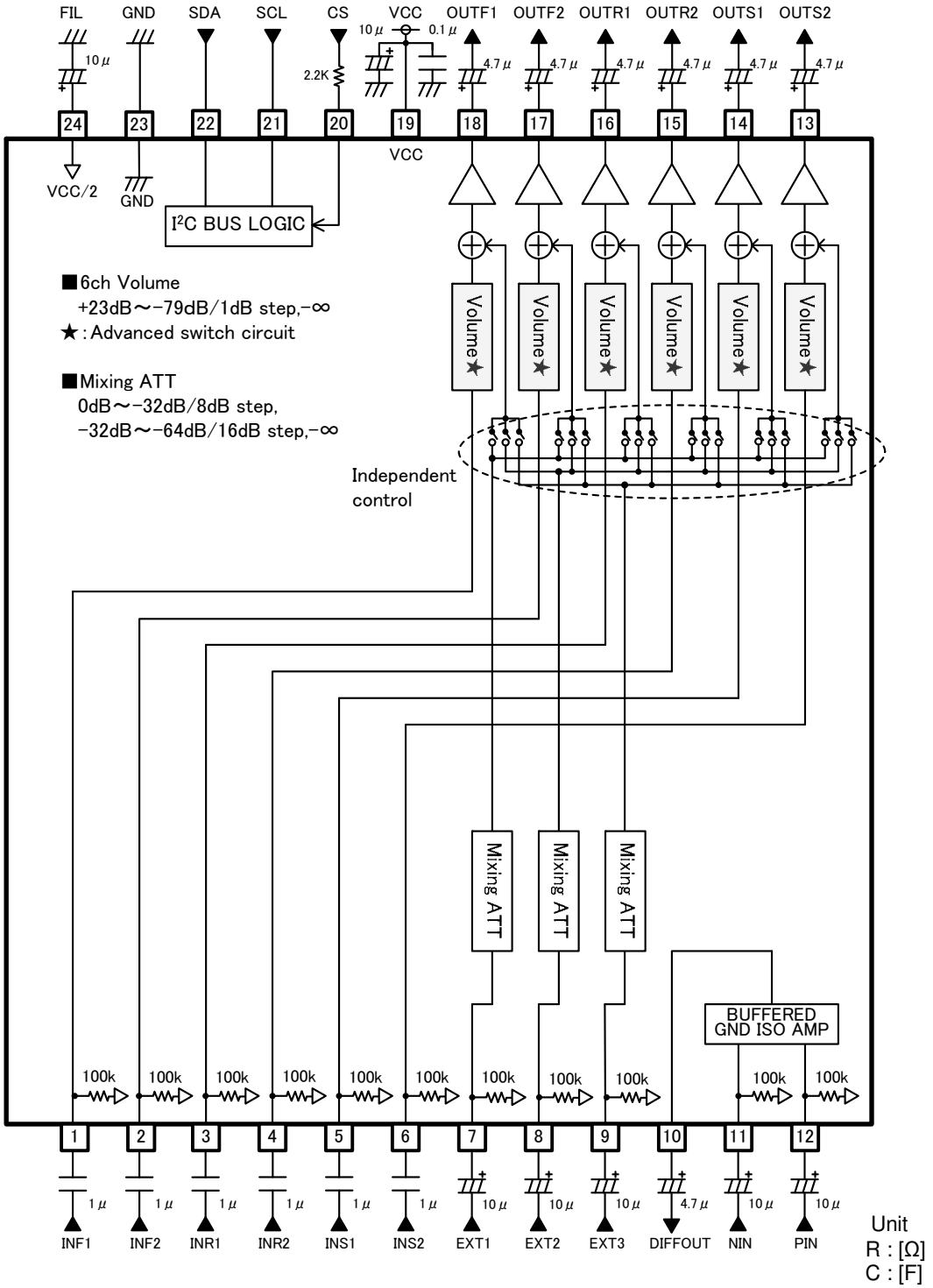


Fig.24 BD3461FS

Notes on wiring

① Please connect the decoupling capacitor of a power supply in the shortest distance as much as possible to GND.
② Lines of GND shall be one-point connected.
③ Wiring pattern of Digital shall be away from that of analog unit and cross-talk shall not be acceptable.
④ Lines of SCL and SDA of I^2C BUS shall not be parallel if possible.
The lines shall be shielded, if they are adjacent to each other.
⑤ Lines of analog input shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.

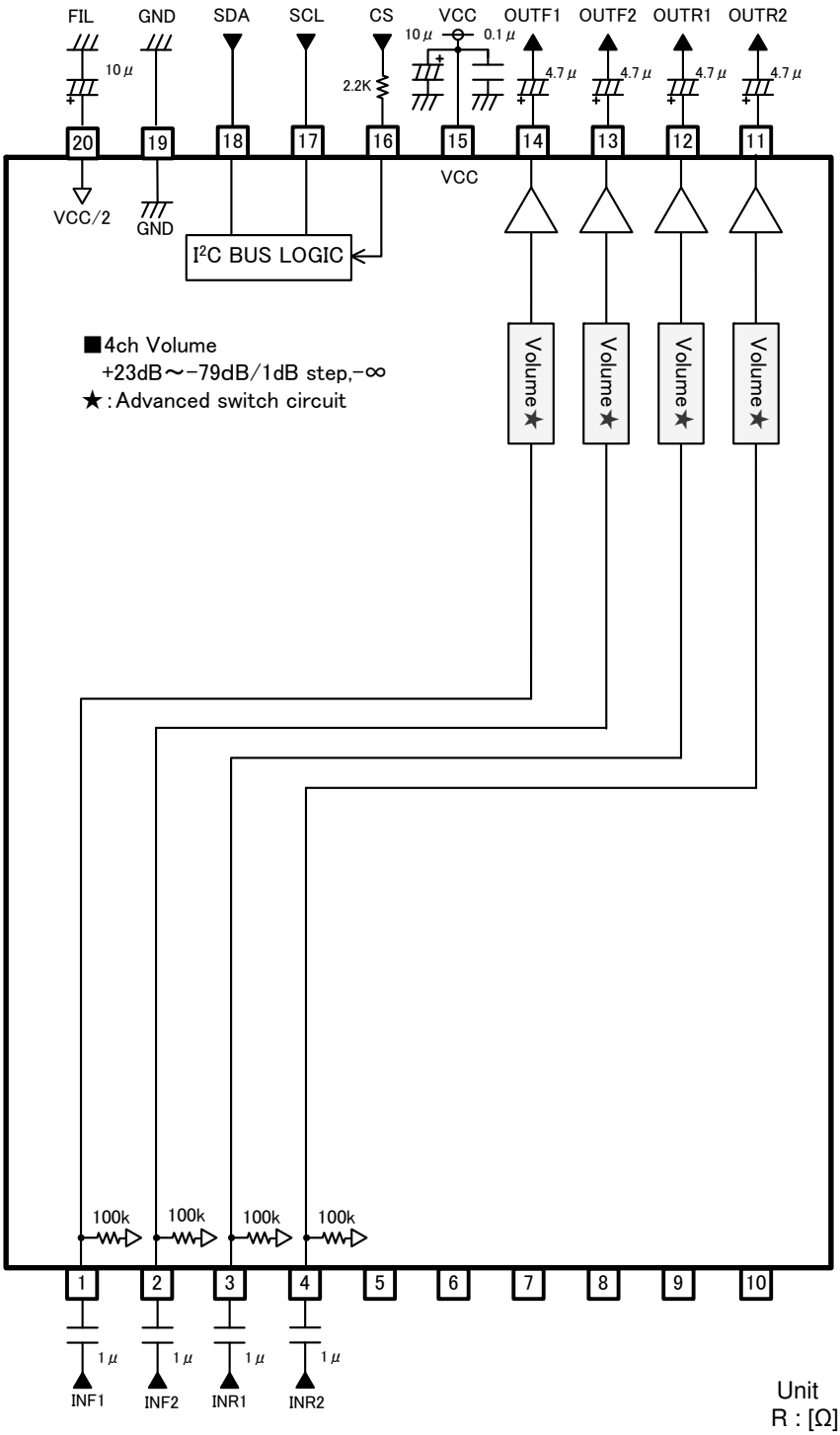


Fig.25 BD3464FV

Notes on wiring

① Please connect the decoupling capacitor of a power supply in the shortest distance as much as possible to GND.
② Lines of GND shall be one-point connected.
③ Wiring pattern of Digital shall be away from that of analog unit and cross-talk shall not be acceptable.
④ Lines of SCL and SDA of I^2C BUS shall not be parallel if possible.
The lines shall be shielded, if they are adjacent to each other.
⑤ Lines of analog input shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.

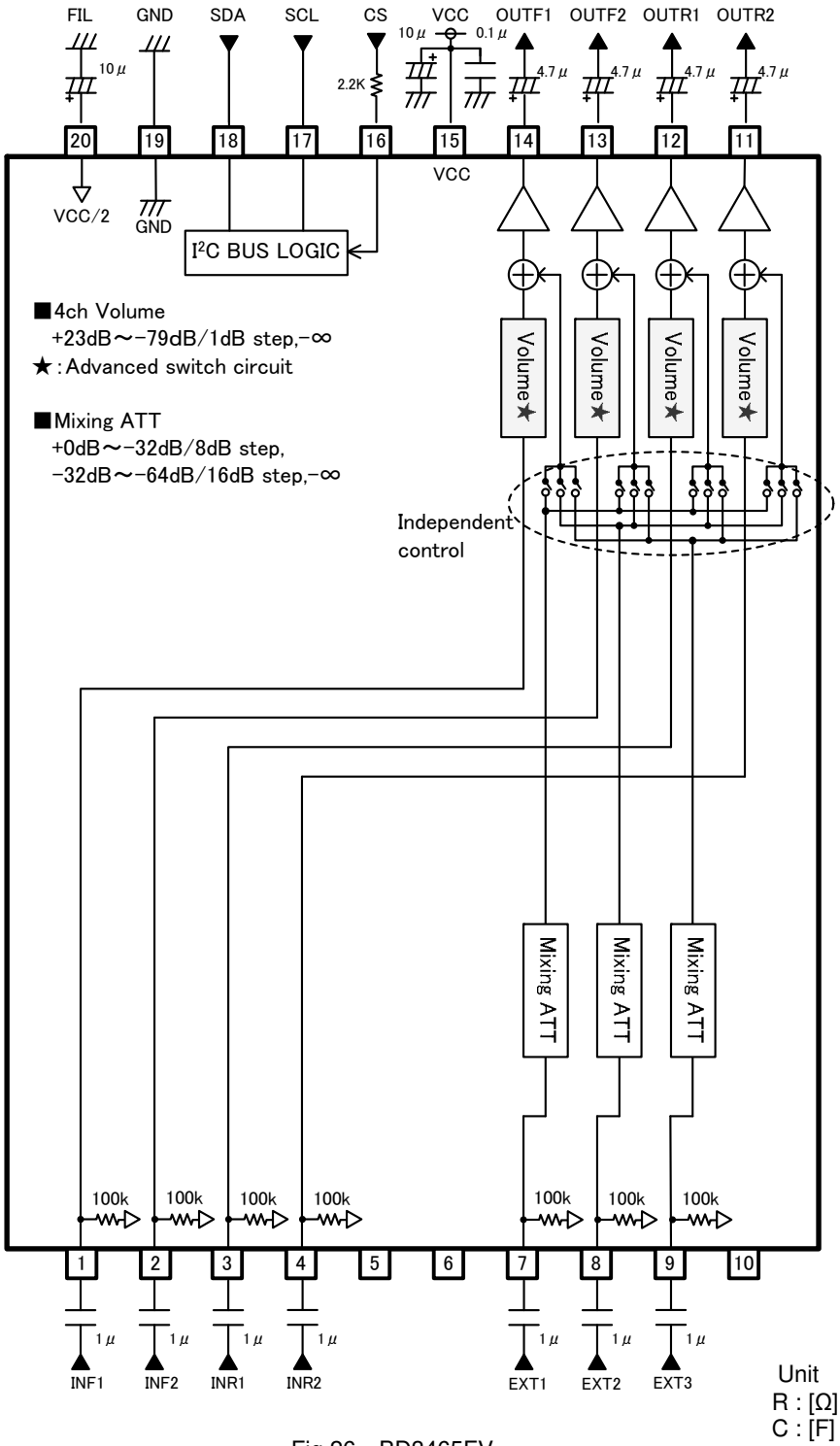
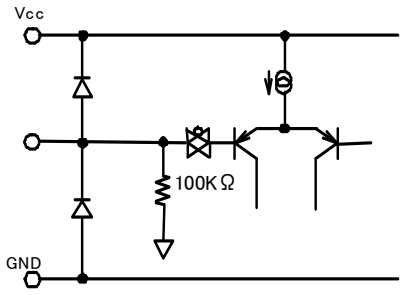
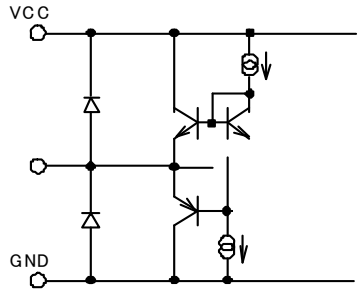
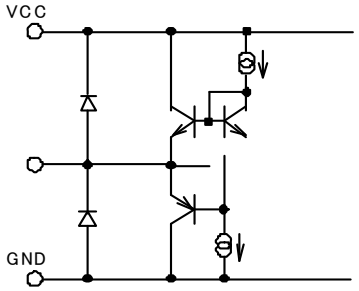


Fig.26 BD3465FV

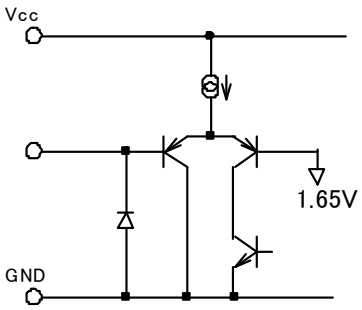
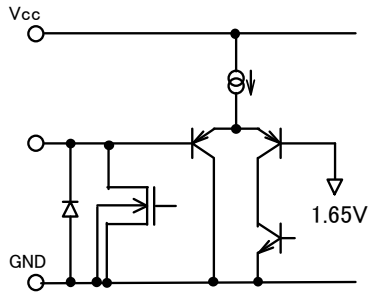
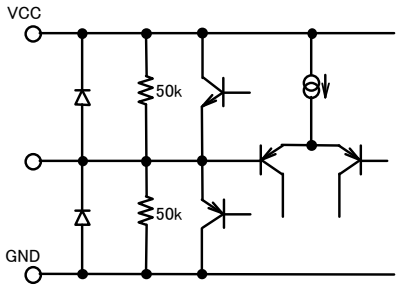
Notes on wiring

① Please connect the decoupling capacitor of a power supply in the shortest distance as much as possible to GND.
② Lines of GND shall be one-point connected.
③ Wiring pattern of Digital shall be away from that of analog unit and cross-talk shall not be acceptable.
④ Lines of SCL and SDA of I^2C BUS shall not be parallel if possible.
The lines shall be shielded, if they are adjacent to each other.
⑤ Lines of analog input shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.

●Interfaces

Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
INF1 INF2 INR1 INR2 INS1 INS2 PIN2 NIN2 NIN1 PIN1 NIN PIN EXT1 EXT2 EXT3	4.25		A terminal for signal input. The input impedance is 100kΩ(typ). INS1 and INS2 are only BD3460FS and BD3461FS's terminals, PIN2,NIN2,NIN1 and PIN1 are only BD3460FS's one, NIN and PIN are only BD3461FS's one, EXT1,EXT2 and EXT3 are only BD3461FS and BD3465FV's one.
DIFOUT2 DIFOUT1 DIFOUT OUTS2 OUTS1 OUTR2 OUTR1 OUTF2 OUTF1	4.25		A terminal for fader output. DIFOUT2 and DIFOUT1 are only BD3460FS's terminals, DIFOUT is only BD3461FS's one, OUTS2, and OUTS1 are only BD3460FS and BD3461FS's one.
CS	–		A terminal for slave addresses selection. "CS" is "High"→slave address "84 H" "CS" is "Low"→ slave address "80 H"

The figure in the pin explanation and input/output equivalent circuit is reference value, it doesn't guarantee the value.

Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
VCC	8.5		Power supply terminal.
SCL	—		A terminal for clock input of I^2C BUS communication.
SDA	—		A terminal for data input of I^2C BUS communication.
GND	0		Ground terminal.
FIL	4.25		Voltage for reference bias of analog signal system. The simple precharge circuit and simple discharge circuit for an external capacitor are built in.

The figure in the pin explanation and input/output equivalent circuit is reference value, it doesn't guarantee the value.

●Notes for use

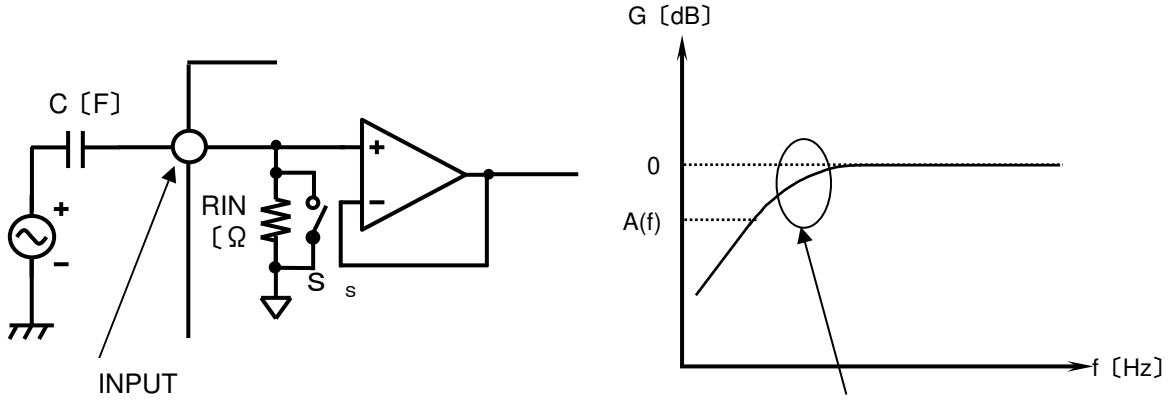
1. Absolute maximum rating voltage

When it impressed the voltage on VCC more than the absolute maximum rating voltage, circuit currents increase rapidly, and there is absolutely a case to reach characteristic deterioration and destruction of a device. In particular in a serge examination of a set, when it is expected the impressing serge at VCC terminal, please do not impress the large and over the absolute maximum rating voltage (including a operating voltage + serge ingredient (around 14V)).

2. About a signal input part

1)About constant set up of input coupling capacitor

In the signal input terminal, the constant setting of input coupling capacitor C(F) be sufficient input impedance $R_{IN}(\Omega)$ inside IC and please decide. The first HPF characteristic of RC is composed.



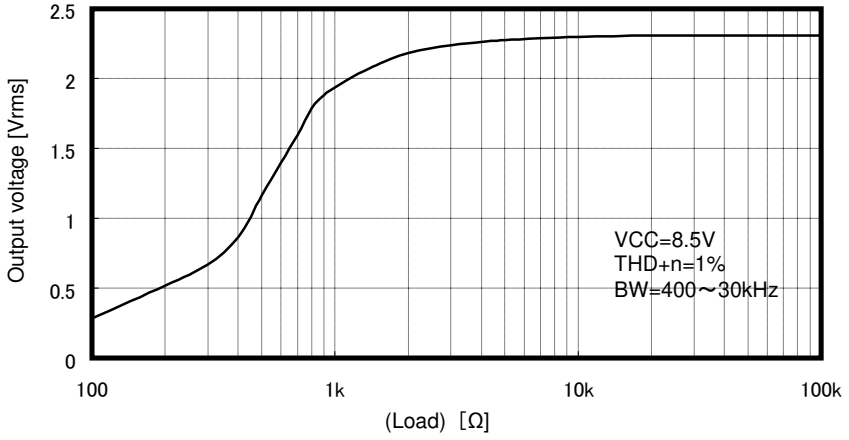
$$A(f) = \sqrt{\frac{(2\pi fCR_{IN})^2}{1+(2\pi fCR_{IN})^2}}$$

3. About output load characteristics)

The usages of load for output are below (reference). Please use the load more than 10[kΩ](TYP).

Output pin on target

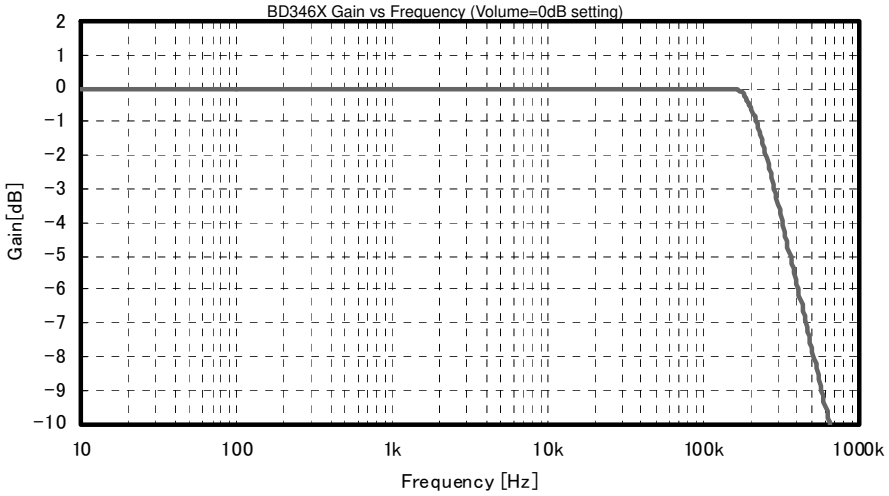
Pin Name	Pin name	Pin name	Pin name	Pin name
OUTF1	OUTR1	OUTS1	DIFOUT1	DIFOUT
OUTF2	OUTR2	OUTS2	DIFOUT2	



Output load characteristic at Vcc=8.5V. (Reference)

4. Frequency characteristic at large output level

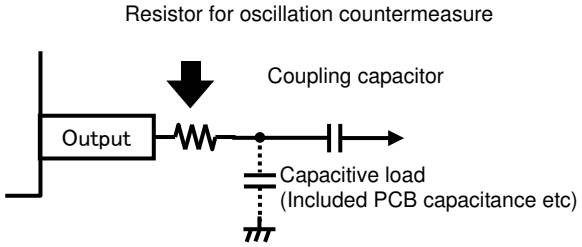
High slew-rate amplifiers are used for high quality sound. This IC is corresponded to “192kHz sampling on DVD-Audio highest quality”. Output level is “2Vrms, 192kHz flat(typ)”.
(See the below graph (reference)).



5. Oscillation countermeasure for GND isolation amplifier outputs

Using higher capacitor than 10pF at GND isolation amplifier outputs (DIFOUT1, DIFOUT2, DIFOUT) may cause oscillation. As oscillation countermeasure, insert resistor in series to terminal directly as below.

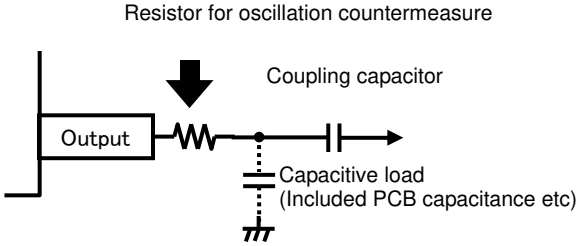
Capacitance	Resistor in series to terminal directly
C＜10pF	Not necessary
10＜C＜100pF	220Ω



6. Oscillation countermeasure for volume outputs at power supply ON/OFF

If using higher capacitor than 22pF at volume outputs, oscillation may occur a moment when turning ON/OFF power supply (when VCC is about 3～4 V). As oscillation countermeasure, insert resistor in series to terminal directly as below, and set volume output mute outside this device when turning ON/OFF power supply.

Capacitance	Resistor in series to terminal directly
C＜22pF	Not necessary
22＜C＜220pF	220Ω



7. I2C BUS Transferring Data

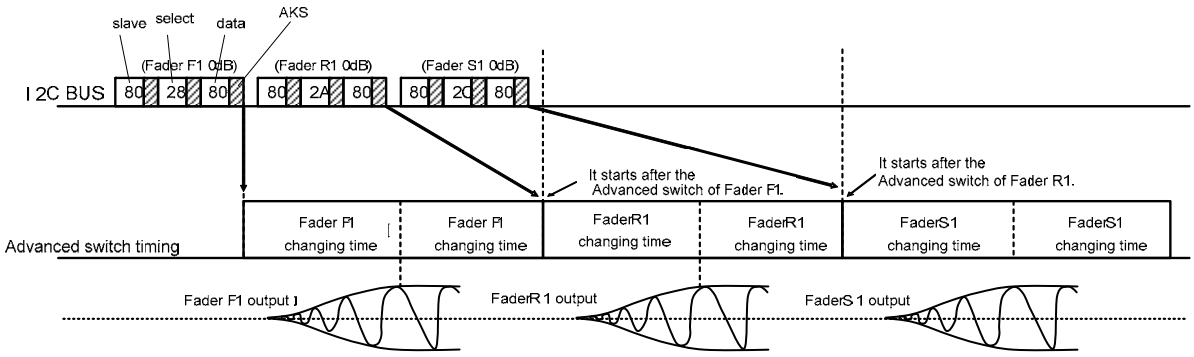
【1】The kind of the Transferring Data

1-1. he data setup except Advanced switch (the data without hatching of a data format) does not have the regulation on transferring data.
1-2. The data setup of Advanced switch (the data with hatching of a data format) does not have the regulation on transferring data too. But Advanced switch order follows the following 【2】.

【2】Transferring data of the Advanced switch

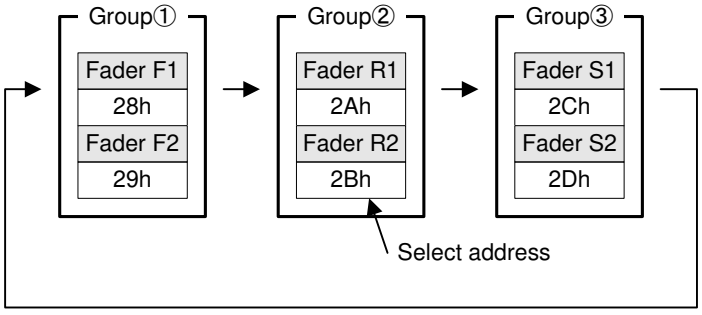
2-1. The timing chart from the transferring data timing to the Advanced switch start timing is as follows.

■Transferring data example 1



It is the same even if it transfers data in auto increment mode.

There are no timing regulations of I^2C BUS transferring data. But the timing of a change start after the end of the present change. In addition, the timing of Advanced switch is not depended of a transferring data turn, but conforms in turn of the following figure.

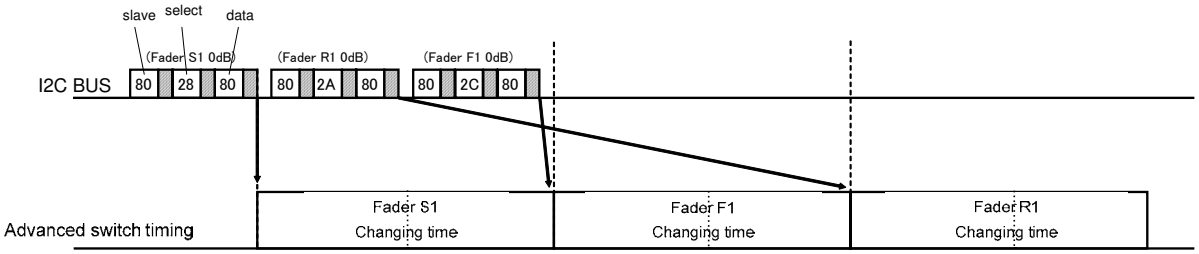


The turn of Advanced switch start

The block in the same group can start the Advanced switch in the same time.

■Transferring data example 2

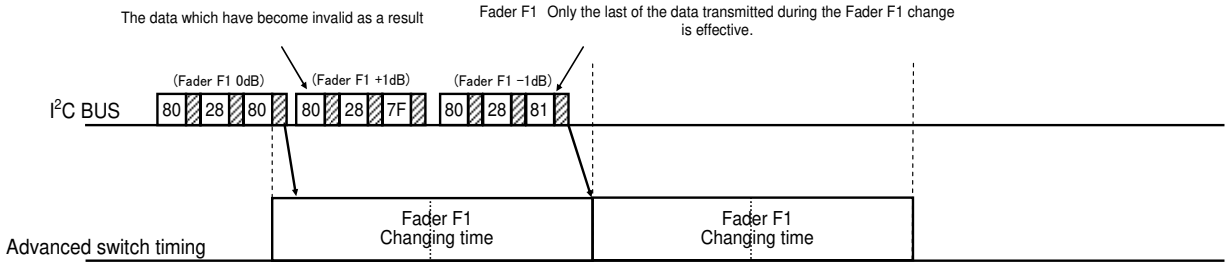
The transferring data turn differs from the actual change turn as below.



Please transfer data after the present Advanced switch, if it wants to make a transferring data turn and Advanced switch turn the same.

■Transferring data example 3

Priority is given to the data of the same select address when it is transferred to the timing which Advanced switch has not ended. In addition, when two or more data are transferred to the same select address, the end transferred data is effective.



■Transferring data example 4

Refresh data is the same as the present setup data, therefore Advanced switch does not change.

The gain change data of other channels are transferred after refresh data as below.