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Sound Processors for Home Theater Systems

7.1ch Sound Processor for High-Quality Audio with Built-in Micro-step Volume

BD34704KS2

General description

The BD34704KS2 is an 8ch independent volume system realized high-quality sound by improved specification of op-amp and optimized layout of the element. The system is designed to allow 7.1ch surround system application. Micro-step volume can reduce the switching pop noise during volume attenuation, so a high quality audio system could be achieved. This IC is available 12ch single-end input selectors to maximum 3 zones. And also available 2 system multi input selector.

Key Specifications

■ Total harmonic distortion:	0.0004%(Typ)
■ Maximum output voltage:	4.2Vrms(Typ)
■ Output noise voltage:	1.2μVrms(Typ)
■ Residual output noise voltage:	1.0μVrms(Typ)
■ Cross-talk between channels:	-105dB(Typ)
■ Cross-talk between selectors:	-105dB(Typ)

Package
SQFP-T80C

W(Typ) x D(Typ) x H(Max)
16.00mm x 16.00mm x 1.60mm

Features

- 12ch input selectors
(It is extendable to up to 18 in case of no use other functions such as Multi input, REC output and SUB output)
- Micro-step volume can reduce the switching pop noise during volume attenuation
- Zone 3 is supported
- 2ch sub-volume for zone output that is available for independent control with a micro step function
- 2-wire serial bus control, corresponding to 3.3/5V



SQFP-T80C

Applications

- Suitable for the AV receivers, home theater systems, etc

Typical Application Circuit

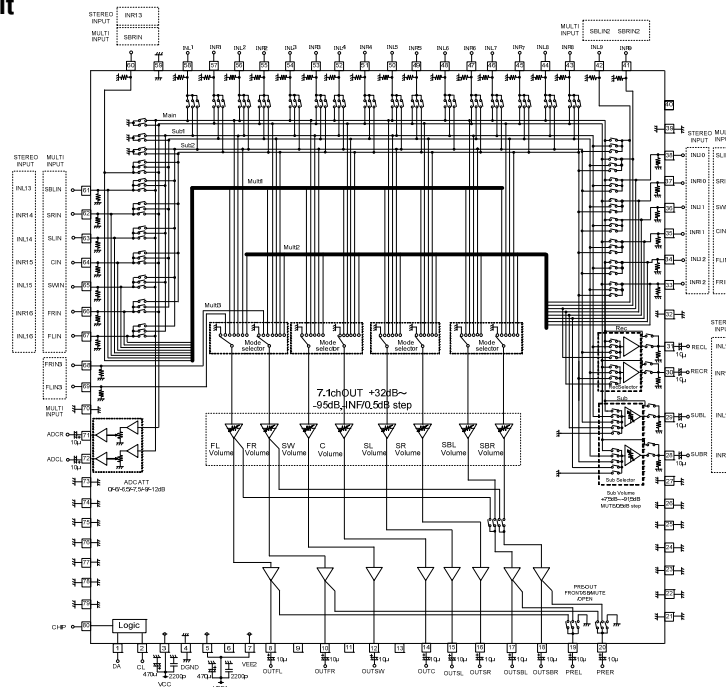


Figure 1. Application Circuit

Pin Configuration

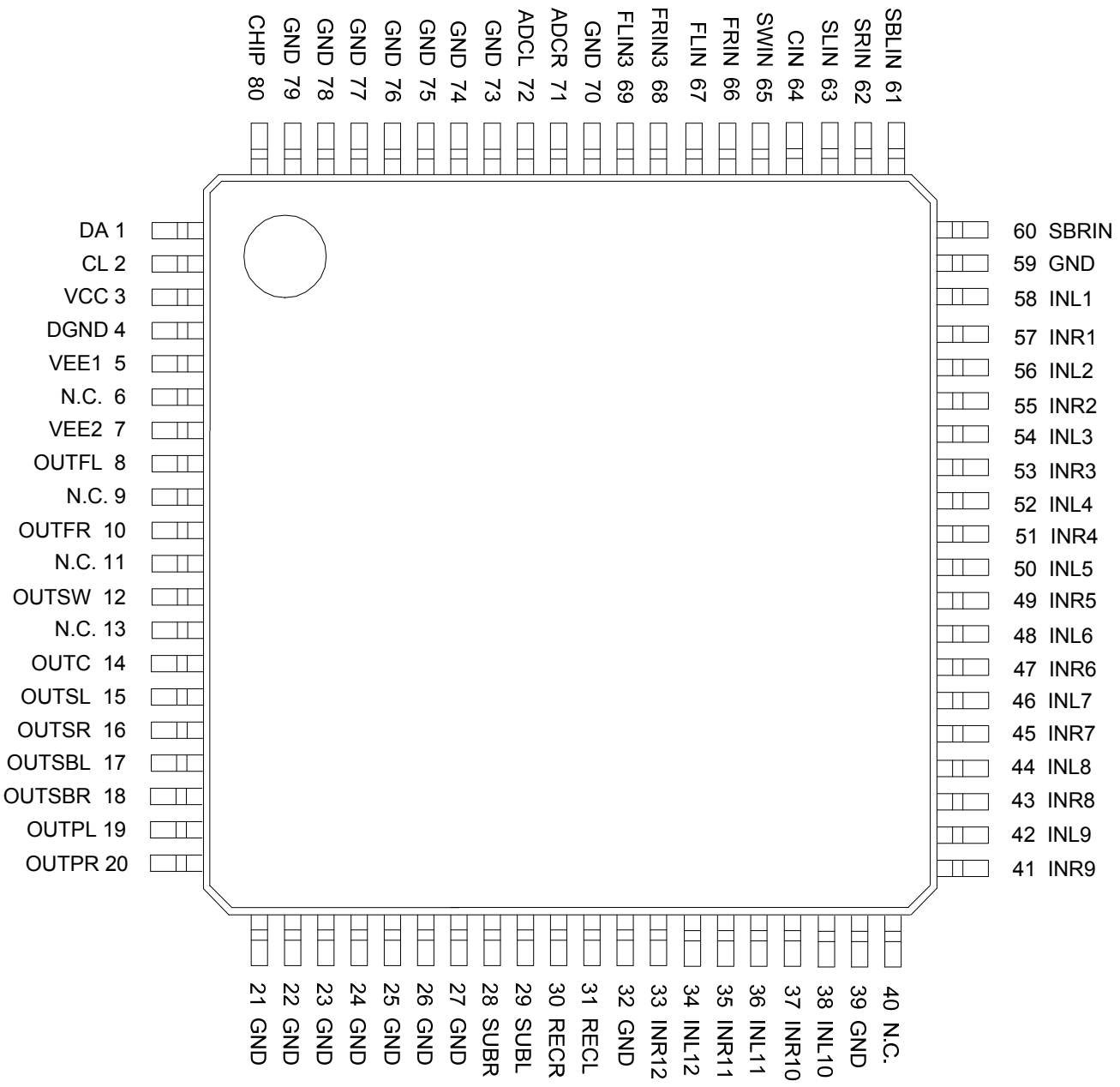


Figure 2. Pin Configuration

Description of terminal

Terminal Number	Symbol	Function	Terminal Number	Symbol	Function
1	DA	Data and latch input terminal	41	INR9(SBRIN2)	Rch input terminal 9
2	CL	Clock input terminal	42	INL9(SBLIN2)	Lch input terminal 9
3	VCC	Positive power supply terminal	43	INR8	Rch input terminal 8
4	DGND	Digital ground terminal	44	INL8	Lch input terminal 8
5	VEE1	Negative power supply terminal 1	45	INR7	Rch input terminal 7
6	N.C.	No connect	46	INL7	Lch input terminal 7
7	VEE2	Negative power supply terminal 2	47	INR6	Rch input terminal 6
8	OUTFL	FLch Output terminal	48	INL6	Lch input terminal 6
9	N.C.	No connect	49	INR5	Rch input terminal 5
10	OUTFR	FRch Output terminal	50	INL5	Lch input terminal 5
11	N.C.	No connect	51	INR4	Rch input terminal 4
12	OUTSW	SWch Output terminal	52	INL4	Lch input terminal 4
13	N.C.	No connect	53	INR3	Rch input terminal 3
14	OUTC	Cch Output terminal	54	INL3	Lch input terminal 3
15	OUTSL	SLch Output terminal	55	INR2	Rch input terminal 2
16	OUTSR	SRch Output terminal	56	INL2	Lch input terminal 2
17	OUTSBL	SBLch Output terminal	57	INR1	Rch input terminal 1
18	OUTSBR	SBRch Output terminal	58	INL1	Lch input terminal 1
19	OUTPL	Lch PRE Output terminal	59	GND	Analog ground terminal
20	OUTPR	Rch PRE Output terminal	60	SBRIN	SBRch DSP input terminal
21	GND	Analog ground terminal	61	SBLIN	SBLch DSP input terminal
22	GND	Analog ground terminal	62	SRIN	SRch DSP input terminal
23	GND	Analog ground terminal	63	SLIN	SLch DSP input terminal
24	GND	Analog ground terminal	64	CIN	Cch DSP input terminal
25	GND	Analog ground terminal	65	SWIN	SWch DSP input terminal
26	GND	Analog ground terminal	66	FRIN	FRch DSP input terminal
27	GND	Analog ground terminal	67	FLIN	FLch DSP input terminal
28	SUBR	Rch SUB Output terminal	68	FRIN3	FRch DSP input terminal 3
29	SUBL	Lch SUB Output terminal	69	FLIN3	FLch DSP input terminal 3
30	RECR	Rch REC Output terminal	70	GND	Analog ground terminal
31	RECL	Lch REC Output terminal	71	ADCR	Rch ADC Output terminal
32	GND	Analog ground terminal	72	ADCL	Lch ADC Output terminal
33	INR12(FRIN2)	Rch input terminal 12	73	GND	Analog ground terminal
34	INL12(FLIN2)	Lch input terminal 12	74	GND	Analog ground terminal
35	INR11(CIN2)	Rch input terminal 11	75	GND	Analog ground terminal
36	INL11(SWIN2)	Lch input terminal 11	76	GND	Analog ground terminal
37	INR10(SRIN)	Rch input terminal 10	77	GND	Analog ground terminal
38	INL10(SLIN2)	Lch input terminal 10	78	GND	Analog ground terminal
39	GND	Analog ground terminal	79	GND	Analog ground terminal
40	N.C.	No connect	80	CHIP	Chip select terminal

Block Diagram

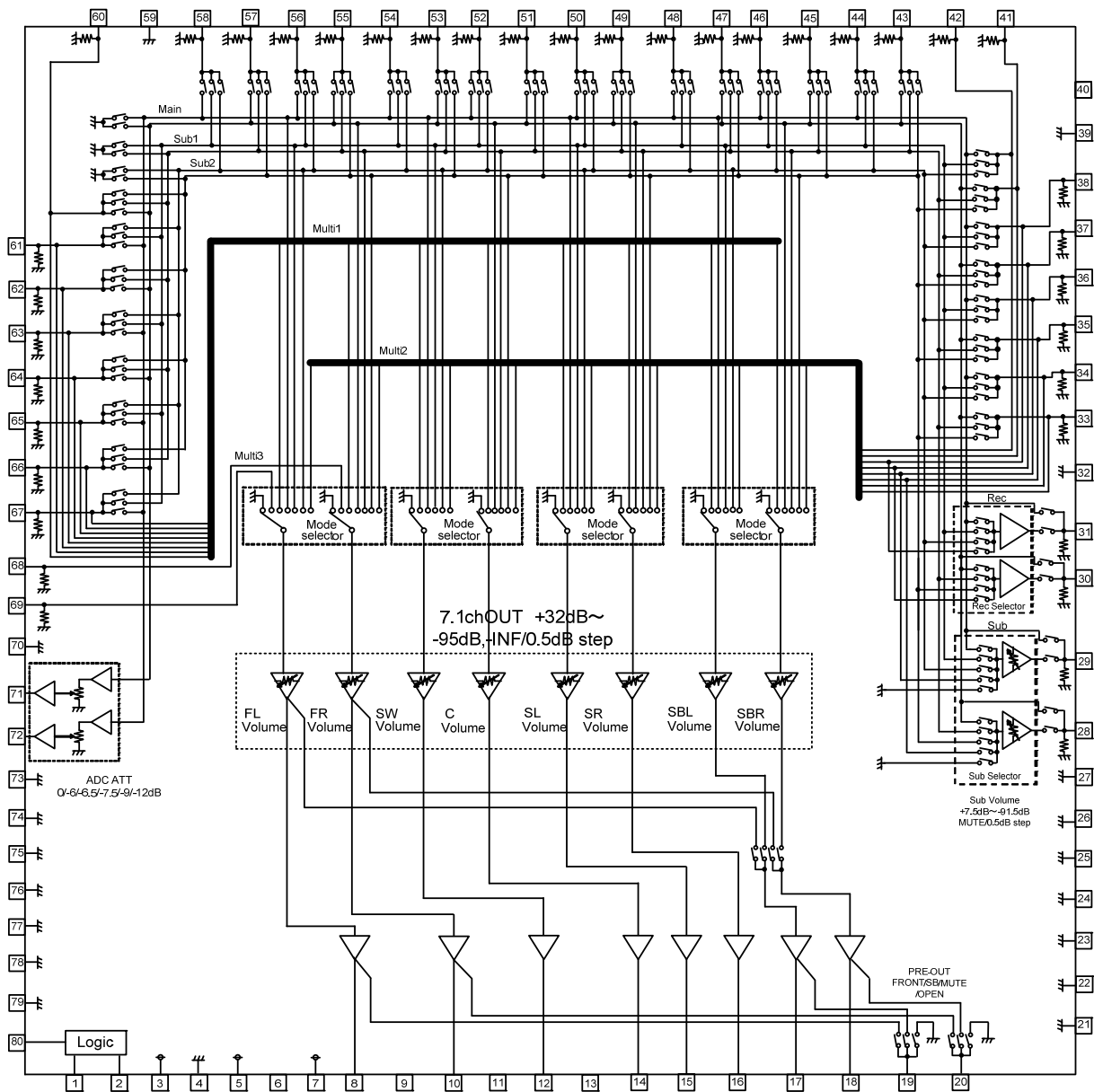


Figure 3. Block Diagram

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Positive power supply	VCC	+7.75 (Note1)	V
Negative power supply	VEE	-7.75 (Note1)	V
Power dissipation	Pd	1.75 (Note2)	W
Input voltage	Vin	VEE-0.2 ~ VCC+0.2	V
Operating temperature	Topr	-40 ~ +85 (Note3)	°C
Storage temperature	Tastg	-55 ~ +150	°C

(Note1) The maximum voltage that can be applied based on GND.

(Note2) Derating at 14.0mW/°C for operating above Ta≥25°C (mounted on 70×70×1.6mm ROHM standard board)

(Note3) If it is within the operating voltage range, circuit functions and operation are guaranteed within this operating temperature.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Operating Condition

Item	Symbol	Rating	Unit
Positive power supply	VCC	+6.5 ~ +7.5 (Note4,5)	V
Negative power supply	VEE	-6.5 ~ -7.5 (Note4,5)	V

(Note4) Applying voltage based on GND.

(Note5) Within the operating temperature range, basic circuit function and operation are guaranteed within this operation voltage range. But please confirm the setting of the constants, temperature, etc. Please take note that electrical characteristics other than defined values cannot be guaranteed, however original function will retain.

Electrical characteristic

Unless otherwise specified, Ta=25°C, VCC=7V, VEE=-7V, f=1kHz, Vin=1Vrms, RL=10kΩ,
 Stereo input selector(MAIN, SUB1, SUB2)=IN1, Mode selector(FL, FRch)=MAIN,
 Mode selector(SW, C, SL, SRch)=MULTI, Mode selector(SBL, SBRch)=MULTI, SB OUTSEL=SB,
 Input Att=0dB, Input gain=0dB, Volume=0dB.

	Item	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
TOTAL	Positive circuit current	Iqp	-	32	45	mA	No signal
	Negative circuit current	Iqn	-45	-32	-	mA	No signal
	Output voltage gain	Gv	-1.5	0	1.5	dB	8, 10, 12, 14~18 pin output
	Channel balance	CB	-0.5	0	0.5	dB	C Channel reference, 8, 10, 12, 14~18 pin output
	Total harmonic distortion + Noise	THD	-	0.0004	0.02	%	BW=400~30kHz 8, 10, 12, 14~18 pin output
	Maximum output voltage	Vom	3.8	4.2	-	Vrms	THD=1%, VOLUME=+10dB 8, 10, 12, 14~18 pin output
	Output noise voltage *	Vno	-	1.2	10	μVrms	Rg=0Ω, BW=IHF-A 8, 10, 12, 14~18 pin output
	Residual output noise voltage *	Vnor	-	1	8	μVrms	Volume=Mute, Rg=0Ω, BW=IHF-A 8, 10, 12, 14~18 pin output
	Cross-talk between channels *	CT	-	-105	-80	dB	Rg=0Ω, BW=IHF-A 8, 10 pin output
	Cross-talk between selectors *	CS	-	-105	-80	dB	Rg=0Ω, BW=IHF-A 8, 10, 12, 14~18 pin output
	Input impedance	Rin	70	100	130	kΩ	28~31, 33~38, 41~58 60~69 pin input
VOLUME	Maximum attenuation *	ATTmax	-	-115	-100	dB	Volume=Mute, BW=IHF-A
REC OUT	Total harmonic distortion	THDR	-	0.0005	0.02	%	BW=400~30kHz, RL=6.8kΩ 28~31 pin output
PRE OUT	Output impedance	Ron	520	800	1080	Ω	19, 20 pin output

※VP-9690(Average value detection, effective value display) filter by Panasonic is used for * measurement.

Typical Performance Curve(s)

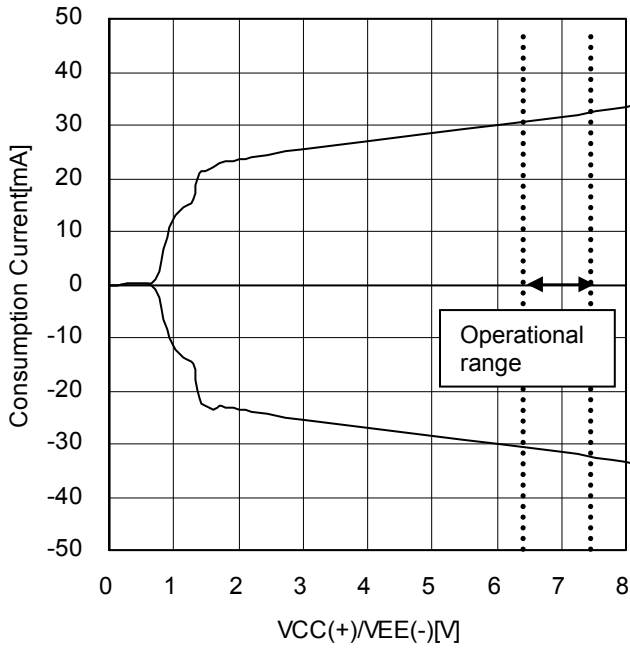


Figure 4. Circuit Currents vs. Circuit Voltage

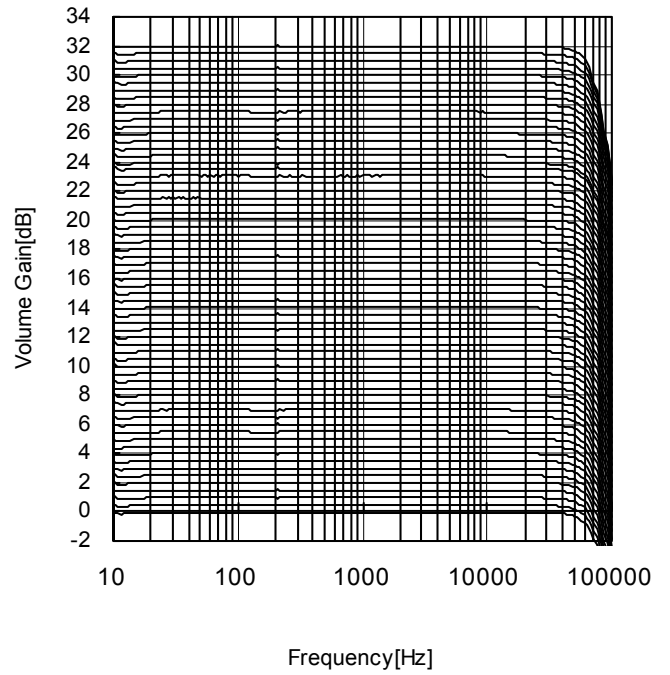


Figure 5. Volume Gain vs. Input Frequency (32dB to 0 dB setting)

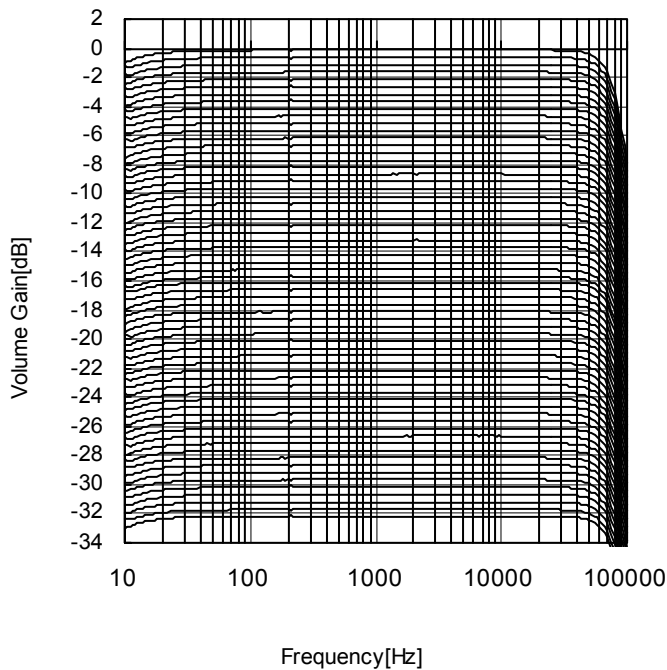


Figure 6. Volume Gain vs. Input Frequency (0dB to -32 dB setting)

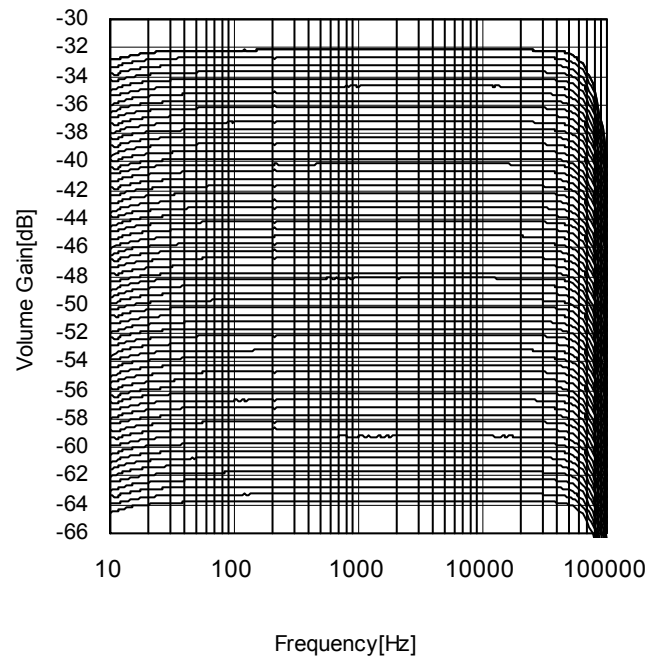


Figure 7. Volume Gain vs. Input Frequency (-32dB to -64 dB setting)

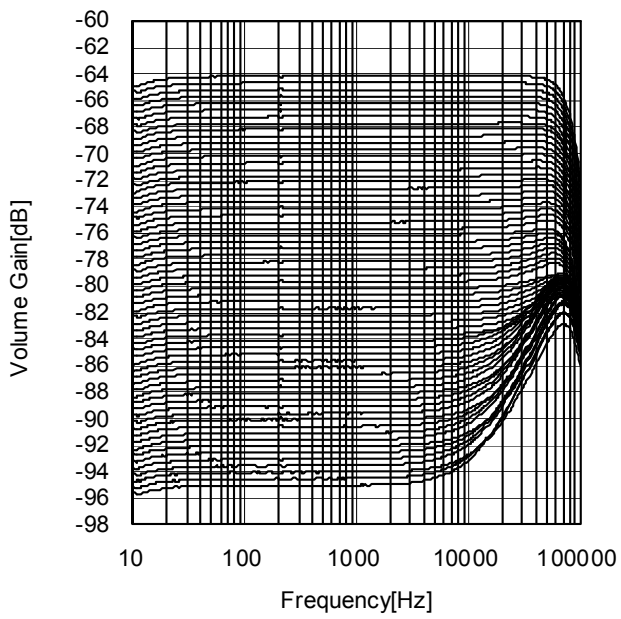


Figure 8. Volume Gain vs. Input Frequency (-64dB to -95 dB setting)

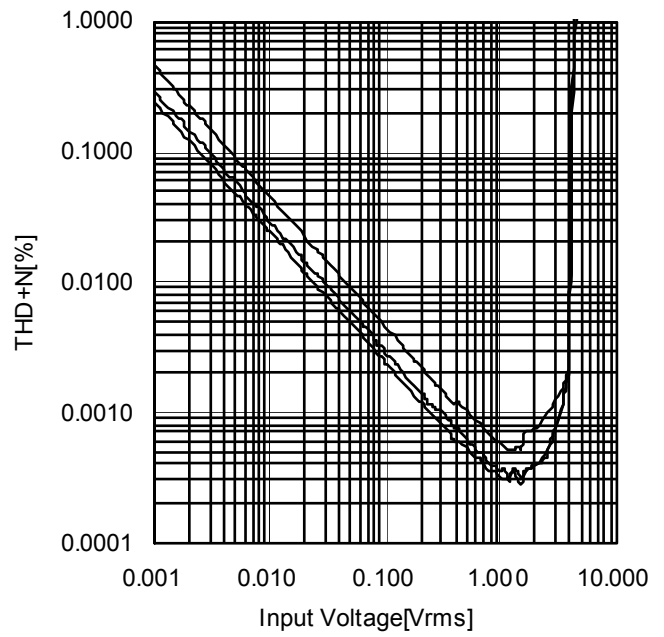


Figure 9. THD + N vs. Input Voltage

(Note) The measurement results of Figure 4 to Figure 8 used by 80kHz LPF.

Specifications for Control Signal

(4) Timing of control signal

Data is read at the rising edge of clock.

Latch is read at the falling edge of clock. Data on the latest 16bit is taken inside the IC.

Ensure to set DA and CL to LOW after Latch.

1byte=16bit

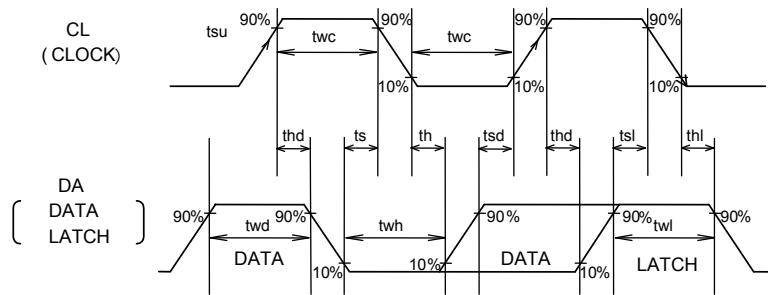


Figure 10. The timing definition of the control signal

Item	Symbol	Limit			Unit
		Min	Typ	Max	
Clock width	twc	1.0	-	-	μsec
Data width	twd	1.0	-	-	μsec
Latch width	twl	1.0	-	-	μsec
Low hold width	twh	1.0	-	-	μsec
Data setup time (DATA→CLK)	tsd	0.5	-	-	μsec
Data hold time (CLK→DATA)	thd	0.5	-	-	μsec
Latch setup time (CLK→LATCH)	tsl	0.5	-	-	μsec
Latch hold time (DATA→LATCH)	thl	0.5	-	-	μsec
Latch Low setup time	ts	0.5	-	-	μsec
Latch Low hold time	th	0.5	-	-	μsec

(2) Voltage of control signal (CL, DA, CHIP)

Item	Conditions	Limit			Unit
		Min	Typ	Max (<VCC)	
High input voltage	VCC=+6.5 to +7.5V VEE=-6.5 to -7.5V	2.3	-	5.5	V
Low input voltage		0	-	1.0	V

(3) Basic Structure of Control Data

← Input Direction

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Data												Select Address			

(4) Table of Control Data

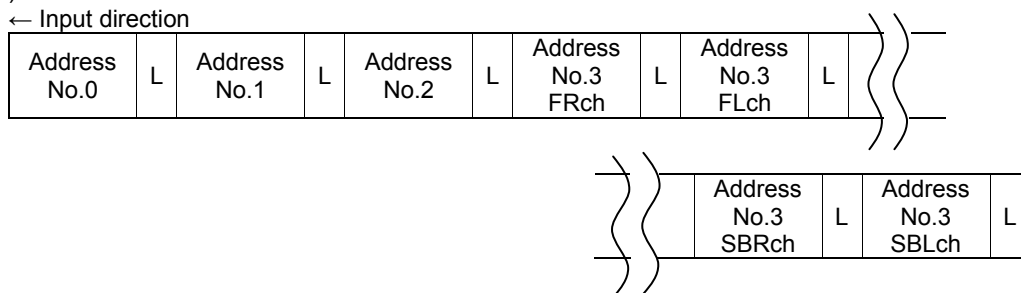
← Input Direction

Select Address No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
0	Input Selector (MAIN)						REC ON/OFF	0	0	SUB ON/OFF	1	0	0	Chip Select	0	0			
1	Input Selector (SUB1)						0	Input Selector (SUB2)				0	0		1				
2	Mode Select FL, FRch		Mode Select C, SWch		Mode Select SL, SRch		Mode Select SBL, SBRch		0	ADC ATT			0		1	0			
3	Volume channel Select			Volume + *Sub Volume												0	1	1	
4	PREOUT SEL		MSEL FRONT	MSEL C,SW	MSEL SUR	MSEL SURB	SB OUTSEL	SUB MUTE	0	0	0	Volume Select2	1		0	0			
6	Mode Select REC		Mode Select SUB		0	0	0	0	0	0	0	0	1		1	0			
7	A→B switch-time			B→A switch-time			Base Clock	0	0	System Reset	0	0	1		1	1			
													BD3843FS (6ch Selector IC)	*	1	0	0		
													BD3841FS (9ch Selector IC)	*	1	0	1		
													BD3812F (2ch volume IC)	*	1	1	*		

- Serial control lines can be shared with BD3471KS2, BD3473KS2 and BD3474KS2. (In case using the serial bus commonly, please set chip select in “1”)
- Serial control lines can be shared with BD3843FS(6ch selector IC), BD3841FS(9ch selector IC) and BD3812F(2chvolume IC).
- Initialize all data at every turning on the power supply.

※The Sub Volume is available by L/Rch independence and 0.5dB step. The Sub volume attenuation is set by address No.3. (A combination of “Volume select2” and “Volume channel select” , please determine the volume setting channel)

(例)



- At the second time after turning on the power supply, eight any data to be changed.

(5) Chip Select Setting Table

CHIP terminal condition	D2
0 (LOW)	0
1 (HIGH)	1

BD34704KS2 can be operated in combination with another by setting the CHP terminal.

Select Address No.0 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Input Selector (MAIN)	MUTE	0	0	0	0	0	0	Rec on/off	0	0	Sub on/off	1	0	0	Chip Select	0	0	
	IN1		0	0	0	0	1											
	IN2		0	0	0	0	1											0
	IN3		0	0	0	0	1											1
	IN4		0	0	0	1	0											0
	IN5		0	0	0	1	0											1
	IN6		0	0	0	1	1											0
	IN7		0	0	0	1	1											1
	IN8		0	1	0	0	0											0
	IN9		0	1	0	0	0											1
	IN10		0	1	0	0	1											0
	IN11		0	1	0	0	1											1
	IN12		0	1	1	0	0											0
	IN13		0	1	1	0	0											1
	IN14		0	1	1	1	1											0
	IN15		0	1	1	1	1											1
	IN16		1	0	0	0	0											0
	IN17(REC)		1	0	0	0	0											1
	IN18(SUB)		1	0	0	0	1											0
Prohibition	1	0	0	0	1	1												
	∴	∴	∴	∴	∴	∴												
	1	1	1	1	1	1												
REC ON/OFF	OFF	Input Selector (MAIN)						0										
	ON							1										
SUB ON/OFF	OFF							Input Selector (MAIN)						Rec on/off				
	ON													0				
		Input Selector (MAIN)												1				
														0				
								1										
								0										

 : Initial condition

Select Address No.1 Setting Table

Function & Setting	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Input Selector (SUB1)	MUTE		0	0	0	0	0	Input Selector (SUB2)					0	Chip Select	0	1	
	IN1		0	0	0	0	1										
	IN2		0	0	0	1	0										
	IN3		0	0	0	1	1										
	IN4		0	0	1	0	0										
	IN5		0	0	1	0	1										
	IN6		0	0	1	1	0										
	IN7		0	0	1	1	1										
	IN8		0	1	0	0	0										
	IN9		0	1	0	0	1										
	IN10		0	1	0	1	0										
	IN11		0	1	0	1	1										
	IN12		0	1	1	0	0										
	IN13		0	1	1	0	1										
	IN14		0	1	1	1	0										
	IN15		0	1	1	1	1										
	IN16		1	0	0	0	0										
Prohibition		1	0	0	0	1											
		∴	∴	∴	∴	∴											
	0	1	1	1	1	1	0										
Input Selector (SUB2)	MUTE		Input Selector (SUB1)						0	0	0	0	0	0	Chip Select	0	1
	IN1							0	0	0	0	1					
	IN2							0	0	0	1	0					
	IN3							0	0	0	1	1					
	IN4							0	0	1	0	0					
	IN5							0	0	1	0	1					
	IN6							0	0	1	1	0					
	IN7							0	0	1	1	1					
	IN8							0	1	0	0	0					
	IN9							0	1	0	0	1					
	IN10							0	1	0	1	0					
	IN11							0	1	0	1	1					
	IN12							0	1	1	0	0					
	IN13							0	1	1	0	1					
	IN14							0	1	1	1	0					
	IN15							0	1	1	1	1					
	IN16							1	0	0	0	0					
Prohibition		1	0	0	0	1											
		∴	∴	∴	∴	∴											
		1	1	1	1	1											

: Initial condition

Select Address No.2 Setting Table ※Select Address No.4 MSEL="0"(Front,C,SW,SR,SRB)

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mode Selector FL, FRch	MUTE	0	0	Mode Selector C, SWch		Mode Selector SL, SRch		Mode Selector SBL, SBRch		0	ADC ATT	0	Chip Select	1	0		
	MAIN	0	1														
	MULTI1	1	0														
	SUB1	1	1														
Mode Selector C, SWch	MUTE	Mode Selector FL, FRch		0	0	Mode Selector SL, SRch		Mode Selector SBL, SBRch		0	ADC ATT	0	Chip Select	1	0		
	MAIN			0	1												
	MULTI1			1	0												
	SUB1			1	1												
Mode Selector SL, SRch	MUTE	Mode Selector FL, FRch		Mode Selector C, SWch		0	0	Mode Selector SL, SRch		0	ADC ATT	0	Chip Select	1	0		
	MAIN					0	1										
	MULTI1					1	0										
	SUB1					1	1										
Mode Selector SBL, SBRch	MUTE	Mode Selector FL, FRch		Mode Selector C, SWch		Mode Selector SL, SRch		0	0	0	ADC ATT	0	Chip Select	1	0		
	MULTI1							0	1								
	SUB1							1	0								
	MAIN							1	1								

 : Initial condition

Select Address No.2 Setting Table ※Select Address No.4 MSEL="1"(Front,C,SW,SR,SRB)

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mode Selector FL, FRch	MUTE	0	0	Mode Selector C, SWch		Mode Selector SL, SRch		Mode Selector SBL, SBRch		0	ADC ATT	0	Chip Select	1	0		
	SUB2	0	1														
	MULTI2	1	0														
	MULTI3	1	1														
Mode Selector C, SWch	MUTE	Mode Selector FL, FRch		0	0	Mode Selector SL, SRch		Mode Selector SBL, SBRch		0	ADC ATT	0	Chip Select	1	0		
	SUB2			0	1												
	MULTI2			1	0												
	Prohibition			1	1												
Mode Selector SL, SRch	MUTE	Mode Selector FL, FRch		Mode Selector C, SWch		0	0	Mode Selector SL, SRch		0	ADC ATT	0	Chip Select	1	0		
	SUB2					0	1										
	MULTI2					1	0										
	Prohibition					1	1										
Mode Selector SBL, SBRch	MUTE	Mode Selector FL, FRch		Mode Selector C, SWch		Mode Selector SL, SRch		0	0	0	ADC ATT	0	Chip Select	1	0		
	SUB2							0	1								
	MULTI2							1	0								
	Prohibition							1	1								

Select Address No.2 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADC ATT	MUTE	Mode Selector FL, FRch		Mode Selector C, SWch		Mode Selector SL, SRch		Mode Selector SBL, SBRch	0		0	0	0	0	Chip Select	1	0
	0dB										0	0	1				
	-6dB										0	1	0				
	-6.5dB										0	1	1				
	-7.5dB										1	0	0				
	-9dB										1	0	1				
	-12dB										1	1	0				
	Prohibition										1	1	1				

Select Address No.3 Setting Table

Function & Setting		Volume Select2	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Volume channel Select	FR	0	0	0	0	Volume									0	Chip Select	1	1	
	FL	0	0	0	1														
	SW	0	0	1	0														
	C	0	0	1	1														
	SR	0	1	0	0														
	SL	0	1	0	1														
	SBR	0	1	1	0														
	SBL	0	1	1	1														
	SUBR	1	0	0	0														
	SUBL	1	0	0	1														
	Prohibition		1	0	1														0
			1	0	1														1
		1	1	0	0														
		1	1	0	1														
		1	1	1	0														
	1	1	1	1															

※Volume Select2 is available setting by Select Address No.4

 : Initial condition

(Note) Considerations in the volume data transmission

- ※Setting range of FR,FL,SW,CEN,SR,SL,SBR and SBL is +32dB to -95dB.
- ※Setting range of SUBR and SUBL is +7.5dB to -91.5dB.
- ※The data transmission to NOT assigned place in data format is prohibition.

Setting table of dynamic range of 7.1ch and Sub Volume

	FR	FL	SW	C	SR	SL	SBR	SBL	SUBR	SUBL
MAX	+32	+32	+32	+32	+32	+32	+32	+32	MUTE	MUTE
MAXS	:	:	:	:	:	:	:	:	+7.5	+7.5
	:	:	:	:	:	:	:	:	:	:
MINS	:	:	:	:	:	:	:	:	-91.5	-91.5
MIN	-95	-95	-95	-95	-95	-95	-95	-95	MUTE	MUTE

MAX : maximum value of 7.1ch Volume MAXS : maximum value of Sub Volume
 MIN : minimum value of 7.1ch Volume MINS : minimum value of Sub Volume

Select Address No.3 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
Volume	MUTE	Volume Channel Select	1	0	1	1	1	1	1	1	1	1	1	0	Chip Select	1	1			
	Prohibition					1	1	1	1	1	1	1	1					1	0	
						⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮					⋮	⋮	
						⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮					⋮	⋮	
						⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮					⋮	⋮	
	+32.0dB					0	1	0	0	0	0	0	0					0	0	1
	+31.5dB					0	1	0	0	0	0	0	0					0	0	0
	+31.0dB					0	0	1	1	1	1	1	1					1	1	1
	+30.5dB					0	0	1	1	1	1	1	1					1	0	0
	+30.0dB					0	0	1	1	1	1	1	1					0	1	1
	+29.5dB					0	0	1	1	1	1	0	1					1	1	1
	+29.0dB					0	0	1	1	1	1	0	1					0	1	0
	+28.5dB					0	0	1	1	1	1	0	0					0	1	1
	+28.0dB					0	0	1	1	1	1	0	0					0	0	0
	+27.5dB					0	0	1	1	0	1	1	1					1	1	1
	+27.0dB					0	0	1	1	0	1	1	1					0	0	0
	+26.5dB					0	0	1	1	0	1	0	1					0	1	1
	+26.0dB					0	0	1	1	0	1	0	1					0	0	0
	+25.5dB					0	0	1	1	0	0	0	1					1	1	1
	+25.0dB					0	0	1	1	0	0	0	1					0	0	0
	+24.5dB					0	0	1	1	0	0	0	0					0	1	1
+24.0dB	0	0	1	1	0	0	0	0	0	0	0									
+23.5dB	0	0	1	0	1	1	1	1	1	1	1									
+23.0dB	0	0	1	0	1	1	1	1	1	0	0									
+22.5dB	0	0	1	0	1	1	1	0	1	0	1									
+22.0dB	0	0	1	0	1	1	1	0	0	0	0									

Select Address No.3 Setting Table

Function & Setting	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume	Volume Channel Select	1	0	Chip Select	1	1	+21.5dB	0	0	1	0	1	0	1	1	
							+21.0dB	0	0	1	0	1	0	1	0	
							+20.5dB	0	0	1	0	1	0	0	1	
							+20.0dB	0	0	1	0	1	0	0	0	
							+19.5dB	0	0	1	0	0	1	1	1	
							+19.0dB	0	0	1	0	0	1	1	0	
							+18.5dB	0	0	1	0	0	1	0	1	
							+18.0dB	0	0	1	0	0	1	0	0	
							+17.5dB	0	0	1	0	0	0	1	1	
							+17.0dB	0	0	1	0	0	0	1	0	
							+16.5dB	0	0	1	0	0	0	0	1	
							+16.0dB	0	0	1	0	0	0	0	0	
							+15.5dB	0	0	0	1	1	1	1	1	
							+15.0dB	0	0	0	1	1	1	1	0	
							+14.5dB	0	0	0	1	1	1	0	1	
							+14.0dB	0	0	0	1	1	1	0	0	
							+13.5dB	0	0	0	1	1	0	1	1	
							+13.0dB	0	0	0	1	1	0	1	0	
							+12.5dB	0	0	0	1	1	0	0	1	
							+12.0dB	0	0	0	1	1	0	0	0	
							+11.5dB	0	0	0	1	0	1	1	1	
							+11.0dB	0	0	0	1	0	1	1	0	
							+10.5dB	0	0	0	1	0	1	0	1	
							+10.0dB	0	0	0	1	0	1	0	0	
							+9.5dB	0	0	0	1	0	0	1	1	
							+9.0dB	0	0	0	1	0	0	1	0	
							+8.5dB	0	0	0	1	0	0	0	1	
							+8.0dB	0	0	0	1	0	0	0	0	
							+7.5dB	0	0	0	0	1	1	1	1	
							+7.0dB	0	0	0	0	1	1	1	0	
							+6.5dB	0	0	0	0	1	1	0	1	
							+6.0dB	0	0	0	0	1	1	0	0	
+5.5dB	0	0	0	0	1	0	1	1								
+5.0dB	0	0	0	0	1	0	1	0								
+4.5dB	0	0	0	0	1	0	0	1								
+4.0dB	0	0	0	0	1	0	0	0								
+3.5dB	0	0	0	0	0	1	1	1								
+3.0dB	0	0	0	0	0	1	1	0								
+2.5dB	0	0	0	0	0	1	0	1								
+2.0dB	0	0	0	0	0	1	0	0								
+1.5dB	0	0	0	0	0	0	1	1								
+1.0dB	0	0	0	0	0	0	1	0								
+0.5dB	0	0	0	0	0	0	0	1								
Prohibition	0	0	0	0	0	0	0	0	0							
-0dB	0	0	0	0	0	0	0	0	0							
-0.5dB		0	0	0	0	0	0	0	1							
-1.0dB		0	0	0	0	0	0	1	0							
-1.5dB		0	0	0	0	0	0	1	1							

Select Address No.3 Setting Table

Function & Setting	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume	-2.0dB	Volume Channel Select	0	0	0	0	0	0	0	1	0	0	0	Chip Select	1	1
	-2.5dB			0	0	0	0	0	0	1	0	1				
	-3.0dB			0	0	0	0	0	0	1	1	0				
	-3.5dB			0	0	0	0	0	0	1	1	1				
	-4.0dB			0	0	0	0	1	0	0	0	0				
	-4.5dB			0	0	0	0	1	0	0	1	0				
	-5.0dB			0	0	0	0	1	0	1	0	0				
	-5.5dB			0	0	0	0	1	0	1	1	0				
	-6.0dB			0	0	0	0	1	1	0	0	0				
	-6.5dB			0	0	0	0	1	1	0	1	0				
	-7.0dB			0	0	0	0	1	1	1	1	0				
	-7.5dB			0	0	0	0	1	1	1	1	1				
	-8.0dB			0	0	0	1	0	0	0	0	0				
	-8.5dB			0	0	0	1	0	0	0	0	1				
	-9.0dB			0	0	0	1	0	0	1	0	0				
	-9.5dB			0	0	0	1	0	0	1	1	0				
	-10.0dB			0	0	0	1	0	1	0	0	0				
	-10.5dB			0	0	0	1	0	1	0	1	0				
	-11.0dB			0	0	0	1	0	1	1	1	0				
	-11.5dB			0	0	0	1	0	1	1	1	1				
	-12.0dB			0	0	0	1	1	0	0	0	0				
	-12.5dB			0	0	0	1	1	0	0	0	1				
	-13.0dB			0	0	0	1	1	0	1	0	0				
	-13.5dB			0	0	0	1	1	0	1	1	1				
	-14.0dB			0	0	0	1	1	1	0	0	0				
	-14.5dB			0	0	0	1	1	1	1	0	1				
	-15.0dB			0	0	0	1	1	1	1	1	0				
	-15.5dB			0	0	0	1	1	1	1	1	1				
	-16.0dB			0	0	1	0	0	0	0	0	0				
	-16.5dB			0	0	1	0	0	0	0	0	1				
	-17.0dB			0	0	1	0	0	0	0	1	0				
	-17.5dB			0	0	1	0	0	0	0	1	1				
-18.0dB	0	0	1	0	0	1	0	0	0							
-18.5dB	0	0	1	0	0	1	0	0	1							
-19.0dB	0	0	1	0	0	1	1	1	0							
-19.5dB	0	0	1	0	0	1	1	1	1							
-20.0dB	0	0	1	0	1	0	0	0	0							
-20.5dB	0	0	1	0	1	0	0	0	1							
-21.0dB	0	0	1	0	1	0	1	0	0							
-21.5dB	0	0	1	0	1	0	1	0	1							
-22.0dB	0	0	1	0	1	1	1	0	0							
-22.5dB	0	0	1	0	1	1	1	0	1							
-23.0dB	0	0	1	0	1	1	1	1	0							
-23.5dB	0	0	1	0	1	1	1	1	1							
-24.0dB	0	0	1	1	0	0	0	0	0							
-24.5dB	0	0	1	1	0	0	0	0	1							
-25.0dB	0	0	1	1	0	0	1	0	0							
-25.5dB	0	0	1	1	0	0	1	0	1							

Select Address No.3 Setting Table

Function & Setting	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume	-26.0dB	Volume Channel Select	0	0	0	0	1	1	0	1	0	0	0	Chip Select	1	1
	-26.5dB				0	0	1	1	0	1	0	1				
	-27.0dB				0	0	1	1	0	1	1	0				
	-27.5dB				0	0	1	1	0	1	1	1				
	-28.0dB				0	0	1	1	1	0	0	0				
	-28.5dB				0	0	1	1	1	0	0	1				
	-29.0dB				0	0	1	1	1	0	1	0				
	-29.5dB				0	0	1	1	1	0	1	1				
	-30.0dB				0	0	1	1	1	1	0	0				
	-30.5dB				0	0	1	1	1	1	0	1				
	-31.0dB				0	0	1	1	1	1	1	0				
	-31.5dB				0	0	1	1	1	1	1	1				
	-32.0dB				0	1	0	0	0	0	0	0				
	-32.5dB				0	1	0	0	0	0	0	1				
	-33.0dB				0	1	0	0	0	0	1	0				
	-33.5dB				0	1	0	0	0	0	1	1				
	-34.0dB				0	1	0	0	0	1	0	0				
	-34.5dB				0	1	0	0	0	1	0	1				
	-35.0dB				0	1	0	0	0	1	1	0				
	-35.5dB				0	1	0	0	0	1	1	1				
	-36.0dB				0	1	0	0	1	0	0	0				
	-36.5dB				0	1	0	0	1	0	0	1				
	-37.0dB				0	1	0	0	1	0	1	0				
	-37.5dB				0	1	0	0	1	0	1	1				
	-38.0dB				0	1	0	0	1	1	0	0				
	-38.5dB				0	1	0	0	1	1	0	1				
	-39.0dB				0	1	0	0	1	1	1	0				
	-39.5dB				0	1	0	0	1	1	1	1				
	-40.0dB				0	1	0	1	0	0	0	0				
	-40.5dB				0	1	0	1	0	0	0	1				
	-41.0dB				0	1	0	1	0	0	1	0				
	-41.5dB				0	1	0	1	0	0	1	1				
-42.0dB	0	1	0	1	0	1	0	0								
-42.5dB	0	1	0	1	0	1	0	1								
-43.0dB	0	1	0	1	0	1	1	0								
-43.5dB	0	1	0	1	0	1	1	1								
-44.0dB	0	1	0	1	1	0	0	0								
-44.5dB	0	1	0	1	1	0	0	1								
-45.0dB	0	1	0	1	1	0	1	0								
-45.5dB	0	1	0	1	1	0	1	1								
-46.0dB	0	1	0	1	1	1	0	0								
-46.5dB	0	1	0	1	1	1	0	1								
-47.0dB	0	1	0	1	1	1	1	0								
-47.5dB	0	1	0	1	1	1	1	1								
-48.0dB	0	1	1	0	0	0	0	0								
-48.5dB	0	1	1	0	0	0	0	1								
-49.0dB	0	1	1	0	0	0	1	0								
-49.5dB	0	1	1	0	0	0	1	1								

Select Address No.3 Setting Table

Function & Setting	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume	-50.0dB	Volume Channel Select	0	0	0	1	1	0	0	1	0	0	0	Chip Select	1	1
	-50.5dB				0	1	1	0	0	1	0	1				
	-51.0dB				0	1	1	0	0	1	1	0				
	-51.5dB				0	1	1	0	0	1	1	1				
	-52.0dB				0	1	1	0	1	0	0	0				
	-52.5dB				0	1	1	0	1	0	0	1				
	-53.0dB				0	1	1	0	1	0	1	0				
	-53.5dB				0	1	1	0	1	0	1	1				
	-54.0dB				0	1	1	0	1	1	0	0				
	-54.5dB				0	1	1	0	1	1	0	1				
	-55.0dB				0	1	1	0	1	1	1	0				
	-55.5dB				0	1	1	0	1	1	1	1				
	-56.0dB				0	1	1	1	0	0	0	0				
	-56.5dB				0	1	1	1	0	0	0	1				
	-57.0dB				0	1	1	1	0	0	1	0				
	-57.5dB				0	1	1	1	0	0	1	1				
	-58.0dB				0	1	1	1	0	1	0	0				
	-58.5dB				0	1	1	1	0	1	0	1				
	-59.0dB				0	1	1	1	0	1	1	0				
	-59.5dB				0	1	1	1	0	1	1	1				
	-60.0dB				0	1	1	1	1	0	0	0				
	-60.5dB				0	1	1	1	1	0	0	1				
	-61.0dB				0	1	1	1	1	0	1	0				
	-61.5dB				0	1	1	1	1	0	1	1				
	-62.0dB				0	1	1	1	1	1	0	0				
	-62.5dB				0	1	1	1	1	1	0	1				
	-63.0dB				0	1	1	1	1	1	1	0				
	-63.5dB				0	1	1	1	1	1	1	1				
	-64.0dB				1	0	0	0	0	0	0	0				
	-64.5dB				1	0	0	0	0	0	0	1				
	-65.0dB				1	0	0	0	0	0	0	0				
	-65.5dB				1	0	0	0	0	0	0	1				
	-66.0dB				1	0	0	0	0	0	1	0				
	-66.5dB				1	0	0	0	0	0	1	0				
	-66.5dB				1	0	0	0	0	0	1	0				
	-67.0dB				1	0	0	0	0	0	1	1				
	-67.0dB				1	0	0	0	0	0	1	1				
	-67.5dB				1	0	0	0	0	0	1	1				
	-67.5dB				1	0	0	0	0	0	1	1				
	-68.0dB				1	0	0	0	0	1	0	0				
-68.5dB	1	0	0	0	0	1	0	0								
-68.5dB	1	0	0	0	0	1	0	0								
-69.0dB	1	0	0	0	0	1	0	1								
-69.0dB	1	0	0	0	0	1	0	1								
-69.5dB	1	0	0	0	0	1	0	1								
-69.5dB	1	0	0	0	0	1	0	1								
-70.0dB	1	0	0	0	0	1	1	0								
-70.0dB	1	0	0	0	0	1	1	0								
-70.5dB	1	0	0	0	0	1	1	0								
-70.5dB	1	0	0	0	0	1	1	0								
-71.0dB	1	0	0	0	0	1	1	1								
-71.0dB	1	0	0	0	0	1	1	1								
-71.5dB	1	0	0	0	0	1	1	1								
-71.5dB	1	0	0	0	0	1	1	1								
-72.0dB	1	0	0	1	0	0	0	0								
-72.0dB	1	0	0	1	0	0	0	0								
-72.5dB	1	0	0	1	0	0	0	1								
-72.5dB	1	0	0	1	0	0	0	1								
-73.0dB	1	0	0	1	0	0	0	0								
-73.0dB	1	0	0	1	0	0	0	0								
-73.5dB	1	0	0	1	0	0	0	1								
-73.5dB	1	0	0	1	0	0	0	1								

Select Address No.3 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume	-74.0dB	Volume Channel Select	0	0	1	0	0	1	0	1	0	0	0	0	Chip Select	1	1
	-74.5dB				1	0	0	1	0	1	0	1					
	-75.0dB				1	0	0	1	0	1	1	0					
	-75.5dB				1	0	0	1	0	1	1	1					
	-76.0dB				1	0	0	1	1	0	0	0					
	-76.5dB				1	0	0	1	1	0	0	1					
	-77.0dB				1	0	0	1	1	0	1	0					
	-77.5dB				1	0	0	1	1	0	1	1					
	-78.0dB				1	0	0	1	1	1	0	0					
	-78.5dB				1	0	0	1	1	1	0	1					
	-79.0dB				1	0	0	1	1	1	1	0					
	-79.5dB				1	0	0	1	1	1	1	1					
	-80.0dB				1	0	1	0	0	0	0	0					
	-80.5dB				1	0	1	0	0	0	0	1					
	-81.0dB				1	0	1	0	0	0	1	0					
	-81.5dB				1	0	1	0	0	0	1	1					
	-82.0dB				1	0	1	0	0	1	0	0					
	-82.5dB				1	0	1	0	0	1	0	1					
	-83.0dB				1	0	1	0	0	1	1	0					
	-83.5dB				1	0	1	0	0	1	1	1					
	-84.0dB				1	0	1	0	1	0	0	0					
	-84.5dB				1	0	1	0	1	0	0	1					
	-85.0dB				1	0	1	0	1	0	1	0					
	-85.5dB				1	0	1	0	1	0	1	1					
	-86.0dB				1	0	1	0	1	1	0	0					
	-86.5dB				1	0	1	0	1	1	0	1					
	-87.0dB				1	0	1	0	1	1	1	0					
	-87.5dB				1	0	1	0	1	1	1	1					
	-88.0dB				1	0	1	1	0	0	0	0					
	-88.5dB				1	0	1	1	0	0	0	1					
	-89.0dB				1	0	1	1	0	0	1	0					
	-89.5dB				1	0	1	1	0	0	1	1					
	-90.0dB				1	0	1	1	0	1	0	0					
	-90.5dB				1	0	1	1	0	1	0	1					
-91.0dB	1	0	1	1	0	1	1	0									
-91.5dB	1	0	1	1	0	1	1	1									
-92.0dB	1	0	1	1	1	0	0	0									
-92.5dB	1	0	1	1	1	0	0	1									
-93.0dB	1	0	1	1	1	0	1	0									
-93.5dB	1	0	1	1	1	0	1	1									
-94.0dB	1	0	1	1	1	1	0	0									
-94.5dB	1	0	1	1	1	1	0	1									
-95.0dB	1	0	1	1	1	1	1	0									
Prohibition	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	1	1	1	1	1	1	1	1	1	1	1	1	1				

Select Address No.4 Setting Table ※ON/OFF of each MSEL is reflected by a mode selector of Address No. 2

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PREOUT SEL	MUTE	0	0	MSEL FRONT	MSEL C.,SW	MSEL SUR	MSEL SURB	SB Select	SUB MUTE	0	0	0	Volume Select2	1	Chip Select	0	0
	FRONT	0	1														
	SURB	1	0														
	OPEN	1	1														
MSEL FRONT	OFF	PREOUT SEL		0													
	ON			1													
MSEL C.,SW	OFF			0													
	ON			1													
MSEL SUR	OFF			0													
	ON			1													
MSEL SURB	OFF			0													
	ON			1													
SB Select	SURB			0													
	FRONT			1													
SUB MUTE	MUTE OFF			0													
	MUTE ON			1													
Volume Select2	OFF			0													
	ON			1													

Select Address No.6 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mode Selector REC	MAIN	0	0	Mode Selector SUB		0	0	0	0	0	0	0	0	1	Chip Select	1	0
	SUB1	0	1														
	SUB2	1	0														
	MULTI	1	1														
Mode Selector SUB	MAIN	Mode Selector REC		0	0												
	SUB1			0	1												
	SUB2			1	0												
	MULTI			1	1												

 : Initial condition

Select Address No.7 setting table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A→B switching-time	11.2msec	0	0	0	B→A switching-time			Base Clock	0	0	System Reset	0	0	1	Chip Select	1	1
	4.7msec	0	0	1													
	7.2msec	0	1	0													
	14.4msec	0	1	1													
	3.2msec	1	0	0													
	2.3msec	1	0	1													
	Prohibition	1	1	0													
B→A switching-time	11.2msec	A→B switching-time			0	0	0	0	0	System Reset	0	0	1	Chip Select	1	1	
	4.7msec				0	0	1										
	7.2msec				0	1	0										
	14.4msec				0	1	1										
	3.2msec				1	0	0										
	2.3msec				1	0	1										
	Prohibition				1	1	0										
Base Clock	x1	B→A switching-time			0			0									
	x1/2							1									
System Reset	Normal	B→A switching-time			Base Clock			0									
	Reset							1									

Initial condition

Select Address No.7, Data = D15-D13 : Below A → B switching time is adjustable.

Select Address No.7, Data = D12-D10 : Below B → A switching time is adjustable.

※Switching time over 11.2msec is recommended for both A→B and B→A.

※Set to same switching time for both A→B, B→A is recommended if the switching times need to be changed.

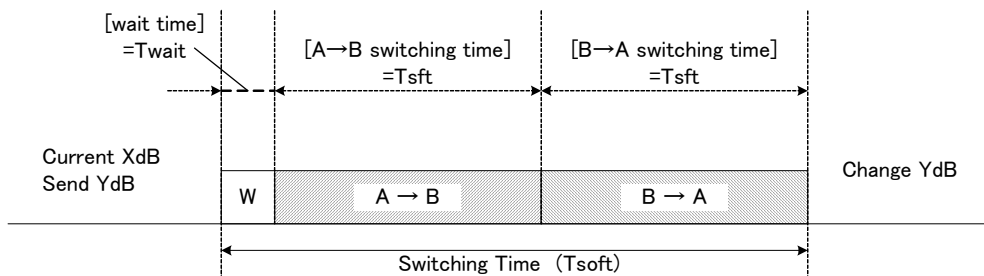


Figure 11. Micro step volume switching time

If the base clock is set to x1/2, the switching time will be doubled.

Micro step volume circuit

- 1. Micro step volume technology.
 - 1-1. Micro step volume effects.

Micro step volume is Rohm original switching pop noise prevention technology. The audible signal is discontinuous during the gain switching instantly which cause the noise to occur. This micro step volume will prevent this discontinuous signal by completing the signal waveform and will significantly reduce the noise.

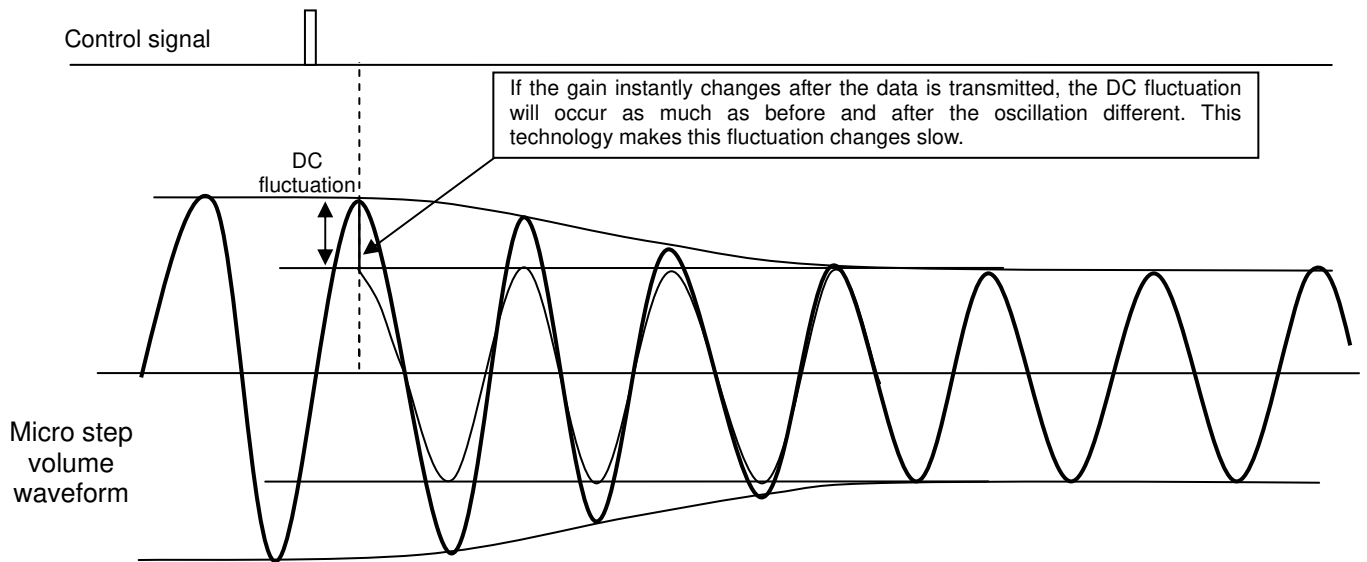


Figure 12. Micro step volume waveform

This micro step volume will start the switching when received the signal sent from the micon.
 At any constant time, the switching waveform is shown as above figure. This IC will optimally operates by internally processes the data sent from the micon to prevent the switching shock.
 However, sometimes the switching waveform is not like the intended form depends on the transmission timing. Therefore, below is the example of the relationship between the transmission timing and actual switching time. Please consider this relationship for the setting.

1-2. Micro step volume application target block

- Micro step volume application target blocks are 7.1ch volume and SUB volume.

2. About data transmission of Micro step volume circuit

2-1. Switching time of Micro step volume

This switching time includes [Wait time], [A→B switching time] and [B→A switching time]. Every switching time needs around 25msec. ($T_{soft} = T_{wait} + 2 * T_{sft}$, $T_{wait}=2.3msec$, $T_{sft}=11.2msec$)

Please take note that T_{wait} is wait time for starting switching and the setting is 2.3msec. (T_{wait} considers the internal IC tolerance, therefore this time need to be set within 1.3msec (Min.) to 4.6msec (Max.).

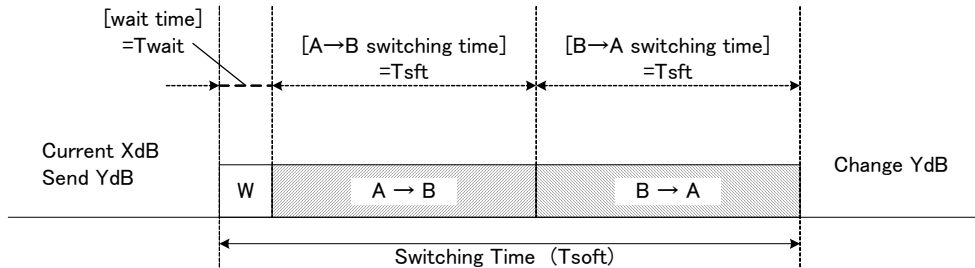


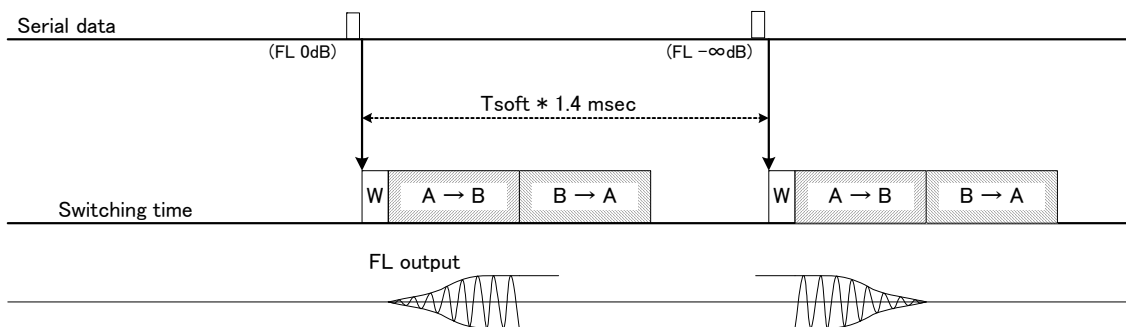
Figure 13. [A→B switching time] and [B→A switching time]

In addition, base clock can change the frequency using the internal oscillation device. For example, when base clock x1/2 is selected, [Wait time], [A→B switching time] and [B→A switching time] are doubled.

2-2. Same block data transmission timing and switching operation.

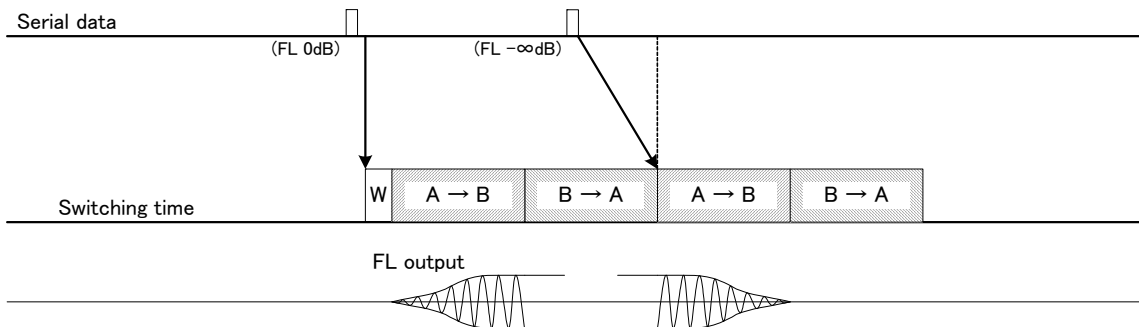
■ Transmission example 1

The time chart from data transmission to switching start time is shown as below. At first, below figure shows transmitted data with the same block which is separated with enough interval. This enough interval refers to the tolerance margin time of T_{soft} multiplied by 1.4.



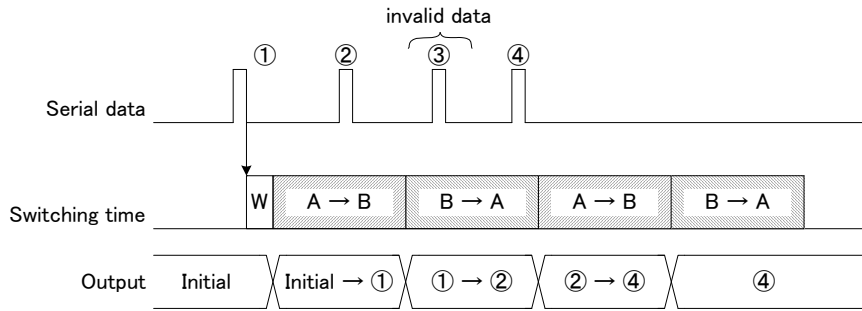
■ Transmission example 2

Next, below figure shows the example of when the transmission interval is not enough (smaller than above interval). When the data transmitted during the first operation of the switching, the second data transmission will continue after complete the first operation. In this case, there is no wait time (T_{wait}) before the second transmission.



■ Transmission example 3

Next is the example for switching operation with smaller data transmission interval.



Data ② is the data during the A→B operation, so this data is valid, and then during B→A operation, data ① promptly switches to data ②.
 Data ③ and data ④ are data during B→A operation, therefore these data are valid for the next switching, but data ③ got overwritten by data ④ so data ③ will become invalid. Only data ④ is valid.
 There is no regulation on the transmission timing.

For data transmission to multi-channels, there is a caution. The combination of Lch and Rch for same block will make the switching is possible to change at same timing. When the setting is data ① for FL (Lch) and data ② for FR (Rch), same switching timing is possible if the data transmission is set as below figure.

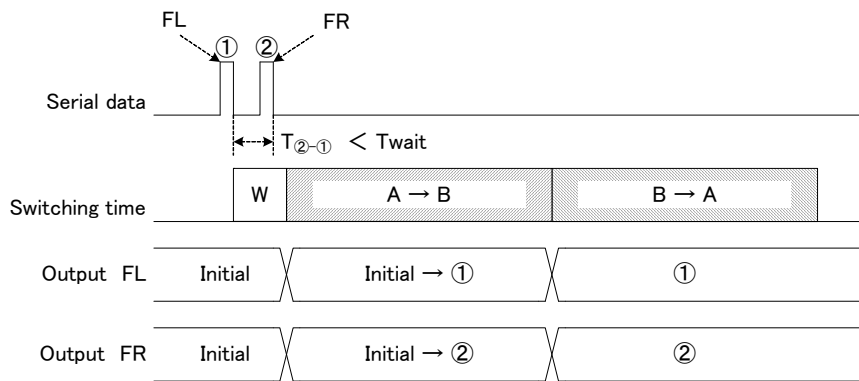


Figure 14. The operation during multi-channels (Lch, Rch) data transmission (smaller than Twait interval).

Next, when data ② is not transmitted during the Twait, the switching operation is as following figure.

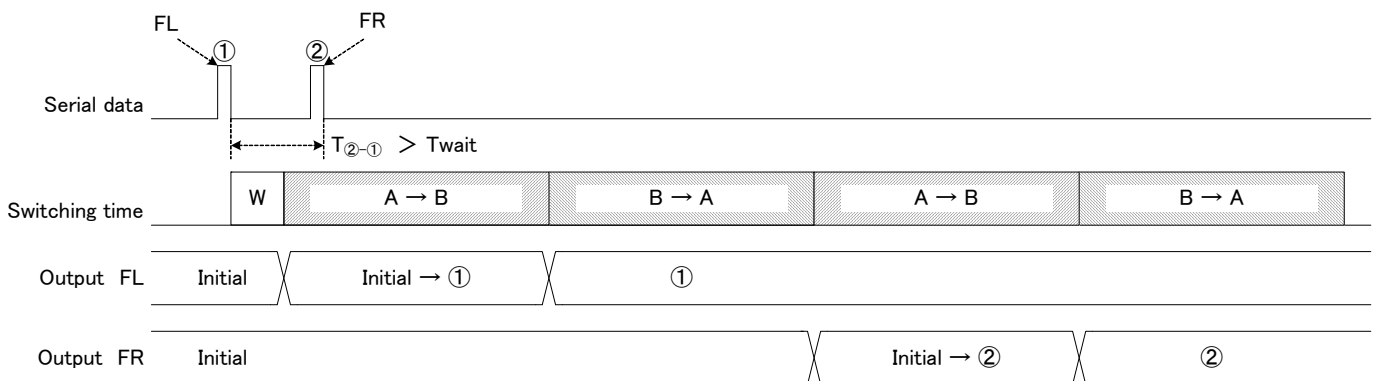


Figure 15. The operation during multi-channels (Lch, Rch) data transmission (larger than Twait interval).