Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Sound Processors for AV Receiver Systems

7.1ch Sound Processor with Built-in Micro-step Volume

BD34705KS2

General description

The BD34705KS2 is an 8ch independent volume system. The system is designed to allow 7.1ch surround system application. It is improvement that sound quality more than the conventional products. Micro-step volume can reduce the switching pop noise during volume attenuation, so a high quality audio system could be achieved.
8ch triple input selectors for zone 3 and multi channel input enable the connection with a number of sources.

Features

- 8ch input selectors
  (It is extendable to up to 14 by other functions and exclusion)
- Micro-step volume can reduce the switching pop noise during volume attenuation.
- Zone 3 is supported.
- Built-in 2ch Volume for ZONE output
- 2-wire serial bus control, corresponding to 3.3/5V.

Applications

- Suitable for the AV receiver, home theater system, etc.

Key Specifications

- Total harmonic distortion: 0.0004%(Typ.)
- Maximum output voltage: 4.2Vrms(Typ.)
- Output noise voltage: 1.2μVrms(Typ.)
- Residual output noise voltage: 1.0μVrms(Typ.)
- Cross-talk between channels: -105dB(Typ.)
- Cross-talk between selectors: -105dB(Typ.)

Package

	W(Typ.) x D(Typ.) x H(Max.)
SQFP-T64	14.00mm x 14.00mm x 1.50mm

SQFP-T64

Typical Application Circuit

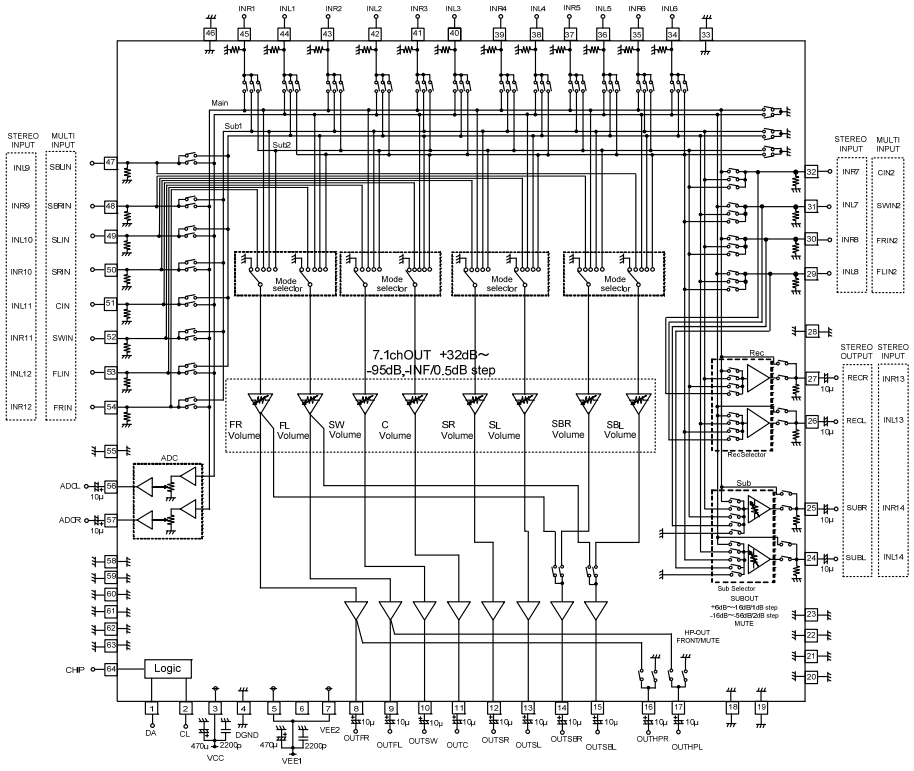


Figure 1. Application Circuit

Pin Configuration

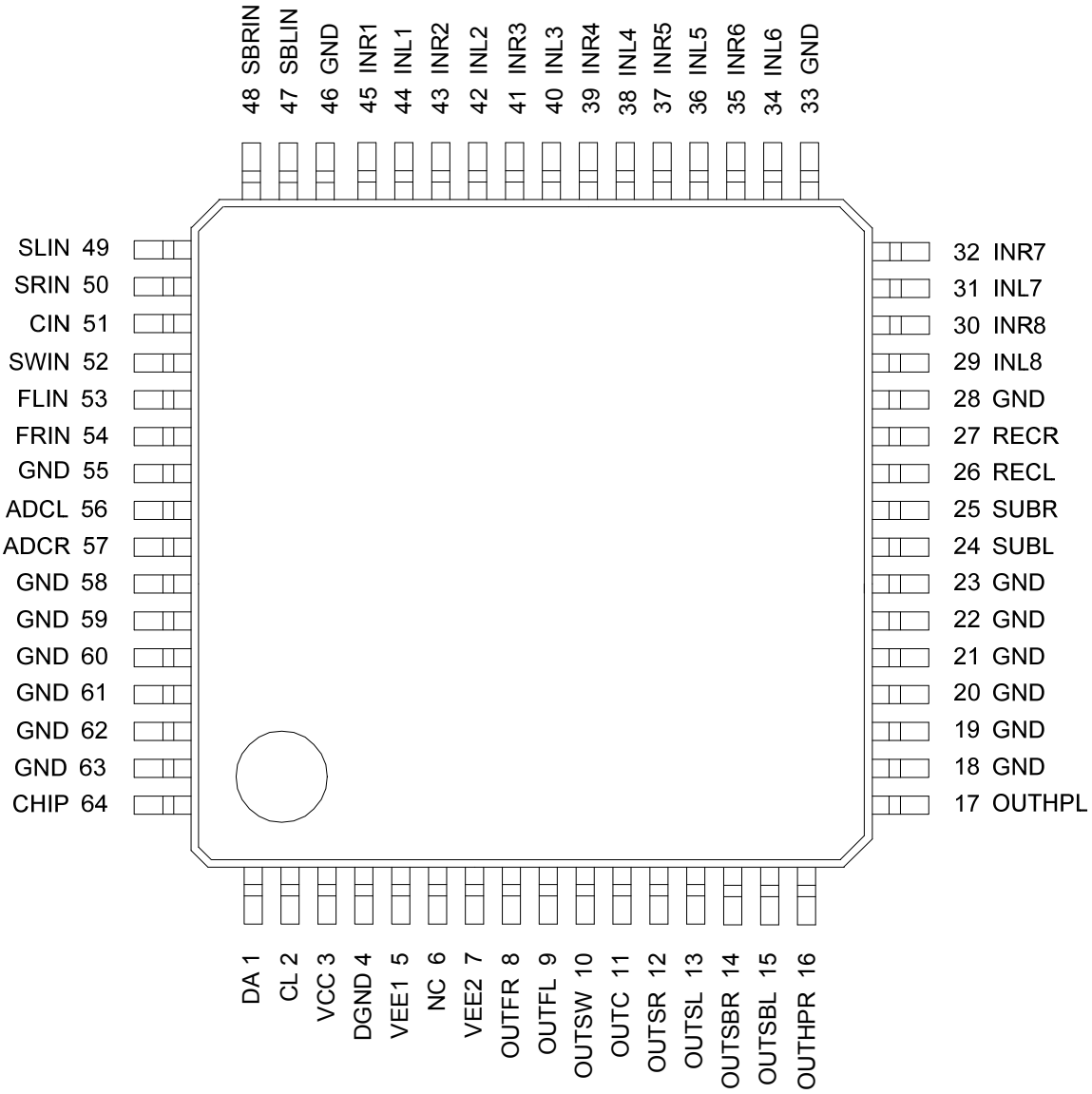


Figure 2. Pin Configuration

Description of terminal

Terminal Number	Symbol	Function	Terminal Number	Symbol	Function
1	DA	Data and latch input terminal	33	GND	Analog ground terminal
2	CL	Clock input terminal	34	INL6	Lch input terminal 6
3	VCC	Positive power supply terminal	35	INR6	Rch input terminal 6
4	DGND	Digital ground terminal	36	INL5	Lch input terminal 5
5	VEE1	Negative power supply terminal 1	37	INR5	Rch input terminal 5
6	NC	No connect	38	INL4	Lch input terminal 4
7	VEE2	Negative power supply terminal 2	39	INR4	Rch input terminal 4
8	OUTFR	FRch Output terminal	40	INL3	Lch input terminal 3
9	OUTFL	FLch Output terminal	41	INR3	Rch input terminal 3
10	OUTSW	SWch Output terminal	42	INL2	Lch input terminal 2
11	OUTC	Cch Output terminal	43	INR2	Rch input terminal 2
12	OUTSR	SRch Output terminal	44	INL1	Lch input terminal 1
13	OUTSL	SLch Output terminal	45	INR1	Rch input terminal 1
14	OUTSBR	SBRch Output terminal	46	GND	Analog ground terminal
15	OUTSBL	SBLch Output terminal	47	SBLIN	SBLch DSP input terminal
16	OUTHPR	HPRch Output terminal	48	SBRLIN	SBRch DSP input terminal
17	OUTHPL	HPLch Output terminal	49	SLIN	SLch DSP input terminal
18	GND	Analog ground terminal	50	SRIN	SRch DSP input terminal
19	GND	Analog ground terminal	51	CIN	Cch DSP input terminal
20	GND	Analog ground terminal	52	SWIN	SWch DSP input terminal
21	GND	Analog ground terminal	53	FLIN	FLch DSP input terminal
22	GND	Analog ground terminal	54	FRIN	FRch DSP input terminal
23	GND	Analog ground terminal	55	GND	Analog ground terminal
24	SUBL	Lch SUB Output terminal	56	ADCL	Lch ADC Output terminal
25	SUBR	Rch SUB Output terminal	57	ADCR	Rch ADC Output terminal
26	RECL	Lch REC Output terminal	58	GND	Analog ground terminal
27	RECR	Rch REC Output terminal	59	GND	Analog ground terminal
28	GND	Analog ground terminal	60	GND	Analog ground terminal
29	INL8	Lch input terminal 8	61	GND	Analog ground terminal
30	INR8	Rch input terminal 8	62	GND	Analog ground terminal
31	INL7	Lch input terminal 7	63	GND	Analog ground terminal
32	INR7	Rch input terminal 7	64	CHIP	Chip select terminal

Block Diagram

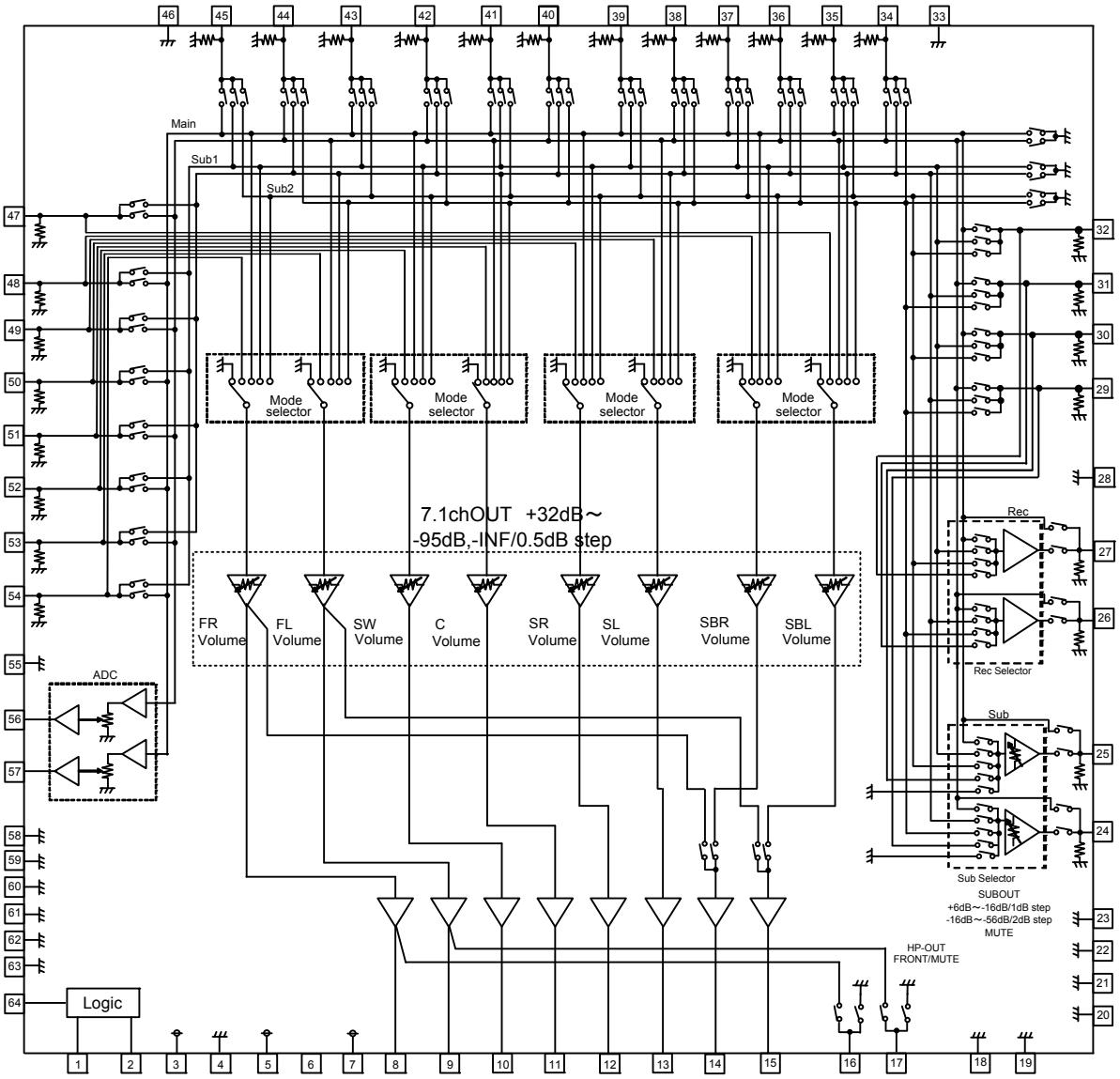


Figure 3. Block Diagram

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Positive power supply	VCC	+7.75 (Note1)	V
Negative power supply	VEE	-7.75 (Note1)	V
Power dissipation	Pd	1.50 (Note2)	W
Input voltage	Vin	VEE-0.2 to VCC+0.2	V
Operating temperature	Topr	-40 to +85 (Note3)	°C
Storage temperature	Tstg	-55 to +150	°C

(Note1) The maximum voltage that can be applied based on GND.
(Note2) Derating at 12.0mW/°C for operating above Ta≥25°C (mounted on 70×70×1.6mm ROHM standard board)
(Note3) If it is within the operation voltage range, circuit functions operation is guaranteed within operation temp.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Operating Condition

Item	Symbol	Rating	Unit
Positive power supply	VCC	+6.5 to +7.5 (Note4,5)	V
Negative power supply	VEE	-6.5 to -7.5 (Note4,5)	V

(Note4) Applying voltage based on GND.
(Note5) Within the operating temperature range, basic circuit function and operation are guaranteed within this operation voltage range. But please confirm the setting of the constants, temperature, etc. Please take note that electrical characteristics other than defined values cannot be guaranteed, however original function will retain.

Electrical characteristic

Unless otherwise specified, Ta=25°C, VCC=7V, VEE=-7V, f=1kHz, Vin=1Vrms, RL=10kΩ,
Stereo input selector(MAIN, SUB1, SUB2)=IN1, Mode selector(FL, FRch)=MAIN,
Mode selector(SW, C, SL, SRch)=MULTI, Mode selector(SBL, SBRch)=MULTI, SB OUTSEL=SB,
Input Att=0dB, Input gain=0dB, Volume=0dB.

	Item	Symbol	Limit			Unit	Conditions
			Min.	Typ.	Max.		
TOTAL	Positive circuit current	Iqp	-	32	45	mA	No signal
	Negative circuit current	Iqn	-45	-32	-	mA	No signal
	Output voltage gain	Gv	-1.5	0	1.5	dB	8 to 15pin output
	Channel balance	CB	-0.5	0	0.5	dB	C Channel reference, 8 to 15pin output
	Total harmonic distortion	THD	-	0.0004	0.02	%	BW=400 to 30kHz 8 to 15pin output
	Maximum output voltage	Vom	3.8	4.2	-	Vrms	THD=1%, VOLUME=+10dB 8 to 15pin output
	Output noise voltage *	Vno	-	1.2	10	μVrms	Rg=0Ω, BW=IHF-A 8 to 15pin output
	Residual output noise voltage *	Vnor	-	1	8	μVrms	Volume=Mute, Rg=0Ω, BW=IHF-A 8 to 15pin output
	Cross-talk between channels *	CT	-	-105	-80	dB	Rg=0Ω, BW=IHF-A 8, 9pin output
	Cross-talk between selectors *	CS	-	-105	-80	dB	Rg=0Ω, BW=IHF-A 8, 9pin output
	Input impedance	Rin	32	47	62	kΩ	24 to 27, 29 to 32 34 to 35, 47 to 54 pin input
VOLUME	Maximum attenuation *	ATTmax	-	-115	-100	dB	Volume=Mute, BW=IHF-A
REC OUT	Total harmonic distortion	THDR	-	0.0005	0.02	%	BW=400 to 30kHz, RL=6.8kΩ 24 to 27pin output
HPOUT	Output impedance	Ron	520	800	1080	Ω	16,17pin output

※VP-9690(Average detection value, effective value display) filter by Panasonic is used for * measurement.

Typical Performance Curve(s) (Reference data)

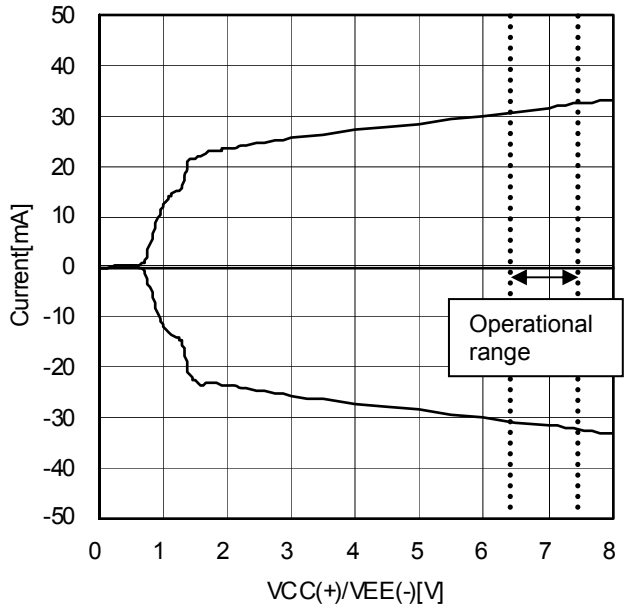


Figure 4. Circuit Currents vs. Circuit Voltage

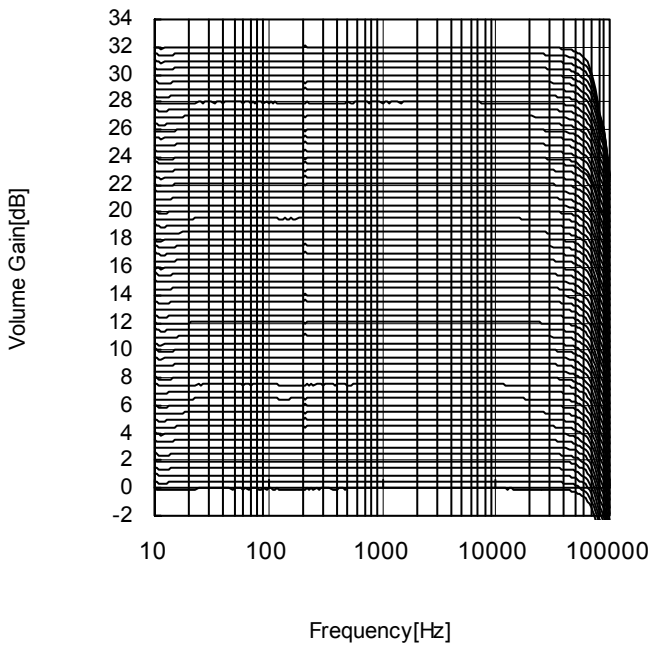


Figure 5. Volume Gain vs. Input Frequency
(32dB to 0 dB setting)

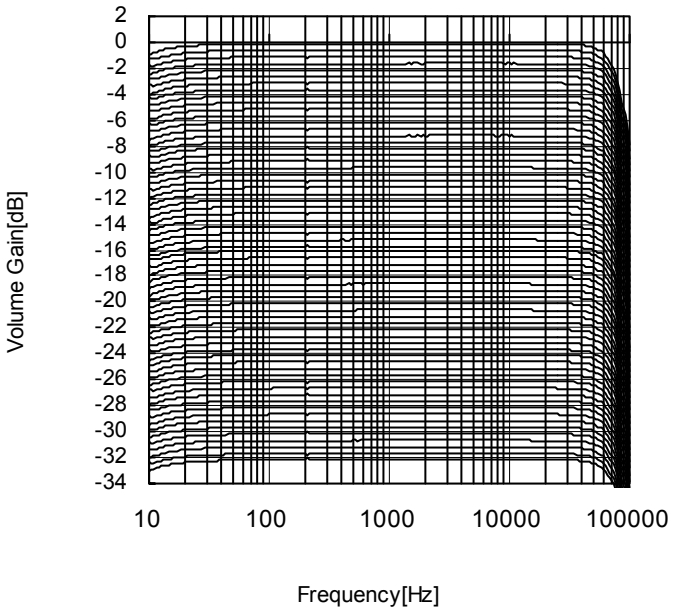


Figure 6. Volume Gain vs. Input Frequency
(0dB to -32 dB setting)

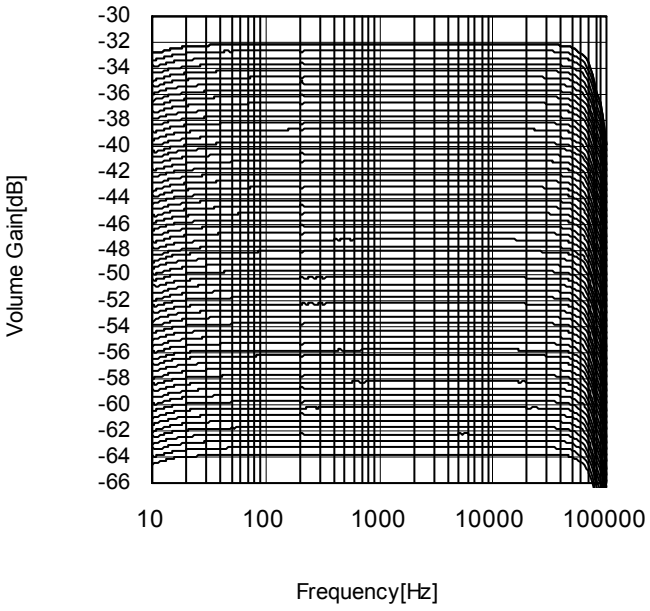


Figure 7. Volume Gain vs. Input Frequency
(-32dB to -64 dB setting)

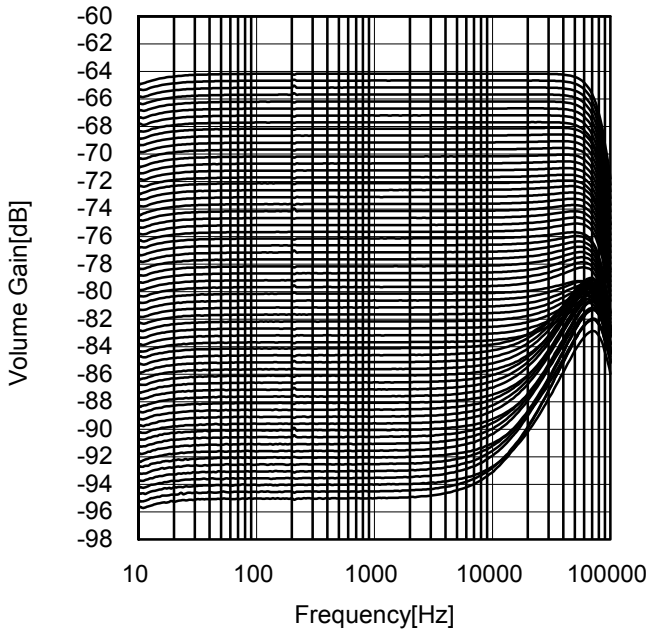


Figure 8. Volume Gain vs. Input Frequency
(-64dB to -95 dB setting)

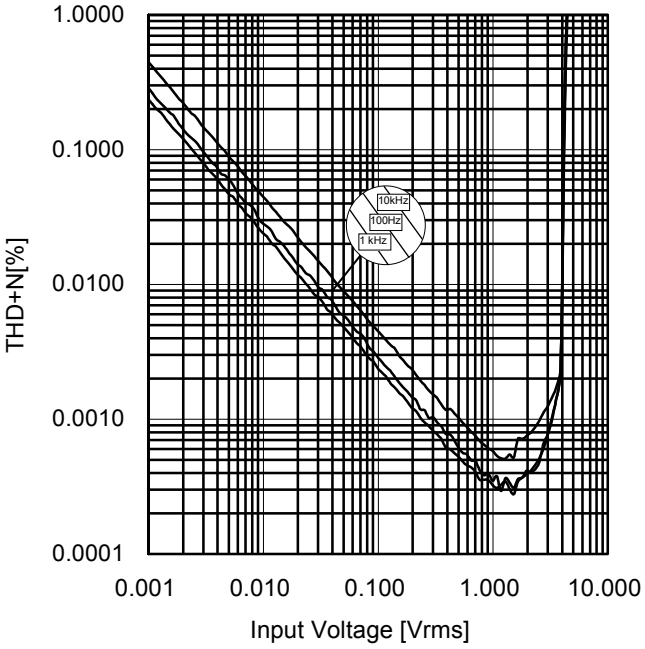


Figure 9. THD + N vs. Input Voltage

(Note) The measurement results of Figure 4 to Figure 8 used by 80kHz LPF.

Specifications for Control Signal

(1) Timing of control signal

Data is read at the rising edge of clock.
Latch is read at the falling edge of clock. Data on the latest 16bit is taken inside the IC.
Ensure to set DA and CL to LOW after Latch.

1byte=16bit

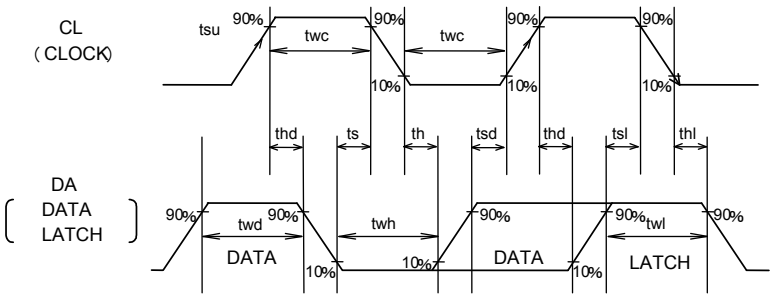


Figure 10. The timing definition of the control signal

Item	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Clock width	twc	1.0	-	-	μsec
Data width	twd	1.0	-	-	μsec
Latch width	twl	1.0	-	-	μsec
Low hold width	twh	1.0	-	-	μsec
Data setup time (DATA→CLK)	tsd	0.5	-	-	μsec
Data hold time (CLK→DATA)	thd	0.5	-	-	μsec
Latch setup time (CLK→LATCH)	tsl	0.5	-	-	μsec
Latch hold time	thl	0.5	-	-	μsec
Latch Low setup time	ts	0.5	-	-	μsec
Latch Low hold time	th	0.5	-	-	μsec

(2) Voltage of control signal (CL, DA, CHIP)

Item	Conditions	Limit			Unit
		Min.	Typ.	Max. (<VCC)	
High input voltage	Vcc=+6.5 to +7.5V Vee=-6.5 to -7.5V	2.3	-	5.5	V
Low input voltage		0	-	1.0	V

(3) Basic Structure of Control Data

←Input Direction

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data												Select Address			

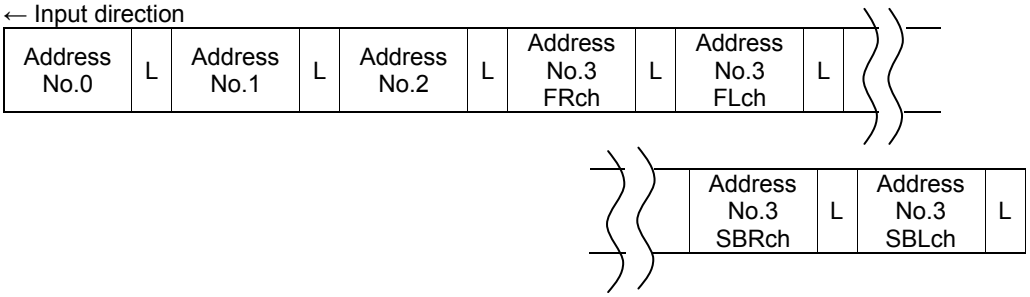
(4) Table of Control Data

←Input Direction

Select Address No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	Input Selector (MAIN)						REC ON/OFF	0	0	SUB ON/OFF	1	0	0		0	0
1	Input Selector (SUB1)						0	0	Input Selector (SUB2)				0		0	1
2	Mode Select FL, FRch		Mode Select C, SWch		Mode Select SL, SRch		Mode Select SBL, SBRch		0	ADC ATT			0		1	0
3	Volume channel Select				Volume								0	Chip Select	1	1
4	0	HPOUT SEL	MSEL FRONT	MSEL C,SW	MSEL SUR	MSEL SURB	SB OUTSEL	SUB MUTE	0	0	0	0	1		0	0
6	Mode Select REC		Mode Select SUB		1		Volume2						1		1	0
7	A→B switch-time			B→A switch-time			Base Clock	0	0	System Reset	0	0	1		1	1
BD3843FS (6ch Selector IC)													*	1	0	0
BD3841FS (9ch Selector IC)													*	1	0	1
BD3812F (2ch volume IC)													*	1	1	*

BD3471KS2, BD3473KS2 and BD3474KS2 could be controlled using same serial control line.
(In case of using the serial bus as common, please set chip select as “1”)
BD3843FS, BD3841FS and BD3812F could be controlled using same serial control line.
(In case of using the serial bus as common, please set chip select as “0”)
All data need to be initialized every time when turning on the power supply.

(Example)



As for second time onwards, after turning on the power supply, sending data of any address could be changed.

(5) Chip Select Setting Table

CHIP terminal condition	D2
0 (LOW)	0
1 (HIGH)	1

BD34705KS2 can operate in combination with another by setting the CHIP terminal.

Select Address No.0 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Input Selector (MAIN)	MUTE	0	0	0	0	0	0	Rec on/off	0	0	Sub on/off	1	0	0	Chip Select	0	0
	IN1	0	0	0	0	0	1										
	IN2	0	0	0	0	1	0										
	IN3	0	0	0	0	1	1										
	IN4	0	0	0	1	0	0										
	IN5	0	0	0	1	0	1										
	IN6	0	0	0	1	1	0										
	IN7	0	0	0	1	1	1										
	IN8	0	0	1	0	0	0										
	IN9	0	0	1	0	0	1										
	IN10	0	0	1	0	1	0										
	IN11	0	0	1	0	1	1										
	IN12	0	0	1	1	0	0										
	IN13(REC)	0	0	1	1	0	1										
	IN14(SUB)	0	0	1	1	1	0										
	Prohibition	0	1	0	0	0	0										
		⋮	⋮	⋮	⋮	⋮	⋮										
		1	1	1	1	1	1										
REC ON/OFF	OFF	Input Selector (MAIN)						0									
	ON							1									
SUB ON/OFF	OFF							Rec on/off			0						
	ON										1						

: Initial condition

Select Address No.1 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Input Selector (SUB1)	MUTE	0	0	0	0	0	0	0	0	Input Selector (SUB2)				0	Chip Select	0	1
	IN1	0	0	0	0	0	1										
	IN2	0	0	0	0	1	0										
	IN3	0	0	0	0	1	1										
	IN4	0	0	0	1	0	0										
	IN5	0	0	0	1	0	1										
	IN6	0	0	0	1	1	0										
	IN7	0	0	0	1	1	1										
	IN8	0	0	1	0	0	0										
	IN9	0	0	1	0	0	1										
	IN10	0	0	1	0	1	0										
	IN11	0	0	1	0	1	1										
	IN12	0	0	1	1	0	0										
	Prohibition	0	0	1	0	0	1										
		⋮	⋮	⋮	⋮	⋮	⋮										
		1	1	1	1	1	1										
Input Selector (SUB2)	MUTE	Input Selector (SUB1)								0	0	0	0				
	IN1									0	0	0	1				
	IN2									0	0	1	0				
	IN3									0	0	1	1				
	IN4									0	1	0	0				
	IN5									0	1	0	1				
	IN6									0	1	1	0				
	IN7									0	1	1	1				
	IN8									1	0	0	0				
	Prohibition									1	0	0	1				
										⋮	⋮	⋮	⋮				
										1	1	1	1				

: Initial condition

Select Address No.2 Setting Table ※Select Address No.4 MSEL=**"0"**(Front,C,SW,SR,SRB)

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mode Selector FL, FRch	MUTE	0	0	Mode Selector C, SWch		Mode Selector SL, SRch		Mode Selector SBL, SBRch		0	ADC ATT			0	Chip Select	1	0
	MAIN	0	1														
	MULTI	1	0														
	SUB1	1	1														
Mode Selector C, SWch	MUTE	Mode Selector FL, FRch		0	0												
	MAIN			0	1												
	MULTI			1	0												
	SUB1			1	1												
Mode Selector SL, SRch	MUTE			Mode Selector C, SWch		0	0										
	MAIN					0	1										
	MULTI					1	0										
	SUB1					1	1										
Mode Selector SBL, SBRch	MUTE					Mode Selector SL, SRch		0	0								
	MULTI							0	1								
	SUB1							1	0								
	MAIN							1	1								

Select Address No.2 Setting Table ※Select Address No.4 MSEL=**"1"**(Front,C,SW,SR,SRB)

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mode Selector FL, FRch	MUTE	0	0	Mode Selector C, SWch		Mode Selector SL, SRch		Mode Selector SBL, SBRch		0	ADC ATT			0	Chip Select	1	0
	SUB2	0	1														
Mode Selector C, SWch	MUTE	Mode Selector FL, FRch		0	0												
	SUB2			0	1												
Mode Selector SL, SRch	MUTE			Mode Selector C, SWch		0	0										
	SUB2					0	1										
Mode Selector SBL, SBRch	MUTE					Mode Selector SL, SRch		0	0								
	SUB2							0	1								

Select Address No.2 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADC ATT	MUTE	Mode Selector FL, FRch		Mode Selector C, SWch		Mode Selector SL, SRch		Mode Selector SBL, SBRch		0	0	0	0	0	Chip Select	1	0
	0dB										0	0	1				
	-6dB										0	1	0				
	-6.5dB										0	1	1				
	-7.5dB										1	0	0				
	-9dB										1	0	1				
	-12dB										1	1	0				
	Prohibition										1	1	1				

: Initial condition

Select Address No.3 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume channel Select	FL	0	0	0	Volume									0	Chip Select	1	1
	FR	0	0	1													
	SW	0	1	0													
	C	0	1	1													
	SL	1	0	0													
	SR	1	0	1													
	SBL	1	1	0													
	SBR	1	1	1													
Volume	MUTE	Volume Channel Select			1	1	1	1	1	1	1	1	1				
	Prohibition					1	1	1	1	1	1	1	0				
						⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮				
						0	1	0	0	0	0	0	1				
	+32.0dB					0	1	0	0	0	0	0	0				
	+31.5dB					0	0	1	1	1	1	1	1				
	+31.0dB					0	0	1	1	1	1	1	0				
	+30.5dB					0	0	1	1	1	1	0	1				
	+30.0dB					0	0	1	1	1	1	0	0				
	+29.5dB					0	0	1	1	1	0	1	1				
	+29.0dB					0	0	1	1	1	0	1	0				
	+28.5dB					0	0	1	1	1	0	0	1				
	+28.0dB					0	0	1	1	1	0	0	0				
	+27.5dB					0	0	1	1	0	1	1	1				
	+27.0dB					0	0	1	1	0	1	1	0				
	+26.5dB					0	0	1	1	0	1	0	1				
	+26.0dB					0	0	1	1	0	1	0	0				
	+25.5dB					0	0	1	1	0	0	1	1				
	+25.0dB					0	0	1	1	0	0	1	0				
	+24.5dB					0	0	1	1	0	0	0	1				
	+24.0dB					0	0	1	1	0	0	0	0				
	+23.5dB					0	0	1	0	1	1	1	1				
	+23.0dB					0	0	1	0	1	1	1	0				
	+22.5dB					0	0	1	0	1	1	0	1				
	+22.0dB					0	0	1	0	1	1	0	0				
	+21.5dB					0	0	1	0	1	0	1	1				
	+21.0dB					0	0	1	0	1	0	1	0				
	+20.5dB					0	0	1	0	1	0	0	1				
	+20.0dB					0	0	1	0	1	0	0	0				
	+19.5dB					0	0	1	0	0	1	1	1				
	+19.0dB					0	0	1	0	0	1	1	0				
	+18.5dB					0	0	1	0	0	1	0	1				
	+18.0dB					0	0	1	0	0	1	0	0				
	+17.5dB					0	0	1	0	0	0	1	1				
	+17.0dB					0	0	1	0	0	0	1	0				
	+16.5dB					0	0	1	0	0	0	0	1				
	+16.0dB					0	0	1	0	0	0	0	0				
	+15.5dB					0	0	0	1	1	1	1	1				

: Initial condition

Select Address No.3 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume	+15.0dB	Volume Channel Select			1	0	0	0	1	1	1	1	0	0	Chip Select	1	1
	+14.5dB					0	0	0	1	1	1	0	1				
	+14.0dB					0	0	0	1	1	1	0	0				
	+13.5dB					0	0	0	1	1	0	1	1				
	+13.0dB					0	0	0	1	1	0	1	0				
	+12.5dB					0	0	0	1	1	0	0	1				
	+12.0dB					0	0	0	1	1	0	0	0				
	+11.5dB					0	0	0	1	0	1	1	1				
	+11.0dB					0	0	0	1	0	1	1	0				
	+10.5dB					0	0	0	1	0	1	0	1				
	+10.0dB					0	0	0	1	0	1	0	0				
	+9.5dB					0	0	0	1	0	0	1	1				
	+9.0dB					0	0	0	1	0	0	1	0				
	+8.5dB					0	0	0	1	0	0	0	1				
	+8.0dB					0	0	0	1	0	0	0	0				
	+7.5dB					0	0	0	0	1	1	1	1				
	+7.0dB					0	0	0	0	1	1	1	0				
	+6.5dB					0	0	0	0	1	1	0	1				
	+6.0dB					0	0	0	0	1	1	0	0				
	+5.5dB					0	0	0	0	1	0	1	1				
	+5.0dB					0	0	0	0	1	0	1	0				
	+4.5dB					0	0	0	0	1	0	0	1				
	+4.0dB					0	0	0	0	1	0	0	0				
	+3.5dB					0	0	0	0	0	1	1	1				
	+3.0dB					0	0	0	0	0	1	1	0				
	+2.5dB					0	0	0	0	0	1	0	1				
	+2.0dB					0	0	0	0	0	1	0	0				
	+1.5dB					0	0	0	0	0	0	1	1				
	+1.0dB					0	0	0	0	0	0	1	0				
	+0.5dB					0	0	0	0	0	0	0	1				
	Prohibition					0	0	0	0	0	0	0	0				
	-0dB				0	0	0	0	0	0	0	0	0				
	-0.5dB					0	0	0	0	0	0	0	1				
	-1.0dB					0	0	0	0	0	0	1	0				
	-1.5dB					0	0	0	0	0	0	1	1				
	-2.0dB					0	0	0	0	0	1	0	0				
	-2.5dB					0	0	0	0	0	1	0	1				
	-3.0dB					0	0	0	0	0	1	1	0				
	-3.5dB					0	0	0	0	0	1	1	1				
	-4.0dB					0	0	0	0	1	0	0	0				
	-4.5dB					0	0	0	0	1	0	0	1				
	-5.0dB					0	0	0	0	1	0	1	0				
	-5.5dB					0	0	0	0	1	0	1	1				
	-6.0dB					0	0	0	0	1	1	0	0				
	-6.5dB					0	0	0	0	1	1	0	1				
	-7.0dB					0	0	0	0	1	1	1	0				
	-7.5dB					0	0	0	0	1	1	1	1				

Select Address No.3 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume	-8.0dB	Volume Channel Select			0	0	0	0	1	0	0	0	0	0	Chip Select	1	1
	-8.5dB					0	0	0	1	0	0	0	1				
	-9.0dB					0	0	0	1	0	0	1	0				
	-9.5dB					0	0	0	1	0	0	1	1				
	-10.0dB					0	0	0	1	0	1	0	0				
	-10.5dB					0	0	0	1	0	1	0	1				
	-11.0dB					0	0	0	1	0	1	1	0				
	-11.5dB					0	0	0	1	0	1	1	1				
	-12.0dB					0	0	0	1	1	0	0	0				
	-12.5dB					0	0	0	1	1	0	0	1				
	-13.0dB					0	0	0	1	1	0	1	0				
	-13.5dB					0	0	0	1	1	0	1	1				
	-14.0dB					0	0	0	1	1	1	0	0				
	-14.5dB					0	0	0	1	1	1	0	1				
	-15.0dB					0	0	0	1	1	1	1	0				
	-15.5dB					0	0	0	1	1	1	1	1				
	-16.0dB					0	0	1	0	0	0	0	0				
	-16.5dB					0	0	1	0	0	0	0	1				
	-17.0dB					0	0	1	0	0	0	1	0				
	-17.5dB					0	0	1	0	0	0	1	1				
	-18.0dB					0	0	1	0	0	1	0	0				
	-18.5dB					0	0	1	0	0	1	0	1				
	-19.0dB					0	0	1	0	0	1	1	0				
	-19.5dB					0	0	1	0	0	1	1	1				
	-20.0dB					0	0	1	0	1	0	0	0				
	-20.5dB					0	0	1	0	1	0	0	1				
	-21.0dB					0	0	1	0	1	0	1	0				
	-21.5dB					0	0	1	0	1	0	1	1				
	-22.0dB					0	0	1	0	1	1	0	0				
	-22.5dB					0	0	1	0	1	1	0	1				
	-23.0dB					0	0	1	0	1	1	1	0				
	-23.5dB					0	0	1	0	1	1	1	1				
	-24.0dB					0	0	1	1	0	0	0	0				
	-24.5dB					0	0	1	1	0	0	0	1				
	-25.0dB					0	0	1	1	0	0	1	0				
	-25.5dB					0	0	1	1	0	0	1	1				
	-26.0dB					0	0	1	1	0	1	0	0				
	-26.5dB					0	0	1	1	0	1	0	1				
	-27.0dB					0	0	1	1	0	1	1	0				
	-27.5dB					0	0	1	1	0	1	1	1				
	-28.0dB					0	0	1	1	1	0	0	0				
	-28.5dB					0	0	1	1	1	0	0	1				
	-29.0dB					0	0	1	1	1	0	1	0				
	-29.5dB					0	0	1	1	1	0	1	1				
	-30.0dB					0	0	1	1	1	1	0	0				
	-30.5dB					0	0	1	1	1	1	0	1				
	-31.0dB					0	0	1	1	1	1	1	0				

Select Address No.3 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume	-31.5dB	Volume Channel Select			0	0	0	1	1	1	1	1	1	0	Chip Select	1	1
	-32.0dB					0	1	0	0	0	0	0	0				
	-32.5dB					0	1	0	0	0	0	0	1				
	-33.0dB					0	1	0	0	0	0	1	0				
	-33.5dB					0	1	0	0	0	0	1	1				
	-34.0dB					0	1	0	0	0	1	0	0				
	-34.5dB					0	1	0	0	0	1	0	1				
	-35.0dB					0	1	0	0	0	1	1	0				
	-35.5dB					0	1	0	0	0	1	1	1				
	-36.0dB					0	1	0	0	1	0	0	0				
	-36.5dB					0	1	0	0	1	0	0	1				
	-37.0dB					0	1	0	0	1	0	1	0				
	-37.5dB					0	1	0	0	1	0	1	1				
	-38.0dB					0	1	0	0	1	1	0	0				
	-38.5dB					0	1	0	0	1	1	0	1				
	-39.0dB					0	1	0	0	1	1	1	0				
	-39.5dB					0	1	0	0	1	1	1	1				
	-40.0dB					0	1	0	1	0	0	0	0				
	-40.5dB					0	1	0	1	0	0	0	1				
	-41.0dB					0	1	0	1	0	0	1	0				
	-41.5dB					0	1	0	1	0	0	1	1				
	-42.0dB					0	1	0	1	0	1	0	0				
	-42.5dB					0	1	0	1	0	1	0	1				
	-43.0dB					0	1	0	1	0	1	1	0				
	-43.5dB					0	1	0	1	0	1	1	1				
	-44.0dB					0	1	0	1	1	0	0	0				
	-44.5dB					0	1	0	1	1	0	0	1				
	-45.0dB					0	1	0	1	1	0	1	0				
	-45.5dB					0	1	0	1	1	0	1	1				
	-46.0dB					0	1	0	1	1	1	0	0				
	-46.5dB					0	1	0	1	1	1	0	1				
	-47.0dB					0	1	0	1	1	1	1	0				
	-47.5dB					0	1	0	1	1	1	1	1				
	-48.0dB					0	1	1	0	0	0	0	0				
	-48.5dB					0	1	1	0	0	0	0	1				
	-49.0dB					0	1	1	0	0	0	1	0				
	-49.5dB					0	1	1	0	0	0	1	1				
	-50.0dB					0	1	1	0	0	1	0	0				
	-50.5dB					0	1	1	0	0	1	0	1				
	-51.0dB					0	1	1	0	0	1	1	0				
	-51.5dB					0	1	1	0	0	1	1	1				
	-52.0dB					0	1	1	0	1	0	0	0				
	-52.5dB					0	1	1	0	1	0	0	1				
	-53.0dB					0	1	1	0	1	0	1	0				
	-53.5dB					0	1	1	0	1	0	1	1				
	-54.0dB					0	1	1	0	1	1	0	0				
	-54.5dB					0	1	1	0	1	1	0	1				

Select Address No.3 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume	-55.0dB	Volume Channel Select			0	0	1	1	0	1	1	1	0	0	Chip Select	1	1
	-55.5dB					0	1	1	0	1	1	1	1				
	-56.0dB					0	1	1	1	0	0	0	0				
	-56.5dB					0	1	1	1	0	0	0	1				
	-57.0dB					0	1	1	1	0	0	1	0				
	-57.5dB					0	1	1	1	0	0	1	1				
	-58.0dB					0	1	1	1	0	1	0	0				
	-58.5dB					0	1	1	1	0	1	0	1				
	-59.0dB					0	1	1	1	0	1	1	0				
	-59.5dB					0	1	1	1	0	1	1	1				
	-60.0dB					0	1	1	1	1	0	0	0				
	-60.5dB					0	1	1	1	1	0	0	1				
	-61.0dB					0	1	1	1	1	0	1	0				
	-61.5dB					0	1	1	1	1	0	1	1				
	-62.0dB					0	1	1	1	1	1	0	0				
	-62.5dB					0	1	1	1	1	1	0	1				
	-63.0dB					0	1	1	1	1	1	1	0				
	-63.5dB					0	1	1	1	1	1	1	1				
	-64.0dB					1	0	0	0	0	0	0	0				
	-64.5dB					1	0	0	0	0	0	0	1				
	-65.0dB					1	0	0	0	0	0	1	0				
	-65.5dB					1	0	0	0	0	0	1	1				
	-66.0dB					1	0	0	0	0	1	0	0				
	-66.5dB					1	0	0	0	0	1	0	1				
	-67.0dB					1	0	0	0	0	1	1	0				
	-67.5dB					1	0	0	0	0	1	1	1				
	-68.0dB					1	0	0	0	1	0	0	0				
	-68.5dB					1	0	0	0	1	0	0	1				
	-69.0dB					1	0	0	0	1	0	1	0				
	-69.5dB					1	0	0	0	1	0	1	1				
	-70.0dB					1	0	0	0	1	1	0	0				
	-70.5dB					1	0	0	0	1	1	0	1				
	-71.0dB					1	0	0	0	1	1	1	0				
	-71.5dB					1	0	0	0	1	1	1	1				
	-72.0dB					1	0	0	1	0	0	0	0				
	-72.5dB					1	0	0	1	0	0	0	1				
	-73.0dB					1	0	0	1	0	0	1	0				
	-73.5dB					1	0	0	1	0	0	1	1				
	-74.0dB					1	0	0	1	0	1	0	0				
	-74.5dB					1	0	0	1	0	1	0	1				
	-75.0dB					1	0	0	1	0	1	1	0				
	-75.5dB					1	0	0	1	0	1	1	1				
	-76.0dB					1	0	0	1	1	0	0	0				
	-76.5dB					1	0	0	1	1	0	0	1				
	-77.0dB					1	0	0	1	1	0	1	0				
	-77.5dB					1	0	0	1	1	0	1	1				
	-78.0dB					1	0	0	1	1	1	0	0				

Select Address No.3 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume	-78.5dB	Volume Channel Select			0	1	0	0	1	1	1	0	1	0	Chip Select	1	1
	-79.0dB					1	0	0	1	1	1	1	0				
	-79.5dB					1	0	0	1	1	1	1	1				
	-80.0dB					1	0	1	0	0	0	0	0				
	-80.5dB					1	0	1	0	0	0	0	1				
	-81.0dB					1	0	1	0	0	0	1	0				
	-81.5dB					1	0	1	0	0	0	1	1				
	-82.0dB					1	0	1	0	0	1	0	0				
	-82.5dB					1	0	1	0	0	1	0	1				
	-83.0dB					1	0	1	0	0	1	1	0				
	-83.5dB					1	0	1	0	0	1	1	1				
	-84.0dB					1	0	1	0	1	0	0	0				
	-84.5dB					1	0	1	0	1	0	0	1				
	-85.0dB					1	0	1	0	1	0	1	0				
	-85.5dB					1	0	1	0	1	0	1	1				
	-86.0dB					1	0	1	0	1	1	0	0				
	-86.5dB					1	0	1	0	1	1	0	1				
	-87.0dB					1	0	1	0	1	1	1	0				
	-87.5dB					1	0	1	0	1	1	1	1				
	-88.0dB					1	0	1	1	0	0	0	0				
	-88.5dB					1	0	1	1	0	0	0	1				
	-89.0dB					1	0	1	1	0	0	1	0				
	-89.5dB					1	0	1	1	0	0	1	1				
	-90.0dB					1	0	1	1	0	1	0	0				
	-90.5dB					1	0	1	1	0	1	0	1				
	-91.0dB					1	0	1	1	0	1	1	0				
	-91.5dB					1	0	1	1	0	1	1	1				
	-92.0dB					1	0	1	1	1	0	0	0				
	-92.5dB					1	0	1	1	1	0	0	1				
	-93.0dB					1	0	1	1	1	0	1	0				
	-93.5dB					1	0	1	1	1	0	1	1				
	-94.0dB					1	0	1	1	1	1	0	0				
	-94.5dB					1	0	1	1	1	1	0	1				
	-95.0dB					1	0	1	1	1	1	1	0				
	Prohibition					1	0	1	1	1	1	1	1				
						⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮				
						1	1	1	1	1	1	1	1				

Select Address No.4 Setting Table ※ON/OFF of each MSEL is reflected by Address No. 2 mode selector

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HPOUT SEL	MUTE	0	0	MSEL FRONT	MSEL C,SW	MSEL SUR	MSEL SURB	SB SELECT	SUB MUTE	0	0	0	0	0	Chip Select	1	1
	FRONT		1														
MSEL FRONT	OFF		HPOUT SEL	0													
	ON			1													
MSEL C,SW	OFF			MSEL FRONT	0												
	ON				1												
MSEL SUR	OFF				MSEL C,SW	0											
	ON					1											
MSEL SURB	OFF					MSEL SUR	0										
	ON						1										
SB Select	SURB						MSEL SURB	0									
	FRONT							1									
SUB MUTE	OFF							SB SELECT	0								
	ON								1								

Select Address No.6 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mode Selector REC	MAIN	0	0	Mode Selector SUB		1	Volume2							1	Chip Select	1	0
	SUB1	0	1														
	SUB2	1	0														
	MULTI	1	1														
Mode Selector SUB	MAIN	Mode Selector REC		0	0												
	SUB1			0	1												
	SUB2			1	0												
	MULTI			1	1												
Volume2	MUTE							1	1	1	1	1	1				
	Prohibition							1	1	1	1	1	0				
								⋮	⋮	⋮	⋮	⋮	⋮				
								0	0	0	1	1	1				
	+6.0dB						1	0	0	0	1	1	0				
	+5.0dB							0	0	0	1	0	1				
	+4.0dB							0	0	0	1	0	0				
	+3.0dB							0	0	0	0	1	1				
	+2.0dB							0	0	0	0	1	0				
	+1.0dB							0	0	0	0	0	1				
	+0.0dB						0	0	0	0	0	0	0				
	-1.0dB							0	0	0	0	0	1				
	-2.0dB							0	0	0	0	1	0				
	-3.0dB							0	0	0	0	1	1				
	-4.0dB							0	0	0	1	0	0				
	-5.0dB							0	0	0	1	0	1				

Select Address No.6 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume2	-6.0dB	Mode Selector REC		Mode Selector SUB		1	0	0	0	0	1	1	0	1	Chip Select	1	0
	-7.0dB							0	0	0	1	1	1				
	-8.0dB							0	0	1	0	0	0				
	-9.0dB							0	0	1	0	0	1				
	-10.0dB							0	0	1	0	1	0				
	-11.0dB							0	0	1	0	1	1				
	-12.0dB							0	0	1	1	0	0				
	-13.0dB							0	0	1	1	0	1				
	-14.0dB							0	0	1	1	1	0				
	-15.0dB							0	0	1	1	1	1				
	-16.0dB							0	1	0	0	0	0				
	-18.0dB							0	1	0	0	0	1				
	-20.0dB							0	1	0	0	1	0				
	-22.0dB							0	1	0	0	1	1				
	-24.0dB							0	1	0	1	0	0				
	-26.0dB							0	1	0	1	0	1				
	-28.0dB							0	1	0	1	1	0				
	-30.0dB							0	1	0	1	1	1				
	-32.0dB							0	1	1	0	0	0				
	-34.0dB							0	1	1	0	0	1				
	-36.0dB							0	1	1	0	1	0				
	-38.0dB							0	1	1	0	1	1				
	-40.0dB							0	1	1	1	0	0				
	-42.0dB							0	1	1	1	0	1				
	-44.0dB							0	1	1	1	1	0				
	-46.0dB							0	1	1	1	1	1				
	-48.0dB							1	0	0	0	0	0				
	-50.0dB							1	0	0	0	0	1				
	-52.0dB							1	0	0	0	1	0				
	-54.0dB							1	0	0	0	1	1				
	-56.0dB							1	0	0	1	0	0				
	Prohibition							1	0	0	1	0	1				
							⋮	⋮	⋮	⋮	⋮	⋮	⋮				
							1	1	1	1	1	1	1				

Select Address No.7 Setting Table

Function & Setting		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A→B switching-time	11msec	0	0	0	B→A switching-time			Base Clock	0	0	System Reset	0	0	1	Chip Select	1	1
	5msec	0	0	1													
	7msec	0	1	0													
	14msec	0	1	1													
	3msec	1	0	0													
	2msec	1	0	1													
	Prohibition	1	1	0													
		1	1	1													
B→A switching-time	11msec	A→B switching-time			0	0	0										
	5msec				0	0	1										
	7msec				0	1	0										
	14msec				0	1	1										
	3msec				1	0	0										
	2msec				1	0	1										
	Prohibition				1	1	0										
					1	1	1										
Base Clock	x1				B→A switching-time			0									
	×1/2							1									
System Reset	Normal							Base Clock			0						
	Reset										1						

: Initial condition

Select Address No.7, Data = D15-D13 : Below A → B switching time is adjustable.
Select Address No.7, Data = D12-D10 : Below B → A switching time is adjustable.

※Switching time over 11.2msec is recommended for both A→B and B→A.
※Set to same switching time for both A→B, B→A is recommended if the switching times need to be changed.

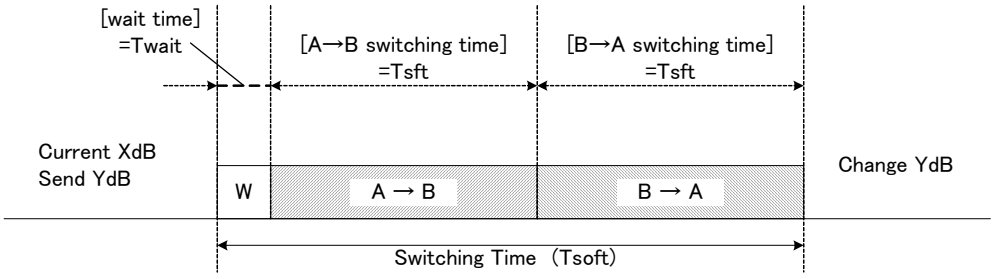


Figure 11. Micro step volume switching time

If the base clock is set to x1/2, the switching time will be doubled.

Micro step volume circuit

1. Micro step volume technology.

1-1. Micro step volume effects.

Micro step volume is ROHM original switching pop noise prevention technology. The audible signal is discontinuous during the gain switching instantly which cause the noise to occur. This micro step volume will prevent this discontinuous signal by completing the signal waveform and will significantly reduce the noise.

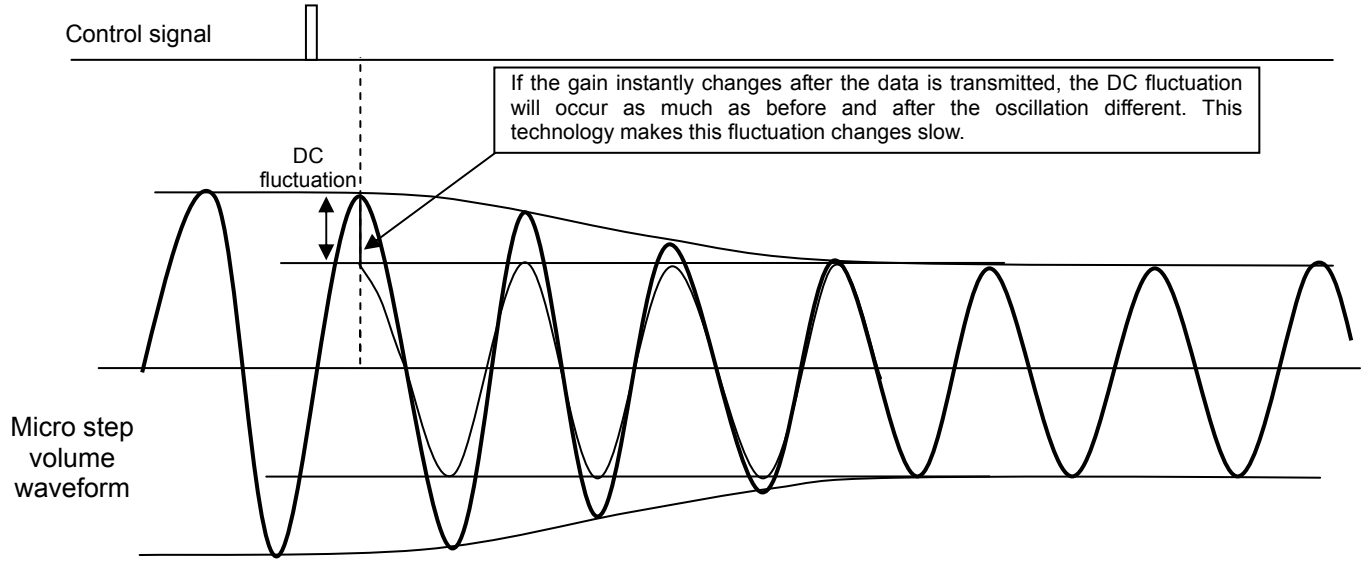


Figure 12. Micro step volume waveform

This micro step volume will start the switching when received the signal sent from the micon.

At any constant time, the switching waveform is shown as above figure. This IC will optimally operates by internally processes the data sent from the micon to prevent the switching shock.

However, sometimes the switching waveform is not like the intended form depends on the transmission timing. Therefore, below is the example of the relationship between the transmission timing and actual switching time. Please consider this relationship for the setting.

1-2. Micro step volume application target block

・Micro step volume application target blocks are 7.1ch volume and SUB volume.

2. About data transmission of Micro step volume circuit

2-1. Switching time of Micro step volume

This switching time includes [Wait time], [A→B switching time] and [B→A switching time]. Every switching time needs around 25msec. (Tsoft = Twait + 2 * Tsft, Twait=2.3msec, Tsft=11.2msec)
Please take note that Twait is wait time for starting switching and the setting is 2.3msec. (Twait considers the internal IC tolerance, therefore this time need to be set within 1.3msec (Min.) to 4.6msec (Max.).

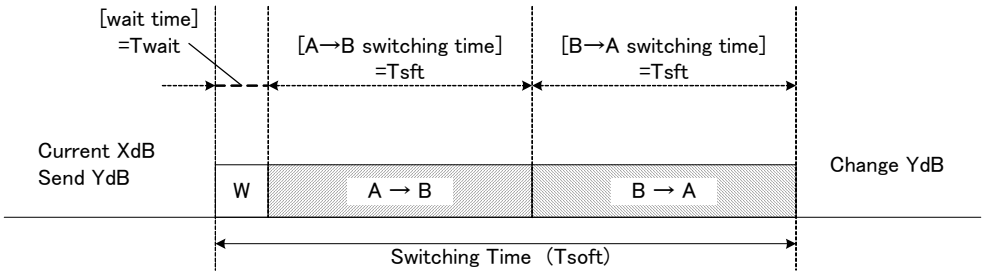


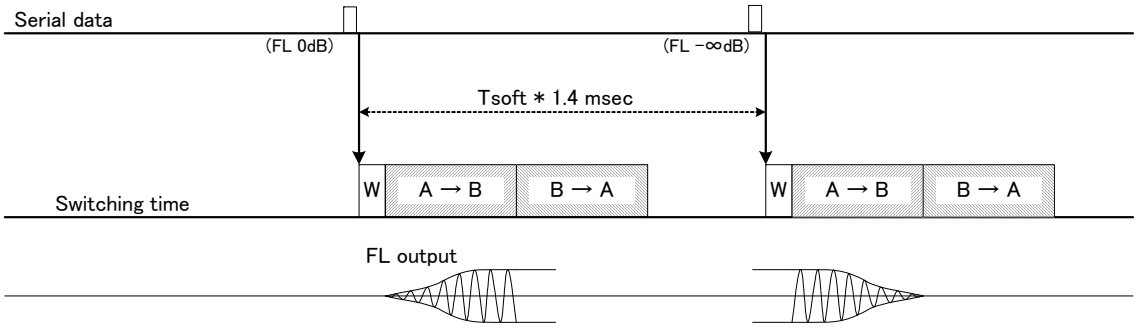
Figure 13. [A→B switching time] and [B→A switching time]

In addition, base clock can change the frequency using the internal oscillation device. For example, when base clock x1/2 is selected, [Wait time], [A→B switching time] and [B→A switching time] are doubled.

2-2. Same block data transmission timing and switching operation.

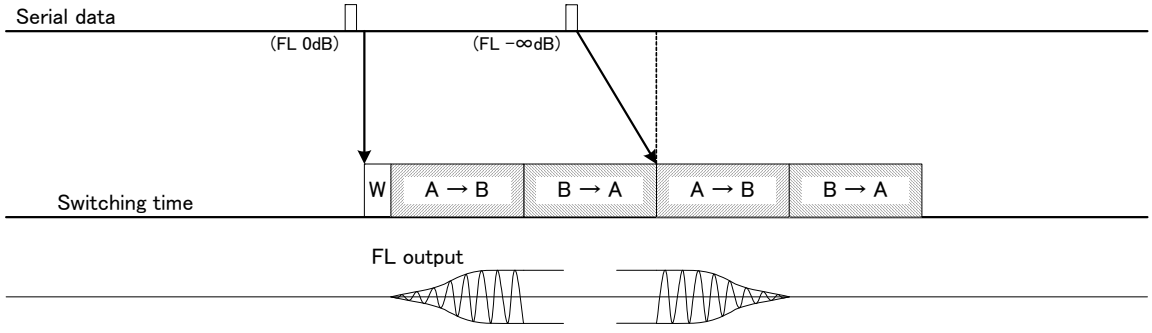
■ Transmission example 1

The time chart from data transmission to switching start time is shown as below.
At first, below figure shows transmitted data with the same block which is separated with enough interval.
This enough interval refers to the tolerance margin time of Tsoft multiplied by 1.4.



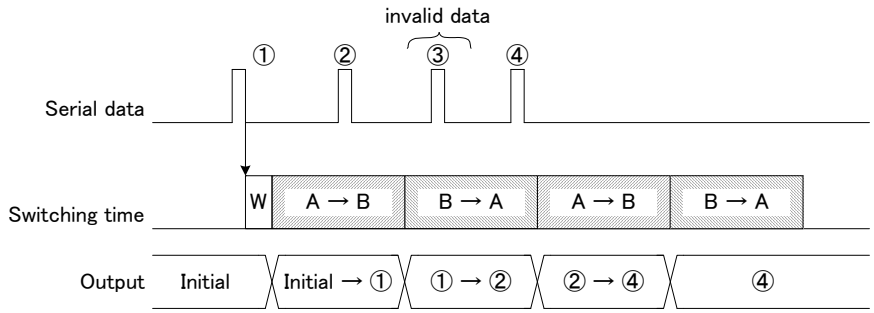
■ Transmission example 2

Next, below figure shows the example of when the transmission interval is not enough (smaller than above interval).
When the data transmitted during the first operation of the switching, the second data transmission will continue after complete the first operation. In this case, there is no wait time (Twait) before the second transmission.



■ Transmission example 3

Next is the example for switching operation with smaller data transmission interval.



Data ② is the data during the A→B operation, so this data is valid, and then during B→A operation, data ① promptly switches to data②.
Data ③ and data ④ are data during B→A operation, therefore these data are valid for the next switching, but data ③ got overwritten by data ④ so data ③ will become invalid. Only data ④ is valid.
There is no regulation on the transmission timing.

For data transmission to multi-channels, there is a caution. The combination of Lch and Rch for same block will make the switching is possible to change at same timing. When the setting is data ① for FL (Lch) and data ② for FR (Rch), same switching timing is possible if the data transmission is set as below figure.

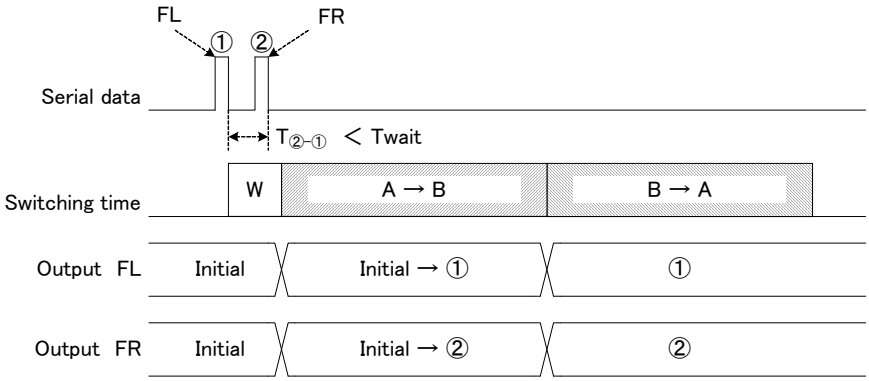


Figure 14. The operation during multi-channels (Lch, Rch) data transmission (smaller than Twait interval).

Next, when data ② is not transmitted during the Twait, the switching operation is as following figure.

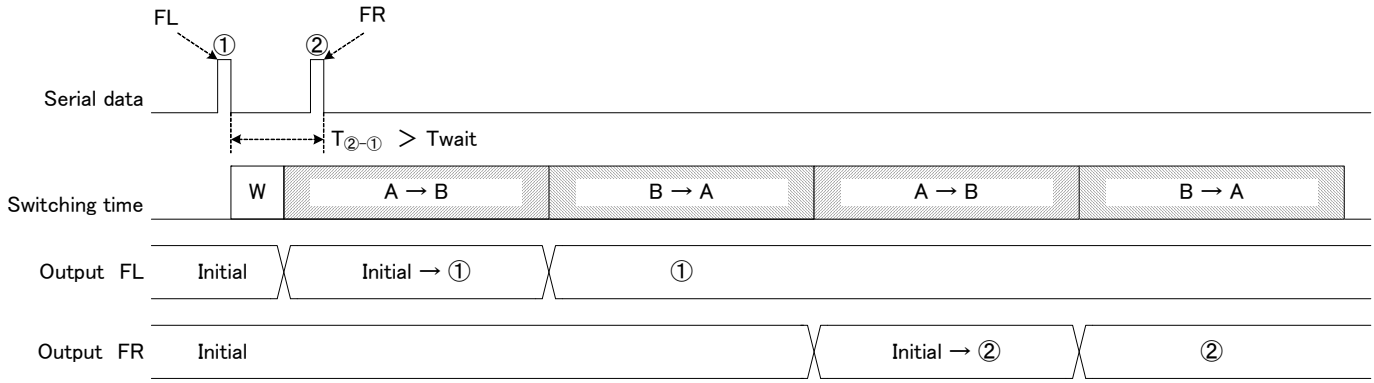


Figure 15. The operation during multi-channels (Lch, Rch) data transmission (larger than Twait interval).