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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Analog Sound Processor series

# Sound Processor with Built-in Surround Sound Function

## BD3491FS

### General Description

Built in stereo 6 input selectors and volume that there is not an impedance change of a volume terminal. And this is sound processor can realize 2-band equalizer (Bass/Treble, Gain  $\pm 14\text{dB}$  / 2dB\_step) and BassBoost, Output gain, Surround by external components.

### Features

- Equipped with 6 single ended stereo input selectors
- Built-in input gain controller suitable for mobile audio.
- Volume input terminal can be used as a microphone input terminal since its impedance remains constant even if volume setting is changed.
- Bi-CMOS process is suitable for the design of low current and low energy. It also provides more quality for Bi-CMOS small scale regulator and heat in a set.
- The package of this IC is SSOP-A32. Sound input terminals and output terminals arrangement is optimized for easy and fast layout of PCB pattern. At the same time, it minimizes PCB area.

### Applications

- Suitable for mini-components or micro components. Used for audio equipment of TV, DVD, etc.

### Key Specification

- Current upon no signal: 7mA(typ)
- Total Harmonic Distortion: 0.002%(typ)
- Maximum Input Voltage: 2.4Vrms(typ)
- Crosstalk between Selectors: 100dB(typ)
- Volume Control Range: 0dB to -87dB
- Output Noise Voltage: 5 $\mu$ Vrms(typ)
- Residual Output Noise Voltage: 5 $\mu$ Vrms(typ)
- Operating Temperature Range: -40°C to +85°C

**Package**  
SSOP-A32

**W(typ) x D(typ) x H(max)**  
13.60mm x 7.80mm x 2.01mm



SSOP-A32

### Typical Application Circuit

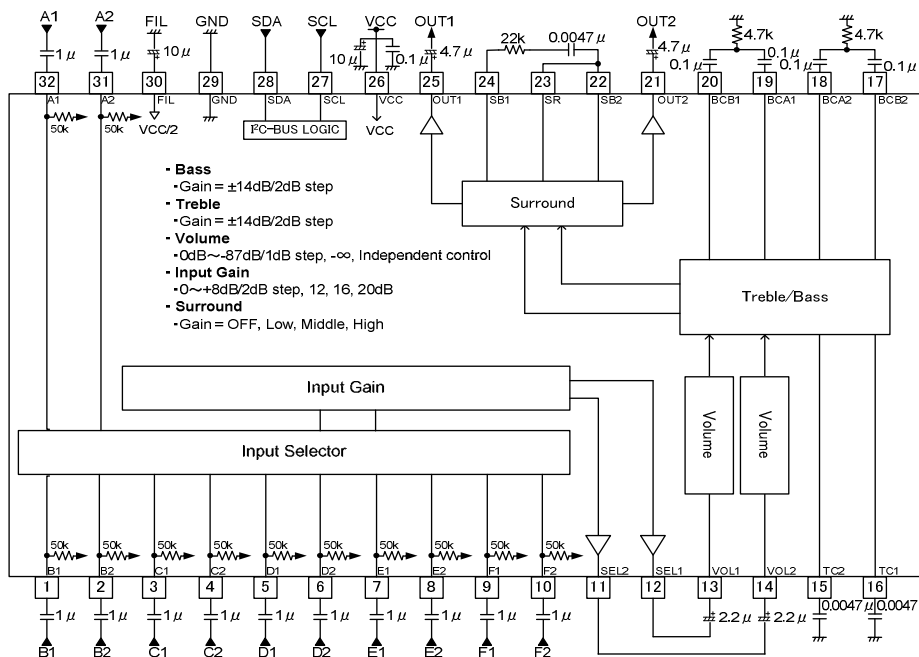


Figure 1. Application Circuit Diagram

## Pin Configuration

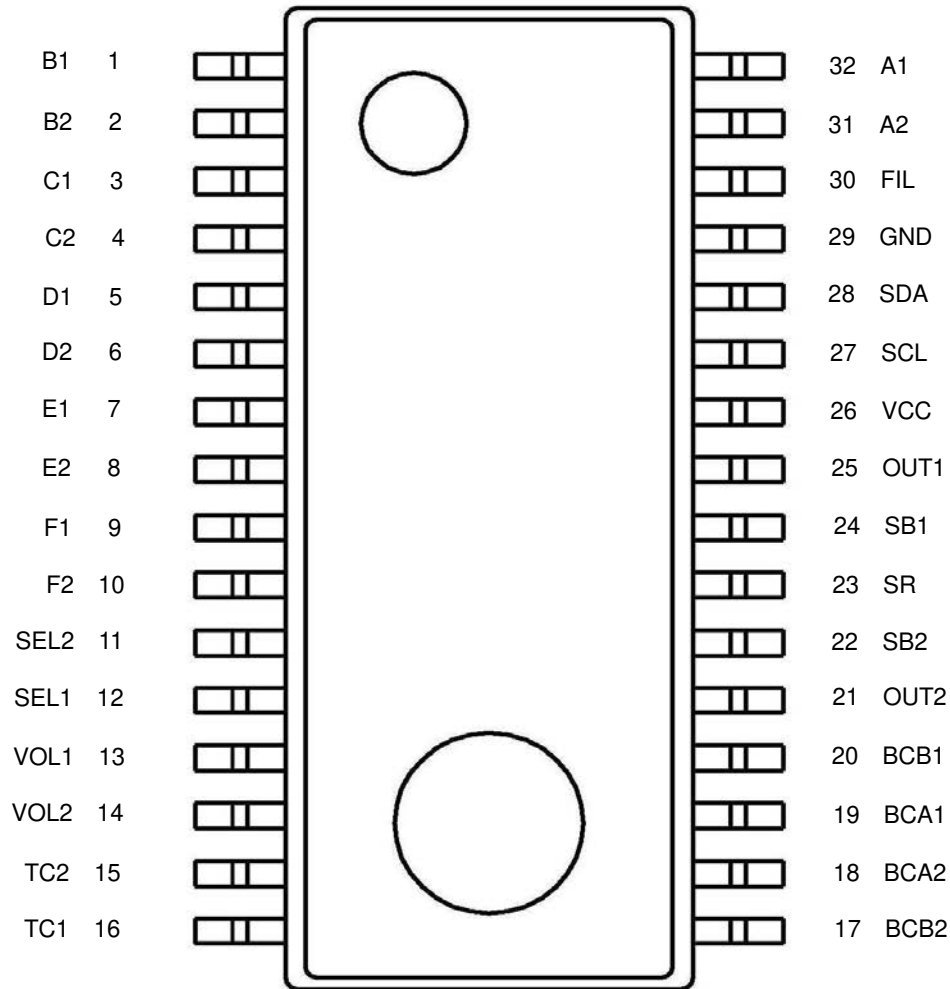


Figure 2. Pin Configuration

## Pin Descriptions

Terminal Number	Terminal Name	Description	Terminal Number	Terminal Name	Description
1	B1	Ch1 of B input terminal	17	BCB2	Ch2 of Bass filter terminal
2	B2	Ch2 of B input terminal	18	BCA2	Ch2 of Bass filter terminal
3	C1	Ch1 of C input terminal	19	BCA1	Ch1 of Bass filter terminal
4	C2	Ch2 of C input terminal	20	BCB1	Ch1 of Bass filter terminal
5	D1	Ch1 of D input terminal	21	OUT2	Ch2 of Output terminal
6	D2	Ch2 of D input terminal	22	SB2	Ch2 of Bass boost terminal
7	E1	Ch1 of E input terminal	23	SR	Surround terminal
8	E2	Ch2 of E input terminal	24	SB1	Ch1 of Bass boost terminal
9	F1	Ch1 of F input terminal	25	OUT1	Ch1 of Output terminal
10	F2	Ch2 of F input terminal	26	VCC	Power supply terminal
11	SEL2	Ch2 of selector output terminal	27	SCL	Serial communication clock terminal
12	SEL1	Ch1 of selector output terminal	28	SDA	Serial communication data terminal
13	VOL1	Ch1 of Volume input terminal	29	GND	GND terminal
14	VOL2	Ch2 of Volume input terminal	30	FIL	VCC/2 terminal
15	TC2	Ch2 of Treble filter terminal	31	A2	Ch2 of A input terminal
16	TC1	Ch1 of Treble filter terminal	32	A1	Ch1 of A input terminal

Block Diagram

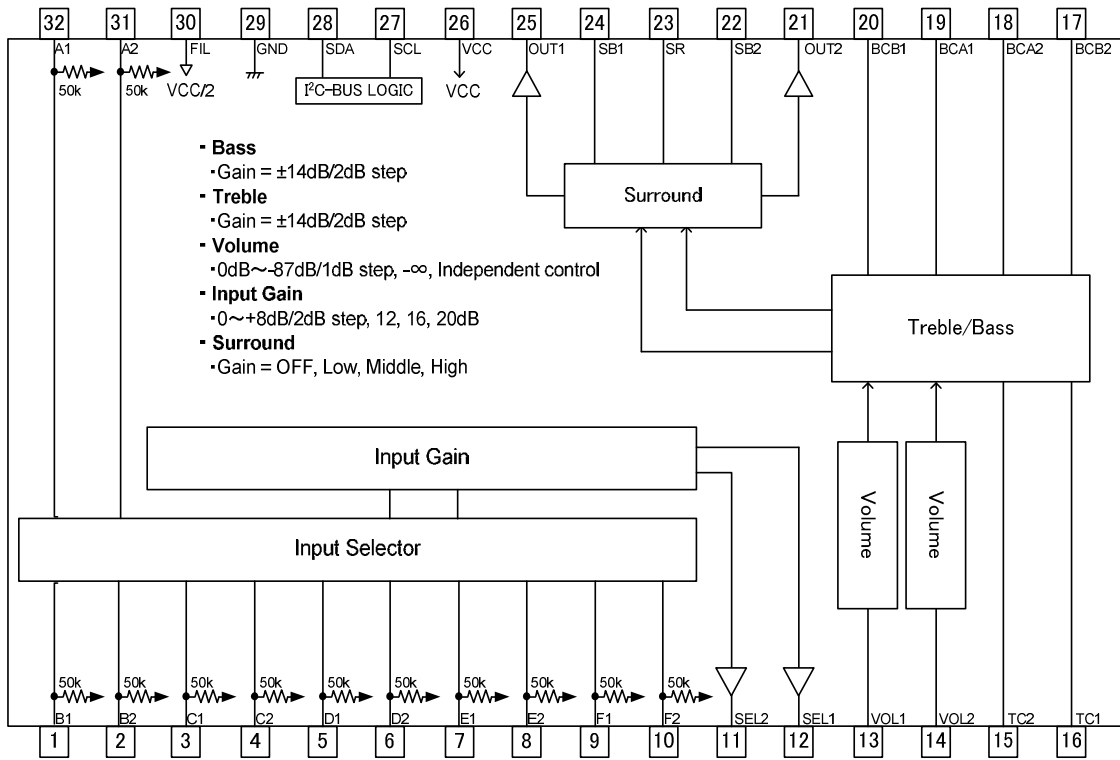


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Power supply Voltage	VCC	10.0	V
Input Voltage	Vin	VCC+0.3 to GND-0.3 SCL, SDA only 7 to GND-0.3	V
Power Dissipation	Pd	0.95 ※1	W
Storage Temperature	Tastg	-55 to +150	°C

※1 Derate by 7.6mW/°C for Ta=25°C or more.

ROHM standard board shall be mounted. Thermal resistance  $\theta_{ja} = 131.6(^{\circ}\text{C}/\text{W})$ .

ROHM standard board Size: 70x70x1.6(mm<sup>3</sup>)

Material: A FR4 glass epoxy board (3% or less of copper foil area)

Operating Range

Parameter	Symbol	Limits	Unit
Power supply voltage	VCC	4.75 to 9.5	V
Temperature	Topr	-40 to +85	°C

## Electrical Characteristics

(Unless specified particularly,  $T_a=25^\circ\text{C}$ ,  $V_{CC}=9.0\text{V}$ ,  $f=1\text{kHz}$ ,  $V_{in}=1\text{Vrms}$ ,  $R_g=600\Omega$ ,  $R_L=10\text{k}\Omega$ , A input, Input gain 0dB, Volume 0dB, Bass 0dB, Treble 0dB, Surround Mode OFF, Surround Gain = OFF)

BLOCK	Item	Symbol	Limit			Unit	Condition
			Min.	Typ.	Max.		
GENERAL	Current upon no signal	$I_Q$	—	7	15	mA	No signal
	Voltage Gain	$G_V$	-1.5	0	+1.5	dB	$G_V=20\log(V_{out}/V_{in})$
	Channel Balance	CB	-1.5	0	+1.5	dB	$CB = G_{V1}-G_{V2}$
	Total Harmonic Distortion	THD+N	—	0.002	0.1	%	$V_{out}=1\text{Vrms}$ $BW=400\text{-}30\text{kHz}$
	Output Noise Voltage	$V_{NO}$	—	5	20	$\mu\text{Vrms}$	$R_g = 0\Omega$ $BW = \text{IHF-A}$
	Residual Output Noise Voltage	$V_{NOR}$	—	5	20	$\mu\text{Vrms}$	$R_g = 0\Omega$ $BW = \text{IHF-A}$ Volume = $-\infty$
	Crosstalk between Channels	CTC	—	-100	-80	dB	$R_g = 0\Omega$ $CTC=20\log(V_{out2}/V_{out1})$ $BW = \text{IHF-A}$
INPUT SELECTOR	Input Impedance	$R_{IN}$	35	50	65	k $\Omega$	
	Maximum Input Voltage	$V_{IM}$	2.1	2.4	-	Vrms	$V_{IM}$ at $THD+N(V_{out})=1\%$ $BW=400\text{-}30\text{kHz}$
	Crosstalk between Selectors	CTS	—	-100	-84	dB	$R_g = 0\Omega$ $CTS=20\log(V_{out}/V_{in})$ $BW = \text{IHF-A}$
VOLUME	Control Range	$G_{V\text{ MAX}}$	-90	-87	-84	dB	$V_{in}=2\text{Vrms}$ $G_V=20\log(V_{out}/V_{in})$
	Maximum Attenuation	$G_{V\text{ MIN}}$	—	-100	-80	dB	Volume = $-\infty$ $G_V=20\log(V_{out}/V_{in})$
BASS	Maximum Boost Gain	$G_{B\text{ BST}}$	11.5	14	16.5	dB	Gain = 14dB, $f = 100\text{Hz}$ $V_{in}=100\text{mVrms}$ $G_V=20\log(V_{out}/V_{in})$
	Maximum Cut Gain	$G_{B\text{ CUT}}$	-16.5	-14	-11.5	dB	Gain = -14dB, $f = 100\text{Hz}$ $V_{in}=2\text{Vrms}$ $G_V=20\log(V_{out}/V_{in})$
TREBLE	Maximum Boost Gain	$G_{T\text{ BST}}$	11.5	14	16.5	dB	Gain = 14dB, $f = 10\text{kHz}$ $V_{in}=100\text{mVrms}$ $G_V=20\log(V_{out}/V_{in})$
	Maximum Cut Gain	$G_{T\text{ CUT}}$	-16.5	-14	-11.5	dB	Gain = -14dB, $f = 10\text{kHz}$ $V_{in}=2\text{Vrms}$ $G_V=20\log(V_{out}/V_{in})$

※Phase between input / output is same.

Typical Performance Curves

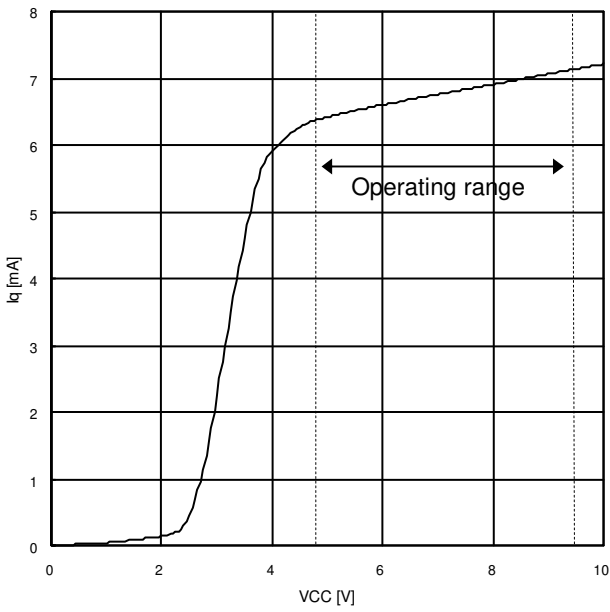


Figure 4. Vcc vs. Iq

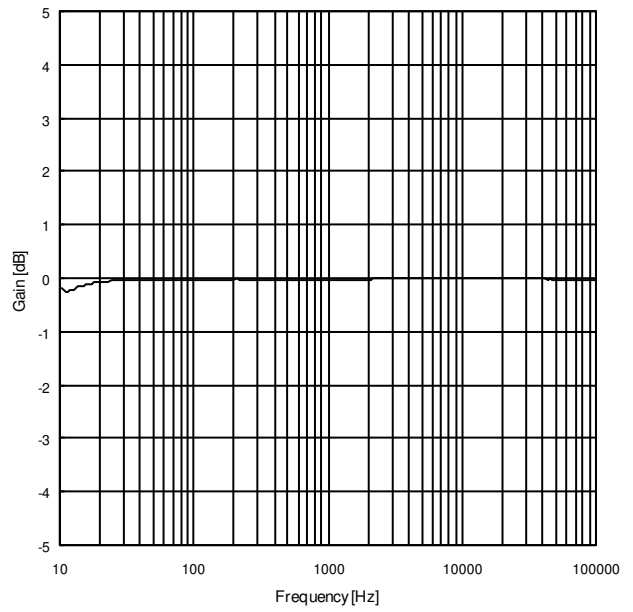


Figure 5. Gain vs. Frequency

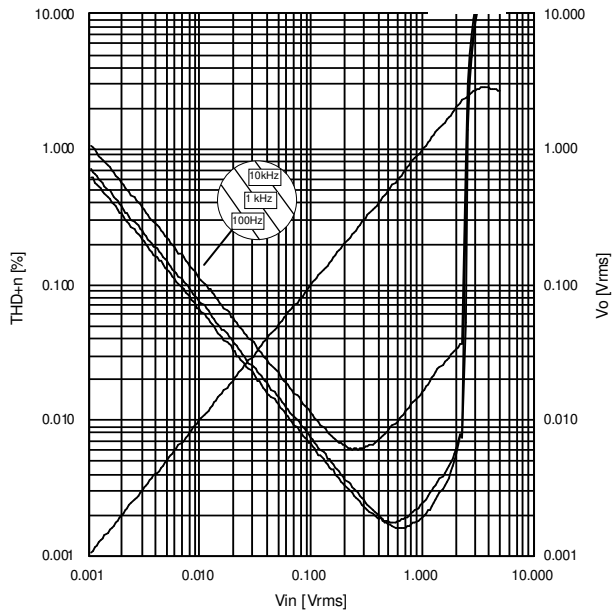


Figure 6. THD+N, Vo vs. Vin

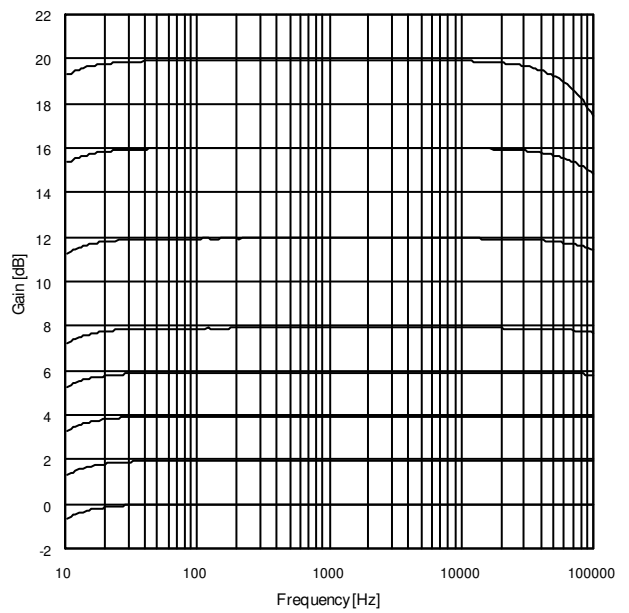


Figure 7. Input Gain vs. Frequency.

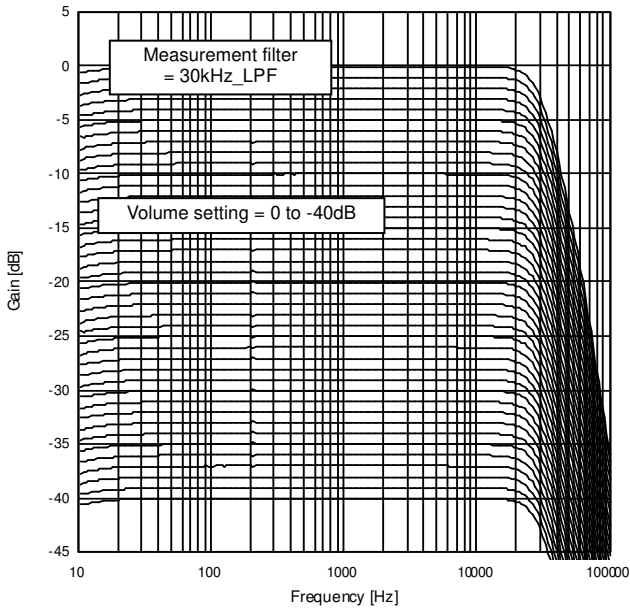


Figure 8. Volume Attenuation 1

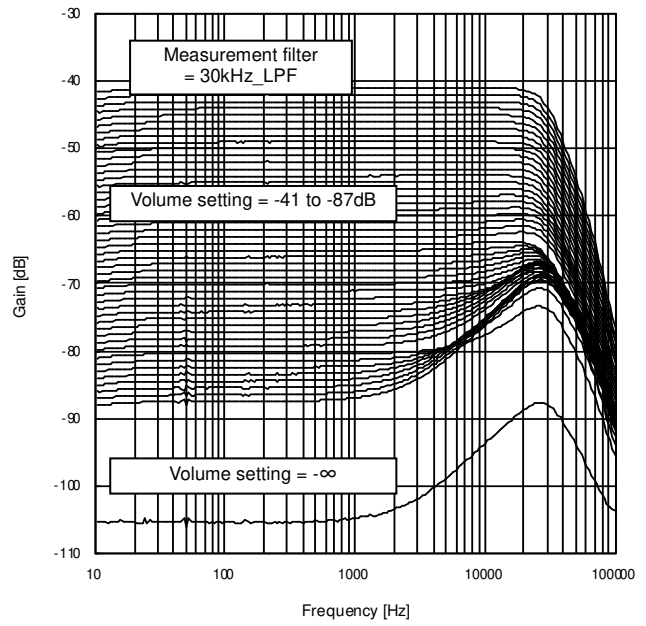


Figure 9. Volume Attenuation 2

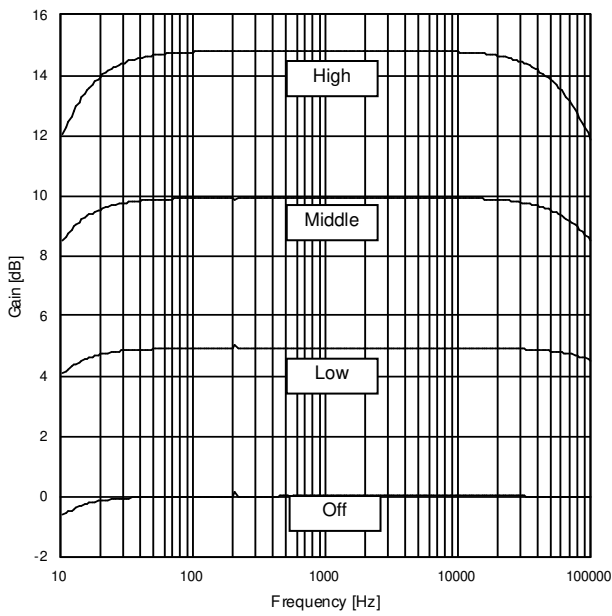


Figure 10. Output Gain vs. Frequency

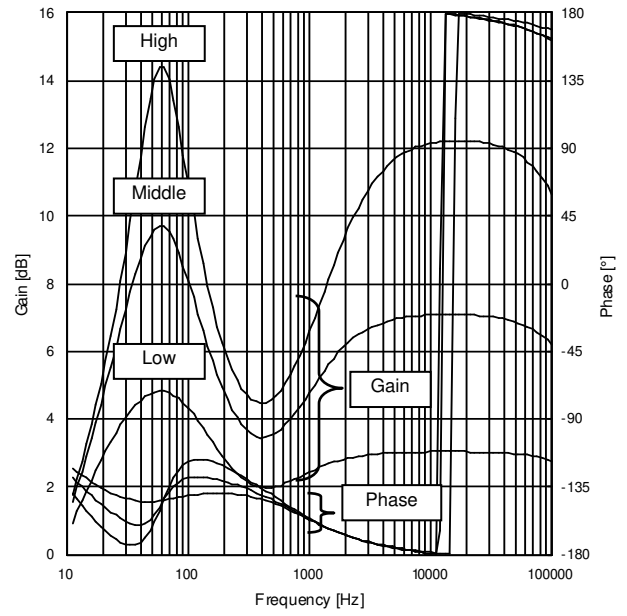


Figure 11. BassBoost & Surround

CONTROL SIGNAL SPECIFICATION

(1) Electrical specifications and timing for bus lines and I/O stages

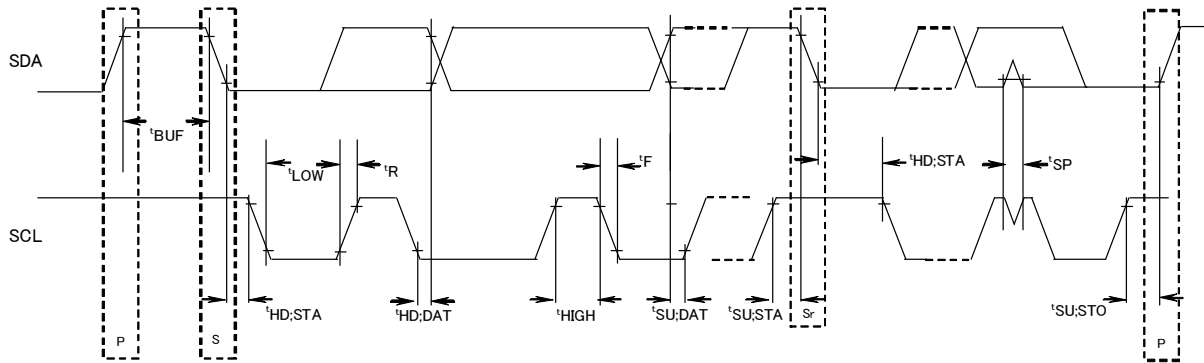


Figure 12. Definition of timing on the I<sup>2</sup>C-BUS

Table 1. Characteristics of the SDA and SCL bus lines for I<sup>2</sup>C-BUS devices

Parameter	Symbol	Fast-mode		Unit
		Min.	Max.	
1 SCL clock frequency	fSCL	0	400	kHz
2 Bus free time between a STOP and START condition	tBUF	1.3	—	μs
3 Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	0.6	—	μs
4 LOW period of the SCL clock	tLOW	1.3	—	μs
5 HIGH period of the SCL clock	tHIGH	0.6	—	μs
6 Set-up time for a repeated START condition	tSU;STA	0.6	—	μs
7 Data hold time	tHD;DAT	300*	—	ns
8 Data set-up time	tSU;DAT	300*	—	ns
9 Set-up time for STOP condition	tSU;STO	0.6	—	μs

All values referred to VIH min and VIL max levels (see Table 2).  
 \*About 7(t<sub>HD;DAT</sub>), 8(t<sub>SU;DAT</sub>), make it the setup which a margin is fully in .

Table 2. Characteristics of the SDA and SCL I/O stages for I<sup>2</sup>C-BUS devices

Parameter	Symbol	Fast-mode		Unit
		Min.	Max.	
10 LOW level input voltage:	VIL	-0.3	1	V
11 HIGH level input voltage:	VIH	2.3	5	V
12 Pulse width of spikes which must be suppressed by the input filter.	tSP	0	50	ns
13 LOW level output voltage (open drain or open collector): at 3mA sink current.	VOL1	0	0.4	V
14 Input current in each I/O pin with an input voltage between 0.4V and 4.5V.	Ii	-10	10	μA

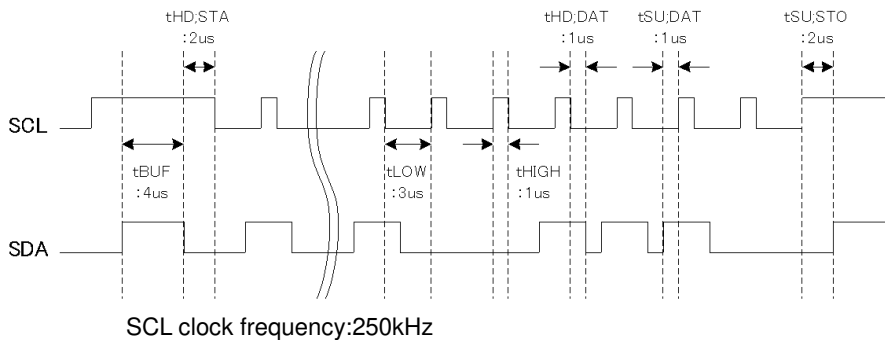


Figure 13. A command timing example in the I<sup>2</sup>C data transmission.



(2) I<sup>2</sup>C-BUS FORMAT

MSB	LSB	MSB	LSB	MSB	LSB		
S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit
	S	= Start conditions (Recognition of start bit)					
	Slave Address	= Recognition of slave address. 7 bits in upper order are voluntary. The least significant bit is "L" due to writing.					
	A	= ACKNOWLEDGE bit (Recognition of acknowledgement)					
	Select Address	= Select every of volume, bass and treble.					
	Data	= Data on every volume and tone.					
	P	= Stop condition (Recognition of stop bit)					

(3) I<sup>2</sup>C-BUS Interface Protocol

1) Basic form

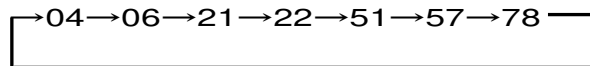
S	Slave Address	A	Select Address	A	Data	A	P
MSB	LSB	MSB	LSB	MSB	LSB		

2) Automatic increment (Assigned select Address is increased according to the number of data.)

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	...	DataN	A	P
MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	

- No.1. Data1 is set as data of address specified by Select Address.
- No.2. Data2 is set as data of next address from the address specified by No.1.
- No.3. DataN is set as data of address incremented N-1 times from the address specified by No.1.

Circulation of Select Address by the automatic increment function is shown below.



3) Configuration unavailable for transmission (In this case, only Select Address1 is set properly.)

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P
MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB

(Note) If any data is transmitted as Select Address 2 next to data, it is recognized as data, not as Select Address 2.

(4) Slave Address

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	0

82H

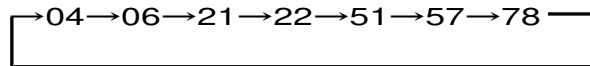
(5) Select Address & Data

Items	Select Address (hex)	Data							
		MSB						LSB	
		D7	D6	D5	D4	D3	D2	D1	D0
Input Selector	04	0	0	0	0	0	Input Selector		
Input Gain	06	0	0	0	Input Gain			0	
Volume Gain 1ch	21	1	Volume Attenuation 1ch						
Volume Gain 2ch	22	1	Volume Attenuation 2ch						
Bass Gain	51	Bass Boost/Cut	0	0	0	Bass Gain		0	
Treble Gain	57	Treble Boost/Cut	0	0	0	Treble Gain		0	
Surround	78	Surround Mode	0	0	0	Surround Gain			
Test Mode	F0	0	0	0	0	0	0	0	0
System Reset	FE	1	0	0	0	0	0	0	1

About the register that a function isn't assigned (above table, D0~D7 is "0" or "1"), set it up as the value of the above table.

Note:

Upon continuous data transfer, the Select Address is circulated by the automatic increment function, as shown below.



Select Address 04 (hex)

Mode	Input Selector							
	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
A	0	0	0	0	0	0	0	0
B						0	0	1
C						0	1	0
D						0	1	1
E						1	0	0
F						1	1	0
INPUT SHORT						1	0	1
INPUT MUTE						1	1	1

INPUT MUTE : Mute is done at the input signal in the part of Input Selector.

Select Address 06 (hex)


Gain	Input Gain							
	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	0	0	0	0	0	0	0	0
2dB				0	0	0	1	
4dB				0	0	1	0	
6dB				0	0	1	1	
8dB				0	1	0	0	
12dB				0	1	1	0	
16dB				1	0	0	0	
20dB				1	0	1	0	
Prohibition				0	1	0	1	
				0	1	1	1	
	1	0	0	1				
	1	0	1	1				
	1	1	0	0				
				1	1	1	0	
				1	1	1	1	

About Input Gain, the allotment of D4/D3/D2/D1 is discontinuous, please be careful.

 : Initial condition

Select Address 21, 22 (hex)

Attenuation	Volume Attenuation							
	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
0dB	1	0	0	0	0	0	0	0
-1dB		0	0	0	0	0	0	1
-2dB		0	0	0	0	0	0	1
-3dB		0	0	0	0	0	0	1
-4dB		0	0	0	0	0	1	0
-5dB		0	0	0	0	0	1	0
-6dB		0	0	0	0	0	1	1
-7dB		0	0	0	0	0	1	1
-8dB		0	0	0	0	1	0	0
-9dB		0	0	0	0	1	0	0
-10dB		0	0	0	0	1	0	1
-11dB		0	0	0	0	1	0	1
-12dB		0	0	0	0	1	1	0
-13dB		0	0	0	0	1	1	0
-14dB		0	0	0	0	1	1	1
-15dB		0	0	0	0	1	1	1
-16dB		0	0	1	0	0	0	0
-17dB		0	0	1	0	0	0	1
-18dB		0	0	1	0	0	1	0
-19dB		0	0	1	0	0	1	1
-20dB		0	0	1	0	1	0	0
-21dB		0	0	1	0	1	0	1
-22dB		0	0	1	0	1	1	0
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮
-83dB		1	0	1	0	0	1	1
-84dB		1	0	1	0	1	0	0
-85dB		1	0	1	0	1	0	1
-86dB		1	0	1	0	1	1	0
-87dB		1	0	1	0	1	1	1
Prohibition		1	0	1	1	0	0	0
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
-∞dB	1	1	1	1	1	1	0	
	1	1	1	1	1	1	1	

 : Initial condition

Select Address 51(hex)

Gain	Bass Gain							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Bass Boost /Cut	0	0	0	0	0	0	0
2dB					0	0	1	
4dB					0	1	0	
6dB					0	1	1	
8dB					1	0	0	
10dB					1	0	1	
12dB					1	1	0	
14dB					1	1	1	

Mode	Bass Boost/Cut							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Boost	0	0	0	0	Bass Gain			0
Cut	1							

Select Address 57(hex)

Gain	Treble Gain							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Treble Boost /Cut	0	0	0	0	0	0	0
2dB					0	0	1	
4dB					0	1	0	
6dB					0	1	1	
8dB					1	0	0	
10dB					1	0	1	
12dB					1	1	0	
14dB					1	1	1	

Mode	Treble Boost/Cut							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Boost	0	0	0	0	Treble Gain			0
Cut	1							

 : Initial condition

Select Address 78(hex)

Gain	Surround Gain							
	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF					0	0	0	0
Low					0	1	0	1
Middle					1	0	1	0
High					1	1	1	1
Prohibition	Surround Mode	0	0	0	0	0	0	1
					0	0	1	0
					0	0	1	1
					0	1	0	0
					0	1	1	0
					0	1	1	1
					1	0	0	0
					1	0	0	1
					1	0	1	1
					1	1	0	0
					1	1	0	1
					1	1	1	0

About Surround Gain, the allotment of D3/D2/D1/D0 is discontinuous, please be careful.

Mode	Surround Mode							
	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Mode OFF	0	0	0	0	Surround Gain			
Surround SW (A)=ON								
Mode ON	1							
Surround SW (B)=ON								

About Surround SW, please refer to Figure 22,25,28,30,32,36 (From P22 to P27).

 : Initial condition

(6) About initial condition at supply voltage on

At on of supply voltage circuit made initialization inside IC is built-in. Please send data to all address as initial data at supply voltage on. And please supply mute at set side until this initial data is sent.

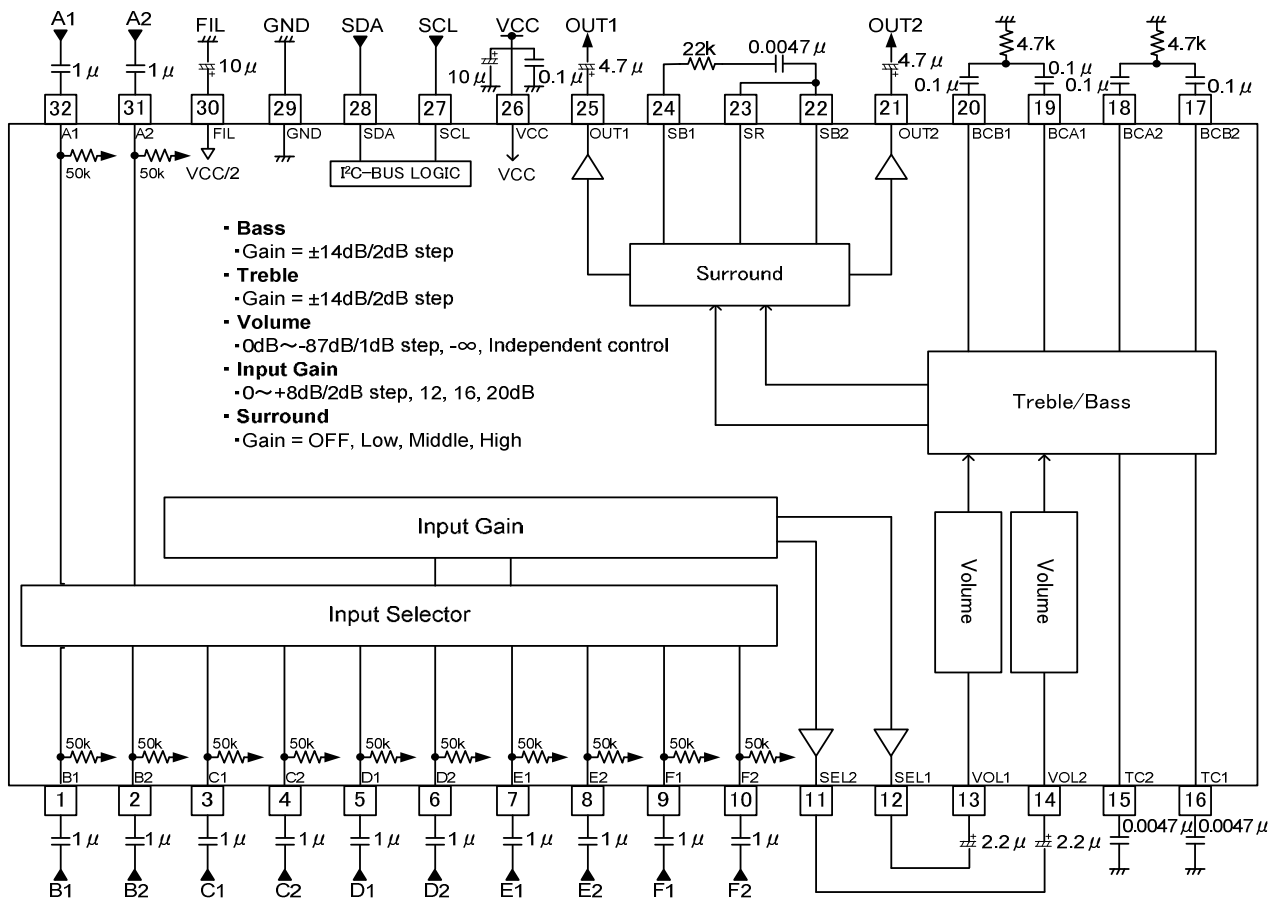
Item	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Rise time of VCC	Trise	20	—	—	usec	VCC rise time from 0V to 3V
VCC voltage of release power on reset	Vpor	—	3.0	—	V	

Volume Attenuation

ATT(dB)	D7	D6	D5	D4	D3	D2	D1	D0	ATT(dB)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	-46	1	0	1	0	1	1	1	0
-1	1	0	0	0	0	0	0	1	-47	1	0	1	0	1	1	1	1
-2	1	0	0	0	0	0	1	0	-48	1	0	1	1	0	0	0	0
-3	1	0	0	0	0	0	1	1	-49	1	0	1	1	0	0	0	1
-4	1	0	0	0	0	1	0	0	-50	1	0	1	1	0	0	1	0
-5	1	0	0	0	0	1	0	1	-51	1	0	1	1	0	0	1	1
-6	1	0	0	0	0	1	1	0	-52	1	0	1	1	0	1	0	0
-7	1	0	0	0	0	1	1	1	-53	1	0	1	1	0	1	0	1
-8	1	0	0	0	1	0	0	0	-54	1	0	1	1	0	1	1	0
-9	1	0	0	0	1	0	0	1	-55	1	0	1	1	0	1	1	1
-10	1	0	0	0	1	0	1	0	-56	1	0	1	1	1	0	0	0
-11	1	0	0	0	1	0	1	1	-57	1	0	1	1	1	0	0	1
-12	1	0	0	0	1	1	0	0	-58	1	0	1	1	1	0	1	0
-13	1	0	0	0	1	1	0	1	-59	1	0	1	1	1	0	1	1
-14	1	0	0	0	1	1	1	0	-60	1	0	1	1	1	1	0	0
-15	1	0	0	0	1	1	1	1	-61	1	0	1	1	1	1	0	1
-16	1	0	0	1	0	0	0	0	-62	1	0	1	1	1	1	1	0
-17	1	0	0	1	0	0	0	1	-63	1	0	1	1	1	1	1	1
-18	1	0	0	1	0	0	1	0	-64	1	1	0	0	0	0	0	0
-19	1	0	0	1	0	0	1	1	-65	1	1	0	0	0	0	0	1
-20	1	0	0	1	0	1	0	0	-66	1	1	0	0	0	0	1	0
-21	1	0	0	1	0	1	0	1	-67	1	1	0	0	0	0	1	1
-22	1	0	0	1	0	1	1	0	-68	1	1	0	0	0	1	0	0
-23	1	0	0	1	0	1	1	1	-69	1	1	0	0	0	1	0	1
-24	1	0	0	1	1	0	0	0	-70	1	1	0	0	0	1	1	0
-25	1	0	0	1	1	0	0	1	-71	1	1	0	0	0	1	1	1
-26	1	0	0	1	1	0	1	0	-72	1	1	0	0	1	0	0	0
-27	1	0	0	1	1	0	1	1	-73	1	1	0	0	1	0	0	1
-28	1	0	0	1	1	1	0	0	-74	1	1	0	0	1	0	1	0
-29	1	0	0	1	1	1	1	0	-75	1	1	0	0	1	0	1	1
-30	1	0	0	1	1	1	1	1	-76	1	1	0	0	1	1	0	0
-31	1	0	0	1	1	1	1	1	-77	1	1	0	0	1	1	0	1
-32	1	0	1	0	0	0	0	0	-78	1	1	0	0	1	1	1	0
-33	1	0	1	0	0	0	0	1	-79	1	1	0	0	1	1	1	1
-34	1	0	1	0	0	0	1	0	-80	1	1	0	1	0	0	0	0
-35	1	0	1	0	0	0	1	1	-81	1	1	0	1	0	0	0	1
-36	1	0	1	0	0	1	0	0	-82	1	1	0	1	0	0	1	0
-37	1	0	1	0	0	1	0	1	-83	1	1	0	1	0	0	1	1
-38	1	0	1	0	0	1	1	0	-84	1	1	0	1	0	1	0	0
-39	1	0	1	0	0	1	1	1	-85	1	1	0	1	0	1	0	1
-40	1	0	1	0	1	0	0	0	-86	1	1	0	1	0	1	1	0
-41	1	0	1	0	1	0	0	1	-87	1	1	0	1	0	1	1	1
-42	1	0	1	0	1	0	1	0		1	1	0	1	1	0	0	0
-43	1	0	1	0	1	0	1	1	Prohibition	·	·	·	·	·	·	·	·
-44	1	0	1	0	1	1	0	0		1	1	1	1	1	1	1	0
-45	1	0	1	0	1	1	0	1	-∞	1	1	1	1	1	1	1	1

 : Initial condition

Application Circuit Diagram



- **Bass**
  - Gain = ±14dB/2dB step
- **Treble**
  - Gain = ±14dB/2dB step
- **Volume**
  - 0dB ~ -87dB/1dB step, -∞, Independent control
- **Input Gain**
  - 0 ~ +8dB/2dB step, 12, 16, 20dB
- **Surround**
  - Gain = OFF, Low, Middle, High

Figure 14. Application Circuit Diagram

UNIT  
RESISTANCE: Ω  
CAPACITANCE: F

**Notes on Wiring**

- ① Decoupling capacitor of the power supply has to be connected in the shortest distance possible.
- ② GND lines has to follow star-point connection.
- ③ Wiring pattern of Digital signal should be away from that of analog unit. At the same time, crosstalk has to be minimized, if not eliminated.
- ④ If possible, SCL and SDA lines of I<sup>2</sup>C-BUS should not be parallel.  
If it cannot be avoided, the lines must, at least, be shielded.
- ⑤ Analog input lines should not be parallel, as well. If it cannot be avoided, the lines must, at least, be shielded.



### Thermal Derating Curve

The temperature, at which it is used, affects the electrical characteristics of an IC. Exceeding absolute maximum ratings may degrade and destroy elements. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.

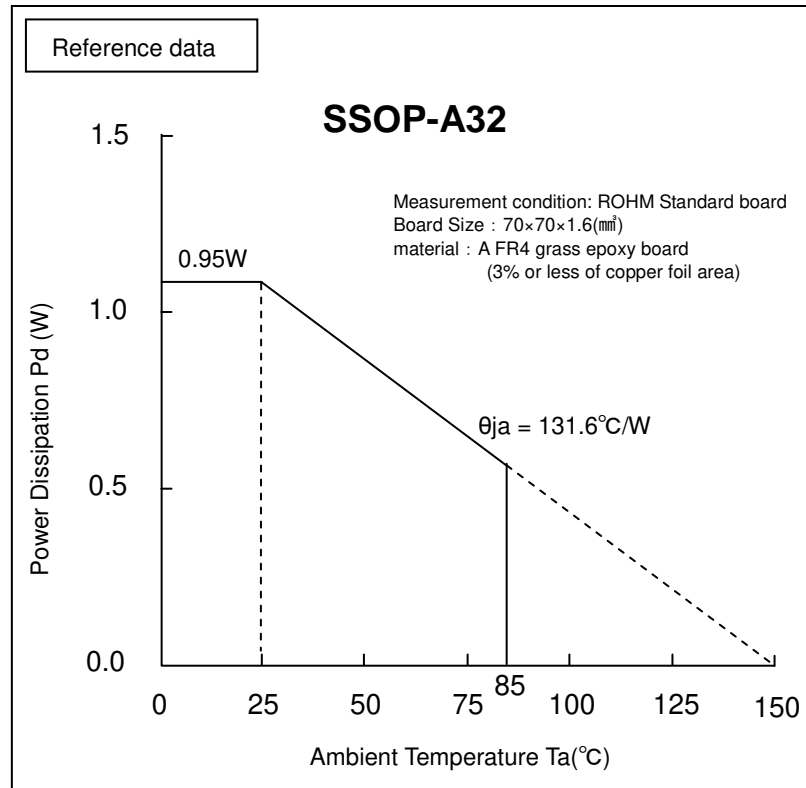


Figure 15. Temperature Derating Curve

Note: Values are actual measurements and are not guaranteed.

Power dissipation values vary according to the board on which the IC is mounted.

Pin Equivalent Circuit and Description

Pin No.	Pin Name	Pin Voltage	Equivalent Circuit	Pin Description
32 31 1 2 3 4 5 6 7 8 9 10	A1 A2 B1 B2 C1 C2 D1 D2 E1 E2 F1 F2	4.5V		Stereo signal input pin Input impedance = 50kΩ(typ)
11 12 21 25	SEL2 SEL1 OUT2 OUT1	4.5V		Output pin
13 14	VOL1 VOL2	4.5V		Volume input pin Input impedance = 50kΩ(typ)
15 16 17 20	TC2 TC1 BCB2 BCB1	4.5V		TC1,TC2 : Treble filter pin Refer to P21, Figure 20, Table 4 for the input impedance.  BCB1,BCB2 : Bass filter pin Refer to P20, Figure 18, Table 3 for the input impedance
18 19	BCA2 BCA1	4.5V		Bass filter pin
26	VCC	9.0V		Power supply pin.

The figure in the pin description, pin voltage and input/output equivalent circuit is reference value only. It does not guarantee the value.

Pin No.	Pin name	Pin voltage	Equivalent Circuit	Pin Description
22 24	SB2 SB1	4.5V		Bass boost pin. Refer to P22, Figure 22, Table 5 for the input impedance.
23	SR	4.5V		Surround pin Refer to P22, Figure 22, Table 5 for the input impedance.
27	SCL	—		Clock input pin of I <sup>2</sup> C-BUS communication.
28	SDA	—		Data input pin of I <sup>2</sup> C-BUS communication.
29	GND	0V		Analog ground pin.
30	FIL	4.5V		1/2 VCC pin. Reference voltage of analog signal system. The simple pre-charge circuit and simple discharge circuit for an external capacitor are built-in.

The figure in the pin description, pin voltage and input/output equivalent circuit is reference value only. It does not guarantee the value.

Cautions on use

1. Absolute Maximum Voltage Rating

When the voltage supplied to VCC is more than the absolute maximum voltage rating, circuit current increases rapidly. This will lead to characteristic deterioration and destruction of the device. Especially in a surge test of the set, when surge application is expected at VCC terminal (26pin), absolute maximum voltage rating must not be exceeded (including a operating voltage + serge ingredient (around 14V)).

2. Input Signal

a) About constant set up of input coupling capacitor

In the signal input terminal, the constant setting of input coupling capacitor C(F) be sufficient input impedance  $R_{IN}(\Omega)$  inside IC and please decide. The 1<sup>st</sup> order HPF characteristic of RC is composed.

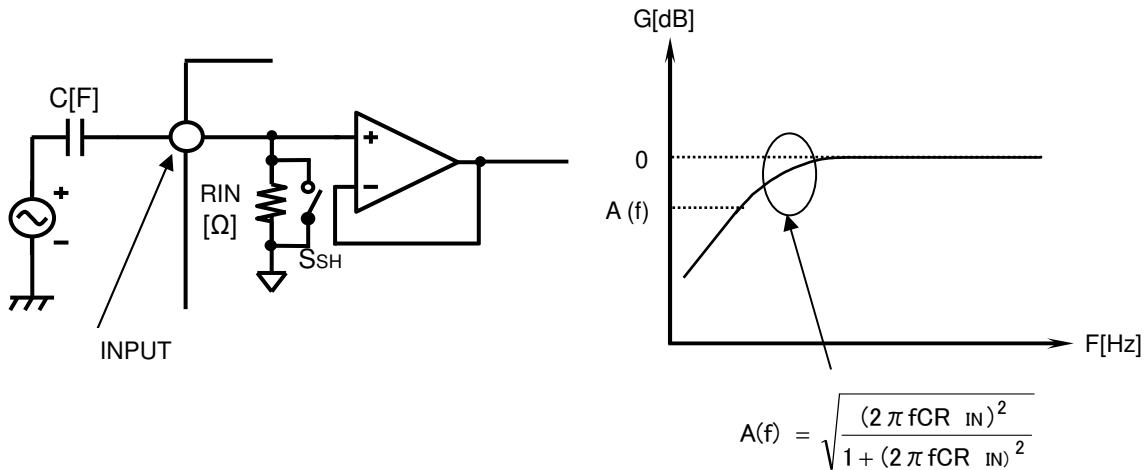


Figure 16. Input Short Circuit

b) Input Selector SHORT

SHORT mode is the command which makes input impedance of all terminals in input selector small by setting switch  $S_{SH}$  is ON. Switch  $S_{SH}$  is OFF, when SHORT command is disabled.

The charge time of an external coupling capacitor becomes short during the command. It is recommended to use SHORT mode when there is no signal.

3. Output Load Characteristics

The usages of load for output are below (reference). Please use the load more than 10kΩ (TYP)

Pin No.	Pin Name	Pin No.	Pin Name
11	SEL2	21	OUT2
12	SEL1	25	OUT1

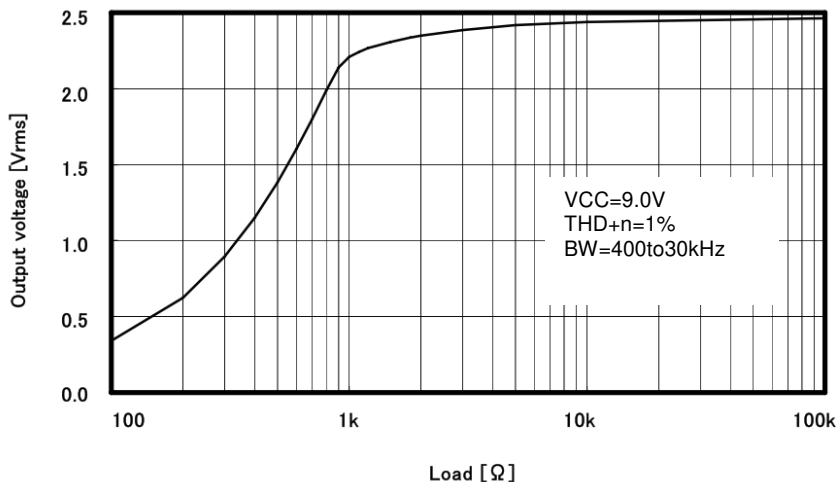


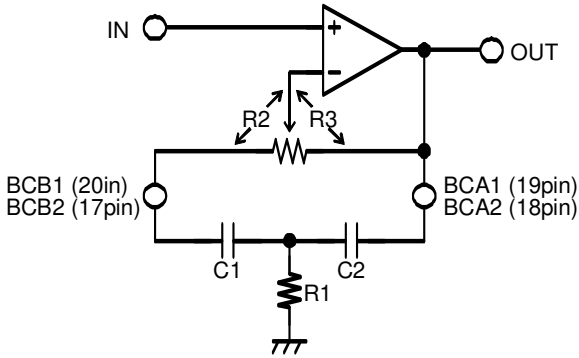
Figure 17. Output Load Characteristic (Reference Vcc=9.0V)

4. Sound Input Terminal

If this terminal is open, the input resistance is 50kΩ which may induce pop noise from the outside. If a sound input terminal is not used, it has to be connected to GND using a capacitor or set up the input selector using a microcomputer so that the unused input terminal will not be selected.

5. Bass Filter Constant Set Up

**Bass Boost**



**Bass Cut**

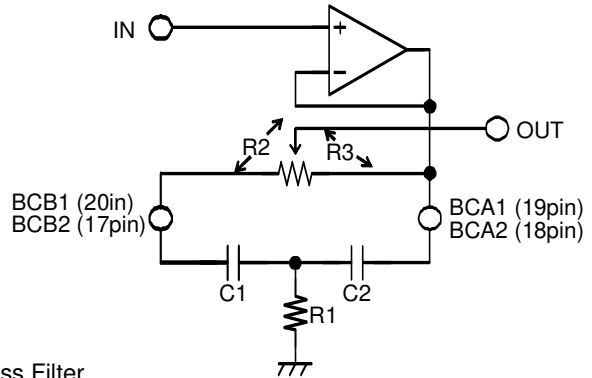


Figure 18. Bass Filter

$$f_o = \frac{1}{2\pi\sqrt{R1(R2+R3) \cdot C1 \cdot C2}} \text{ [Hz]}$$

$$Q = \frac{\sqrt{R1(R2+R3) \cdot C1 \cdot C2}}{R1(C1+C2) + R2C1}$$

$$\text{BOOST GAIN} = 20\log \frac{\frac{R2+R3}{R1} + \frac{C2}{C1} + 1}{\frac{R2}{R1} + \frac{C2}{C1} + 1} \text{ [dB]}$$

$$\text{CUT GAIN} = 20\log \frac{\frac{R2}{R1} + \frac{C2}{C1} + 1}{\frac{R2+R3}{R1} + \frac{C2}{C1} + 1} \text{ [dB]}$$

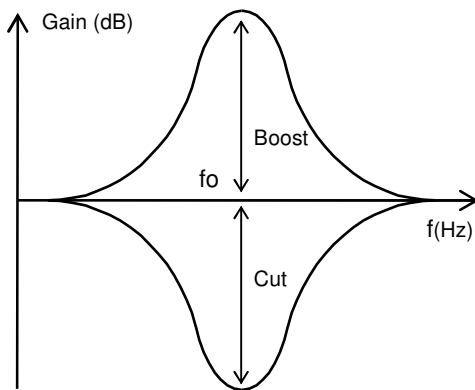


Figure 19. Bass Frequency Characteristics

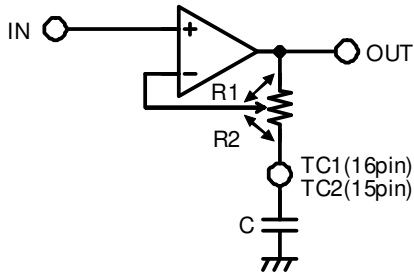
Table 3. Standard value of R2 and R3

Bass Boost/Cut Gain	Resistance(kΩ) ※TYP.	
	R2	R3
±0dB	53.5	0
±2dB	40.9	12.6
±4dB	30.5	23.0
±6dB	22.3	31.2
±8dB	15.8	37.7
±10dB	10.6	42.9
±12dB	6.5	47.0
±14dB	3.2	50.3

Actual boost/cut value may vary slightly .

6. Treble Filter Constant Set Up

**Treble Boost**



**Treble Cut**

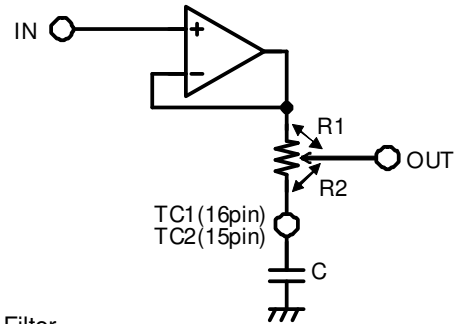


Figure 20. Treble Filter

$$f_c = \frac{1}{2\pi R2 \cdot C} \text{ [Hz]}$$

$$\text{BOOST GAIN} = 20 \log \frac{R1 + R2 + ZC}{R2 + ZC} \text{ [dB]}$$

$$\text{CUT GAIN} = 20 \log \frac{R2 + ZC}{R1 + R2 + ZC} \text{ [dB]}$$

$$ZC = \frac{1}{j\omega C} \text{ [\Omega]}$$

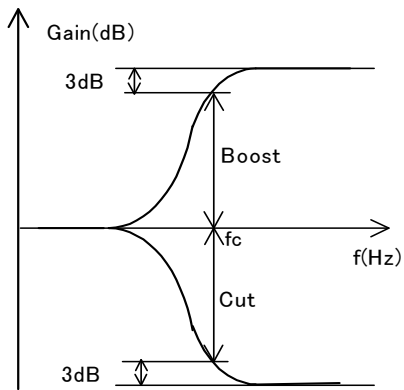


Figure 21. Treble Frequency Characteristics

Table 4. Standard value of R1 and R2(reference)

Treble Boost/Cut Gain	Resistance(kΩ) ※TYP.	
	R1	R2
±0dB	0	29.1
±2dB	6.1	23.0
±4dB	10.9	18.2
±6dB	14.8	14.3
±8dB	17.9	11.2
±10dB	20.5	8.6
±12dB	22.6	6.5
±14dB	24.4	4.7

Actual boost/cut value may vary slightly

7. BassBoost Application

7-1. BassBoost Application Circuit

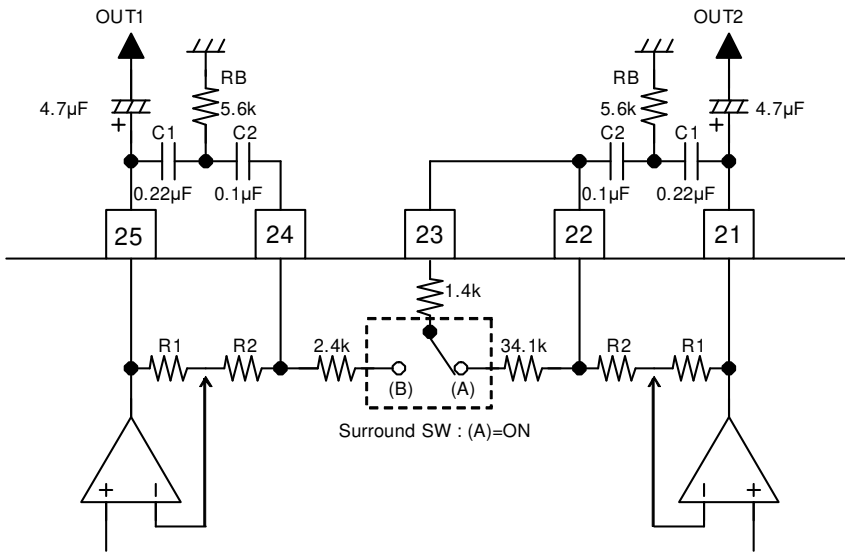


Table 5. Standard value of R1 and R2

Surround Gain	R1[kΩ]	R2[kΩ]
OFF	0	84.5
Low	44.8	39.7
Middle	70.0	14.5
High	84.2	0.3

Figure 22. Example of a BassBoost Application Circuit

7-2. The computation formula and the BassBoost Gain Characteristic Curve (fo=50Hz, Q=1.8(Surround Gain=High))

$$\text{Gain} = 20 \log \frac{\frac{R1 + R2}{RB} + \frac{C1}{C2} + 1}{\frac{R2}{RB} + \frac{C1}{C2} + 1} \text{ [dB]}$$

$$f_o = \frac{1}{2\pi \sqrt{RB(R1 + R2) \cdot C1 \cdot C2}} \text{ [Hz]}$$

$$Q = \frac{\sqrt{RB(R1 + R2) \cdot C1 \cdot C2}}{RB(C1 + C2) + R2 \cdot C2}$$

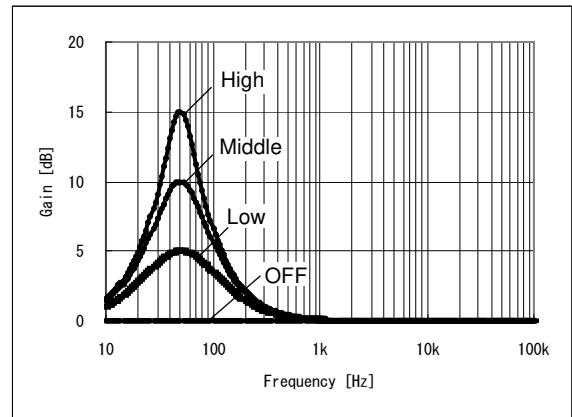


Figure 23. BassBoost Gain Characteristic Curve

7-3. The Characteristic Curve in fixed number change

Table 6. The fixed number example (\*1)

No.	The specification	C1 [μF]	C2 [μF]	RB [kΩ]
①	fo=60Hz, Q=1.8, Gain=16.8dB	0.15	0.1	5.6
②	fo=72Hz, Q=1.7, Gain=15.0dB	0.15	0.068	5.6
③	fo=79Hz, Q=1.9, Gain=16.2dB	0.15	0.068	4.7
④	fo=89Hz, Q=1.8, Gain=16.9dB	0.1	0.068	5.6

(\*1): Surround Gain=High

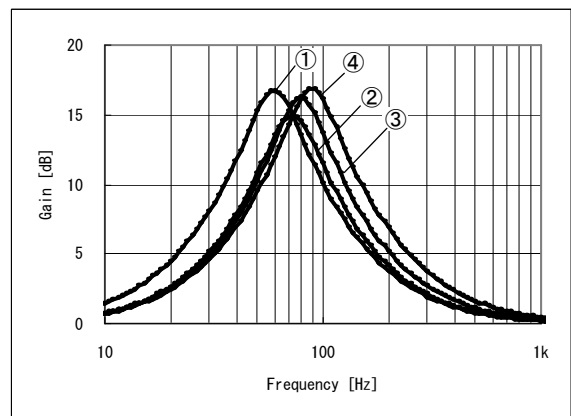


Figure 24. BassBoost Gain Characteristic Curve in fixed number change

8. BassBoost & Surround Application

8-1. BassBoost & Surround Application Circuit

In this application circuit example, it isn't possible to do the use only of Surround. Also, Surround Gain depends on the setting value of BassBoost Gain.

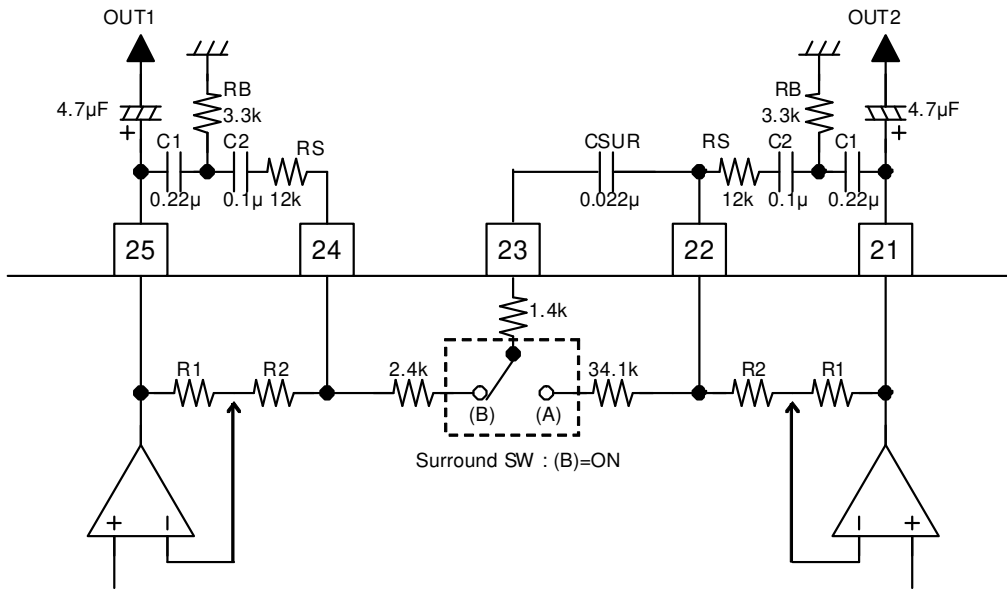


Figure 25. Example of BassBoost & Surround Application Circuit

8-2. BassBoost & Surround Characteristic Curve and the computation formula of BassBoost Gain(Surround SW : (A)=ON)

$$\text{Gain} = 20 \log \frac{R1 + R2 + RS + \frac{C1}{C2} + 1}{\frac{RB}{R2 + RS} + \frac{C1}{C2} + 1} \text{ [dB]}$$

$$f_o = \frac{1}{2 \pi \sqrt{RB(R1 + R2 + RS) \cdot C1 \cdot C2}} \text{ [Hz]}$$

$$Q = \frac{\sqrt{RB(R1 + R2 + RS) \cdot C1 \cdot C2}}{RB(C1 + C2) + C2(R2 + RS)}$$

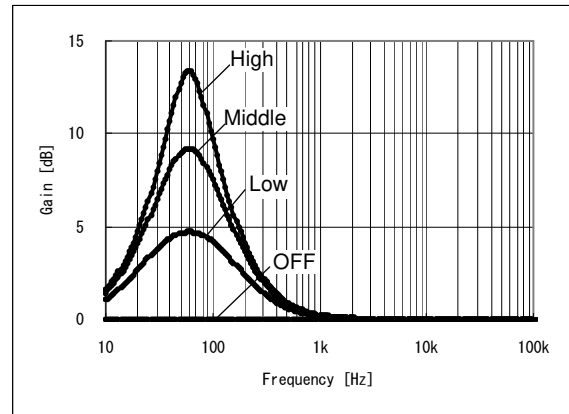


Figure 26. BassBoost & Surround Characteristic Curve(Surround SW : (A)=ON)

8-3. BassBoost & Surround Characteristic Curve(Surround SW : (B)=ON)

In this application circuit example, it isn't possible to do the use only of Surround. Also, Surround Gain depends on the setting value of BassBoost Gain.

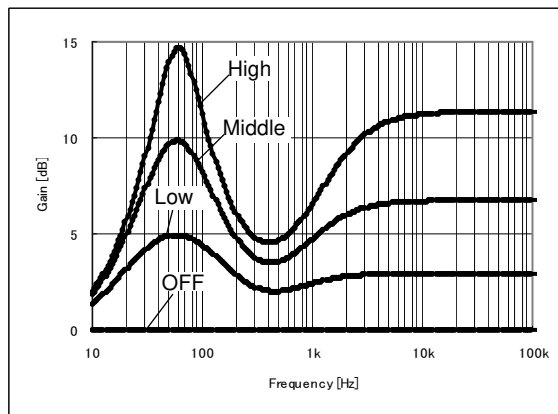


Figure 27. BassBoost & Surround Characteristic Curve(Surround SW : (B)=ON)



9. Easy Surround Application

9. Easy Surround Application Circuit

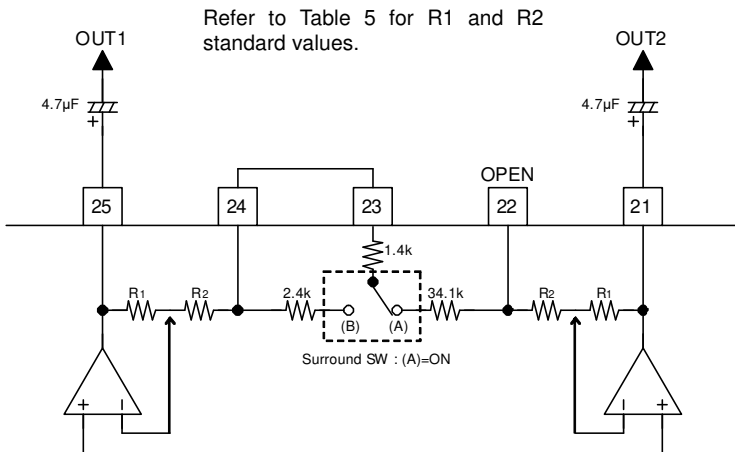


Figure 28. Example of Easy Surround Application Circuit

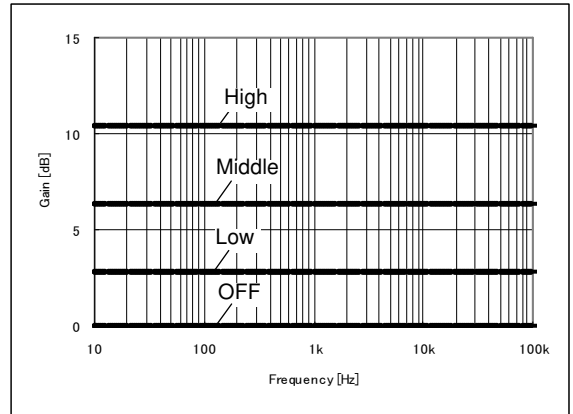
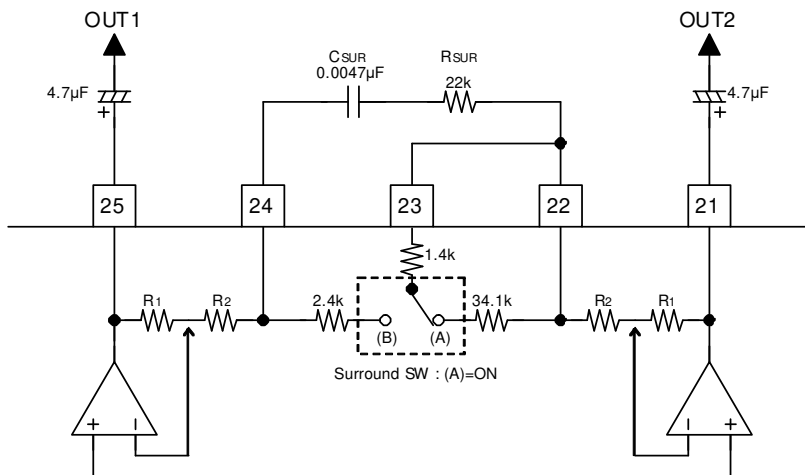


Figure 29. Easy Surround Characteristic Curve

10. Surround Application

10-1. Surround Application Circuit



Refer to Table 5 for R1 and R2 standard values.

Figure 30. Example of Surround Application Circuit

10-2. Surround Characteristic Curve

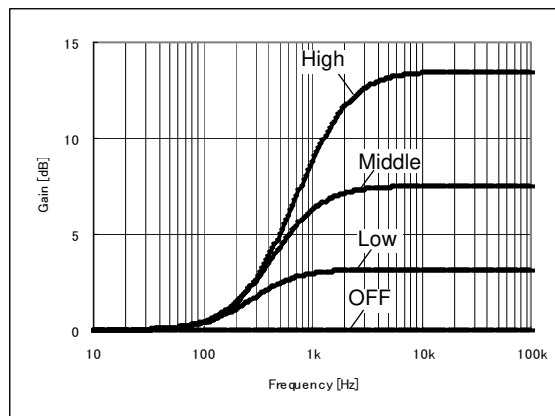


Figure 31. Surround Characteristic Curve

11. Output Gain Application

11-1. Output Gain Application Circuit

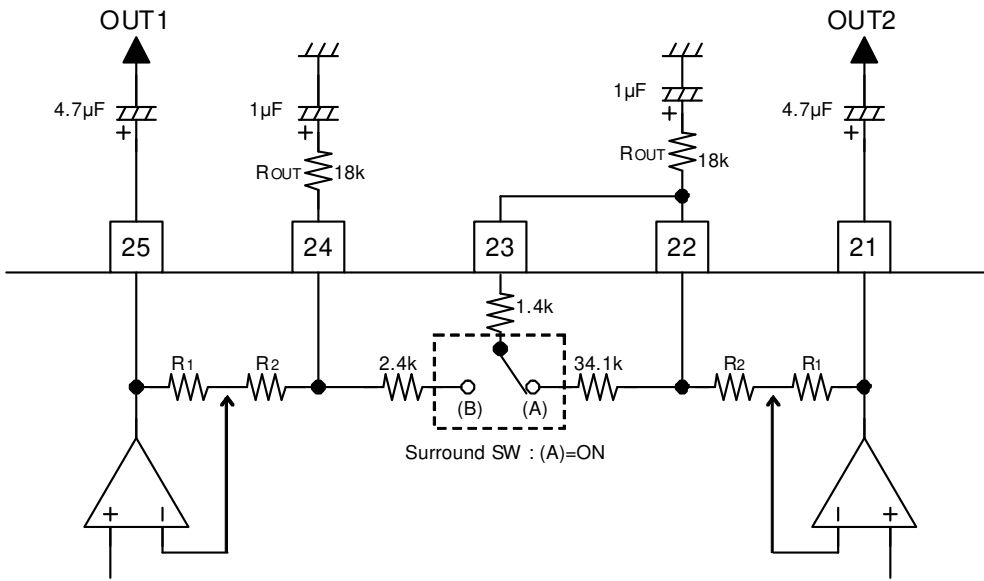


Figure 32. Example of Output Gain Application Circuit

11-2. The computation formula and the Output Gain Characteristic Curve

$$\text{Gain} = 20 \log \frac{R1 + R2 + R_{OUT}}{R2 + R_{OUT}} \text{ [dB]}$$

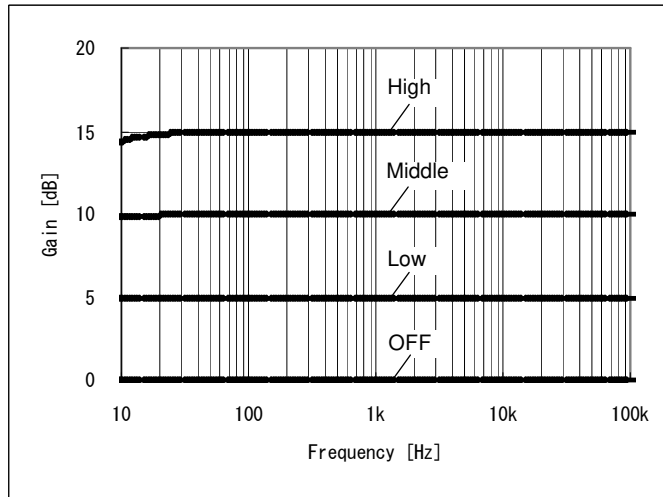


Figure 33. Output Gain Characteristic Curve