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Datasheet

Analog Sound Processors series

Sound Processor for car audio built-in High-Voltage function and 2nd order post filter

BD37068FV-M

General Description

It is built-in input selector of 6 stereo source and output to ADC after adjusting signal level. And built-in 2nd order post filter to reduce out of band noise and 6ch Volume circuit. It is possible to out until 5.2V_{RMS} at maximum output. (High Voltage function) Moreover, it is simple to design set by built-in TDMA noise reduction systems.

Features

- AEC-Q100 (Grade3) Qualified
- Built-in differential input selector that can select single-ended / differential input
- Reduce the pop noise when switching gain due to built-in advanced switch circuit
- Less out-of-band noise of DAC by built-in 2nd order post filter.
- Built-in buffered ground isolation amplifier to realize high CMRR characteristics
- Built-in TDMA noise reduction circuit reduces the additional components for external filter.
- It is possible to output 5.2V_{RMS} by High-Voltage function
- Package is SSOP-B40. Putting same direction input-terminals and output-terminals make PCB layout easier and PCB area smaller.
- Available to control by 3.3V/5V for I2C-bus controller

Applications

It is the optimal for the car audio. Besides, it is possible to use for the audio equipment of mini Compo, micro Compo.

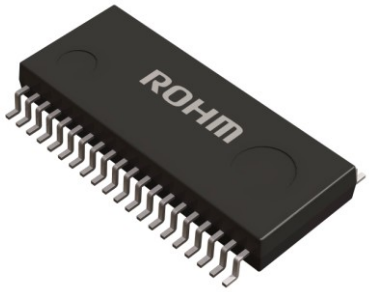
Key Specifications(Note1)

Total Harmonic Distortion :	0.003%(Typ)
Maximum Input Voltage :	2.2V_{RMS}(Typ)
Common Mode Rejection Ratio :	55dB(Min)
Maximum Output Voltage :	5.2V_{RMS}(Typ)
Output Noise Voltage :	23μV_{RMS}(Typ)
Residual Output Noise Voltage :	10.5μV_{RMS}(Typ)
Ripple Rejection:	-70dB (Typ)
Operating Temperature Range:	-40˚C to +85˚C

(Note1) These specifications are condition of High-Voltage ON.

Package

Package	W(Typ) x D(Typ) x H(Max)
SSOP-B40	13.60mm x 7.80mm x 2.00mm



SSOP-B40

Typical Application Circuit

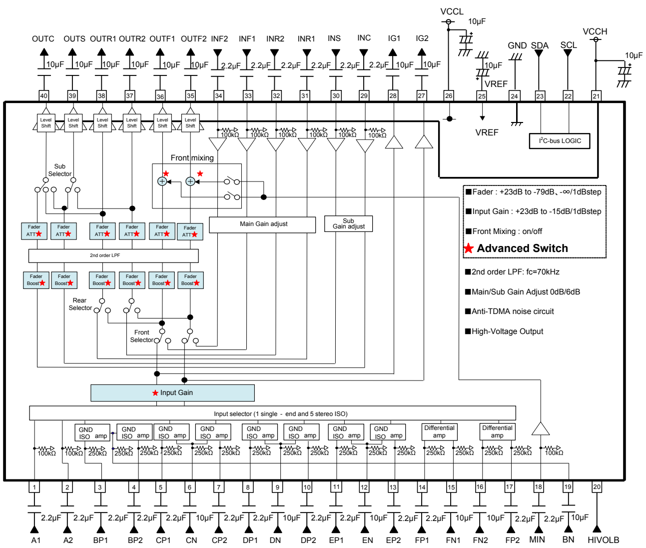


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

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Contents

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Pin Configuration

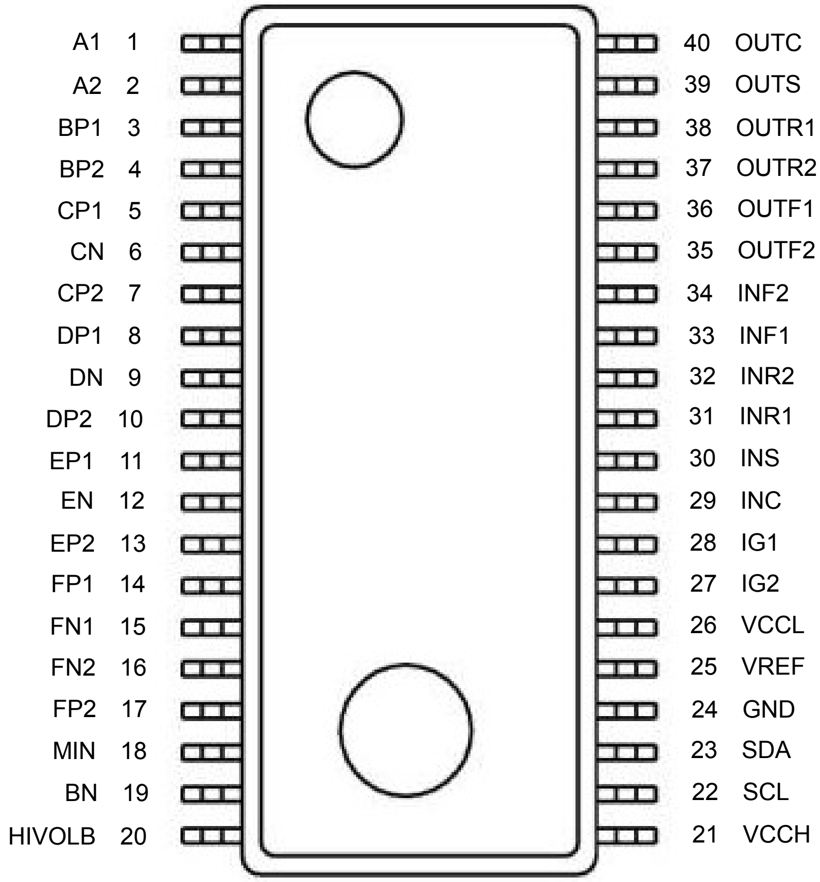

Figure 2. Pin configuration

Pin Descriptions

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	A1	A input terminal of 1ch	21	VCCH	VCCH terminal for power supply
2	A2	A input terminal of 2ch	22	SCL	I^2C Communication clock terminal
3	BP1	B positive input terminal of 1ch	23	SDA	I^2C Communication data terminal
4	BP2	B positive input terminal of 2ch	24	GND	GND terminal
5	CP1	C positive input terminal of 1ch	25	VREF	BIAS terminal
6	CN	C negative input terminal	26	VCCL	VCCL terminal for power supply
7	CP2	C positive input terminal of 2ch	27	IG2	Input Gain output terminal of 2ch
8	DP1	D positive input terminal of 1ch	28	IG1	Input Gain output terminal of 1ch
9	DN	D negative input terminal	29	INC	Center input terminal
10	DP2	D positive input terminal of 2ch	30	INS	Subwoofer input terminal
11	EP1	E positive input terminal of 1ch	31	INR1	Rear input terminal of 1ch
12	EN	E negative input terminal	32	INR2	Rear input terminal of 2ch
13	EP2	E positive input terminal of 2ch	33	INF1	Front input terminal of 1ch
14	FP1	F positive input terminal of 1ch	34	INF2	Front input terminal of 2ch
15	FN1	F negative input terminal of 1ch	35	OUTF2	Front output terminal of 2ch
16	FN2	F negative input terminal of 2ch	36	OUTF1	Front output terminal of 1ch
17	FP2	F positive input terminal of 2ch	37	OUTR2	Rear output terminal of 2ch
18	MIN	Mixing input terminal	38	OUTR1	Rear output terminal of 1ch
19	BN	B negative input terminal	39	OUTS	Subwoofer output terminal
20	HIVOLB	Output Gain control terminal	40	OUTC	Center output terminal

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Block Diagram

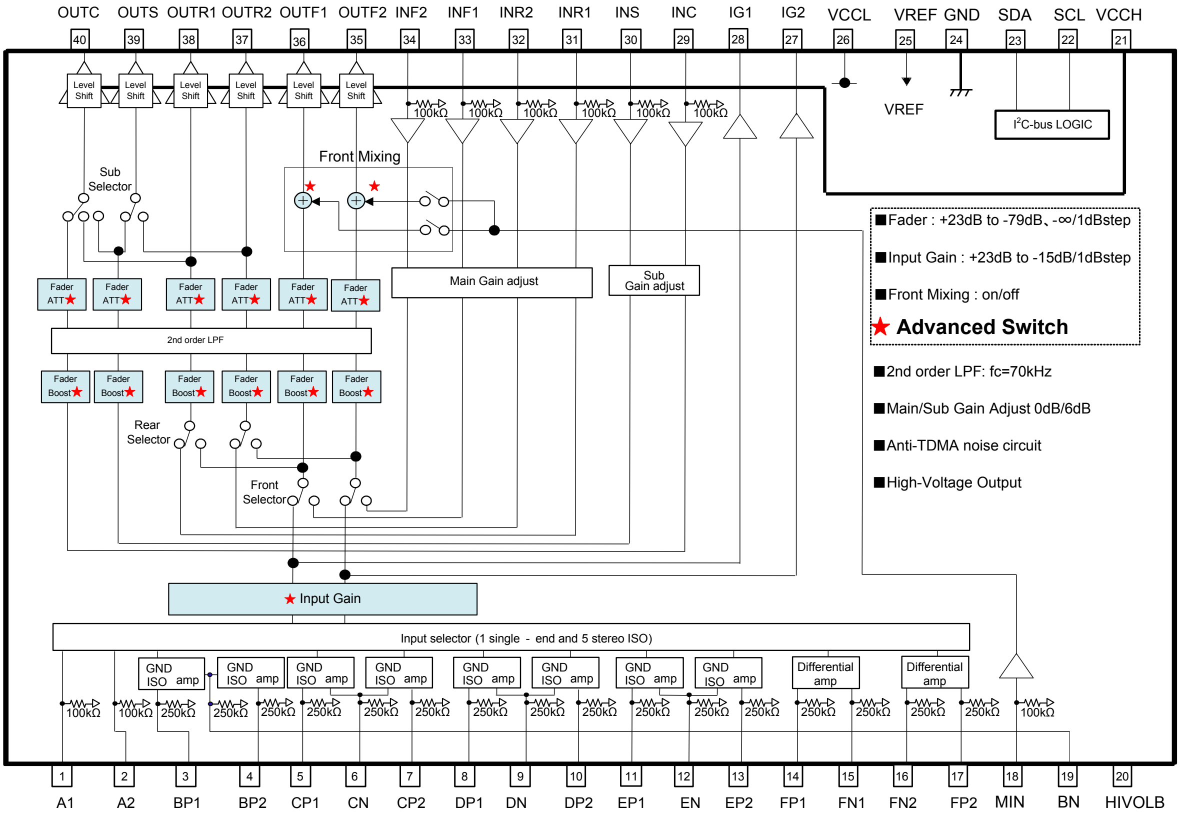

Figure 3. Block diagram and pin assign

Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VCCL	10	V
	VCCH	18	V
Input Voltage	V_{IN}	VCCL+0.3 to GND-0.3 Only SCL, SDA 7 to GND-0.3	V
Power Dissipation	Pd	1.12(Note1)	W
Storage Temperature	T_{STG}	-55 to +150	˚C

(Note1) This value decreases 9mW/˚C for Ta=25˚C or more.
ROHM standard board shall be mounted. Thermal resistance θja = 111.1(˚C /W).
ROHM Standard board size : 70x70x1.6(㎣)
material : A FR4 grass epoxy board(3% or less of copper foil area)

Operating Range

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VCCL	7.0	8.5	9.5	V
	VCCH	VCCL	17	17.8	V
Temperature	Topr	-40	-	+85	˚C

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Electrical Characteristic

(Unless specified particularly, Ta=25°C, VCCL=8.5V, VCCH=17.0V, f=1kHz, V_{IN}=1V_{RMS}, R_G=600Ω, R_L=10kΩ, A input, Input Gain 0dB, Gain Adjust +6dB, High-Voltage ON, LPF ON, Fader 0dB, Input point=A1/A2, Monitor point=IG1/IG2)

Block	Parameter	Symbol	Limit Min	Limit Typ	Limit Max	Unit	Conditions
General	Current upon no signal (VCCL)	I_{Q_VCCL}	—	30	43	mA	No signal
	Current upon no signal (VCCH)	I_{Q_VCCH}	-	7	10	mA	No signal
Input Selector	Input Impedance (A)	R_{IN_S}	70	100	130	kΩ	
	Input Impedance (B, C, D, E, F)	R_{IN_D}	175	250	325	kΩ	
	Voltage Gain	G_V	-1.5	+0	+1.5	dB	G_V=20log(V_{OUT}/V_{IN})
	Channel Balance	CB	-1.5	+0	+1.5	dB	CB = G_{V1}-G_{V2}
	Total Harmonic Distortion	THD+N	—	0.003	0.05	%	V_{OUT}=1V_{RMS} BW=400-30kHz
	Output Noise Voltage(Note1)	V_{NO1}	—	3.1	8.0	μV_{RMS}	R_G = 0Ω BW = IHF-A
	Maximum Input Voltage	V_{IM}	2.0	2.2	—	V_{RMS}	V_{IM} at THD+N(V_{OUT})=1% BW=400-30kHz
	Crosstalk Between Channels(Note1)	CTC	—	-100	-90	dB	R_G = 0Ω CTC=20log(V_{OUT}/V_{OUT}´) BW = IHF-A
	Crosstalk Between Selectors(Note1)	CTS	—	-100	-90	dB	R_G = 0Ω CTS=20log(V_{OUT}/V_{OUT}´) BW = IHF-A
	Common Mode Rejection Ratio (B, C, D, E, F) (Note1)	CMRR	55	65	—	dB	XP1 and XN input XP2 and XN input CMRR=20log(V_{IN}/V_{OUT}) BW = IHF-A, [X=B,C,D,E,F]
Input Gain	Minimum Input Gain	$G_{IN\ MIN}$	-17	-15	-13	dB	Input gain -15dB G_{IN}=20log(V_{OUT}/V_{IN})
	Maximum Input Gain	$G_{IN\ MAX}$	21	23	25	dB	Input gain 23dB V_{IN}=100mV_{RMS} G_{IN}=20log(V_{OUT}/V_{IN})
	Gain Set Error	$G_{IN\ ERR}$	-2	+0	+2	dB	GAIN=-15 to +23dB
	Output Impedance	R_{OUT}	-	—	50	Ω	V_{IN}=100mV_{RMS}
	Maximum Output Voltage	V_{OM}	2.0	2.2	—	V_{RMS}	THD+N=1% BW=400-30kHz

(Note1) VP-9690A (Average value detection, effective value display) filter by Panasonic is used for measurement. Input and output are in-phase.

(Unless specified particularly, Ta=25°C, VCCL=8.5V, VCCH=17.0V, f=1kHz, V_{IN}=0.9V_{RMS}, R_G=600Ω, R_L=10kΩ, A input, Input Gain 0dB, Gain Adjust +6dB, High-Voltage ON, LPF ON, Fader 0dB, Input point=INF1/INF2/INR1/INR2/INC/INS, Monitor point=OUTF1/OUTF2/OUTR1/OUTR2/OUTC/OUTS)

Block	Parameter	Symbol	Limit Min	Limit Typ	Limit Max	Unit	Conditions
Output	Output Impedance	R_{OUT}	-	—	50	Ω	V_{IN}=100mV_{RMS}
	Maximum Output Voltage	V_{OM}	5.1	5.2	—	V_{RMS}	V_{IN}=1V_{RMS} THD+N=1% BW=400-30kHz
	Maximum Output Gain	G_{Hout}	6.3	8.3	10.3	dB	G_{Hout}=20log(V_{OUT}/V_{IN})

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(Unless specified particularly, Ta=25˚C, VCCL=8.5V, VCCH=17.0V, f=1kHz, V_{IN}=0.9V_{RMS}, R_G=600Ω, R_L=10kΩ, A input, Input Gain 0dB, Gain Adjust +6dB, High-Voltage ON, LPF ON, Fader 0dB, Input point=INF1/INF2/INR1/INR2/INC/INS, Monitor point=OUTF1/OUTF2/OUTR1/OUTR2/OUTC/OUTS)

Block	Parameter	Symbol	Limit Min	Typ	Max	Unit	Conditions
Fader	Maximum Boost Gain	$G_{F\ BST}$	21	23	25	dB	Gain=23dB V_{IN}=100mV_{RMS} G_F=20log(V_{OUT}/V_{IN})-G_{Hout} Gain Adjust=0dB
	Channel Balance	CB	-1.5	+0	+1.5	dB	CB = G_{V1}-G_{V2}
	Total Harmonic Distortion	THD+N	—	0.003	0.05	%	BW=400-30kHz
	Output Noise Voltage(Note1)	V_{NO1}	—	23	40	μV_{RMS}	R_G = 0Ω BW = IHF-A
	Residual Output Noise Voltage(Note1)	V_{NOR}	—	10.5	20	μV_{RMS}	Fader = -∞dB R_G = 0Ω BW = IHF-A
	Maximum Input Voltage	V_{IM}	2.0	2.1	—	V_{RMS}	V_{IM} at THD+N(V_{OUT})=1% BW=400-30kHz Gain Adjust = 0dB
	Crosstalk Between Channels(Note1)	CTC	—	-100	-90	dB	R_G = 0Ω CTC=20log(V_{OUT}/V_{OUT}´) BW = IHF-A
	Maximum Attenuation(Note1)	$G_{F\ MIN}$	—	-100	-90	dB	Fader = -∞dB G_F=20log(V_{OUT}/V_{IN}) BW = IHF-A
	Gain Set Error	$G_{F\ ERR}$	-2	+0	+2	dB	Gain=+1 to +23dB
	Attenuation Set Error 1	$G_{F\ ERR1}$	-2	+0	+2	dB	Attenuation=0 to -15dB
	Attenuation Set Error 2	$G_{F\ ERR2}$	-3	+0	+3	dB	Attenuation=-16 to -47dB
	Attenuation Set Error 3	$G_{F\ ERR3}$	-4	+0	+4	dB	Attenuation=-48 to -79dB
	Ripple Rejection	$PSRR_{VCCL}$	—	-70	-40	dB	f=1kHz V_{PSRL}=100mV_{RMS} $PSRR_{VCCL}$=20log(V_{OUT} /VCCL)
		$PSRR_{VCCH}$	—	-70	-40	dB	f=1kHz V_{PSRH}=100mV_{RMS} $PSRR_{VCCH}$=20log(V_{OUT}/VCCH)
Mixing	Input Impedance	R_{IN_M}	70	100	130	kΩ	
	Maximum Input voltage	V_{IM_M}	2.0	2.2	-	V_{RMS}	V_{IM} at THD+N(V_{OUT})=1% BW=400-30kHz MIN input
	Maximum Attenuation(Note1)	$G_{MX\ MIN}$	-	-100	-85	dB	Front Mixing OFF G_{MX}=20log(V_{OUT}/V_{IN}) BW=IHF-A MIN input
	Mixing Gain	G_{MX}	-2	+0	+2	dB	Front Mixing ON G_{MX}=20log(V_{OUT}/V_{IN})-G_{Hout}
Gain Adjust	Input Impedance	R_{IN_M}	70	100	130	kΩ	
	Boost Gain	$G_{F\ BST}$	4	6	8	dB	Gain=6dB V_{IN}=100mV_{RMS} G_F=20log(V_{OUT}/V_{IN})-G_{Hout}
	Channel Balance	CB	-1.5	+0	+1.5	dB	CB = G_{V1}-G_{V2}

(Note1) VP-9690A (Average value detection, effective value display) filter by Panasonic is used for measurement. Input and output are in-phase.

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Typical Performance Curve(s)

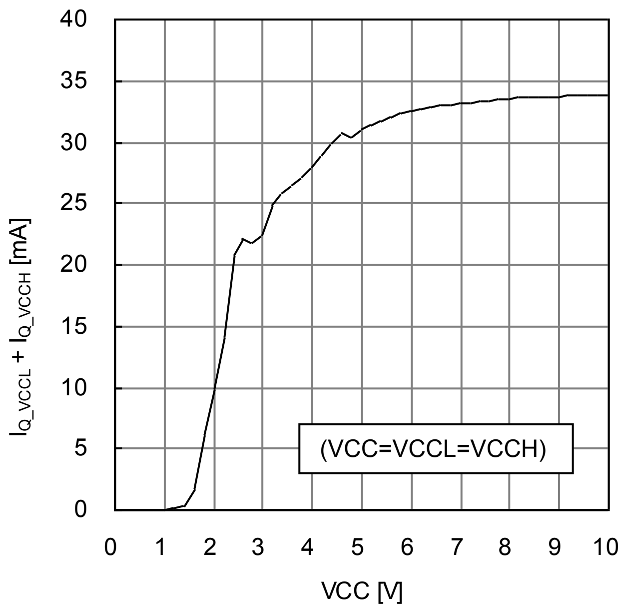

Figure 4. I_{Q_VCCL}+I_{Q_VCCH} vs VCC

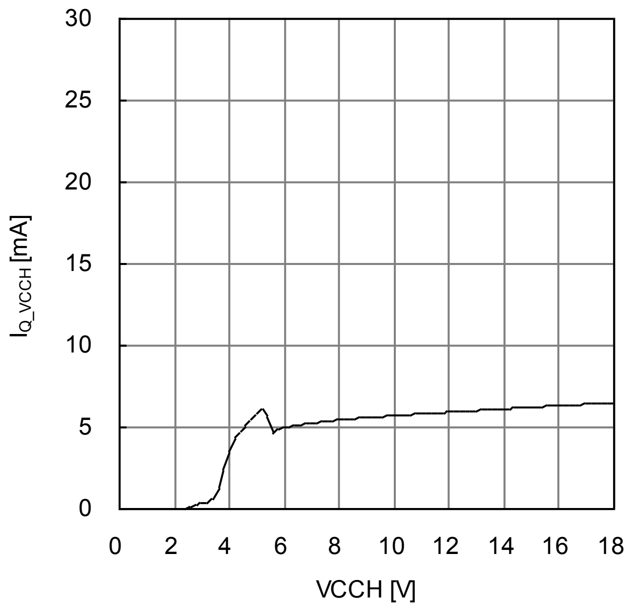

Figure 5. I_{Q_VCCH} vs VCCH
(High-Voltage ON)

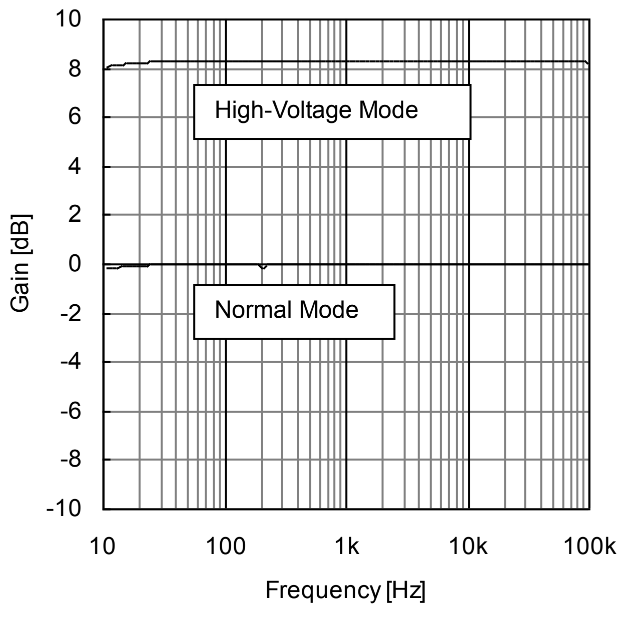

Figure 6. Gain vs Frequency
(Normal / High-Voltage mode)

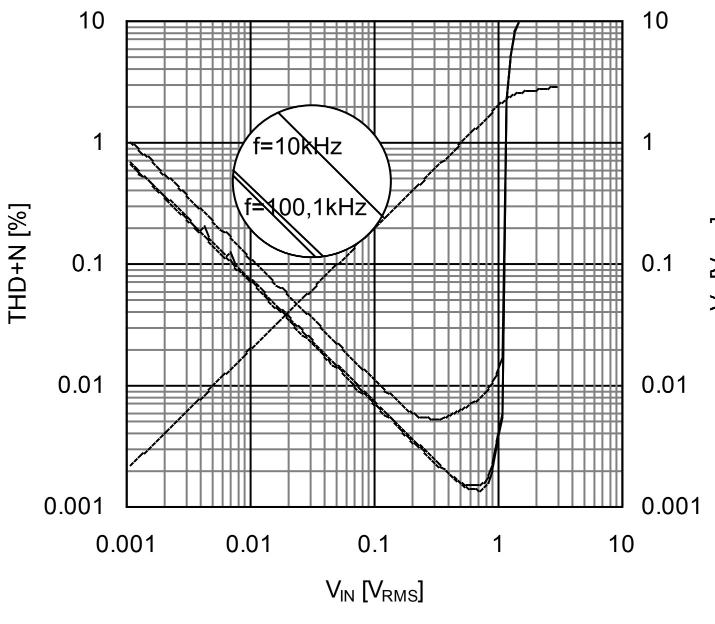

Figure 7. THD+N, V_O vs V_{IN}
(Gain Adjust=+6dB)

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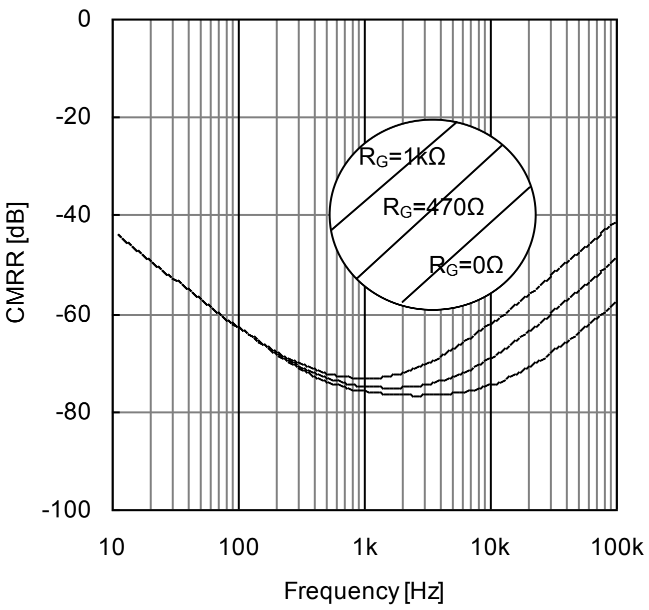

Figure 8. CMRR vs Frequency

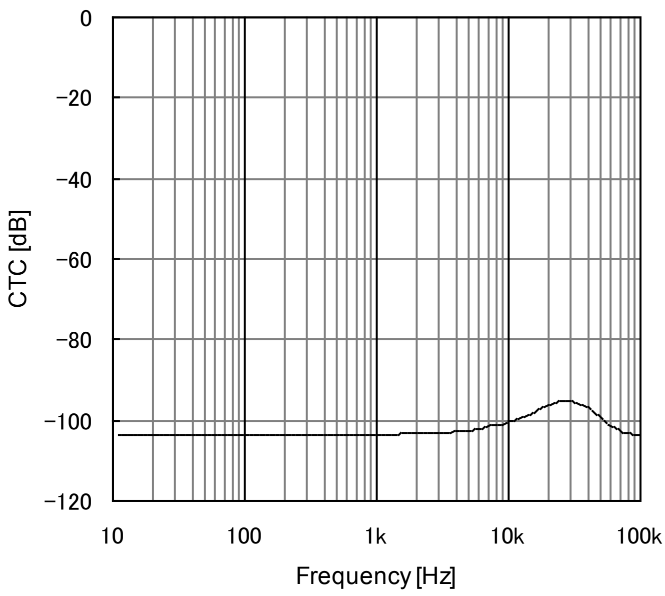

Figure 9. CTC vs Frequency

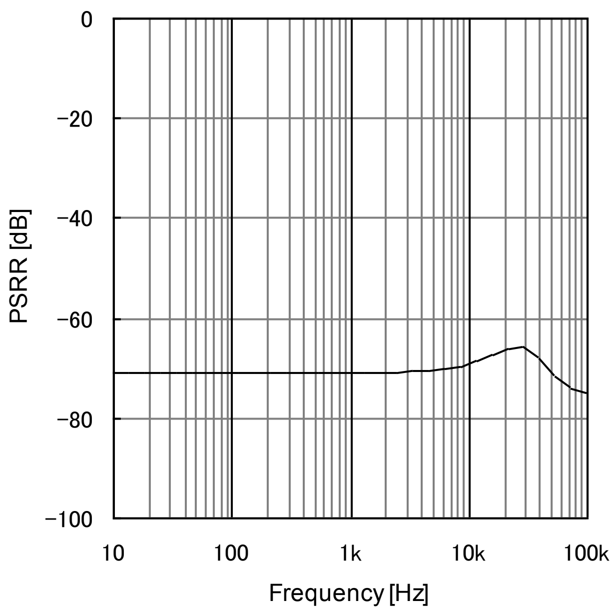

Figure 10. PSRR vs Frequency

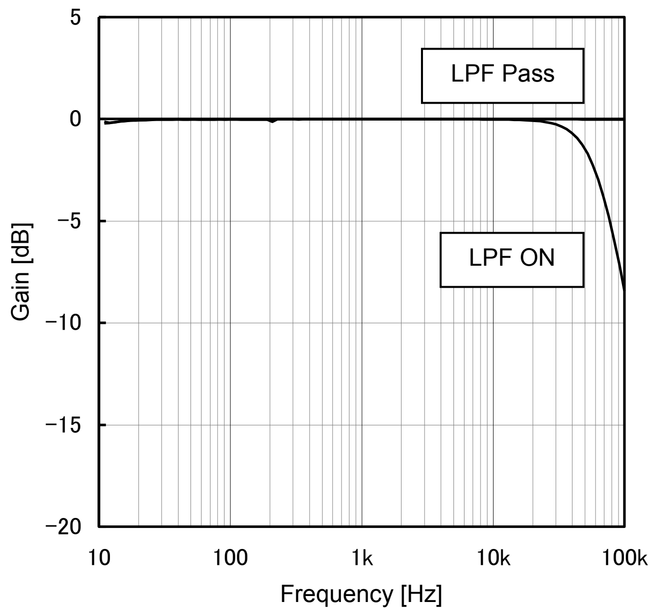

Figure 11. Gain vs Frequency
(LPF ON/Pass)

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I²C-bus Control Signal Specification

1. Electrical specifications and timing for bus lines and I/O stages

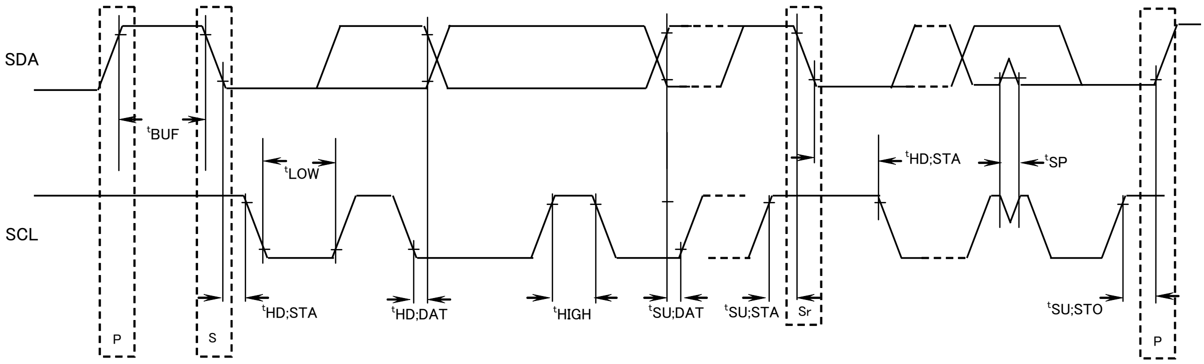


Figure 12. Definition of timing on the I²C-bus

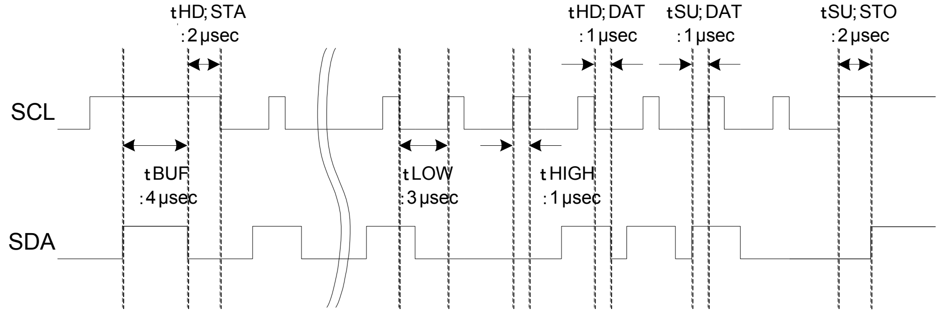
Table 1 Characteristics of the SDA and SCL bus lines for I²C-bus devices

	Parameter	Symbol	Fast-mode I²C-bus		Unit
			Min	Max	
1	SCL Clock Frequency	fSCL	0	400	kHz
2	Bus Free time between a STOP and START condition	tBUF	1.3	—	μsec
3	Hold Time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	0.6	—	μsec
4	LOW Period of the SCL Clock	tLOW	1.3	—	μsec
5	HIGH Period of the SCL Clock	tHIGH	0.6	—	μsec
6	Set-up time for a Repeated START Condition	tSU;STA	0.6	—	μsec
7	Data Hold Time	tHD;DAT	0*	—	μsec
8	Data set-up Time	tSU;DAT	100	—	nsec
9	Set-up Time for STOP Condition	tSU;STO	0.6	—	μsec

All values referred to VIH min. and VIL max. Levels (see Table 2).

Table 2 Characteristics of the SDA and SCL I/O stages for I²C-bus devices

	Parameter	Symbol	Fast-mode I²C-bus		Unit
			Min	Max	
10	LOW level input voltage: Fixed input levels	VIL	-0.5	+1	V
11	HIGH level input voltage: Fixed input levels	VIH	2.3	-	V
12	Pulse width of spikes, which must be suppressed by the input filter.	tSP	0	50	nsec
13	LOW level output voltage (open drain or open collector): At 3mA sink current	VOL1	0	0.4	V
14	Input current each I/O pin with an input voltage between 0.4V and 0.9 VDD max.	I_i	-10	+10	μA



SCL clock frequency:250kHz

Figure 13. I²C data transmission timing

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2. I²C-bus Format

S	Slave Address	A	Select Address	A	Data	A	P
	MSB … LSB		MSB … LSB		MSB … LSB		
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S = Start condition (Recognition of start bit)
Slave Address = Recognition of slave address. 7 bits in upper order are optional.
The last bit must be "L" for writing.
A = Acknowledge bit (Recognition of acknowledgement)
Select Address = Address for each function
Data = Data of each function
P = Stop condition (Recognition of stop bit)

3. I²C-bus Interface Protocol

1) Basic form

S	Slave Address	A	Select Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

2) Automatic increment(Select Address increases (+1) according to the number of data)

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	· · · ·	Data N	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB			MSB LSB		

(Example)①Data 1 shall be set as data of address specified by Select Address.
②Data 2 shall be set as data of address specified by Select Address +1.
③Data N shall be set as data of address specified by Select Address +(N-1).

3) Configuration unavailable for transmission (In this case, only Select Address 1 is set.)

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

(Note)If any data is transmitted as Select Address 2 next to data,
It is recognized as data, not as Select Address 2.

4. Slave Address

MSB … LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	0

80(hex)

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5. Select Address & Data

Items	Select Address (hex)	MSB	Data						LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Initial Setup 1	01	Advanced switch ON/OFF	0	Advanced switch time of Input Gain/Fader		0	0	0	0
Initial Setup 2	02	0	0	Sub Selector		0	0	Rear Selector	Front Selector
Input Selector	05	0	0	0	0	Input Selector			
Input Gain	06	0	0	Input Gain					
Fader 1ch Front	28	Fader Gain / Attenuation							
Fader 2ch Front	29	Fader Gain / Attenuation							
Fader 1ch Rear	2A	Fader Gain / Attenuation							
Fader 2ch Rear	2B	Fader Gain / Attenuation							
Fader Center	2C	Fader Gain / Attenuation							
Fader Subwoofer	2D	Fader Gain / Attenuation							
LPF setup Mixing	30	Front Mixing ON/OFF	LPF fc	0	0	0	0	Sub Gain Adjust	Main Gain Adjust
System Reset	FE	1	0	0	0	0	0	0	1

Advanced switch

Note) Set up bit (It is written with “0” by the above table) which hasn’t been used in “0”.

Notes on data format

1. “Advanced switch” function is available for the hatched parts on the above table.

2. In case of transferring data continuously, Select Address (hex) flows by Automatic increment function, as shown below.

→01→02→05→06→28→29→2A→2B→2C→2D→30

3. Input selector that is not corresponded for “Advanced switch” function, cannot reduce the noise caused when changing the input selector. Therefore, it is recommended to turn on mute when changing these settings.

4. In case of setting to infinite “-∞” by using Fader when input selector setting is changed, please consider “Advanced switch” time.

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Select Address 01 (hex)

Mode	MSB	Advanced switch time of Input Gain/Fader						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
4.7 msec	Advanced switch ON/OFF	0	0	0	0	0	0	0
7.1 msec			0	1				
11.2 msec			1	0				
14.4 msec			1	1				

Mode	MSB	Advanced switch ON/OFF						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	Advanced switch time of Input Gain/Fader		0	0	0	0
ON	1							

Select Address 02 (hex)

Mode	MSB	Front Selector						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
FRONT	0	0	Sub Selector		0	0	Rear Selector	0
INSIDE THROUGH								1

Mode	MSB	Rear Selector						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
REAR	0	0	Sub Selector		0	0	0	Front Selector
FRONT COPY							1	

Mode (Note1)	MSB	Sub Selector						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OUTC(INS) OUTS(INS)	0	0	0	0	0	0	Rear Selector	Front Selector
OUTC(INR1) OUTS(INR2)			0	1				
OUTC (INC) OUTS(INS)			1	0				
Prohibition			1	1				

(Note1) xxx(INxx) : “xxx” means “Output terminal”, “(INxx)” means “Output signal”

(shaded) : Initial condition

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Select Address 05(hex)

Mode	MSB			Input Selector				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
A					0	0	0	0
B single					0	0	0	1
C single					0	0	1	0
D single					0	0	1	1
E single					0	1	0	0
F single					0	1	0	1
C diff					0	1	1	0
D diff	0	0	0	0	0	1	1	1
E diff					1	0	0	0
F full-diff					1	0	0	1
B diff					1	0	1	0
Prohibition					1	0	1	1
					:	:	:	:
					1	1	1	1

: Initial condition

List of active input terminal when set input selector

Mode	Lch positive input terminal	Lch negative input terminal	Rch positive input terminal	Rch negative input terminal
A	1pin(A1)	-	2pin(A2)	-
B single	3pin(BP1)	-	4pin(BP2)	-
C single	5pin(CP1)	-	7pin(CP2)	-
D single	8pin(DP1)	-	10pin(DP2)	-
E single	11pin(EP1)	-	13pin(EP2)	-
F single	14pin(FP1)	-	17pin(FP2)	-
B diff	3pin(BP1)	19pin(BN)	4pin(BP2)	19pin(BN)
C diff	5pin(CP1)	6pin(CN)	7pin(CP2)	6pin(CN)
D diff	8pin(DP1)	9pin(DN)	10pin(DP2)	9pin(DN)
E diff	11pin(EP1)	12pin(EN)	13pin(EP2)	12pin(EN)
F full-diff	14pin(FP1)	15pin(FN1)	17pin(FP2)	16pin(FN2)

〔About Ground Isolation Amplifier〕

Ground Isolation Amplifier : B diff to E diff

Please select this mode when you use them as a ground isolation amplifier.

Full Differential Amplifier : F full-diff

Please select this mode when you use it as a differential amplifier

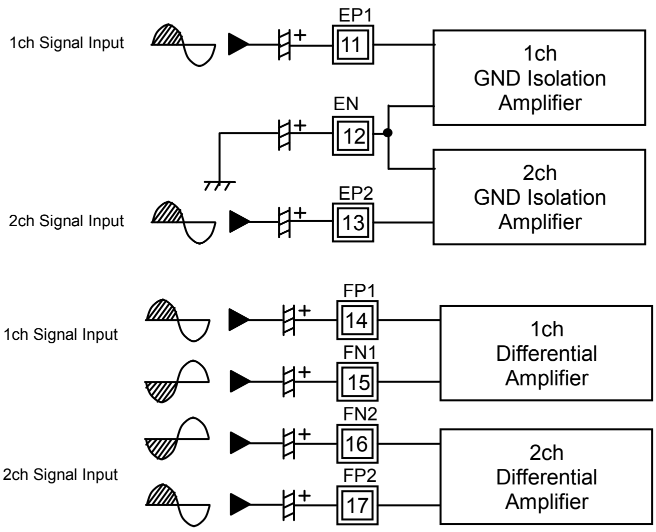

Figure 14. About Ground Isolation Amplifier

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Select Address 06 (hex)

Mode	MSB		Input Gain					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition	0	0	0	0	0	0	0	0
			:	:	:	:	:	:
			0	0	1	0	0	0
+23dB			0	0	1	0	0	1
+22dB			0	0	1	0	1	0
+21dB			0	0	1	0	1	1
+20dB			0	0	1	1	0	0
+19dB			0	0	1	1	0	1
+18dB			0	0	1	1	1	0
+17dB			0	0	1	1	1	1
+16dB			0	1	0	0	0	0
+15dB			0	1	0	0	0	1
+14dB			0	1	0	0	1	0
+13dB			0	1	0	0	1	1
+12dB			0	1	0	1	0	0
+11dB			0	1	0	1	0	1
+10dB			0	1	0	1	1	0
+9dB			0	1	0	1	1	1
+8dB			0	1	1	0	0	0
+7dB			0	1	1	0	0	1
+6dB			0	1	1	0	1	0
+5dB			0	1	1	0	1	1
+4dB			0	1	1	1	0	0
+3dB			0	1	1	1	0	1
+2dB			0	1	1	1	1	0
+1dB			0	1	1	1	1	1
0dB			1	0	0	0	0	0
-1dB			1	0	0	0	0	1
-2dB			1	0	0	0	1	0
-3dB			1	0	0	0	1	1
-4dB			1	0	0	1	0	0
-5dB			1	0	0	1	0	1
-6dB			1	0	0	1	1	0
-7dB			1	0	0	1	1	1
-8dB			1	0	1	0	0	0
-9dB			1	0	1	0	0	1
-10dB			1	0	1	0	1	0
-11dB			1	0	1	0	1	1
-12dB			1	0	1	1	0	0
-13dB			1	0	1	1	0	1
-14dB			1	0	1	1	1	0
-15dB			1	0	1	1	1	1
Prohibition			1	1	0	0	0	0
			:	:	:	:	:	:
			1	1	1	1	1	1

(shaded) : Initial condition

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Select Address 28, 29, 2A, 2B, 2C, 2D (hex)

Gain & ATT	MSB		Fader Gain / Attenuation					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
	0	1	1	0	1	0	0	0
+23dB	0	1	1	0	1	0	0	1
+22dB	0	1	1	0	1	0	1	0
+21dB	0	1	1	0	1	0	1	1
:	:	:	:	:	:	:	:	:
+10dB	0	1	1	1	0	1	1	0
+9dB	0	1	1	1	0	1	1	1
+8dB	0	1	1	1	1	0	0	0
+7dB	0	1	1	1	1	0	0	1
+6dB	0	1	1	1	1	0	1	0
+5dB	0	1	1	1	1	0	1	1
+4dB	0	1	1	1	1	1	0	0
+3dB	0	1	1	1	1	1	0	1
+2dB	0	1	1	1	1	1	1	0
+1dB	0	1	1	1	1	1	1	1
0dB	1	0	0	0	0	0	0	0
-1dB	1	0	0	0	0	0	0	1
-2dB	1	0	0	0	0	0	1	0
-3dB	1	0	0	0	0	0	1	1
: :	: :	: :	: :	: :	: :	: :	: :	: :
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
Prohibition	1	1	0	1	0	0	0	0
	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
-∞dB	1	1	1	1	1	1	1	1

: Initial condition

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Select Address 30(hex)

Mode	MSB			Main Gain Adjust				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Front Mixing	LPF fc	0	0	0	0	Sub Gain Adjust	0
+6dB								1

Mode	MSB			Sub Gain Adjust				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Front Mixing	LPF fc	0	0	0	0	0	Main Gain Adjust
+6dB							1	

Mode	MSB			LPF fc				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
70kHz	Front Mixing	0	0	0	0	0	Sub Gain Adjust	Main Gain Adjust
PASS		1						

Mode	MSB			Front Mixing ON/OFF				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	LPF fc	0	0	0	0	Sub Gain Adjust	Main Gain Adjust
ON	1							

: Initial condition

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6. About power on reset

It is possible for the reset circuit inside the IC to initialize when supply voltage is turned on. Please send data to all address as initial data when the supply is turned on, and turn on mute until all initial data are sent.

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Rise time of VCC	t_{RISE}	33	－	－	μsec	VCC rise time from 0V to 5V
VCC voltage of release power on reset	V_{POR}	－	4.1	－	V	

7. About start-up and power off sequence on IC

By setting the terminal voltage of HIVOLB, it is possible to change the output gain.
At the same time, output DC voltage will also be changed at each mode.

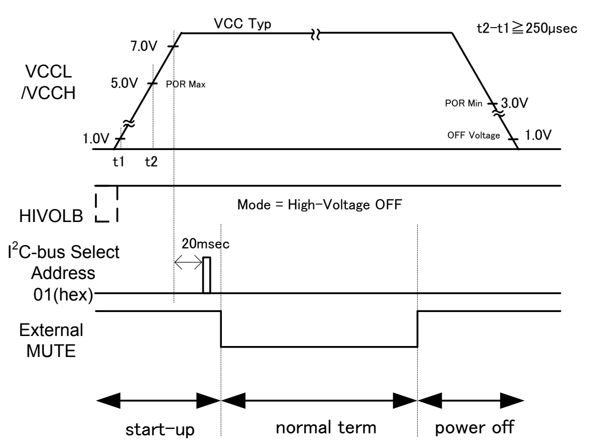
HIVOLB terminal voltage	High-Voltage
GND to 1.0V	ON
2.3V to VCCL	OFF

Please set HIVOLB terminal voltage between the ranges showed by the above tables. If HIVOLB terminal is open, the terminal voltage will be set to 5V due to the pull-up voltage inside the IC. In this case, the IC will be set to "High-Voltage OFF" mode.
The relationship between DC Bias and Output Gain to the configuration of HIVOLB terminal shows as the following table.

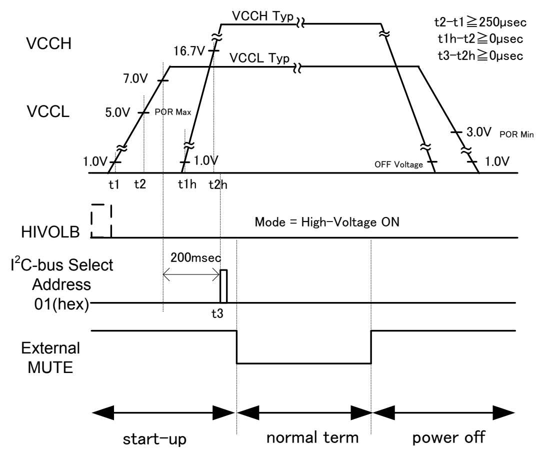
VCCH Supplied Voltage	8.5 V	17 V
HIVOLB Terminal Voltage	Open (5 V) (High-Voltage OFF)	0 V (High-Voltage ON)
Output DC Bias Voltage	4.15 V	8.35 V
Output Gain	0 dB	8.3 dB

If HIVOLB terminal voltage is changed during its operation, Output DC voltage will be also changed shown as above. For reducing these variations, turn the power on after setting the status of the HIVOLB terminal according to the output gain. The start-up and power off sequence is shown next.

.



Normal mode operation (HIVOLB terminal = OPEN)



High-Voltage mode operation

Figure 15. Power off and start-up sequence in each mode

This IC will become active-state by sending data of Select Address 01(hex) on I^{2}C-bus. Therefore, this command must always send in start-up sequence. In addition, External MUTE means recommended period that the muting outside IC. In addition, the starting sequence of VCCL and VCCH does not have the limit, but please start VCCL earlier to reduce a pop noise.
About HIVOLB terminal, but measures have been made spike removal, please note that the IC may accept when receiving input more than 50nsec.

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Fader Volume Attenuation of the Detail

(dB)	D7	D6	D5	D4	D3	D2	D1	D0	(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+23	0	1	1	0	1	0	0	1	-29	1	0	0	1	1	1	0	1
+22	0	1	1	0	1	0	1	0	-30	1	0	0	1	1	1	1	0
+21	0	1	1	0	1	0	1	1	-31	1	0	0	1	1	1	1	1
+20	0	1	1	0	1	1	0	0	-32	1	0	1	0	0	0	0	0
+19	0	1	1	0	1	1	0	1	-33	1	0	1	0	0	0	0	1
+18	0	1	1	0	1	1	1	0	-34	1	0	1	0	0	0	1	0
+17	0	1	1	0	1	1	1	1	-35	1	0	1	0	0	0	1	1
+16	0	1	1	1	0	0	0	0	-36	1	0	1	0	0	1	0	0
+15	0	1	1	1	0	0	0	1	-37	1	0	1	0	0	1	0	1
+14	0	1	1	1	0	0	1	0	-38	1	0	1	0	0	1	1	0
+13	0	1	1	1	0	0	1	1	-39	1	0	1	0	0	1	1	1
+12	0	1	1	1	0	1	0	0	-40	1	0	1	0	1	0	0	0
+11	0	1	1	1	0	1	0	1	-41	1	0	1	0	1	0	0	1
+10	0	1	1	1	0	1	1	0	-42	1	0	1	0	1	0	1	0
+9	0	1	1	1	0	1	1	1	-43	1	0	1	0	1	0	1	1
+8	0	1	1	1	1	0	0	0	-44	1	0	1	0	1	1	0	0
+7	0	1	1	1	1	0	0	1	-45	1	0	1	0	1	1	0	1
+6	0	1	1	1	1	0	1	0	-46	1	0	1	0	1	1	1	0
+5	0	1	1	1	1	0	1	1	-47	1	0	1	0	1	1	1	1
+4	0	1	1	1	1	1	0	0	-48	1	0	1	1	0	0	0	0
+3	0	1	1	1	1	1	0	1	-49	1	0	1	1	0	0	0	1
+2	0	1	1	1	1	1	1	0	-50	1	0	1	1	0	0	1	0
+1	0	1	1	1	1	1	1	1	-51	1	0	1	1	0	0	1	1
0	1	0	0	0	0	0	0	0	-52	1	0	1	1	0	1	0	0
-1	1	0	0	0	0	0	0	1	-53	1	0	1	1	0	1	0	1
-2	1	0	0	0	0	0	1	0	-54	1	0	1	1	0	1	1	0
-3	1	0	0	0	0	0	1	1	-55	1	0	1	1	0	1	1	1
-4	1	0	0	0	0	1	0	0	-56	1	0	1	1	1	0	0	0
-5	1	0	0	0	0	1	0	1	-57	1	0	1	1	1	0	0	1
-6	1	0	0	0	0	1	1	0	-58	1	0	1	1	1	0	1	0
-7	1	0	0	0	0	1	1	1	-59	1	0	1	1	1	0	1	1
-8	1	0	0	0	1	0	0	0	-60	1	0	1	1	1	1	0	0
-9	1	0	0	0	1	0	0	1	-61	1	0	1	1	1	1	0	1
-10	1	0	0	0	1	0	1	0	-62	1	0	1	1	1	1	1	0
-11	1	0	0	0	1	0	1	1	-63	1	0	1	1	1	1	1	1
-12	1	0	0	0	1	1	0	0	-64	1	1	0	0	0	0	0	0
-13	1	0	0	0	1	1	0	1	-65	1	1	0	0	0	0	0	1
-14	1	0	0	0	1	1	1	0	-66	1	1	0	0	0	0	1	0
-15	1	0	0	0	1	1	1	1	-67	1	1	0	0	0	0	1	1
-16	1	0	0	1	0	0	0	0	-68	1	1	0	0	0	1	0	0
-17	1	0	0	1	0	0	0	1	-69	1	1	0	0	0	1	0	1
-18	1	0	0	1	0	0	1	0	-70	1	1	0	0	0	1	1	0
-19	1	0	0	1	0	0	1	1	-71	1	1	0	0	0	1	1	1
-20	1	0	0	1	0	1	0	0	-72	1	1	0	0	1	0	0	0
-21	1	0	0	1	0	1	0	1	-73	1	1	0	0	1	0	0	1
-22	1	0	0	1	0	1	1	0	-74	1	1	0	0	1	0	1	0
-23	1	0	0	1	0	1	1	1	-75	1	1	0	0	1	0	1	1
-24	1	0	0	1	1	0	0	0	-76	1	1	0	0	1	1	0	0
-25	1	0	0	1	1	0	0	1	-77	1	1	0	0	1	1	0	1
-26	1	0	0	1	1	0	1	0	-78	1	1	0	0	1	1	1	0
-27	1	0	0	1	1	0	1	1	-79	1	1	0	0	1	1	1	1
-28	1	0	0	1	1	1	0	0	-∞	1	1	1	1	1	1	1	1

(shaded) : Initial condition

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About bias voltage of output terminal(27,28,35 to 40pin) vs. VCC

Bias voltage of output terminal (27,28,35 to 40pin) keep fixed voltage in operational range of VCC.

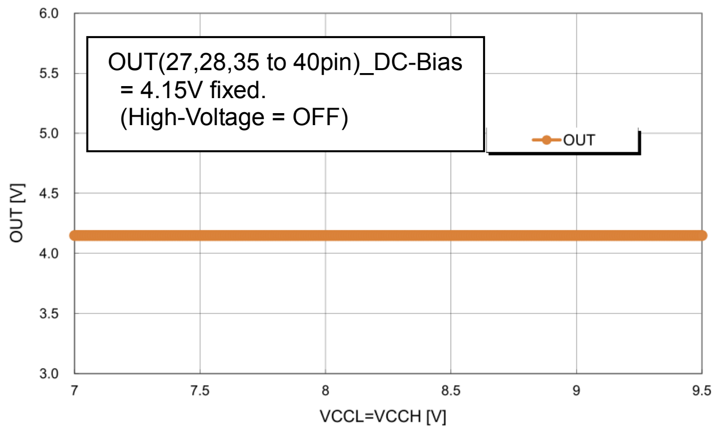

Figure 16. OUT(27,28,35 to 40pin)_DC-Bias = 4.15V fixed. (High-Voltage Mode = OFF)

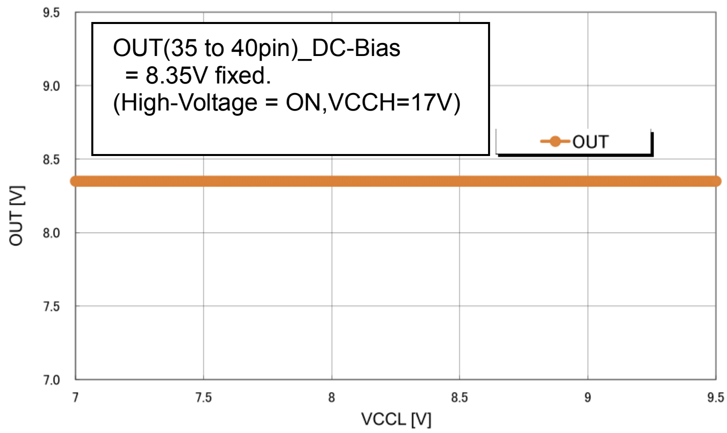

Figure 17. OUT(35 to 40pin)_DC-Bias = 8.35V fixed. (High-Voltage Mode = ON, VCCH=17V)

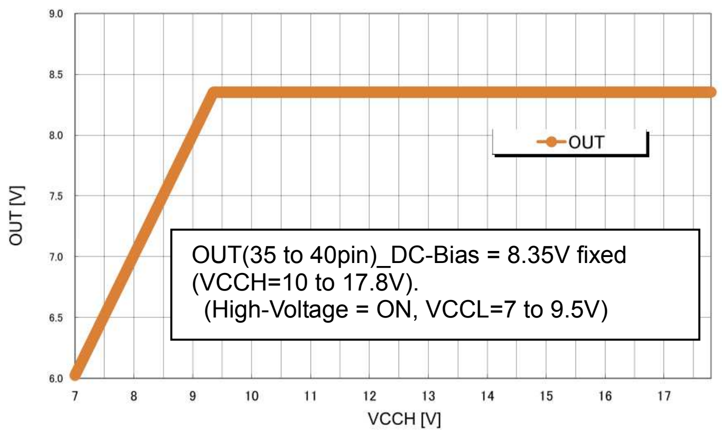

Figure 18. OUT(35 to 40pin)_DC-Bias = 8.35V fixed(VCCH=10 to 17.8V). (High-Voltage Mode = ON, VCCL=7 to 9.5V)

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About Advanced Switch Circuit

【1】Advanced switch technology

1-1. Advanced switch effects

Advanced switch technology is ROHM original technology that can prevent from switching pop noise. If changing the gain setting (for example Fader) immediately, the audible signal will become discontinuously and pop noise will be occurred. This Advanced switch technology will prevent this discontinuous signal by completing the signal waveform and will significantly reduce the noise.

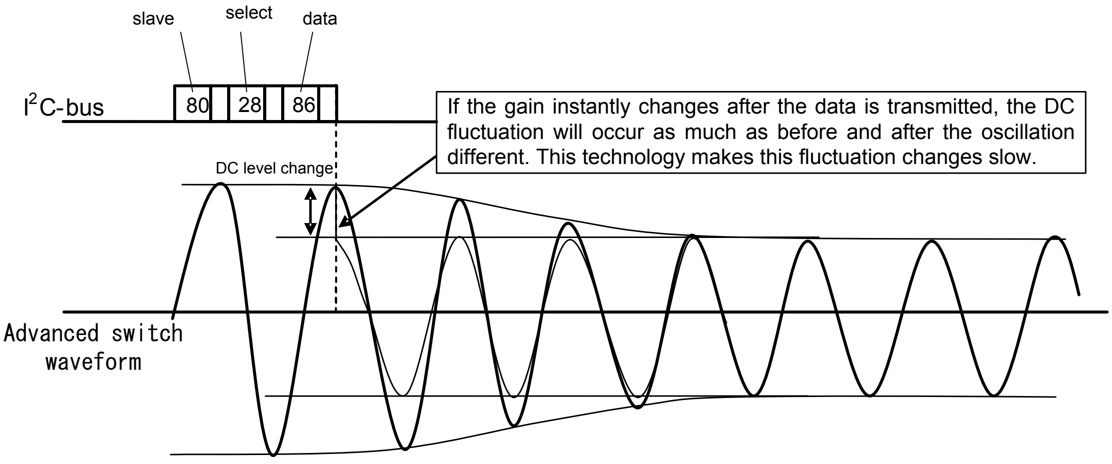

Figure 17. The explanation of advanced switch waveform

This Advanced switch circuit will start operating when the data is transmitted from microcontroller.

Advanced switch waveform is shown as the figure above. For preventing switching noise, this IC will operate optimally by internal processing after the data is transmitted from microcontroller.

However, sometimes the switching waveform is not like the intended form depends on the transmission timing. Therefore, below is the example of the relationship between the transmission timing and actual switching time. Please consider this relationship for the setting.

1-2. The kind of the Transferring Data

・Data setting that is not corresponded to Advanced switch
(Page11 Select Address & Data　Data format without hatching)
There is no particular rule about transferring data.

・Data setting that is corresponded to Advanced switch
（Page11 Select Address & Data　Data format with hatching）
There is no particular rule about transferring data, but Advanced switch must follow the switching sequence as mentioned in【2】as follows.

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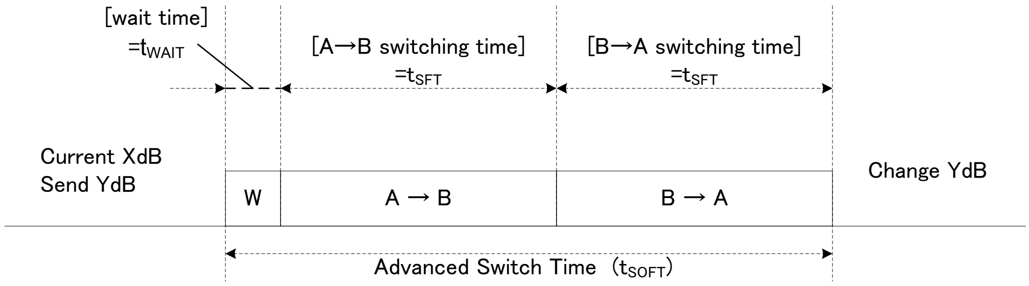
【2】Data transmission that is corresponded to Advanced switch

2-1. Switching time of Advanced switch

Switching time includes [t_{WAIT}(Wait time)], [t_{SFT}(A→B switching time)] and [t_{SFT}(B→A switching time)].
25msec is needed per 1 switching. ($t_{SOFT} = t_{WAIT} + 2 * t_{SFT}$, t_{WAIT} =2.3msec, t_{SFT} =11.2msec)



In the figure above, Start/Stop state is expressed as "A" and temporary state is expressed as "B".
The switching sequence of Advanced switch consists of the cycle "A(start)→B(temporary)→A(stop)". Therefore, switching sequence will not stop at B state.

For example, switching is performed from A(Initial gain)→B(set gain)→A(set gain) when switching from initial gain to set gain. And switching time (t_{SFT}) of A→B or B→A are equal.

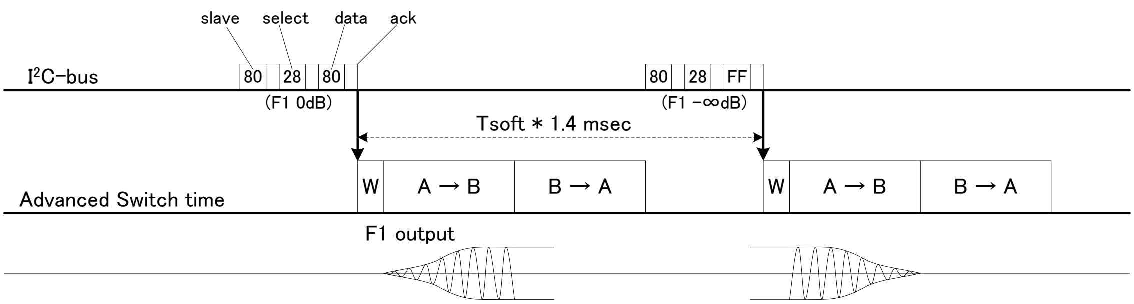
2-2. About the data transmission's timing in same block state and switching operation

■ Transmitting example 1

This is an example when transmitting data in same block with "enough interval for data transmission".
(enough interval for data transmission : 1.4 x t_{SOFT} * "1.4" includes tolerance margin.)

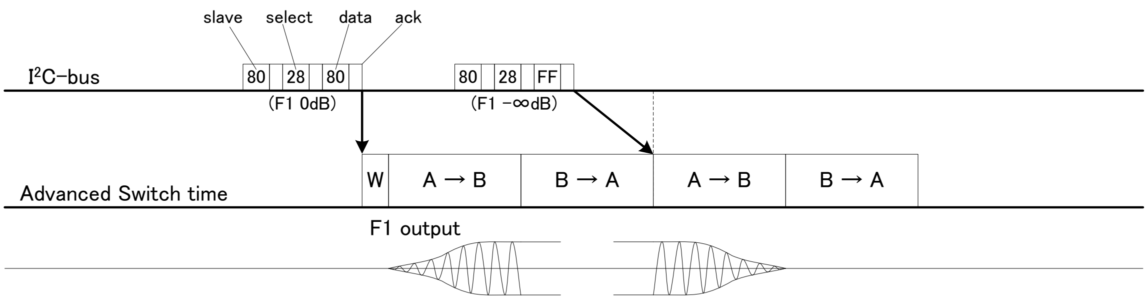
Definition of example expression :

F1=Fader 1ch Front, F2=Fader 2ch Front, R1=Fader 1ch Rear, R2=Fader 2ch Rear
C=Fader Center, S=Fader Subwoofer, MIX=Front Mixing



■ Transmitting example 2

This is an example when the transmission interval is not enough (smaller than "Transmission example 1"). When the data is transmitted during first switching operation, the second data will be reflected after the first switching operation. In this case, there is no wait time (t_{WAIT}) before the second switching operation.



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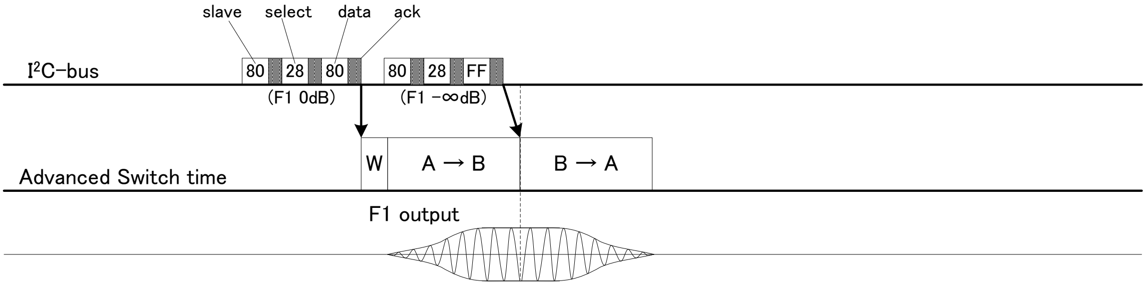
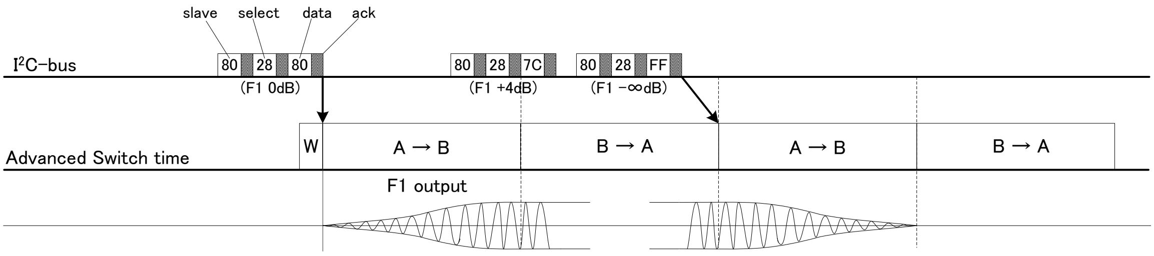
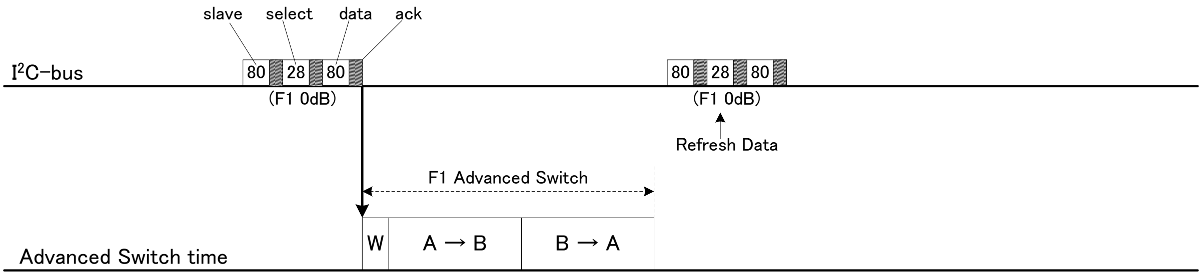
■ Transmitting example 3
This is an example of switching operation when transmission interval is smaller than “Transmission example 2”).
When the data is transmitted during the first switching operation, and transmission timing is just during A→B switching operation, the second data will be reflected at B→A switching term.



■ Transmitting example 4
The below figure shows an example of switching operation that the data are transmitted serially with smaller transmission interval than “Transmission example 3”.
IC has internal data-storage buffer and buffer transmitted data as storage data constantly.
However, only the latest data is kept so, in this example, +4dB data transmitted secondly is ignored.



■ Transmitting example 5
Transmitted data is firstly buffered and written to setting data which set gain. However, when there is no difference between transmitted data and setting data such as refresh data, advanced switch operation doesn’t start.



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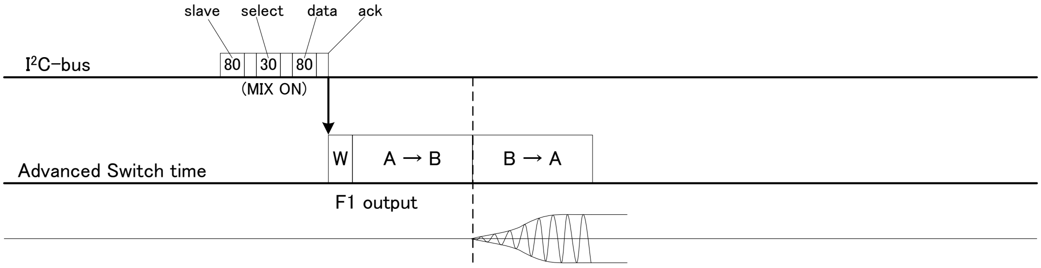
2-3. Mixing ON/OFF switching operation of Front mixing

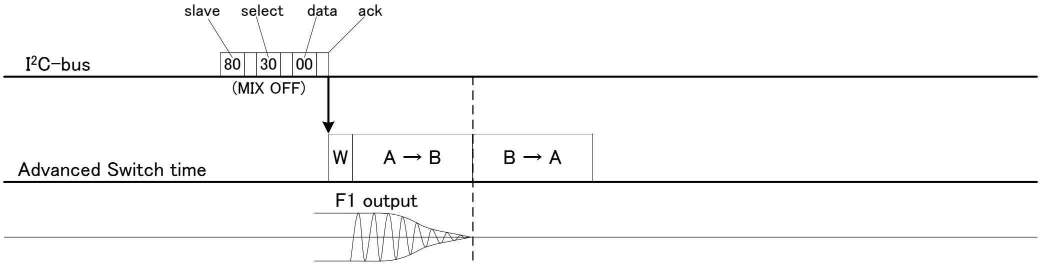
The action of the Mixing switching waveform is different in OFF to ON or ON to OFF.

■ Transmission example 1

This is an example of Mixing OFF to ON state.



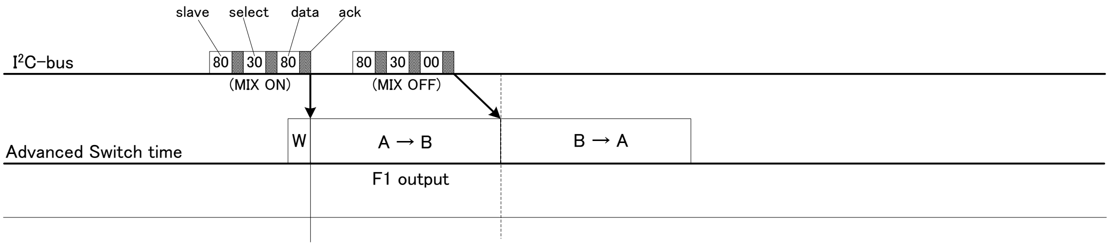
This is an example of Mixing ON to OFF state



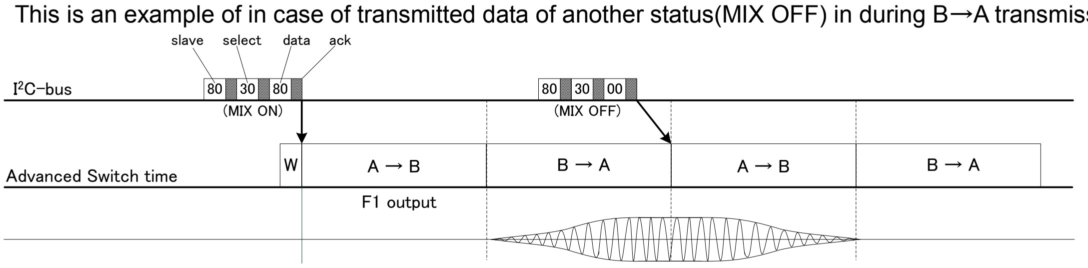
■ Transmission example 2

This is an example when transmission ON to OFF in short interval during to Mixing switching operation.

This is an example of in case of transmitted data of another status(MIX OFF) in during A→B transmission timing.



This is an example of in case of transmitted data of another status(MIX OFF) in during B→A transmission timing.



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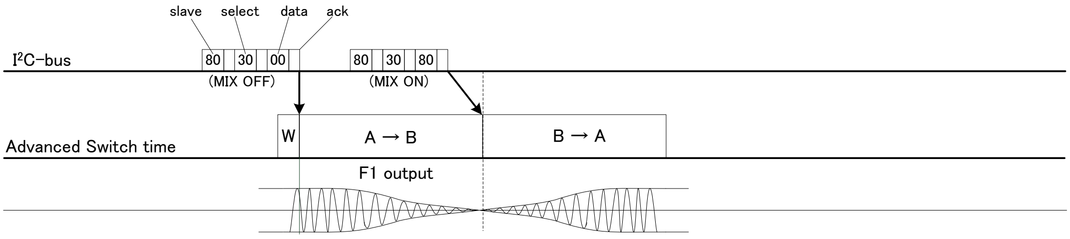
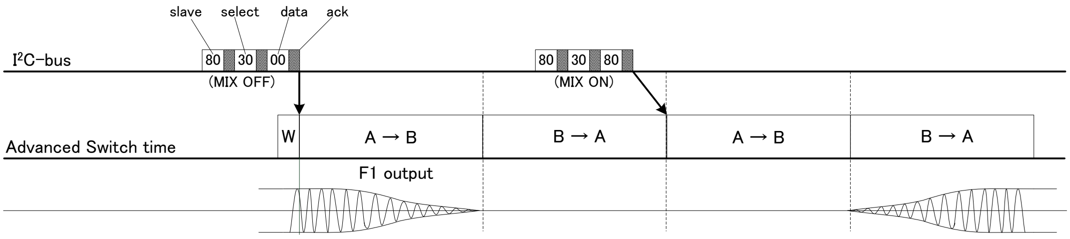
■ Transmission example 3
This is an example when transmission OFF to ON in short interval during to Mixing switching operation.

This is an example of in case of transmitted data of another status(MIX ON) in during A→B transmission timing.

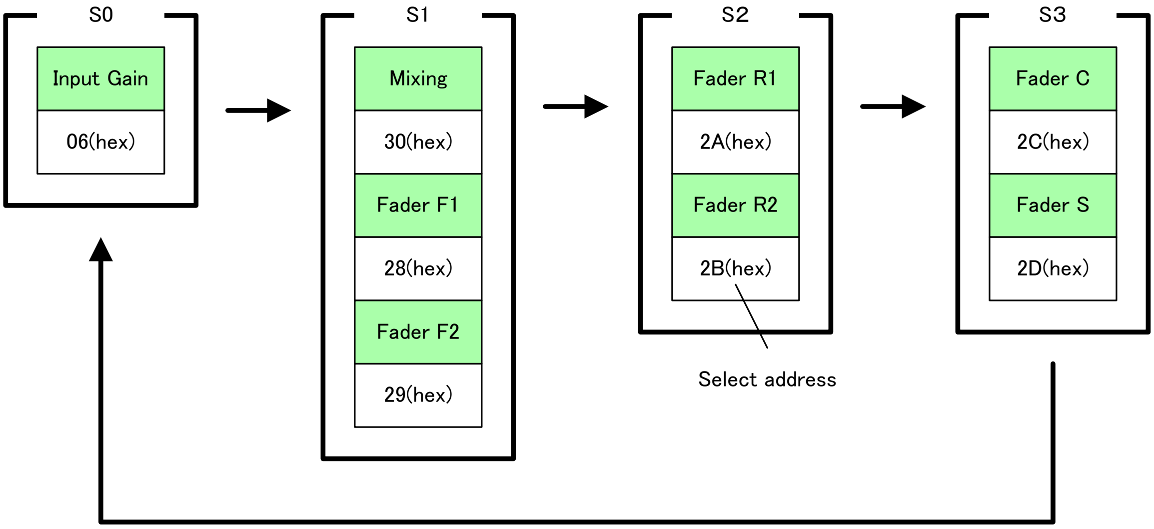


This is an example of in case of transmitted data of another status(MIX ON) in during B→A transmission timing.



2-3. About the data transmitting timing and the switching movement in several block state

When data are transmitted to several blocks, treatment in the BS (block state) unit is carried out inside the IC. The order of advanced switch movement start is decided in advance dependent on BS.



The order of advanced switch start

Note) It is possible that blocks in the same BS start switching at the same timing.

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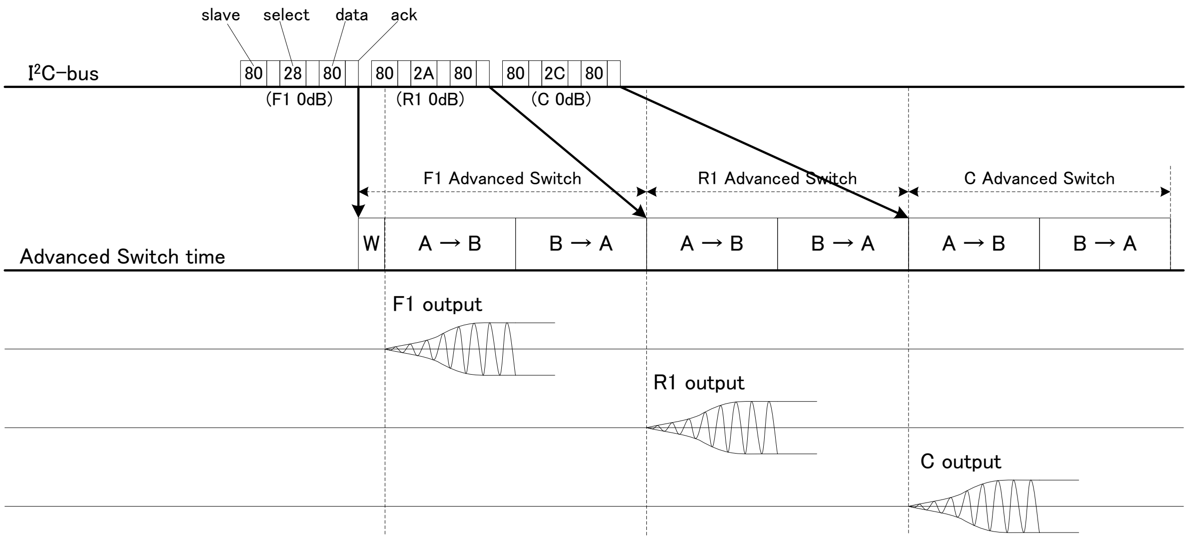
■ Transmitting example 1

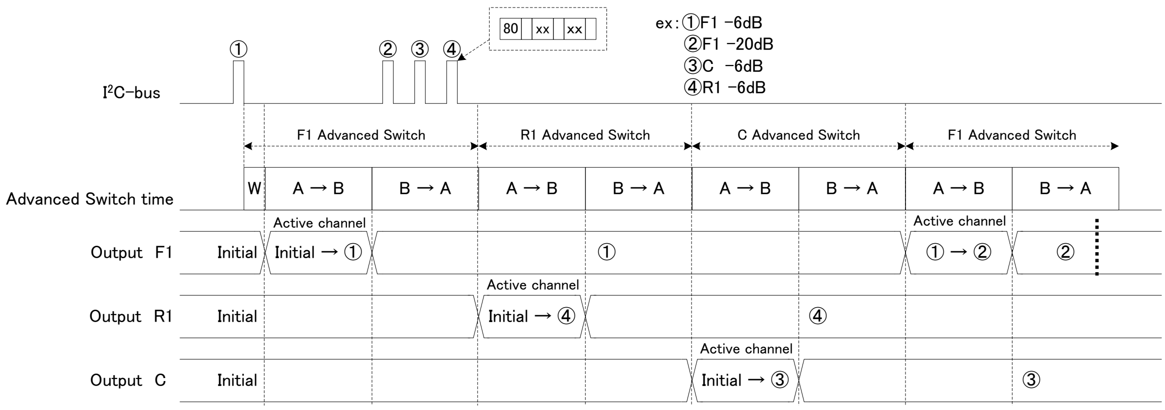
About the transmission to several blocks also, as explained in the previous section, though there is no restriction of the I^{2}C- bus data transmitting timing, the start timing of switching follows the figure of previous page, The order of advanced switch start.

Therefore, it isn't based on the data transmitting order, and an actual switching order becomes as the figure of previous page, "The order of advanced switch start".
Each block data is being transmitted separately in the transmitting example 5, but it becomes the same result even if data are transmitted by automatic increment.



■ Transmitting example 2

In the case that data transmission order and actual switching order is different, or data is transmitted to the block in other BS before the advanced switch operation finished, switching of next BS starts after current switching.



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