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Sound Processor for Car Audio with Built-in High-Voltage Amplifier and 2nd Order Post Filter

BD37069FV-M

General Description

BD37069FV-M is a sound processor developed for car audio with built-in selector of six stereo inputs and output interfaced to ADC after adjusting signal level.
BD37069FV-M has a 6-channel volume circuit and built-in 2nd order post filter which reduces the out-of-band noise. The High-Voltage function is capable to reach up to 5.2V_{RMS} maximum output. Furthermore, the IC is simple to design due to the built-in TDMA noise reduction systems.

Features

- AEC-Q100 Qualified (Note1)
- Built-in differential input selector that can select single-ended / differential input
- Reduce switching pop noise of input gain control due to the built-in advanced switch circuit
- Less out-of-band noise of DAC by built-in 2nd order post filter
- Built-in buffered ground isolation amplifier to achieve high CMRR characteristics
- Built-in TDMA noise reduction circuit reduces the additional components for external filter
- Available to output 5.2V_{RMS} by High-Voltage function (This device is possible to 3.2V_{RMS} output by using another High-Voltage mode, VCCH=11.5V)
- Available to control by 3.3V / 5V for I^2C-bus controller
- The input and output terminals are located together to arrange the flow of signal in a same direction making the PCB layout easier and PCB area smaller

(Note 1) Grade 3

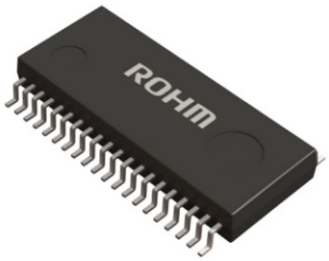
Key Specifications (Note2)

■Total Harmonic Distortion:	0.003%(Typ)
■Maximum Input Voltage:	2.1V_{RMS}(Typ)
■Common Mode Rejection Ratio :	55dB(Min)
■Maximum Output Voltage:	5.2V_{RMS}(Typ)
■Output Noise Voltage:	23μV_{RMS}(Typ)
■Residual Output Noise Voltage:	10.5μV_{RMS}(Typ)
■Ripple Rejection Ratio:	-70dB (Typ)
■Operating Temperature Range:	-40°C to +85°C

(Note2)These specifications are High-Voltage mode2.

Package

	W(Typ) x D(Typ) x H(Max)
SSOP-B40	13.60mm x 7.80mm x 2.00mm



Applications

Car Audio and Other Audio Equipment

Typical Application Circuit

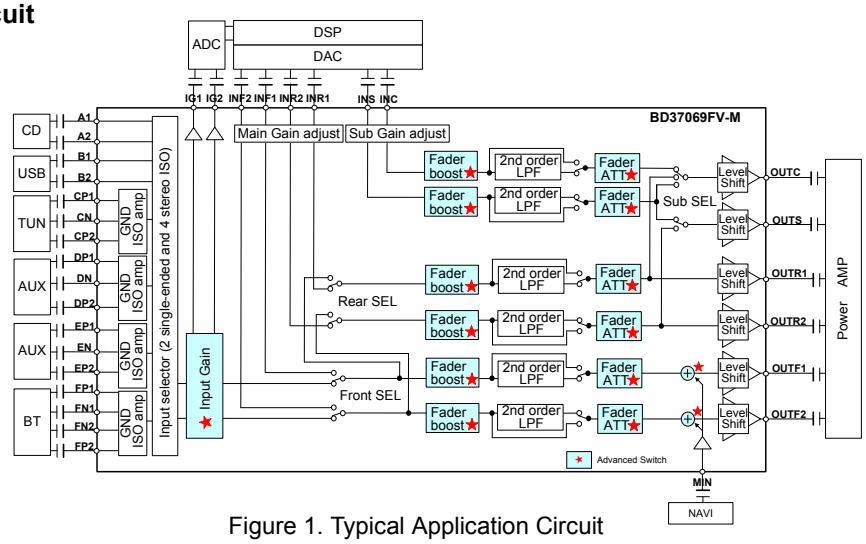


Figure 1. Typical Application Circuit

Contents

Pin Configuration

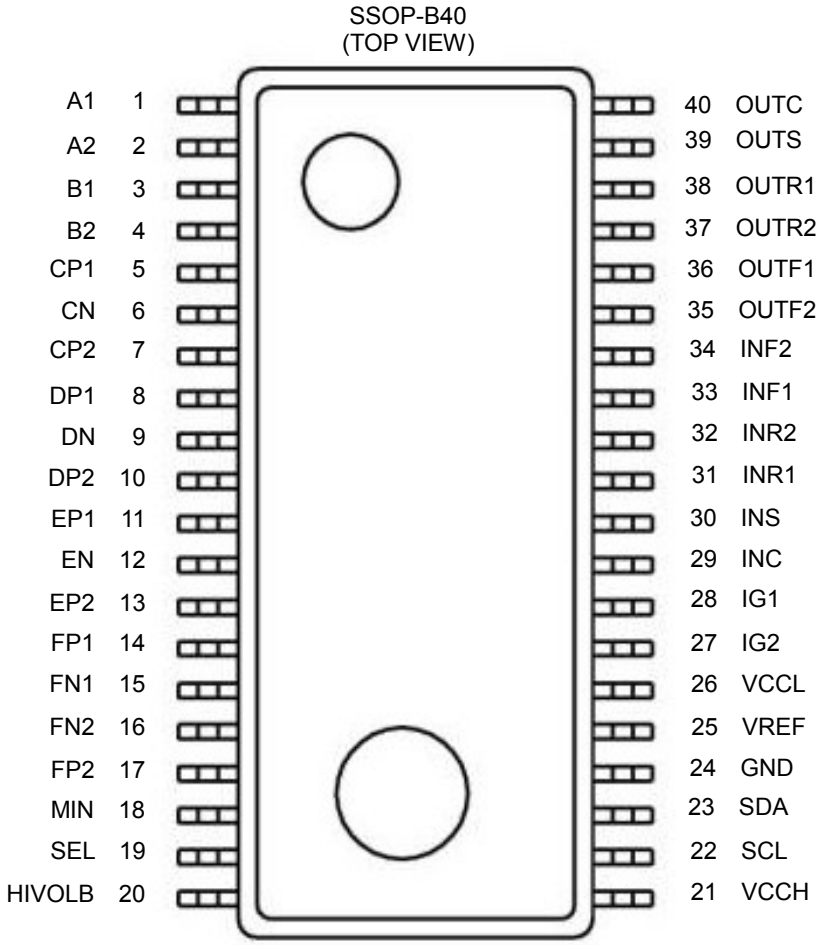


Figure 2.Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	A1	A input terminal of 1ch	21	VCCH	VCCH terminal for power supply
2	A2	A input terminal of 2ch	22	SCL	I^2C-bus clock terminal
3	B1	B input terminal of 1ch	23	SDA	I^2C-bus data terminal
4	B2	B input terminal of 2ch	24	GND	GND terminal
5	CP1	C positive input terminal of 1ch	25	VREF	BIAS terminal
6	CN	C negative input terminal	26	VCCL	VCCL terminal for power supply
7	CP2	C positive input terminal of 2ch	27	IG2	Input gain output terminal of 2ch
8	DP1	D positive input terminal of 1ch	28	IG1	Input gain output terminal of 1ch
9	DN	D negative input terminal	29	INC	Center input terminal
10	DP2	D positive input terminal of 2ch	30	INS	Subwoofer input terminal
11	EP1	E positive input terminal of 1ch	31	INR1	Rear input terminal of 1ch
12	EN	E negative input terminal	32	INR2	Rear input terminal of 2ch
13	EP2	E positive input terminal of 2ch	33	INF1	Front input terminal of 1ch
14	FP1	F positive input terminal of 1ch	34	INF2	Front input terminal of 2ch
15	FN1	F negative input terminal of 1ch	35	OUTF2	Front output terminal of 2ch
16	FN2	F negative input terminal of 2ch	36	OUTF1	Front output terminal of 1ch
17	FP2	F positive input terminal of 2ch	37	OUTR2	Rear output terminal of 2ch
18	MIN	Mixing input terminal	38	OUTR1	Rear output terminal of 1ch
19	SEL	High Voltage output mode Select	39	OUTS	Subwoofer output terminal
20	HIVOLB	Output Gain control terminal	40	OUTC	Center output terminal

Block Diagram

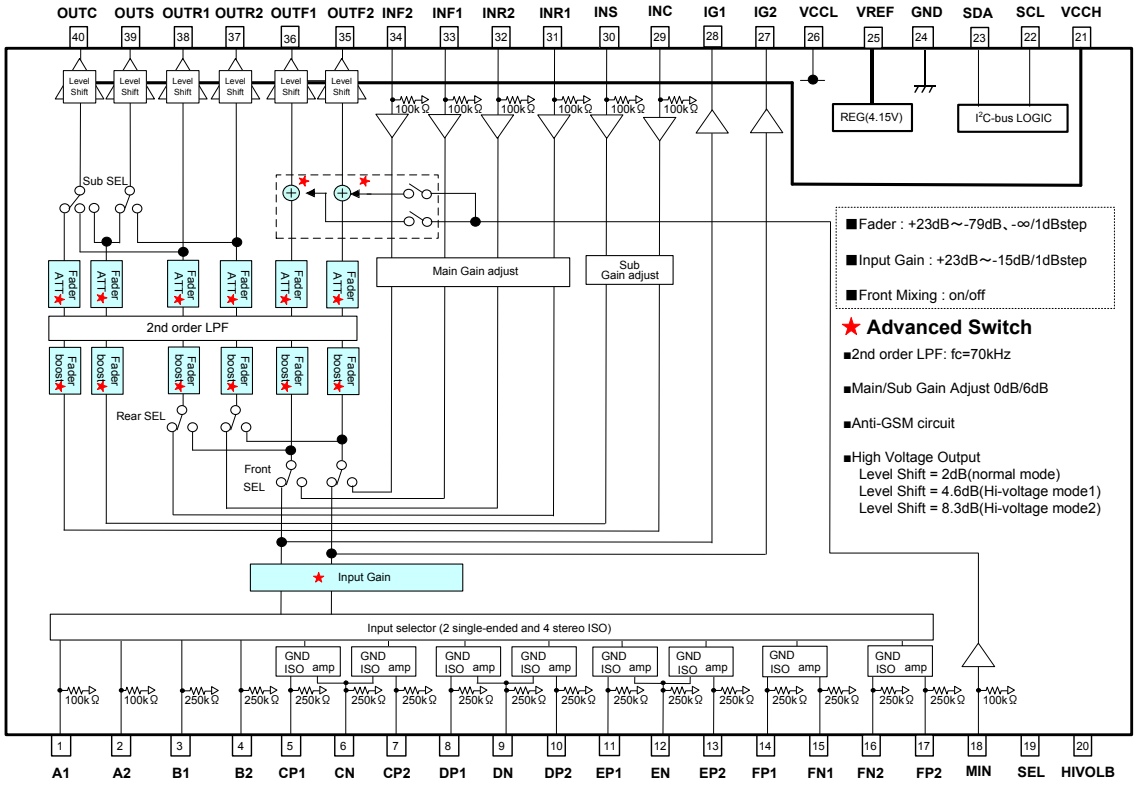


Figure 3. Block Diagram

・The outputs of Pin 27 and Pin 28 are selected by the input selector, from the inputs Pin 1 to Pin 17. Otherwise, these signals are possible to output directly on Pin 35 to Pin 40.
・6-channel input signals from DSP on Pin 29 to Pin 34 pass through the volume circuit (Fader) and 2nd order post filter to the output terminals Pin 35 to Pin 40 .
・It is possible for 6-channel inputs to set the gain up to +6dB by Gain adjust function and to set the gain up to +8.3dB by Level Shift Circuit (High-Voltage Mode).

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating		Unit
Power Supply Voltage	V_{CCL}	10		V
	V_{CCH}	18		V
Input Voltage	V_{IN}	SCL, SDA	GND-0.3 to +7	V
		Other	GND-0.3 to V_{CCL}+0.3	
Storage Temperature	T_{STG}	-55 to +150		°C
Maximum Junction Temperature	T_{JMAX}	+150		°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SSOP-B40				
Junction to Ambient	θ_{JA}	103.6	58.8	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	17	10	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air)
*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 3)*Using a PCB board based on JESD51-3.
*(Note 4)*Using a PCB board based on JESD51-7

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.6mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

Recommended Operating Condition (Ta= -40°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CCL}	7.0	9	9.5	V
	V_{CCH}	V_{CCL}	17	17.8	V

Electrical Characteristics

Unless otherwise specified, Ta=25°C, V_{CCL}=9V, V_{CCH}=17V, f=1kHz, V_{IN}=1V_{RMS}, R_L=10kΩ,
Input selector A, Input Gain 0dB, Gain Adjust +6dB, High-Voltage ON (High-Voltage mode2), LPF ON, Fader 0dB,
Input point=A1/A2, Monitor point=IG1/IG2

Block	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
General	Current Consumption (VCCL)	I_{Q_VCCL}	-	30	43	mA	No signal
	Current Consumption (VCCH)	I_{Q_VCCH}	-	7	10	mA	No signal
Input Selector	Input Impedance (A)	R_{IN_S}	70	100	130	kΩ	
	Input Impedance (B, C, D, E, F)	R_{IN_D}	175	250	325	kΩ	
	Voltage Gain	G_V	-1.5	0	1.5	dB	$G_V = 20\log(V_{OUT}/V_{IN})$
	Channel Balance	CB	-1.5	0	1.5	dB	$CB = G_{V1}-G_{V2}$
	Total Harmonic Distortion	THD+N	-	0.003	0.05	%	V_{OUT} = 1V_{RMS} BW = 400-30kHz
	Output Noise Voltage (Note1)	V_{NO1}	-	3.1	8.0	μV_{RMS}	R_G = 0Ω BW = IHF-A
	Maximum Input Voltage	V_{IM}	2.0	2.2	-	V_{RMS}	V_{IM} at THD+N(V_{OUT}) = 1% BW = 400-30kHz
	Crosstalk Between Channels (Note1)	CTC	-	-100	-90	dB	R_G = 0Ω $CTC = 20\log(V_{OUT}/V_{OUT}')$ BW = IHF-A
	Crosstalk Between Selectors(Note1)	CTS	-	-100	-90	dB	R_G = 0Ω $CTS = 20\log(V_{OUT}/V_{OUT}')$ BW = IHF-A
	Common Mode Rejection Ratio (C, D, E, F) (Note1)	CMRR	55	65	-	dB	XP1 and XN input XP2 and XN input $CMRR = 20\log(V_{IN}/V_{OUT})$ BW = IHF-A, [X=C,D,E,F]
Input Gain	Minimum Input Gain	G_{IN_MIN}	-17	-15	-13	dB	Input Gain = -15dB V_{IN} = 0.1V_{RMS} $G_{IN} = 20\log(V_{OUT}/V_{IN})$
	Maximum Input Gain	G_{IN_MAX}	21	23	25	dB	Input Gain = 23dB V_{IN} = 0.1V_{RMS} $G_{IN} = 20\log(V_{OUT}/V_{IN})$
	Gain Set Error	G_{IN_ERR}	-2	0	+2	dB	Input Gain = -15 to +23dB
	Output Impedance	R_{OUT}	-	-	50	Ω	
	Maximum Output Voltage	V_{OM}	2.0	2.2	-	V_{RMS}	THD+N = 1% BW = 400-30kHz

(Note1) VP-9690A (Average value detection, effective value display) filter by Panasonic is used for measurement. Input and output are in-phase.

Unless otherwise specified, Ta=25°C, V_{CCL}=V_{CCH}=9V, f=1kHz, V_{IN}=0.9V_{RMS}, R_L=10kΩ,
Input selector A, Input Gain 0dB, Gain Adjust +6dB, High-Voltage OFF(normal mode), LPF ON, Fader 0dB,
Input point=INF1/INF2/INR1/INR2/INC/INS, Monitor point=OUTF1/OUTF2/OUTR1/OUTR2/OUTC/OUTS

Block	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
Level Shift	Output Impedance	R_{OUT}	-	-	50	Ω	
	☆Maximum Output Voltage	V_{OM}	2.3	2.5	-	V_{RMS}	V_{IN} = 1V_{RMS} THD+N = 1% BW = 400-30kHz
	☆Output Gain	$G_{H(OUT)}$	0.5	2	3.5	dB	$G_{H(OUT)}$ = 20log(V_{OUT}/V_{IN})

☆This Item is designated by ROHM only to discriminate between other items and it.

Unless otherwise specified, Ta=25°C, V_{CCL}=9V, V_{CCH}=11.5V, f=1kHz, V_{IN}=0.9V_{RMS}, R_L=10kΩ,
Input selector A, Input Gain 0dB, Gain Adjust +6dB, High-Voltage ON(High-Voltage mode1), LPF ON, Fader 0dB,
Input point=INF1/INF2/INR1/INR2/INC/INS, Monitor point=OUTF1/OUTF2/OUTR1/OUTR2/OUTC/OUTS

Block	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
Level Shift	Output Impedance	R_{OUT}	-	-	50	Ω	
	☆Maximum Output Voltage	V_{OM}	3.2	3.4	-	V_{RMS}	V_{IN}=1V_{RMS} THD+N=1% BW=400-30kHz
	☆Output Gain	$G_{H(OUT)}$	2.6	4.6	6.6	dB	$G_{H(OUT)}$=20log(V_{OUT}/V_{IN})

☆This Item is designated by ROHM only to discriminate between other items and it.

Unless otherwise specified, Ta=25°C, V_{CCL}=9V, V_{CCH}=17V, f=1kHz, V_{IN}=0.9V_{RMS}, R_L=10kΩ,
Input selector A, Input Gain 0dB, Gain Adjust +6dB, High-Voltage ON(High-Voltage mode2), LPF ON, Fader 0dB,
Input point=INF1/INF2/INR1/INR2/INC/INS, Monitor point=OUTF1/OUTF2/OUTR1/OUTR2/OUTC/OUTS

Block	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
Level Shift	Output Impedance	R_{OUT}	-	-	50	Ω	
	☆Maximum Output Voltage	V_{OM}	5.0	5.2	-	V_{RMS}	V_{IN}=1V_{RMS} THD+N=1% BW=400-30kHz
	☆Output Gain	$G_{H(OUT)}$	6.3	8.3	10.3	dB	$G_{H(OUT)}$=20log(V_{OUT}/V_{IN})

☆This Item is designated by ROHM only to discriminate between other items and it.

Unless otherwise specified, Ta=25°C, V_{CCL}=9V, V_{CCH}=17V, f=1kHz, V_{IN}=0.9V_{RMS}, R_L=10kΩ,
Input selector A, Input Gain 0dB, Gain Adjust +6dB, High-Voltage ON(High-Voltage mode2), LPF ON, Fader 0dB,
Input point=INF1/INF2/INR1/INR2/INC/INS, Monitor point=OUTF1/OUTF2/OUTR1/OUTR2/OUTC/OUTS

Block	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
Fader	Maximum Boost Gain	$G_{F\ BST}$	21	23	25	dB	Fader Boost Gain = +23dB V_{IN}=0.1V_{RMS} G_F=20log(V_{OUT}/V_{IN})-$G_{H(OUT)}$ Gain Adjust=0dB
	Channel Balance	CB	-1.5	0	1.5	dB	CB = GV1-GV2
	Total Harmonic Distortion	THD+N	—	0.003	0.05	%	BW=400-30kHz Gain Adjust = 0dB
	Output Noise Voltage (Note1)	V_{NO1}	—	23	40	μV_{RMS}	R_G = 0Ω BW = IHF-A
	Residual Output Noise Voltage (Note1)	V_{NOR}	—	10.5	20	μV_{RMS}	Fader Attenuation = -∞dB R_G = 0Ω BW = IHF-A
	Maximum Input Voltage	V_{IM}	2.0	2.1	—	V_{RMS}	V_{IM} at THD+N(V_{OUT})=1% BW=400-30kHz Gain Adjust = 0dB
	Crosstalk Between Channels (Note1)	CTC	—	-100	-90	dB	R_G = 0Ω CTC=20log(V_{OUT}/$V_{OUT'}$) BW = IHF-A
	Maximum Attenuation (Note1)	$G_{F\ MIN}$	—	-100	-90	dB	Fader Attenuation = -∞dB G_F=20log(V_{OUT}/V_{IN}) BW = IHF-A
	Gain Set Error	$G_{F\ ERR}$	-2	0	2	dB	Fader Boost Gain = +1 to +23dB
	Attenuation Set Error 1	$G_{F\ ERR1}$	-2	0	2	dB	Fader Attenuation = 0 to -15dB
	Attenuation Set Error 2	$G_{F\ ERR2}$	-3	0	3	dB	Fader Attenuation = -16 to -47dB
	Attenuation Set Error 3	$G_{F\ ERR3}$	-4	0	4	dB	Fader Attenuation = -48 to -79dB
	Power Supply Rejection Ratio	RR_{VCCL}	—	-70	-40	dB	V_{RR}=0.1V_{RMS} f_{RR}=1kHz RR_{VCCL}=20log(V_{OUT} /V_{CCL})
		RR_{VCCH}	—	-70	-40	dB	V_{RR}=0.1V_{RMS} f_{RR}=1kHz RR_{VCCH}=20log(V_{OUT} /V_{CCH})
Mixing	Input Impedance	R_{IN_M}	70	100	130	kΩ	
	Maximum Input Voltage	V_{IM_M}	2.0	2.2	-	V_{RMS}	V_{IM_M} at THD+N(V_{OUT})=1% BW=400-30kHz Input point=MIN
	Maximum Attenuation (Note1)	$G_{MX\ MIN}$	-	-100	-85	dB	Front Mixing=OFF G_{MX}=20log(V_{OUT} /V_{IN}) BW=IHF-A Input point=MIN
	Mixing Gain	G_{MX}	-2	0	2	dB	Front Mixing=ON G_{MX}=20log(V_{OUT}/V_{IN})- $G_{H(OUT)}$
Gain Adjust	Input Impedance	R_{IN_M}	70	100	130	kΩ	
	Boost Gain	$G_{F\ BST}$	4	6	8	dB	Gain Adjust=6dB V_{IN}=0.1V_{RMS} G_F=20log(V_{OUT}/V_{IN})- $G_{H(OUT)}$
	Channel Balance	CB	-1.5	0	1.5	dB	CB = GV1-GV2

(Note1) VP-9690A (Average value detection, effective value display) filter by Panasonic is used for measurement. Input and output are in-phase.

Typical Performance Curve(s)

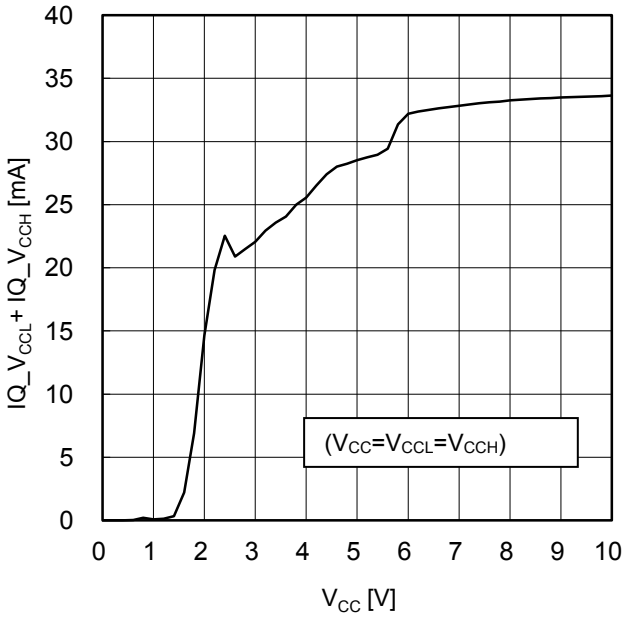


Figure 4. V_{CC} vs. $I_{Q\_VCCL}+I_{Q\_VCCH}$

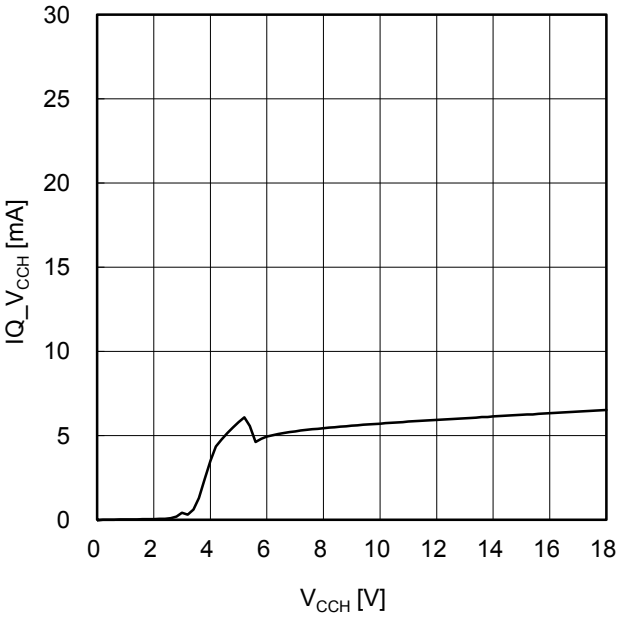


Figure 5. V_{CCH} vs. I_{Q_VCCH}
(High-Voltage mode)

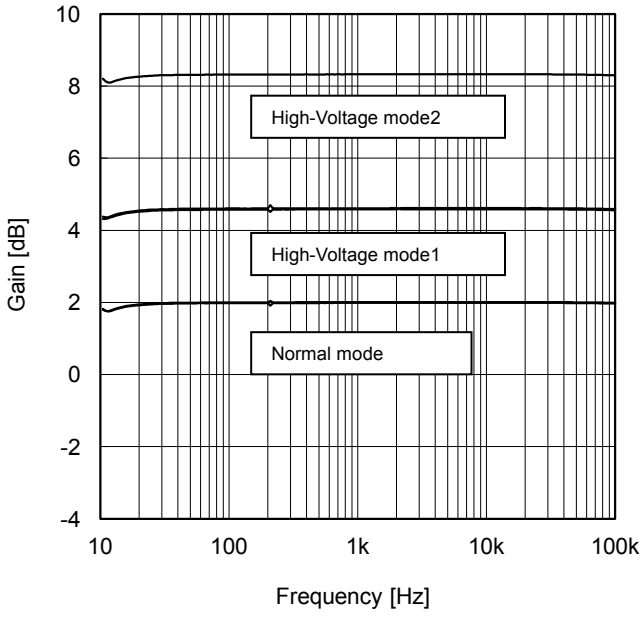


Figure 6. Gain vs. frequency
(Normal / High-Voltage mode)

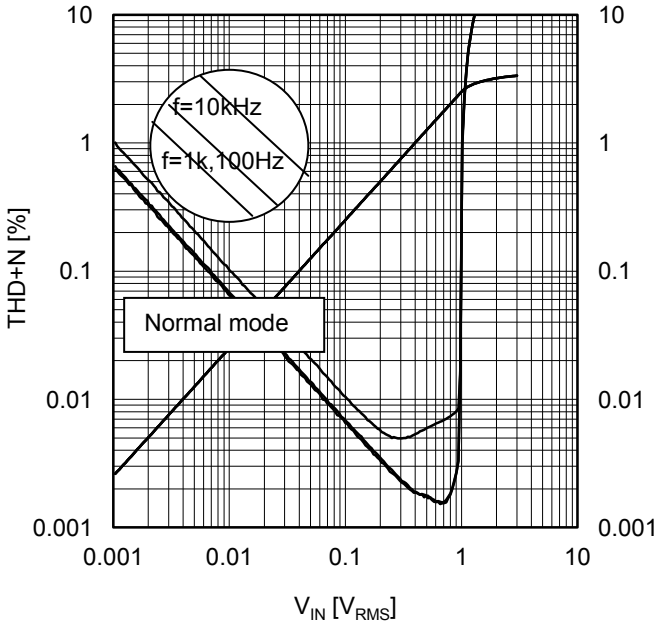


Figure 7. THD+N vs. V_{IN} / V_O
(Gain Adjust=+6dB)

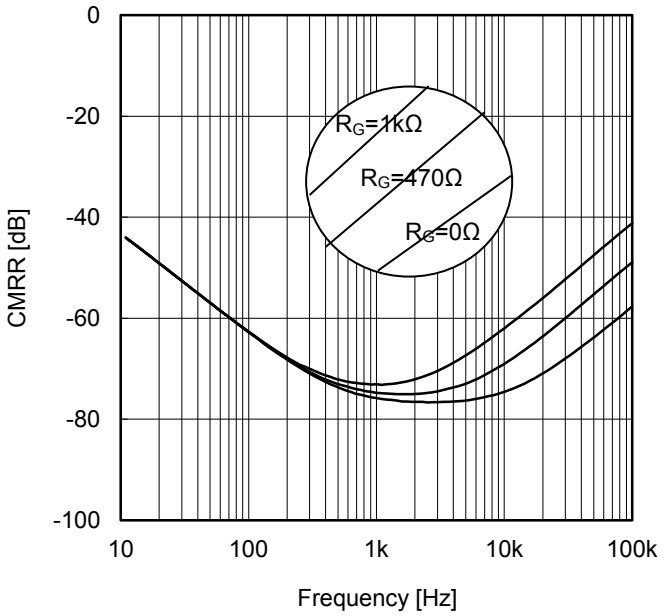


Figure 8. CMRR vs. frequency

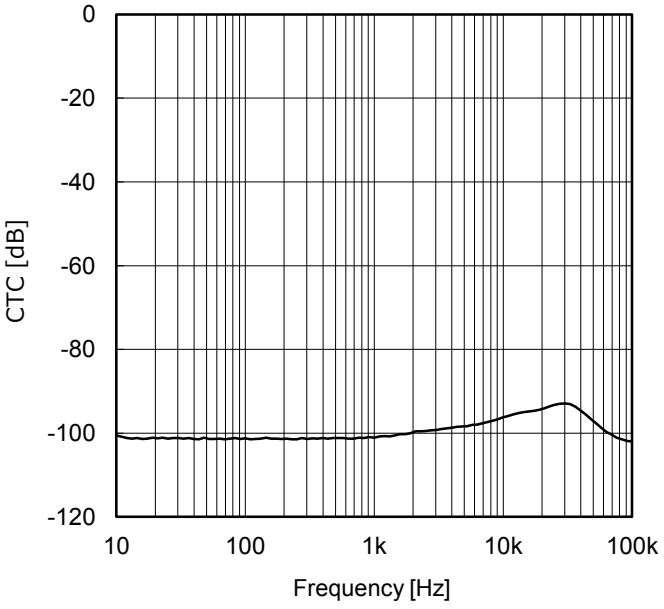


Figure 9. Crosstalk (between Channels) vs. frequency

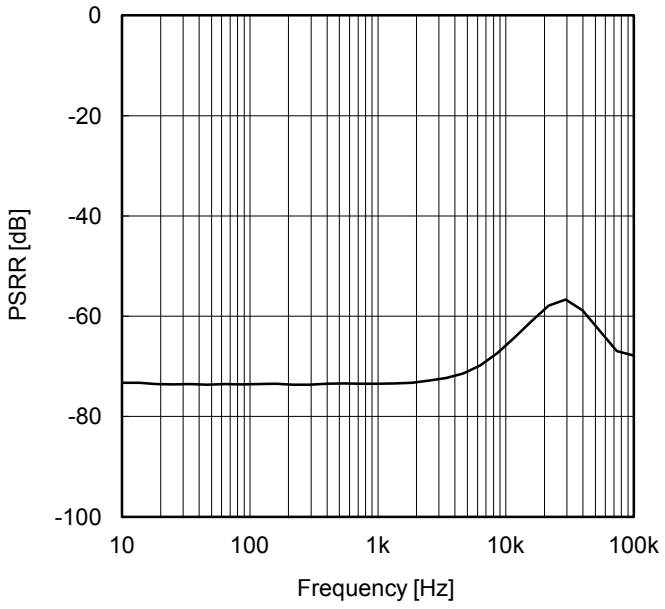


Figure 10. PSRR vs. frequency

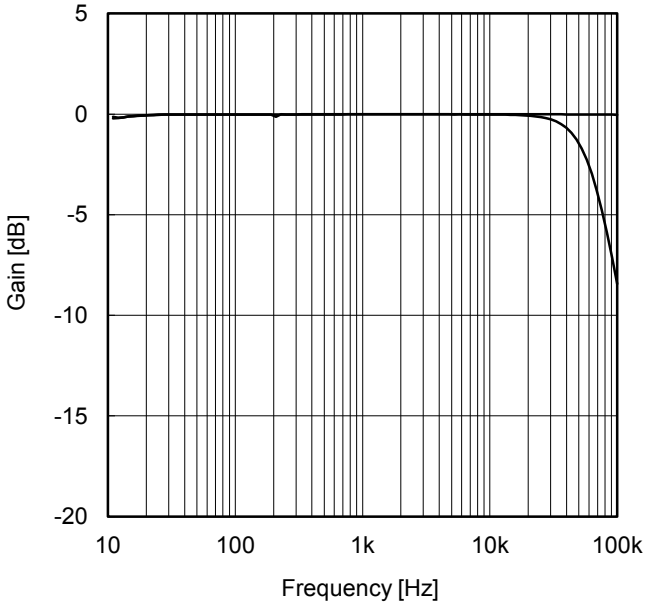


Figure 11. Gain(LPF ON/pass) vs. frequency

I²C-bus CONTROL SIGNAL SPECIFICATION

(1) Electrical specifications and timing for bus lines and I/O stages

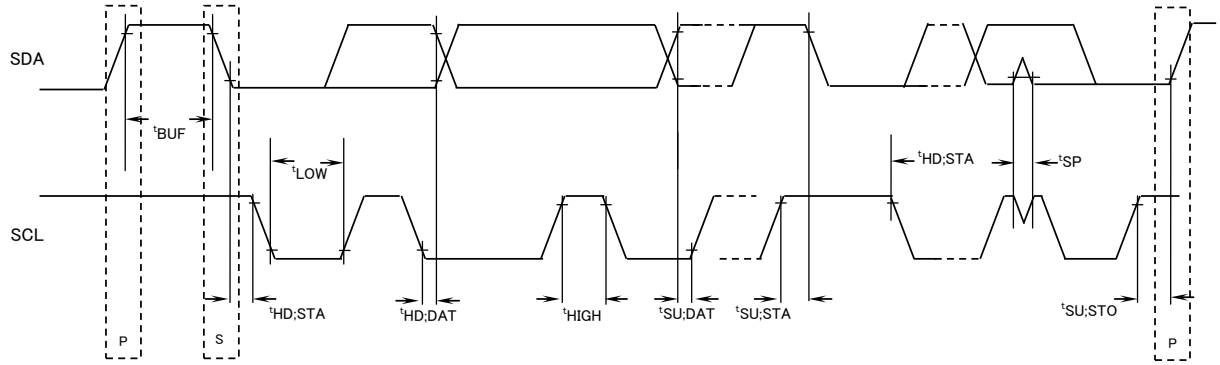


Figure 12. Definition of Timing on the I²C-bus

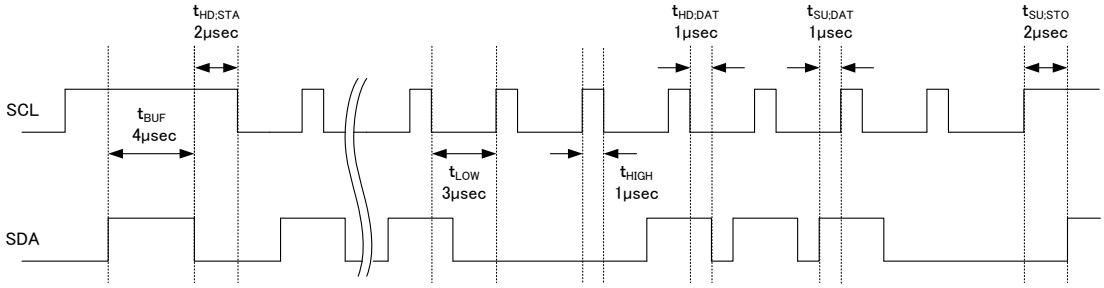
Table 1 Characteristics of the SDA and SCL bus lines for I²C-bus devices

	Parameter	Symbol	Fast-mode I²C-bus		Unit
			Min	Max	
1	SCL Clock Frequency	f_{SCL}	0	400	kHz
2	Bus Free Time between STOP and START Condition	t_{BUF}	1.3	—	µsec
3	Hold Time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	—	µsec
4	LOW Period of the SCL Clock	t_{LOW}	1.3	—	µsec
5	HIGH Period of the SCL Clock	t_{HIGH}	0.6	—	µsec
6	Set-up Time for a Repeated START Condition	$t_{SU;STA}$	0.6	—	µsec
7	Data Hold Time	$t_{HD;DAT}$	0*	—	µsec
8	Data Set-up Time	$t_{SU;DAT}$	100	—	nsec
9	Set-up Time for STOP Condition	$t_{SU;STO}$	0.6	—	µsec

All values referred to V_{IH} min. and V_{IL} max. Levels (see Table 2).

Table 2 Characteristics of the SDA and SCL I/O stages for I²C-bus devices

	Parameter	Symbol	Fast-mode I²C-bus		Unit
			Min	Max	
10	LOW level input voltage: Fixed input levels	V_{IL}	-0.5	1	V
11	HIGH level input voltage: Fixed input levels	V_{IH}	2.3	-	V
12	Pulse width of spikes, which must be suppressed by the input filter.	t_{SP}	0	50	nsec
13	LOW level output voltage (open drain or open collector): At 3mA sink current	V_{OL1}	0	0.4	V
14	Input current each I/O pin with an input voltage between 0.4V and 0.9 VDD max.	I_I	-10	10	µA



SCL clock frequency:250kHz

Figure 13. I²C-bus data transmission timing

(2) I²C-bus FORMAT

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S = Start condition (Recognition of start bit)
Slave Address = Recognition of slave address. 7 bits in upper order are optional.
The least significant bit is “L” due to write format.
A = ACKNOWLEDGE bit (Recognition of acknowledgement)
Select Address = Selection of register that contain data on volume, bass and treble settings.
Data = Data on every volume and tone to be stored in selected register.
P = Stop condition (Recognition of stop bit)

(3) I²C-bus Interface Protocol

1)Basic form

S	Slave Address	A	Select Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

2) Automatic increment (Select Address increases (+1) according to the number of data.)

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	····	DataN	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB			MSB LSB		

(Example) ① Data1 shall be set as data of address specified by Select Address.
② Data2 shall be set as data of address specified by Select Address +1.
③ DataN shall be set as data of address specified by Select Address +N-1.

3) Configuration unavailable for transmission (In this case, only Select Address1 is set.)

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

(Note)If any data is transmitted as Select Address 2 next to data,
It is recognized as data, not as Select Address 2.

(4) Slave address

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	0

(5) Select Address & Data

Items	Select Address (hex)	MSB	Data						LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Initial Setup 1	01	Advanced Switch ON/OFF	0	Advanced Switch Time of Input Gain/Fader		0	High-Voltage Mode Select	0	0
Initial Setup 2	02	0	0	Sub Selector		0	0	Rear Selector	Front Selector
Input Selector	05	0	0	0	0	Input Selector			
Input Gain	06	0	0	Input Gain					
Fader 1ch Front	28	Fader Boost Gain / Attenuation							
Fader 2ch Front	29	Fader Boost Gain / Attenuation							
Fader 1ch Rear	2A	Fader Boost Gain / Attenuation							
Fader 2ch Rear	2B	Fader Boost Gain / Attenuation							
Fader Center	2C	Fader Boost Gain / Attenuation							
Fader Subwoofer	2D	Fader Boost Gain / Attenuation							
LPF Setup Mixing ON/OFF	30	Front Mixing ON/OFF	LPF fc	0	0	0	0	Sub Gain Adjust	Main Gain Adjust
Test Mode	F0	0	0	0	0	0	0	0	0
System Reset	FE	1	0	0	0	0	0	0	1

Advanced switch

Notes on data format

1. “Advanced switch” function is available for the hatched parts on the above table.

2. In case of transferring data continuously, Select Address flows by *Automatic Increment function*, as shown below.

→ 01(hex)→02(hex)→05(hex)→06(hex)→28(hex)→29(hex)→2A(hex)→2B(hex)→2C(hex)→2D(hex)→ 30(hex)

3. Input selector that is not corresponded for “Advanced switch” function, cannot reduce the noise caused when changing the input selector. Therefore, it is recommended to turn on mute when changing these settings.

4. In case of setting to infinite “-∞” by using Fader when input selector setting is changed, please consider “Advanced switch” time.

Explanation of each Select Address

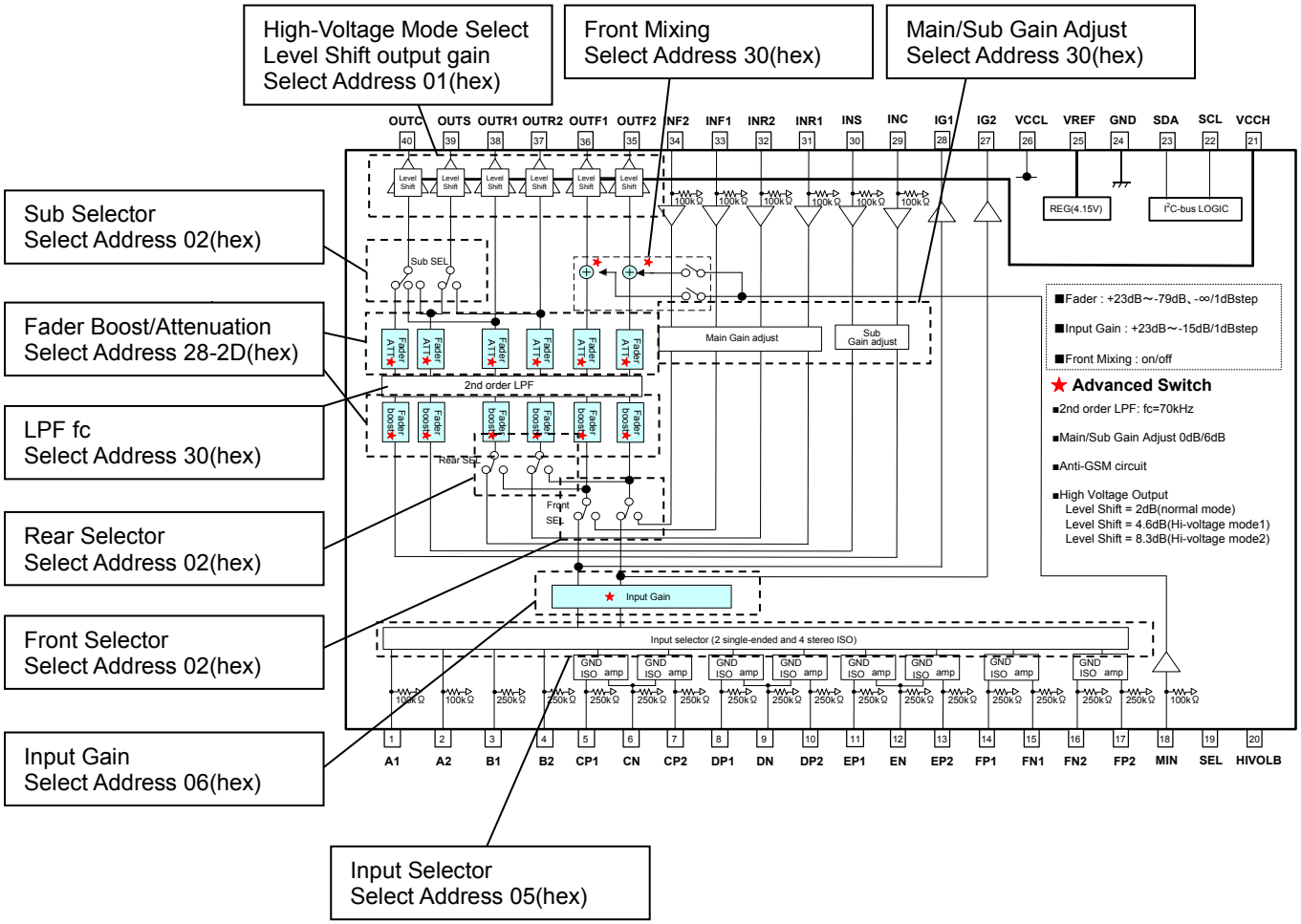


Figure 14. Block diagram for explanation of Select Address

Command Specification

Initial Condition, 1/0 Fixed value Do not send the data not designated

Select Address 01 (hex)

Mode	MSB			High-Voltage Mode Select				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
High-Voltage mode2 (+8.3dB)		0			0	0	0	0
High-Voltage mode1 (+4.6dB)						1		

Mode	MSB		Advanced Switch Time of Input Gain/Fader(Note1,2)					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
4.7 msec		0	0	0	0		0	0
7.1 msec			0	1				
11.2 msec			1	0				
14.4 msec			1	1				

(Note1) Advanced switch time is Typ value. Max value is 1.4 times of Typ value.
(Note2) If changing Advanced switch time while Advanced switch function is activated, Advance switch time is changed immediately.

Mode	MSB			Advanced Switch ON/OFF(Note3)				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0			0		0	0
ON	1							

(Note3) If Advanced switch ON/OFF is changed while Advanced switch function is activated, it will become effective from the next switching operation.

Select Address 02 (hex)

Mode	MSB			Front Selector				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Front	0	0			0	0		0
Inside Through								1

Mode	MSB			Rear Selector				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Rear	0	0			0	0	0	
Front Copy							1	

Mode(Note4)	MSB			Sub Selector				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OUTC(INS)/OUTS(INS)	0	0	0	0	0	0		
OUTC(INR1)/OUTS(INR2)			0	1				
OUTC (INC)/OUTS(INS)			1	0				
Prohibition			1	1				

(Note4) xxx(INxx) : “xxx” means “Output terminal”, “(INxx)” means “Output signal”

Command Specification

Initial Condition, 1/0 Fixed value Do not send the data not designated

Select Address 05(hex)

Mode	MSB				Input Selector			LSB
	D7	D6	D5	D4	D3	D2	D1	D0
A	0	0	0	0	0	0	0	0
B					0	0	0	1
C single					0	0	1	0
D single					0	0	1	1
E single					0	1	0	0
F single					0	1	0	1
C diff.					0	1	1	0
D diff.					0	1	1	1
E diff.					1	0	0	0
F full-diff.					1	0	0	1
Prohibition					1	0	1	0
					1	0	1	1
					:	:	:	:
					1	1	1	1

List of active input terminal when set input selector

Mode	Lch positive input terminal	Lch negative input terminal	Rch positive input terminal	Rch negative input terminal
A	1pin(A1)	-	2pin(A2)	-
B	3pin(B1)	-	4pin(B2)	-
C single	5pin(CP1)	-	7pin(CP2)	-
D single	8pin(DP1)	-	10pin(DP2)	-
E single	11pin(EP1)	-	13pin(EP2)	-
F single	14pin(FP1)	-	17pin(FP2)	-
C diff.	5pin(CP1)	6pin(CN)	7pin(CP2)	6pin(CN)
D diff.	8pin(DP1)	9pin(DN)	10pin(DP2)	9pin(DN)
E diff.	11pin(EP1)	12pin(EN)	13pin(EP2)	12pin(EN)
F full-diff.	14pin(FP1)	15pin(FN1)	17pin(FP2)	16pin(FN2)

Command Specification

Initial Condition, 1/0 Fixed value Do not send the data not designated

Select Address 06 (hex)

Mode	MSB		Input Gain					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition	0	0	0	0	0	0	0	0
			:	:	:	:	:	:
			0	0	1	0	0	0
+23dB			0	0	1	0	0	1
+22dB			0	0	1	0	1	0
+21dB			0	0	1	0	1	1
+20dB			0	0	1	1	0	0
+19dB			0	0	1	1	0	1
+18dB			0	0	1	1	1	0
+17dB			0	0	1	1	1	1
+16dB			0	1	0	0	0	0
+15dB			0	1	0	0	0	1
+14dB			0	1	0	0	1	0
+13dB			0	1	0	0	1	1
+12dB			0	1	0	1	0	0
+11dB			0	1	0	1	0	1
+10dB			0	1	0	1	1	0
+9dB			0	1	0	1	1	1
+8dB			0	1	1	0	0	0
+7dB			0	1	1	0	0	1
+6dB			0	1	1	0	1	0
+5dB			0	1	1	0	1	1
+4dB			0	1	1	1	0	0
+3dB			0	1	1	1	0	1
+2dB			0	1	1	1	1	0
+1dB			0	1	1	1	1	1
0dB			1	0	0	0	0	0
-1dB			1	0	0	0	0	1
-2dB			1	0	0	0	1	0
-3dB			1	0	0	0	1	1
-4dB			1	0	0	1	0	0
-5dB			1	0	0	1	0	1
-6dB			1	0	0	1	1	0
-7dB			1	0	0	1	1	1
-8dB			1	0	1	0	0	0
-9dB			1	0	1	0	0	1
-10dB			1	0	1	0	1	0
-11dB			1	0	1	0	1	1
-12dB			1	0	1	1	0	0
-13dB			1	0	1	1	0	1
-14dB			1	0	1	1	1	0
-15dB			1	0	1	1	1	1
Prohibition			1	1	0	0	0	0
			:	:	:	:	:	:
			1	1	1	1	1	1

Command Specification

Initial Condition, 1/0 Fixed value Do not send the data not designated

Select Address 28, 29, 2A, 2B, 2C, 2D (hex)

Boost & Attenuation	MSB		Fader Boost / Attenuation					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
	0	1	1	0	1	0	0	0
+23dB	0	1	1	0	1	0	0	1
+22dB	0	1	1	0	1	0	1	0
+21dB	0	1	1	0	1	0	1	1
・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・
+10dB	0	1	1	1	0	1	1	0
+9dB	0	1	1	1	0	1	1	1
+8dB	0	1	1	1	1	0	0	0
+7dB	0	1	1	1	1	0	0	1
+6dB	0	1	1	1	1	0	1	0
+5dB	0	1	1	1	1	0	1	1
+4dB	0	1	1	1	1	1	0	0
+3dB	0	1	1	1	1	1	0	1
+2dB	0	1	1	1	1	1	1	0
+1dB	0	1	1	1	1	1	1	1
0dB	1	0	0	0	0	0	0	0
-1dB	1	0	0	0	0	0	0	1
-2dB	1	0	0	0	0	0	1	0
-3dB	1	0	0	0	0	0	1	1
・ ・ ・ ・	・ ・ ・ ・	・ ・ ・ ・	・ ・ ・ ・	・ ・ ・ ・	・ ・ ・ ・	・ ・ ・ ・	・ ・ ・ ・	・ ・ ・ ・
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
Prohibition	1	1	0	1	0	0	0	0
	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
-∞dB	1	1	1	1	1	1	1	1

Details of Fader Boost / Attenuation

Initial Condition,

(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+23	0	1	1	0	1	0	0	1
+22	0	1	1	0	1	0	1	0
+21	0	1	1	0	1	0	1	1
+20	0	1	1	0	1	1	0	0
+19	0	1	1	0	1	1	0	1
+18	0	1	1	0	1	1	1	0
+17	0	1	1	0	1	1	1	1
+16	0	1	1	1	0	0	0	0
+15	0	1	1	1	0	0	0	1
+14	0	1	1	1	0	0	1	0
+13	0	1	1	1	0	0	1	1
+12	0	1	1	1	0	1	0	0
+11	0	1	1	1	0	1	0	1
+10	0	1	1	1	0	1	1	0
+9	0	1	1	1	0	1	1	1
+8	0	1	1	1	1	0	0	0
+7	0	1	1	1	1	0	0	1
+6	0	1	1	1	1	0	1	0
+5	0	1	1	1	1	0	1	1
+4	0	1	1	1	1	1	0	0
+3	0	1	1	1	1	1	0	1
+2	0	1	1	1	1	1	1	0
+1	0	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0	0
-1	1	0	0	0	0	0	0	1
-2	1	0	0	0	0	0	1	0
-3	1	0	0	0	0	0	1	1
-4	1	0	0	0	0	1	0	0
-5	1	0	0	0	0	1	0	1
-6	1	0	0	0	0	1	1	0
-7	1	0	0	0	0	1	1	1
-8	1	0	0	0	1	0	0	0
-9	1	0	0	0	1	0	0	1
-10	1	0	0	0	1	0	1	0
-11	1	0	0	0	1	0	1	1
-12	1	0	0	0	1	1	0	0
-13	1	0	0	0	1	1	0	1
-14	1	0	0	0	1	1	1	0
-15	1	0	0	0	1	1	1	1
-16	1	0	0	1	0	0	0	0
-17	1	0	0	1	0	0	0	1
-18	1	0	0	1	0	0	1	0
-19	1	0	0	1	0	0	1	1
-20	1	0	0	1	0	1	0	0
-21	1	0	0	1	0	1	0	1
-22	1	0	0	1	0	1	1	0
-23	1	0	0	1	0	1	1	1
-24	1	0	0	1	1	0	0	0
-25	1	0	0	1	1	0	0	1
-26	1	0	0	1	1	0	1	0
-27	1	0	0	1	1	0	1	1
-28	1	0	0	1	1	1	0	0

(dB)	D7	D6	D5	D4	D3	D2	D1	D0
-29	1	0	0	1	1	1	0	1
-30	1	0	0	1	1	1	1	0
-31	1	0	0	1	1	1	1	1
-32	1	0	1	0	0	0	0	0
-33	1	0	1	0	0	0	0	1
-34	1	0	1	0	0	0	1	0
-35	1	0	1	0	0	0	1	1
-36	1	0	1	0	0	1	0	0
-37	1	0	1	0	0	1	0	1
-38	1	0	1	0	0	1	1	0
-39	1	0	1	0	0	1	1	1
-40	1	0	1	0	1	0	0	0
-41	1	0	1	0	1	0	0	1
-42	1	0	1	0	1	0	1	0
-43	1	0	1	0	1	0	1	1
-44	1	0	1	0	1	1	0	0
-45	1	0	1	0	1	1	0	1
-46	1	0	1	0	1	1	1	0
-47	1	0	1	0	1	1	1	1
-48	1	0	1	1	0	0	0	0
-49	1	0	1	1	0	0	0	1
-50	1	0	1	1	0	0	1	0
-51	1	0	1	1	0	0	1	1
-52	1	0	1	1	0	1	0	0
-53	1	0	1	1	0	1	0	1
-54	1	0	1	1	0	1	1	0
-55	1	0	1	1	0	1	1	1
-56	1	0	1	1	1	0	0	0
-57	1	0	1	1	1	0	0	1
-58	1	0	1	1	1	0	1	0
-59	1	0	1	1	1	0	1	1
-60	1	0	1	1	1	1	0	0
-61	1	0	1	1	1	1	0	1
-62	1	0	1	1	1	1	1	0
-63	1	0	1	1	1	1	1	1
-64	1	1	0	0	0	0	0	0
-65	1	1	0	0	0	0	0	1
-66	1	1	0	0	0	0	1	0
-67	1	1	0	0	0	0	1	1
-68	1	1	0	0	0	1	0	0
-69	1	1	0	0	0	1	0	1
-70	1	1	0	0	0	1	1	0
-71	1	1	0	0	0	1	1	1
-72	1	1	0	0	1	0	0	0
-73	1	1	0	0	1	0	0	1
-74	1	1	0	0	1	0	1	0
-75	1	1	0	0	1	0	1	1
-76	1	1	0	0	1	1	0	0
-77	1	1	0	0	1	1	0	1
-78	1	1	0	0	1	1	1	0
-79	1	1	0	0	1	1	1	1
-∞	1	1	1	1	1	1	1	1

Command Specification

Initial Condition, 1/0 Fixed value Do not send the data not designated

Select Address 30(hex)

Mode	MSB			Main Gain Adjust				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB			0	0	0	0		0
+6dB								1

Mode	MSB			Sub Gain Adjust				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB			0	0	0	0	0	
+6dB							1	

Mode	MSB			LPF fc				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
70kHz		0	0	0	0	0		
PASS		1						

Mode	MSB			Front Mixing ON/OFF				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0		0	0	0	0		
ON	1							

(6) About power on reset

It is possible for the reset circuit inside the IC to initialize when supply voltage is turned on. Please send data to all address as initial data when the supply is turned on, and turn on mute until all initial data are sent.

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Rise time of VCCL	t_{RISE}	250	—	—	μsec	V_{CCL} rise time to 5V
VCCL voltage of release power on reset	V_{POR}	—	4.1	—	V	

(7) About start-up and power off sequence on IC

By setting the terminal voltage of HIVOLB and SEL, it is possible to change the output gain.
At the same time, output DC voltage will also be changed at each mode.

HIVOLB Terminal Voltage	High-Voltage
GND to 1.0V	ON
2.3V to VCCL	OFF

SEL Terminal Voltage	High-Voltage mode
GND to 0.5V	High-Voltage mode1
1.5V to VCCL	High-Voltage mode2

Please set HIVOLB terminal voltage between the ranges showed by the above tables. If HIVOLB terminal is open, the terminal voltage will be set to 5V due to the pull-up voltage inside the IC. In this case, the IC will be set to “High-Voltage OFF” mode. SEL terminal is 4.15V due to the pull-up voltage inside the IC.
Output DC voltage and Output gain, that are changed by the combination of “HIVOLB” terminal and “SEL” terminal shows as the following table.

VCCH Supplied Voltage	9 V		11.5 V	17 V
HIVOLB Terminal Voltage	5 V (High-Voltage OFF)		0V (High-Voltage ON)	
SEL Terminal Voltage	0V (High-Voltage mode1)	Open (4.15 V) (High-Voltage mode2)	0 V (High-Voltage mode1)	Open (4.15 V) (High-Voltage mode2)
Output DC Bias Voltage	4.35 V		5.6 V	8.35 V
Level Shift Output gain	2 dB		4.6 dB	8.3 dB

If HIVOLB terminal voltage is changed during its operation, Output DC voltage will be also changed shown as above. For reducing these variations, turn the power on after setting the status of the HIVOLB and SEL terminal according to the output gain. The start-up and power off sequence is shown next.

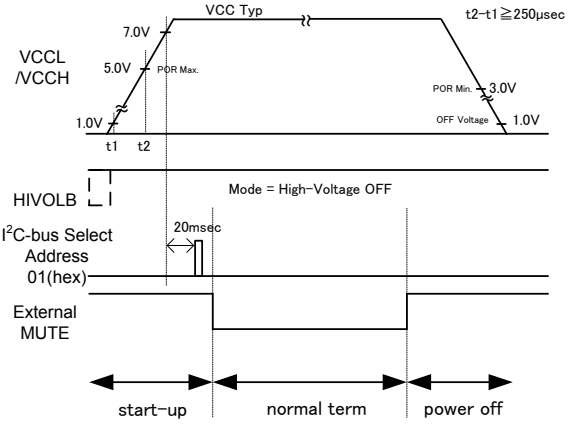


Figure 15. Normal mode(High-Voltage OFF) operation

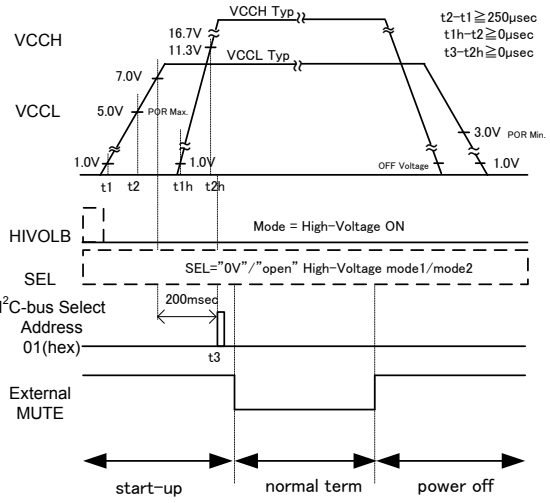


Figure 16. High-Voltage mode operation
(High-Voltage mode1 and mode2 common)

HIVOLB in the figure above is used to select the Output gain. This IC will become active-state by sending data of Select Address 01(hex) on I^2C-bus after 20msec from that VCCL reaches over 7.0V. High-Voltage Output gain is selected by setting SEL terminal voltage and sending I^2C-bus data. Therefore, this command must always be sent in the start-up sequence. In addition, “External MUTE” in the figure above is the recommended period that the muting is activated from outside the IC. In addition, the starting sequence of VCCL and VCCH does not have the limit, but please start VCCL earlier to reduce a pop noise.

For HIVOLB terminal, there is countermeasure taken for protection from voltage spikes. But, please take care that the output DC voltage may fluctuate, if the period of voltage spike is over 50nsec.

(8) About relations of power supply voltage and the DC-bias voltage

Output DC-bias voltage is decided by the regulator that is embedded in this IC, DC-bias does not fluctuate up to a constant level even if power supply voltage is lowered. The following graphs show the relationship between DC-bias voltage and power supply voltage.

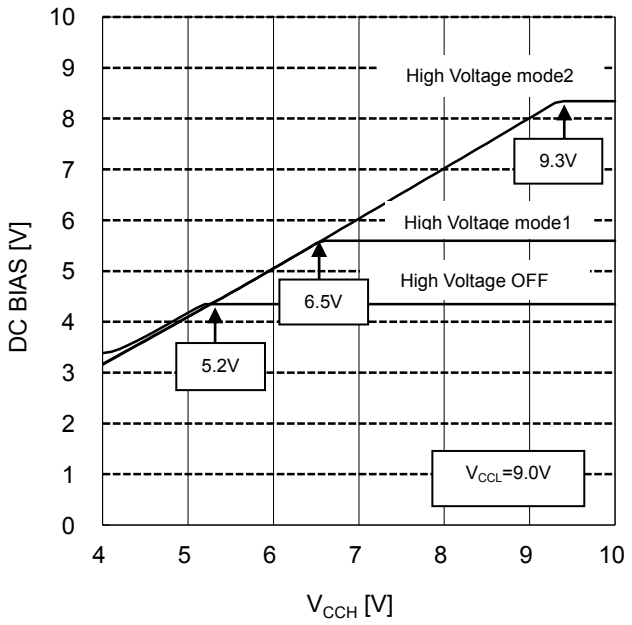


Figure 17. V_{CCH} vs DC Bias

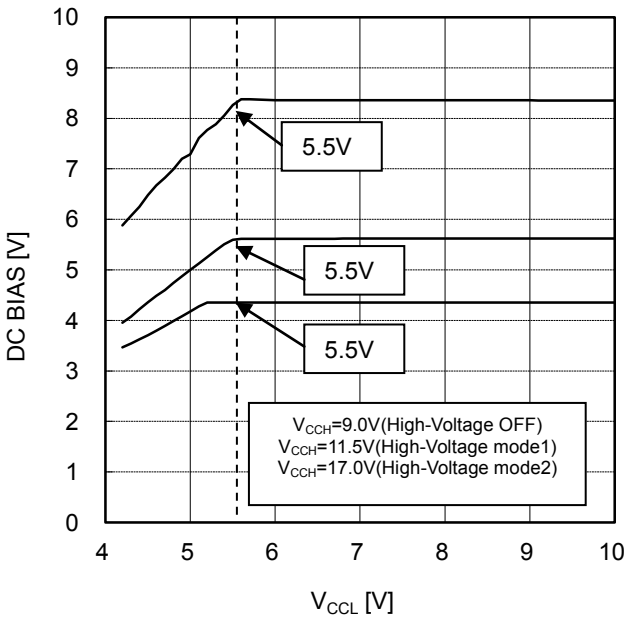


Figure 18. V_{CCL} vs DC Bias

About advanced switch circuit

【1】Advanced switch technology
1-1. Advanced switch effects

Advanced switch technology is ROHM original technology that can prevent from switching pop noise. If changing the gain setting (for example Fader) immediatery, the audible signal will become discontinuously and pop noise will be occured. This Advanced switch technology will prevent this discontinuous signal by completing the signal waveform and will significantly reduce the noise.

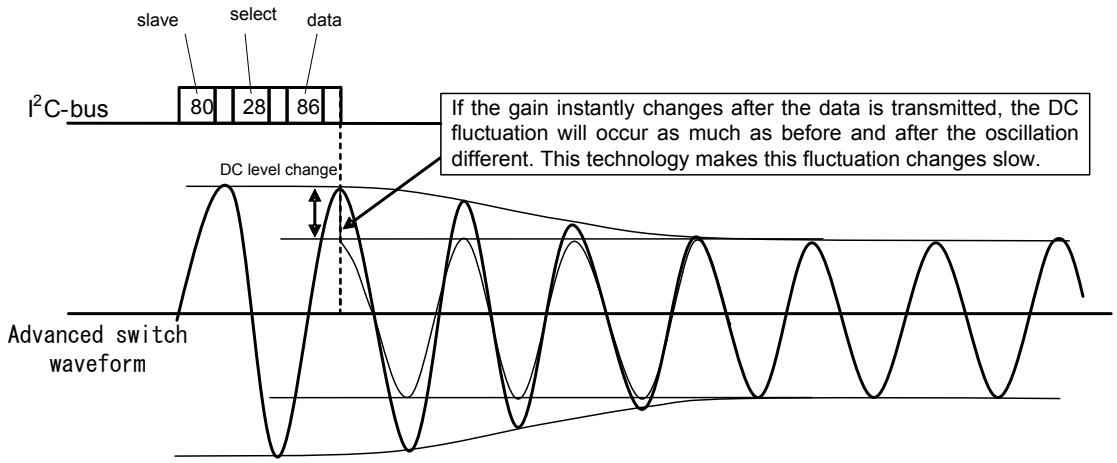


Figure 19. Advanced switch waveform

This Advanced switch circuit will start operating when the data is transmitted from microcontroller.
Advanced switch waveform is shown as the figure above. For preventing switching noise, This IC will operate optimally by internal processing after the data is transmitted from microcontroller.

However, sometimes the switching waveform is not like the intended form depends on the transmission timing. Therefore, below is the example of the relationship between the transmission timing and actual switching time. Please consider this relationship for the setting.

1-2. The kind of the Transferring Data

・Data setting that is not corresponded to Advanced switch
((5)Select Address & data Data format without hatching)
There is no particular rule about transferring data.

・Data setting that is corresponded to Advanced switch (Note1)
((5)Select Address & data Data format with hatching)
There is no particular rule about transferring data, but Advanced switch must follow the switching sequence as mentioned in【2】as follows.

(Note1) The blocks that are corresponded Advanced switch are “Input Gain”, “Fader” and ”Front Mixing ON/OFF” (In detail, please refer to (5) Select Address & data).

【2】Data transmission that is corresponded to Advanced switch

2-1. Switching time of Advanced switch

Switching time includes [Twait(Wait time)], [Tsft(A→B switching time)] and [Tsft(B→A switching time)]. 25msec is needed per 1 switching. (Tsoft = Twait + 2 * Tsft, Twait=2.3msec, Tsft=11.2msec)

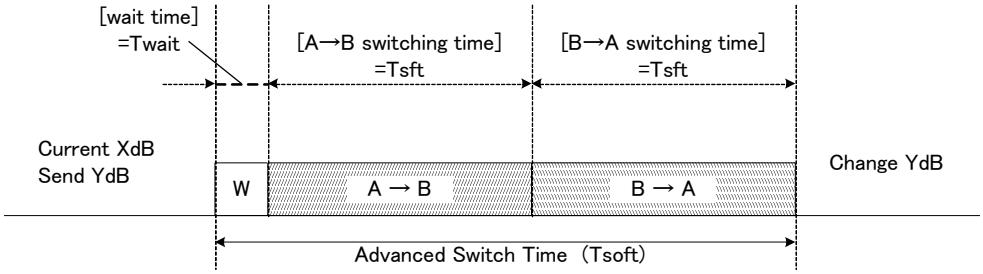


Figure 20. About Advanced switching time

In the figure above, Start/Stop state is expressed as “A” and temporary state is expressed as “B”.
The switching sequence of Advanced switch consists of the cycle “A(start)→B(temporary)→A(stop)”. Therefore, switching sequence will not stop at B state.
For example, switching is performed from A(Initial gain)→B(set gain)→A(set gain) when switching from initial gain to set gain. And switching time (Tsft) of A→B or B→A are equal.

2-2. Explanation on data transmission’s timing and switching operation.

The following examples show the timing chart from data transmission to starting of switching.
Definition of example expression :
F1=Fader 1ch Front, F2=Fader 2ch Front, R1=Fader 1ch Rear, R2=Fader 2ch Rear
C=Fader Center, S=Fader Subwoofer, MIX=Front Mixing

■ Transmission example 1
This is an example when transmitting data in same block with “enough interval for data transmission”.
(enough interval for data transmission : 1.4 x Tsoft * ”1.4” includes tolerance margin.)

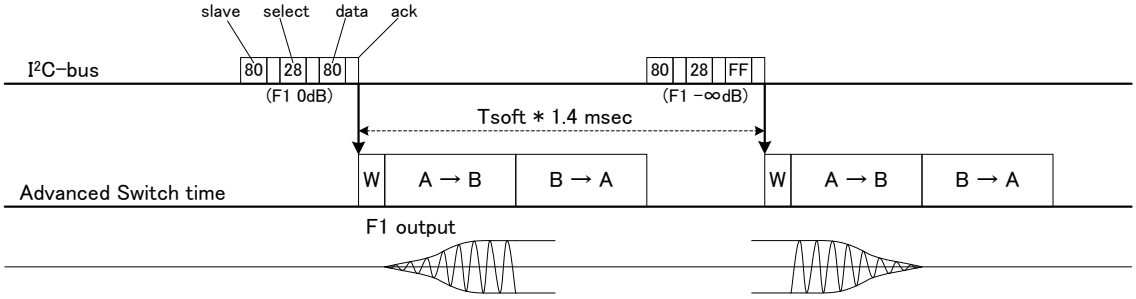


Figure 21. Transmission example 1

■ Transmission example 2
■ This is an example when the transmission interval is not enough (smaller than “Transmission example 1”).
■ When the data is transmitted during first switching operation, the second data will be reflected after the first switching operation. In this case, there is no wait time (Twait) before the second switching operation.

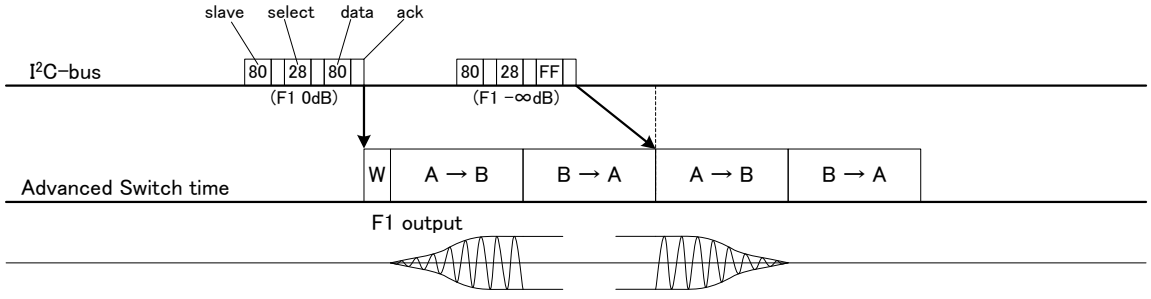


Figure 22. Transmission example 2

■ Transmission example 3
This is an example when transmission interval is smaller than “Transmission example 2”).
When the data is transmitted during the first switching operation, and transmission timing is just during A→B switching operation, the second data will be reflected at B→A switching term in case of Fader.

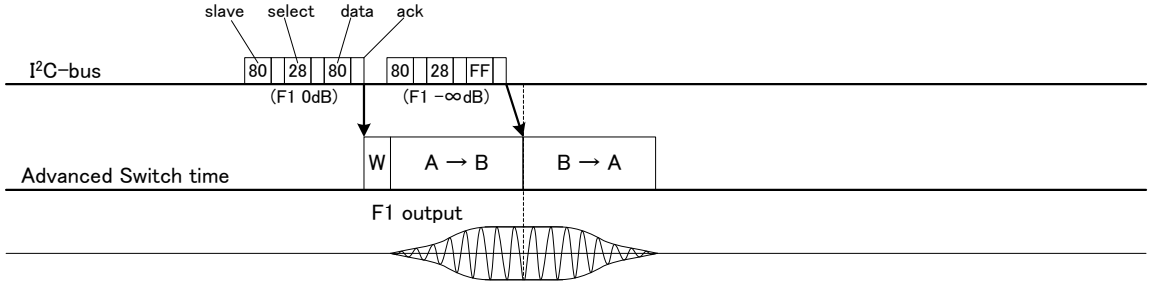


Figure 23. Transmission example 3

Please take care as follows when transmitting data to multiple channels.
It is possible that Lch and Rch in same block(Front/Rear/Center,Subwoofer) can be switched at the same timing.
For example, if the data transmission is set as the figure below, F1 and F2 can be switched at the same timing.
(Data ①is sent for F1 (Lch) and data ②is sent for F2 (Rch).)
Twait (designed to 2.3 msec) is the wait time for starting switching.
Twait may change from 1.2msec (Min.) to 4.6msec (Max.) by considering tolerance margin.

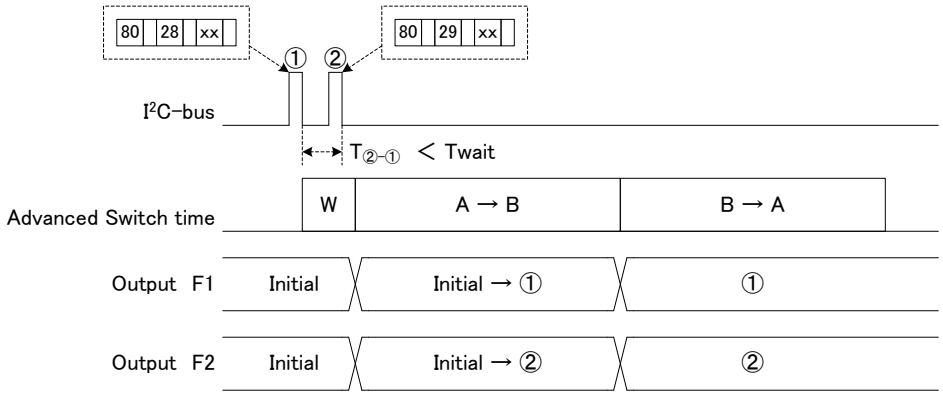


Figure 24. The operation during multi-channels (Lch, Rch) data transmission (smaller than Twait interval).

Next, if data ②is not transmitted during the Twait, the switching operation will be as the figure below.

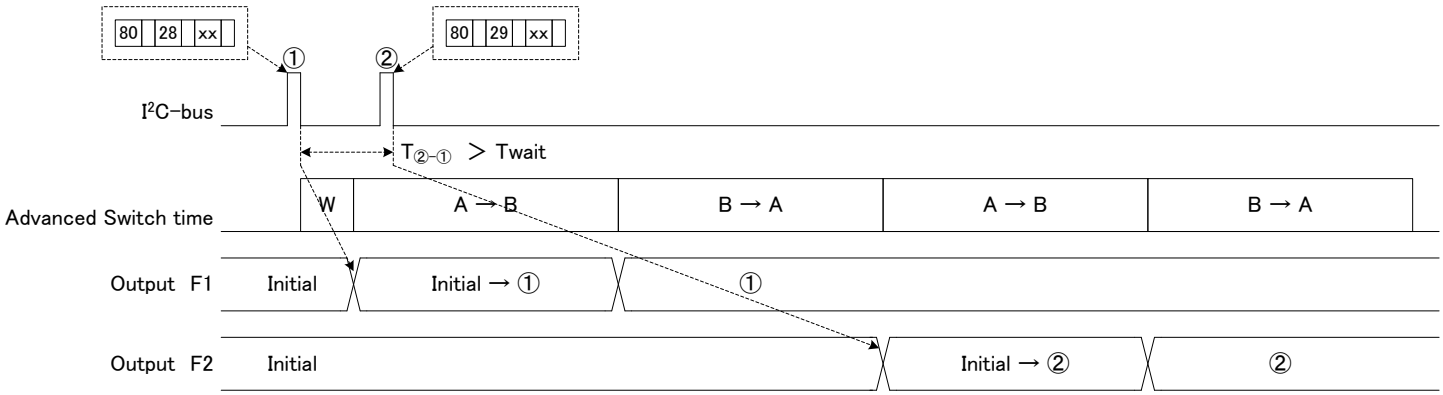


Figure 25. The operation during multiple channels (Lch, Rch) data transmission (larger than Twait interval).