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Sound Processor with Built-in 2-band Equalizer

BD37522FS

General Description

BD37522FS is a sound processor with built-in 2-band equalizer for car audio. Other features are stereo 5ch input selector, input-gain control, main volume, loudness and a 4ch fader volume. It is equipped with an “Advanced switch circuit”, which is an original ROHM technology, that reduces various switching noise (ex. No-signal, low frequency like 20Hz & large signal inputs).The “Advanced switch” makes controlling of microcomputer easier and can be used for designing high quality car audio systems.

Features

- Reduced switching noise of input gain control, mute, main volume, fader volume, bass, treble, and loudness by using advanced switch circuit.
- Built-in 1 differential input selector and 4 single-ended input selectors
- Built-in ground isolation amplifier inputs which is ideal for external stereo input.
- Built-in input gain controller which reduces switching noise for volume of a portable audio input.
- Lesser number of external components due to built-in 2-band equalizer filter and loudness filter. These make it possible to control Q, Gv, fo of 2-band equalizer, and Gv of loudness by I^2C BUS
- A gain adjustment quantity of ±20dB with a 1 dB step gain adjustment is possible for the bass, middle, and treble.
- Energy-saving design resulting in low current consumption is achieved by utilizing the BiCMOS process. It has the advantage in quality over scaling down the power heat control of the internal regulators.
- Input pins and output pins are organized and separately laid out to keep the signal flow in one direction which consequently, simplify pattern layout of the set board and decrease the board dimensions.
- It is possible to be controlled by a 3.3V / 5V I^2C BUS

Key Specifications

- Power Supply Voltage Range: 7.0V to 9.5V
- Circuit Current (No Signal): 38mA(Typ)
- Total Harmonic Distortion: 0.001%(Typ)
- Maximum Input Voltage: 2.3Vrms(Typ)
- Crosstalk Between Selectors: -100dB(Typ)
- Volume Control Range: +15dB to -79dB
- Output Noise Voltage: 3.8µVrms(Typ)
- Residual Output Noise Voltage: 1.8µVrms (Typ)
- Operating Temperature Range: -40°C to +85°C

Package

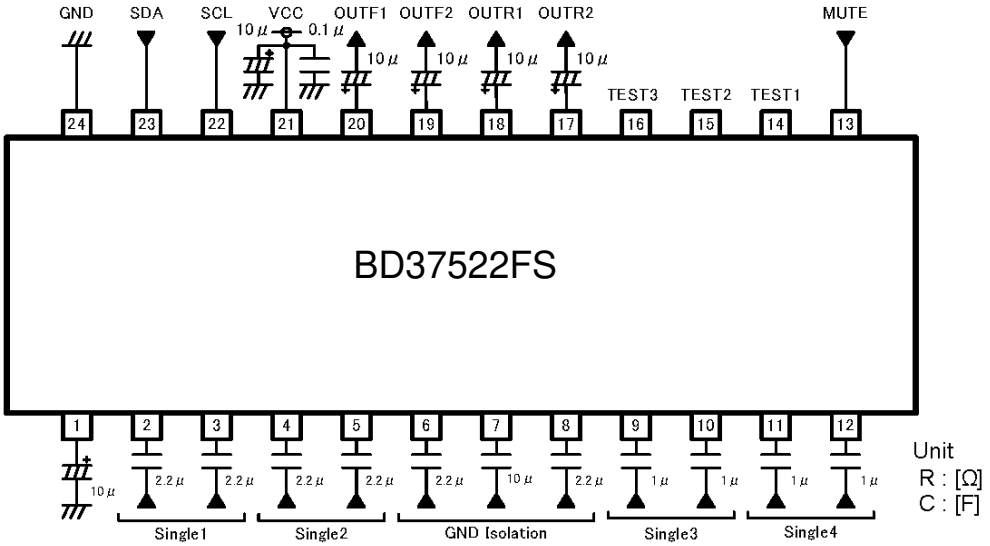
W(Typ) x D(Typ) x H(Max)

SSOP-A24
10.00mm x 7.80mm x 2.10mm

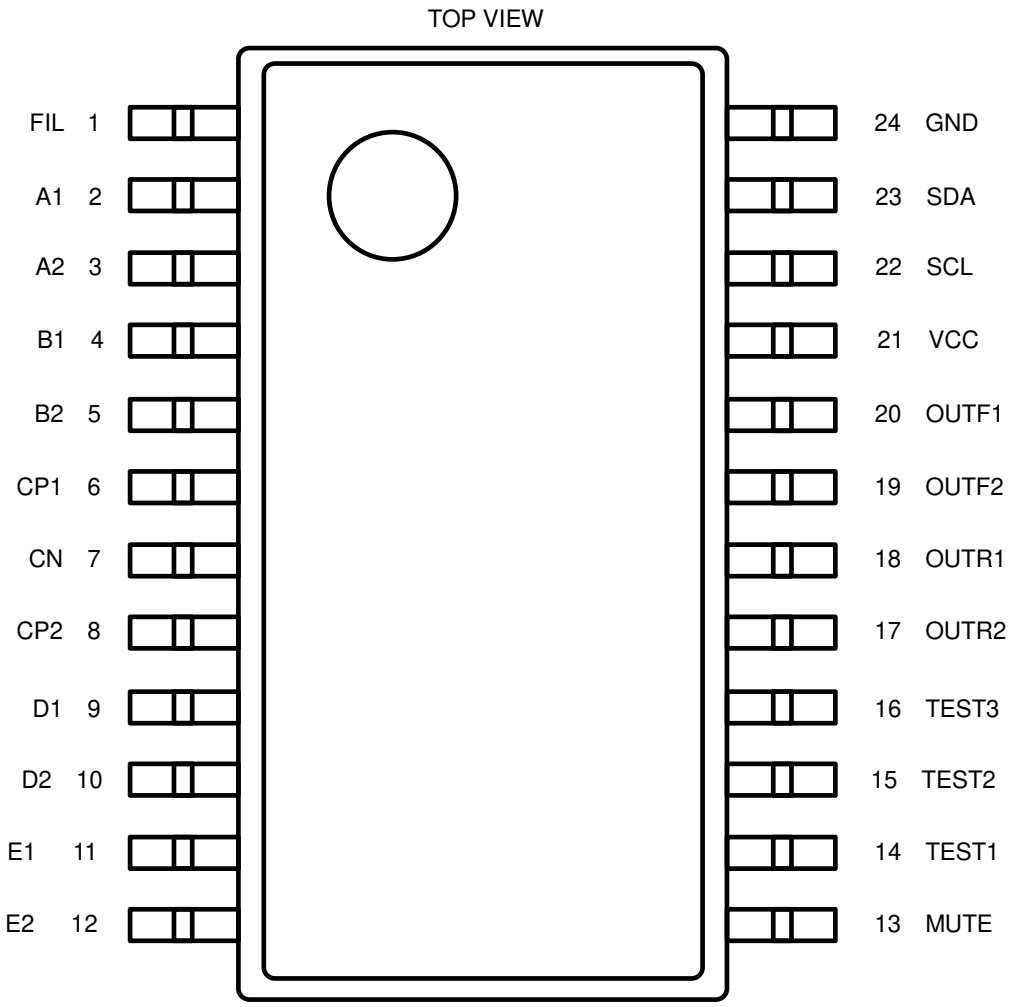
Applications

It is optimal for car audio systems. It can also be used for audio equipment like mini Compo, micro Compo, TV etc.

Typical Application Circuit



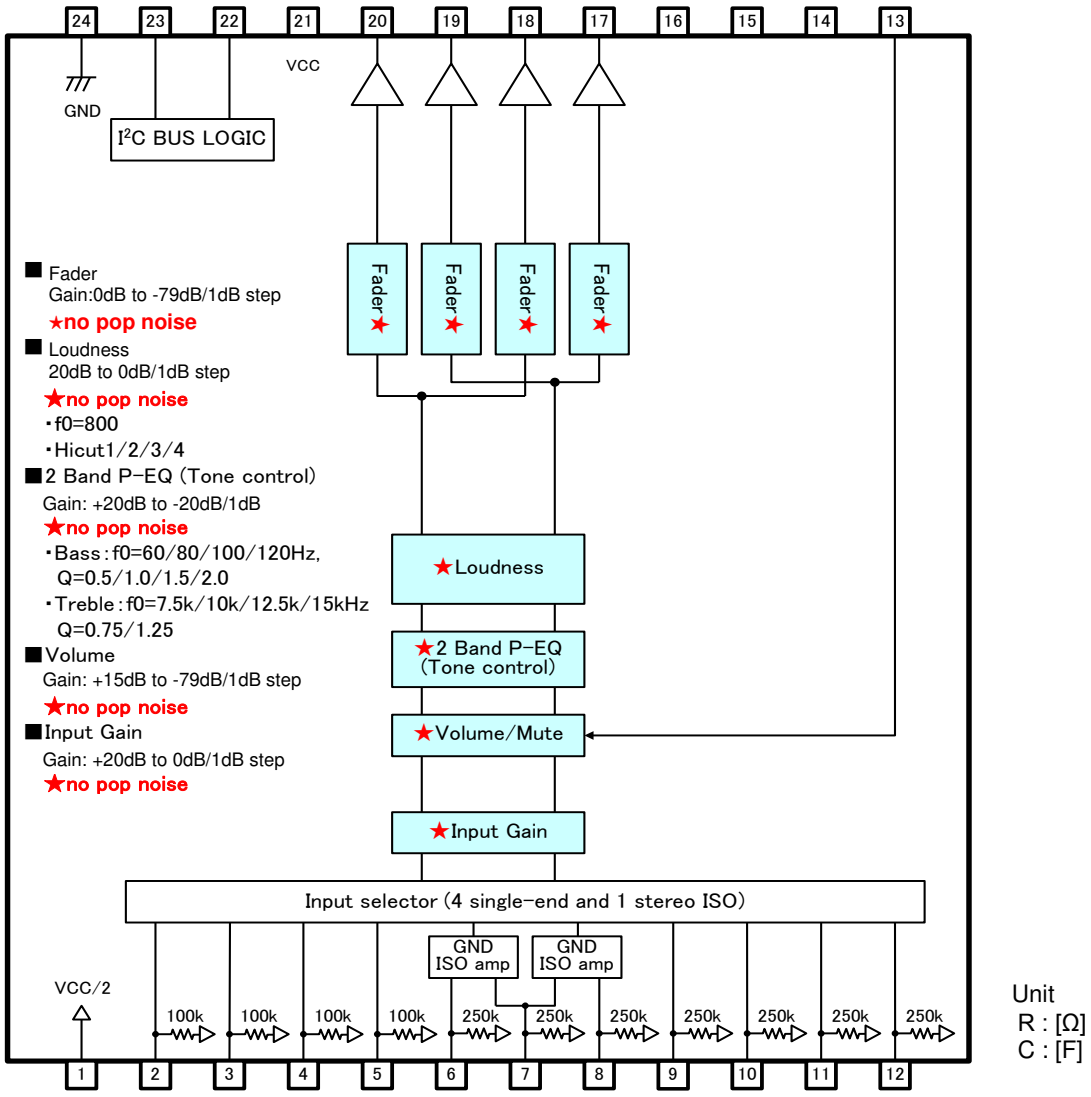
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	FIL	VCC/2 terminal	13	MUTE	External compulsory mute terminal
2	A1	A input terminal of 1ch	14	TEST1	Test Pin
3	A2	A input terminal of 2ch	15	TEST2	Test Pin
4	B1	B input terminal of 1ch	16	TEST3	Test Pin
5	B2	B input terminal of 2ch	17	OUTR2	Rear output terminal of 2ch
6	CP1	C positive input terminal of 1ch	18	OUTR1	Rear output terminal of 1ch
7	CN	C negative input terminal	19	OUTF2	Front output terminal of 2ch
8	CP2	C positive input terminal of 2ch	20	OUTF1	Front output terminal of 1ch
9	D1	D input terminal of 1ch	21	VCC	Power supply terminal
10	D2	D input terminal of 2ch	22	SCL	I²C Communication clock terminal
11	E1	E input terminal of 1ch	23	SDA	I²C Communication data terminal
12	E2	E input terminal of 2ch	24	GND	GND terminal

Block Diagram



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	10.0	V
Input Voltage	V_{IN}	V_{CC}+0.3 to GND-0.3	V
Power Dissipation	Pd	1 (Note)	W
Storage Temperature	Tstg	-55 to +150	°C

(Note) When mounted on standard board (70 x 70 x 1.6(mm^3)), derate by 8mW/°C for Ta above 25°C.
Thermal resistance θja = 125(°C/W)
Material : A FR4 grass epoxy board(3% or less of copper foil area)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	-	9.5	V
Temperature	Topr	-40	-	+85	°C

Electrical Characteristics

(Unless otherwise noted, Ta=25°C, V_{CC}=8.5V, f=1kHz, V_{IN} =1Vrms, Rg=600Ω, R_L=10kΩ, A1 input, Input gain 0dB, Mute OFF, Volume 0dB, Tone control 0dB, Loudness 0dB, Fader 0dB)

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
GENERAL	Circuit Current (No Signal)	I_Q	-	38	48	mA	No signal
	Voltage Gain	G_V	-1.5	0	+1.5	dB	G_V=20log(V_{OUT}/V_{IN})
	Channel Balance	CB	-1.5	0	+1.5	dB	CB = G_{V1}-G_{V2}
	Total Harmonic Distortion 1 (FRONT,REAR)	THD+N1	-	0.001	0.05	%	V_{OUT}=1Vrms BW=400Hz-30KHz
	Output Noise Voltage 1 (FRONT,REAR) *	V_{NO1}	-	3.8	15	μVrms	Rg = 0Ω BW = IHF-A
	Residual Output Noise Voltage *	V_{NOR}	-	1.8	10	μVrms	Fader = -∞db Rg = 0Ω BW = IHF-A
	Crosstalk Between Channels *	CTC	-	-100	-90	dB	Rg = 0Ω CTC=20log(V_{OUT}/V_{IN}) BW = IHF-A
	Ripple Rejection	RR	-	-70	-40	dB	f=1kHz V_{RR}=100mVrms RR=20log(V_{CC} IN/V_{OUT})
INPUT SELECTOR	Input Impedance(A, B)	R_{IN_S}	70	100	130	kΩ	
	Input Impedance (C,D,E)	R_{IN_D}	175	250	325	kΩ	
	Maximum Input Voltage	V_{IM}	2.1	2.3	-	Vrms	V_{IM} at THD+N(V_{OUT})=1% BW=400Hz-30KHz
	Crosstalk Between Selectors *	CTS	-	-100	-90	dB	Rg = 0Ω CTS=20log(V_{OUT}/V_{IN}) BW = IHF-A
	Common Mode Rejection Ratio *	CMRR	50	65	-	dB	CP1 and CN input CP2 and CN input CMRR=20log(V_{IN}/V_{OUT}) BW = IHF-A
INPUT GAIN	Minimum Input Gain	G_{IN_MIN}	-2	0	+2	dB	Input gain 0dB V_{IN}=100mVrms G_{IN}=20log(V_{OUT}/V_{IN})
	Maximum Input Gain	G_{IN_MAX}	+18	+20	+22	dB	Input gain +20dB V_{IN}=100mVrms G_{IN}=20log(V_{OUT}/V_{IN})
	Gain Set Error	G_{IN_ERR}	-2	0	+2	dB	GAIN=+20dB to +1dB
MUTE	Mute Attenuation *	G_{MUTE}	-	-105	-85	dB	Mute ON G_{MUTE}=20log(V_{OUT}/V_{IN}) BW = IHF-A

Electrical Characteristics - continued

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
VOLUME	Maximum Gain	G_{V_MAX}	+13	+15	+17	dB	Volume = +15dB V_{IN}=100mVrms G_V=20log(V_{OUT}/V_{IN})
	Maximum Attenuation *	G_{V_MIN}	-	-100	-85	dB	Volume = -∞dB G_V=20log(V_{OUT}/V_{IN}) BW = IHF-A
	Attenuation Set Error 1	G_{V_ERR1}	-2	0	+2	dB	GAIN & ATT=+15dB to -15dB
	Attenuation Set Error 2	G_{V_ERR2}	-3	0	+3	dB	ATT=-16dB to -47dB
	Attenuation Set Error 3	G_{V_ERR3}	-4	0	+4	dB	ATT=-48dB to -79dB
BASS	Maximum Boost Gain	G_{B_BST}	18	20	22	dB	GAIN=+20dB f=100Hz V_{IN}=100mVrms G_B=20log (V_{OUT}/V_{IN})
	Maximum Cut Gain	G_{B_CUT}	-22	-20	-18	dB	GAIN=-20dB f=100Hz V_{IN}=2Vrms G_B=20log (V_{OUT}/V_{IN})
	Gain Set Error	G_{B_ERR}	-2	0	+2	dB	Gain=+20dB to -20dB f=100Hz
TREBLE	Maximum Boost Gain	G_{T_BST}	17	20	23	dB	Gain=+20dB f=10kHz V_{IN}=100mVrms G_T=20log (V_{OUT}/V_{IN})
	Maximum Cut Gain	G_{T_CUT}	-23	-20	-17	dB	Gain=-20dB f=10kHz V_{IN}=2Vrms G_T=20log (V_{OUT}/V_{IN})
	Gain Set Error	G_{T_ERR}	-2	0	+2	dB	Gain=+20dB to -20dB f=10kHz
FADER / SUBWOOFER	Maximum Attenuation *	G_{F_MIN}	-	-100	-90	dB	Fader = -∞dB G_F=20log(V_{OUT}/V_{IN}) BW = IHF-A
	Attenuation Set Error 1	G_{F_ERR1}	-2	0	+2	dB	ATT=-1dB to -15dB
	Attenuation Set Error 2	G_{F_ERR2}	-3	0	+3	dB	ATT=-16dB to -47dB
	Attenuation Set Error 3	G_{F_ERR3}	-4	0	+4	dB	ATT=-48dB to -79dB
	Output Impedance	R_{OUT}	-	-	50	Ω	V_{IN} =100mVrms
	Maximum Output Voltage	V_{OM}	2	2.2	-	Vrms	THD+N=1% BW=400Hz-30KHz
LOUDNESS	Maximum Gain	G_{L_MAX}	17	20	23	dB	Gain 20dB V_{IN}=100mVrms G_L=20log(V_{OUT}/V_{IN})
	Gain Set Error	G_{L_ERR}	-2	0	+2	dB	GAIN=+20dB to +1dB

VP-9690A(Average value detection, effective value display) filter by Matsushita Communication is used for * measurement.
Phase between input / output is same.

Typical Performance Curves

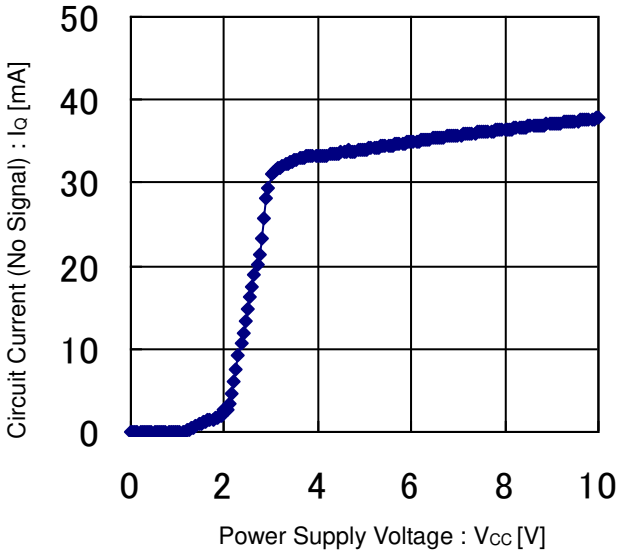


Figure 1. Circuit Current (No Signal) vs Power Supply Voltage

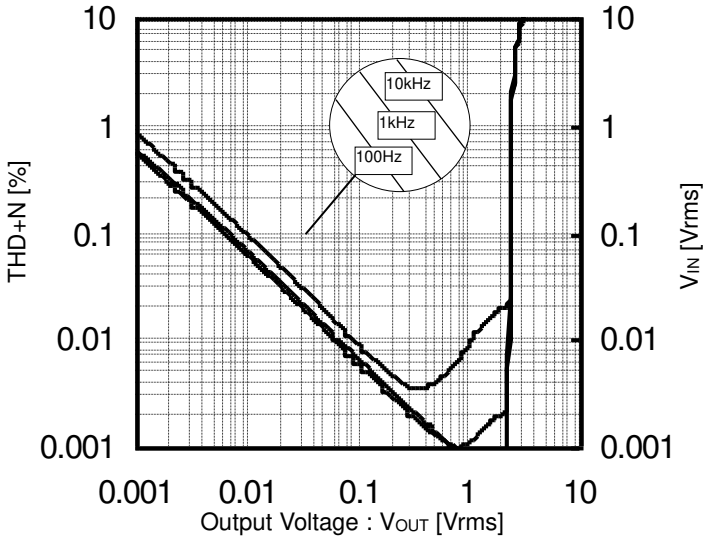


Figure 2. THD+N vs Output Voltage

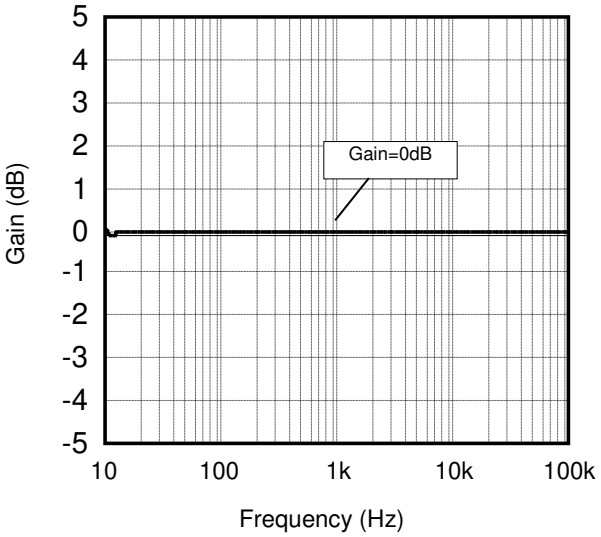


Figure 3. Gain vs Frequency

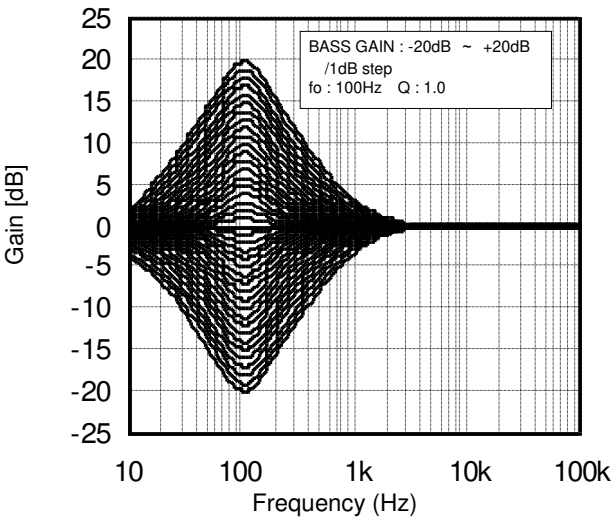


Figure 4. Bass Gain vs Frequency

Typical Performance Curves – continued

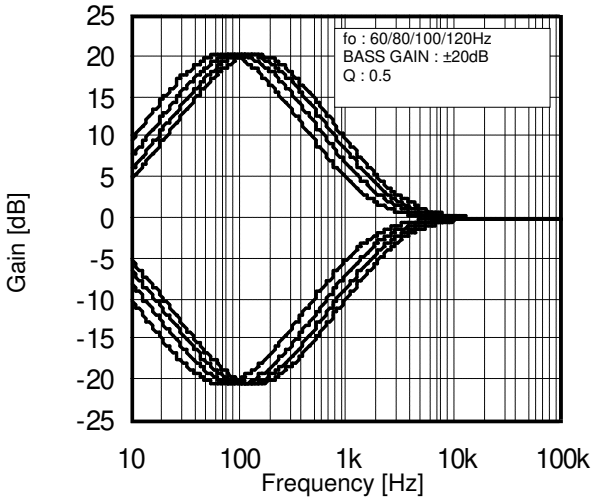


Figure 5. Bass fo vs Frequency

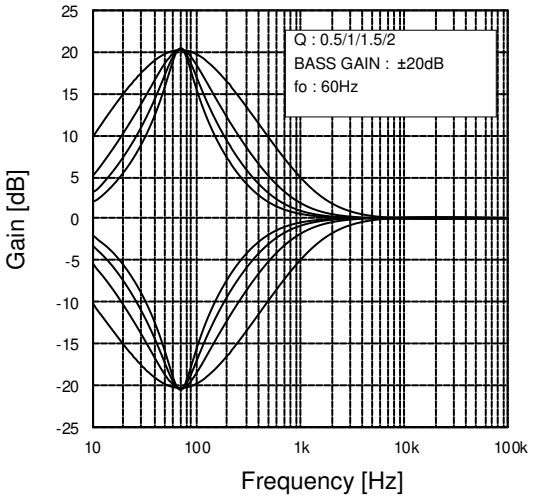


Figure 6. Bass Q vs Frequency

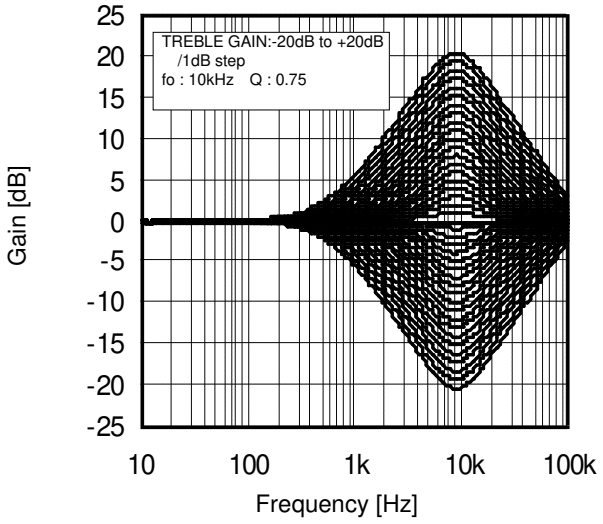


Figure 7. Treble Gain vs Frequency

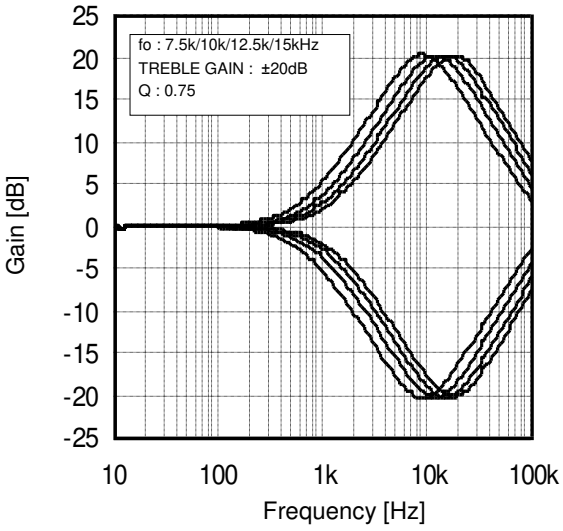


Figure 8 Treble fo vs Frequency

Typical Performance Curves - continued

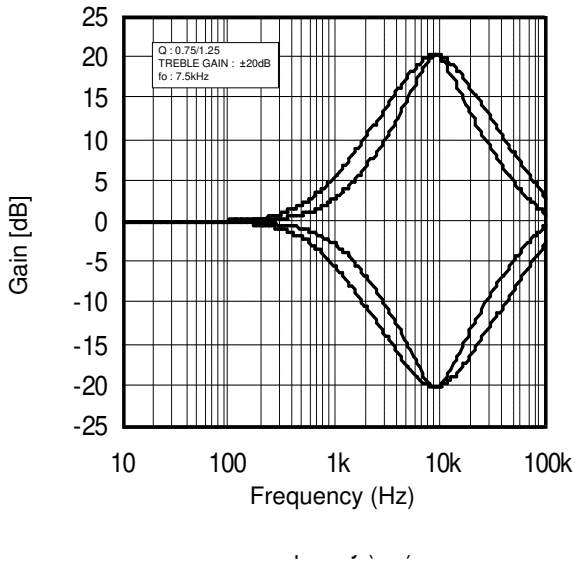


Figure 9.Treble Q vs Frequency

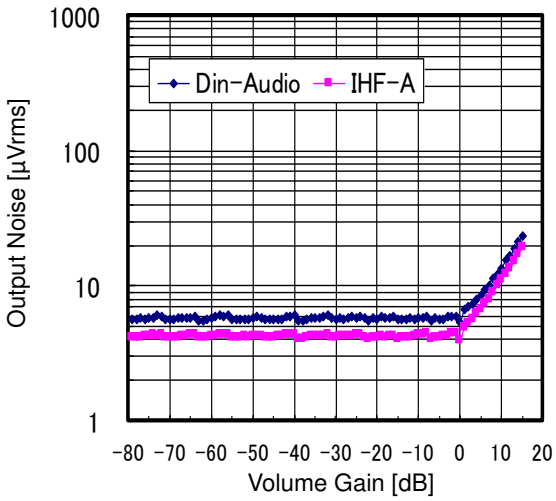


Figure 10. Output Noise vs Volume Gain

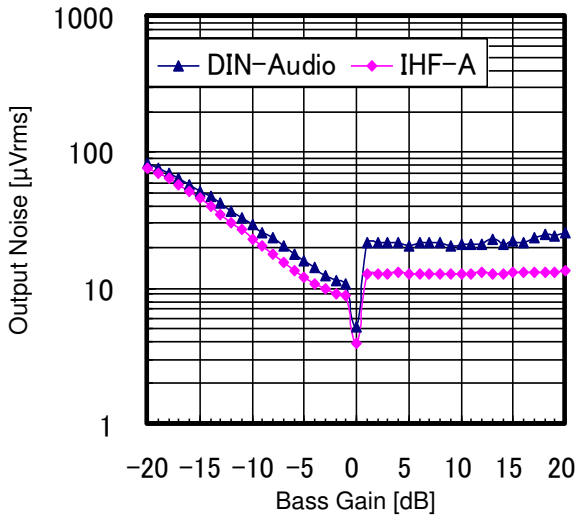


Figure 11. Output Noise vs Bass Gain

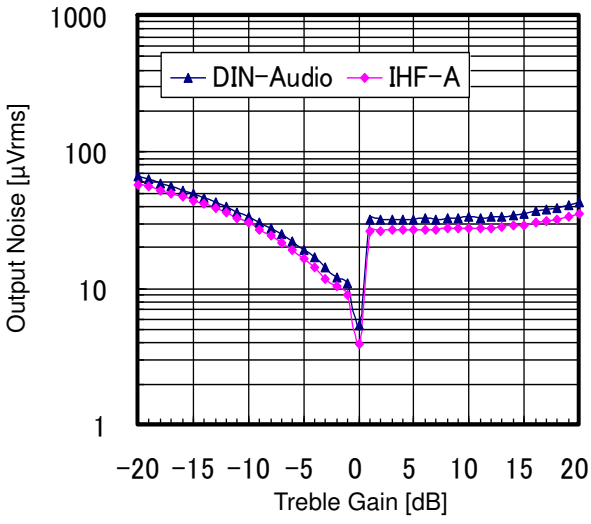


Figure 12. Output Noise vs Treble Gain

Typical Performance Curves - continued

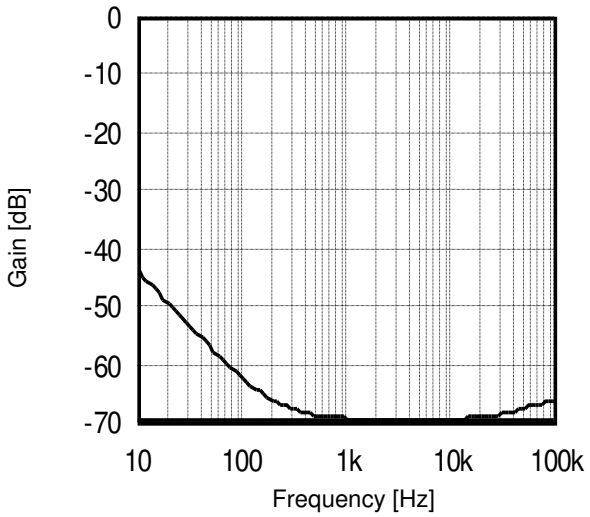


Figure 13. CMRR vs Frequency

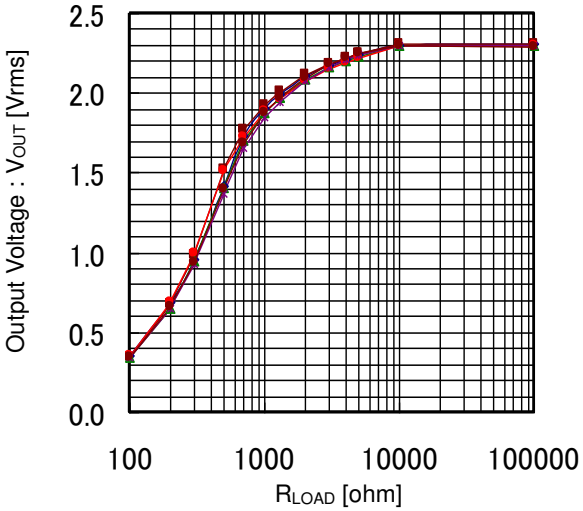


Figure 14. Output Voltage vs R_{LOAD}

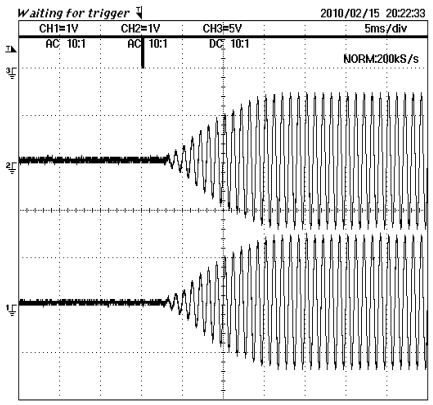


Figure 15. Advanced Switch 1

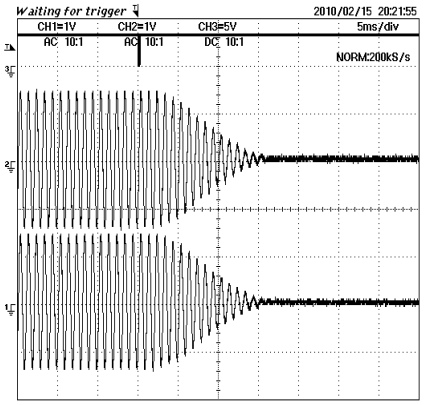


Figure 16. Advanced Switch 2

Timing Chart

CONTROL SIGNAL SPECIFICATION

(1) Electrical Specifications and Timing for Bus Lines and I/O Stages

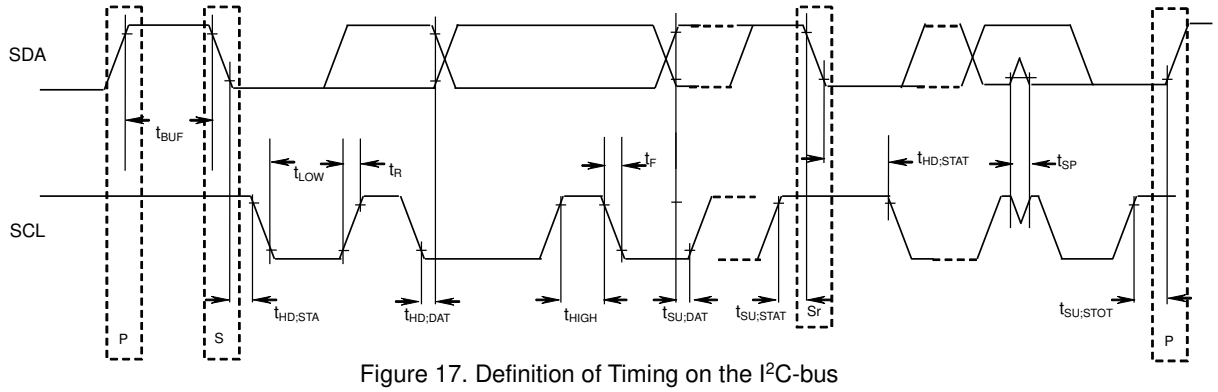


Figure 17. Definition of Timing on the I²C-bus

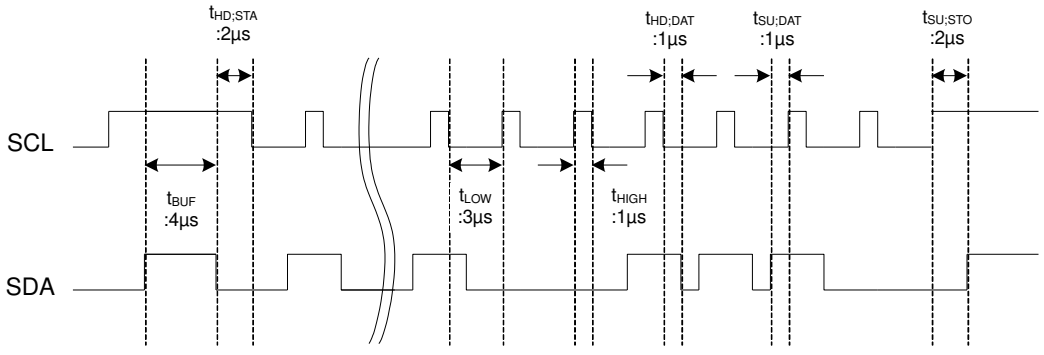
Table 1 Characteristics of the SDA and SCL bus lines for I²C-bus devices
(Unless otherwise specified, Ta=25°C, V_{CC}=8.5V)

	Parameter	Symbol	Fast-mode I²C-bus		Unit
			Min	Max	
1	SCL clock frequency	f_{SCL}	0	400	kHz
2	Bus free time between a STOP and START condition	t_{BUF}	1.3	-	µs
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	µs
4	LOW period of the SCL clock	t_{LOW}	1.3	-	µs
5	HIGH period of the SCL clock	t_{HIGH}	0.6	-	µs
6	Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	µs
7	Data hold time:	$t_{HD;DAT}$	0.06(Note)	-	µs
8	Data set-up time	$t_{SU;DAT}$	120	-	ns
9	Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	µs

All values referred to VIH Min and VIL max Levels (see Table 2).
(Note) The device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH Min of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
About 7($t_{HD;DAT}$), 8($t_{SU;DAT}$), make the setup in which the margin is fully in .

Table 2 Characteristics of the SDA and SCL I/O stages for I²C-bus devices

	Parameter	Symbol	Fast-mode devices		Unit
			Min	Max	
10	LOW level input voltage:	V_{IL}	-0.3	+1	V
11	HIGH level input voltage:	V_{IH}	2.3	5	V
12	Pulse width of spikes which must be suppressed by the input filter.	t_{SP}	0	50	ns
13	LOW level output voltage: at 3mA sink current	V_{OL1}	0	0.4	V
14	Input current each I/O pin with an input voltage between 0.4V and 4.5V.	I_I	-10	+10	µA



SCL clock frequency : 250kHz

Figure 18. A Command Timing Example in the I²C Data Transmission

(2) I²C BUS FORMAT

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S = Start condition (Recognition of start bit)
Slave Address = Recognition of slave address. 7 bits in upper order are voluntary. The least significant bit is “L” due to writing.
A = ACKNOWLEDGE bit (Recognition of acknowledgement)
Select Address = Select every of volume, bass and treble.
Data = Data on every volume and tone.
P = Stop condition (Recognition of stop bit)

(3) I²C BUS Interface Protocol

(a) Basic Form

S	Slave Address	A	Select Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

(b) Automatic Increment (Select Address increases (+1) according to the number of data.

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	····	DataN	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB			MSB LSB		

(Example) ① Data1 shall be set as data of address specified by Select Address.
② Data2 shall be set as data of address specified by Select Address +1.
③ DataN shall be set as data of address specified by Select Address +N-1.

(c) Configuration Unavailable for Transmission (In this case, only Select Address1 is set.

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

(Note) If any data is transmitted as Select Address 2 next to data, it is recognized as data, not as Select Address 2.

(4) Slave Address

MSB							LSB	
A6	A5	A4	A3	A2	A1	A0	R/W	
1	0	0	0	0	0	0	0	80H

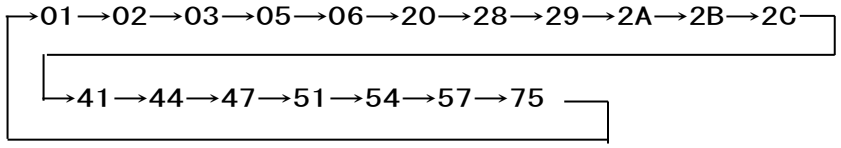
(5) Select Address & Data

Items	Select Address (hex)	MSB Data LSB							
		D7	D6	D5	D4	D3	D2	D1	D0
Initial setup 1	01	Advanced switch ON/OFF	0	Advanced switch time of Input Gain/Volume Tone/Fader/Loudness		0	0	Advanced switch time of Mute	
Initial setup 2	02	0	0	0	0	0	0	0	0
Initial setup 3	03	0	0	0	1	0	0	0	1
Input Selector	05	0	0	0	Input selector				
Input gain	06	Mute ON/OFF	0	0	Input Gain				
Volume gain	20	Volume / Attenuation							
Fader 1ch Front	28	Fader Attenuation							
Fader 2ch Front	29	Fader Attenuation							
Fader 1ch Rear	2A	Fader Attenuation							
Fader 2ch Rear	2B	Fader Attenuation							
Test mode 1	2C	1	1	1	1	1	1	1	1
Bass setup	41	0	0	Bass fo		0	0	Bass Q	
Test mode 2	44	0	0	0	0	0	0	0	0
Treble setup	47	0	0	Treble fo		0	0	0	Treble Q
Bass gain	51	Bass Boost/ Cut	0	0	Bass Gain				
Test mode 3	54	0	0	0	0	0	0	0	0
Treble gain	57	Treble Boost/ Cut	0	0	Treble Gain				
Loudness Gain	75	0	Loudness HiCut		Loudness Gain				
System Reset	FE	1	0	0	0	0	0	0	1

Advanced switch

Note

1. The advance switch works in the latch part while changing from one function to another.
2. Upon continuous data transfer, the Select Address rolls back to the first address on automatic increment function, as shown below.



3. Advanced switch is not used for the function of input selector etc. Therefore, please turn on MUTE when changing the settings of this side of a set.
4. When using Mute function when changing input selector, please switch Mute ON/OFF for waiting advanced-mute time.

Select address 01 (hex)

Time	MSB Advanced switch time of Mute LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
0.6msec	Advanced Switch ON/OFF	0	Advanced switch time of Input gain/Volume Tone/Fader/Loudness		0	0	0	0
1.0msec							0	1
1.4msec							1	0
3.2msec							1	1

Time	MSB	Advanced switch time of Input gain/Volume/Tone/Fader/Loudness					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
4.7 msec	Advanced Switch ON/OFF	0	0	0	0	0	Advanced switch Time of Mute	
7.1 msec			0	1				
11.2 msec			1	0				
14.4 msec			1	1				

Mode	MSB	Advanced switch ON/OFF					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	Advanced switch time of Input gain/Volume Tone/Fader/Loudness		0	0	Advanced switch Time of Mute	
ON	1							

Select address 05(hex)

Mode	OUT F1/R1	OUT F2/R2	MSB	Input Selector					LSB
			D7	D6	D5	D4	D3	D2	D1	D0
Initial			0	0	0	0	0	0	0	0
A	A1	A2					0	0	0	1
B	B1	B2					0	0	1	0
C diff	CP1	CP2					0	1	1	0
D	D1	D2					1	0	1	0
E	E1	E2					1	0	1	1
Input SHORT							1	0	0	1
Prohibition							Other setting			

Input SHORT : The input impedance of each input terminal is lowered from 100kΩ(Typ) to 6 kΩ(Typ).
(For quick charge of coupling capacitor)

: Initial condition

Select address 06 (hex)

Gain	MSB			Input Gain				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Mute ON/OFF	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	1	0	1	1
				:	:	:	:	:
				1	1	1	1	1

Mode	MSB			Mute ON/OFF				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	0	Input Gain				
ON	1							

Select address 20, 28, 29, 2A, 2B (hex)

Gain & ATT	MSB	Vol, Fader Gain / Attenuation						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
	0	1	1	1	0	0	0	0
15dB	0	1	1	1	0	0	0	1
14dB	0	1	1	1	0	0	1	0
13dB	0	1	1	1	0	0	1	1
:	:	:	:	:	:	:	:	:
-77dB	1	1	0	0	1	1	0	1
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
Prohibition	1	1	0	1	0	0	0	0
	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
-∞dB	1	1	1	1	1	1	1	1

(Only 0dB to -∞dB are available at address 28, 29, 2A, 2B)

: Initial condition

Select address 41(hex)

Q factor	MSB Bass Q factor							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0.5	0	0	Bass fo		0	0	0	0
1.0							0	1
1.5							1	0
2.0							1	1

fo	MSB Bass fo							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
60Hz	0	0	0	0	0	0	Bass Q factor	
80Hz			0	1				
100Hz			1	0				
120Hz			1	1				

Select address 47 (hex)

Q factor	MSB Treble Q factor							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0.75	0	0	Treble fo		0	0	0	0
1.25								1

fo	MSB Treble fo							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
7.5kHz	0	0	0	0	0	0	0	Treble Q factor
10kHz			0	1				
12.5kHz			1	0				
15kHz			1	1				

Select address 51, 57 (hex)

Gain	MSB Bass/ Treble Gain							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Bass/ Treble Boost /Cut	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	0	1	0	1
				:	:	:	:	:
				1	1	1	1	0
				1	1	1	1	1

Mode	MSB Bass/ Treble Boost/Cut							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Boost	0	0	0	Bass/Treble Gain				
Cut	1							

: Initial condition

Select address 75 (hex)

Mode	MSB		Loudness HiCut					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
HiCut1	0	0	0	Loudness Gain				
HiCut2		0	1					
HiCut3		1	0					
HiCut4		1	1					

Gain	MSB		Loudness Gain					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	0	Loudness HiCut		0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	0	1	0	1
				:	:	:	:	:
				1	1	1	1	1

: Initial condition

(6) About Power ON Reset

The IC has a built-in initialization circuit that triggers at power ON of supply voltage..Please send initial data to all address at supply voltage ON. Also, please turn ON MUTE at the set side until this initial data is sent.

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Rise Time of VCC	t_{RISE}	33	-	-	μsec	V_{CC} rise time from 0V to 5V
VCC Voltage of Release Power ON Reset	V_{POR}	-	4.1	-	V	

(7) About External Compulsory Mute Terminal

It is possible to forcibly set MUTE externally by setting the input voltage at the MUTE terminal.

Mute Voltage Condition	Mode
GND to 1.0V	MUTE ON
2.3V to V_{CC}	MUTE OFF

Establish the voltage of MUTE in the condition to be defined.

Application Information

1. Function and Specifications

Function	Specifications
Input selector	・Stereo 4 input ・Differential 1 input
Input gain	・+20dB to 0dB (1dB step) ・Possible to use “Advanced switch” for prevention of switching noise.
Mute	・Possible to use “Advanced switch” for prevention of switching noise.
Volume	・+15dB to -79dB (1dB step), -∞dB ・Possible to use “Advanced switch” for prevention of switching noise.
Bass	・+20dB to -20dB (1dB step) ・Q=0.5, 1, 1.5, 2 variable ・fo=60, 80, 100, 120Hz ・Possible to use “Advanced switch” when changing gain
Treble	・+20dB to -20dB (1dB step) ・Q=0.75, 1.25 variable ・fo=7.5k, 10k, 12.5k, 15kHz ・Possible to use “Advanced switch” when changing gain
Fader	・0dB to -79dB, -∞dB ・Possible to use “Advanced switch” for prevention of switching noise.
Loudness	・20dB to 0dB(1dB step) ・fo=800Hz ・Possible to use “Advanced switch” for prevention of switching noise.

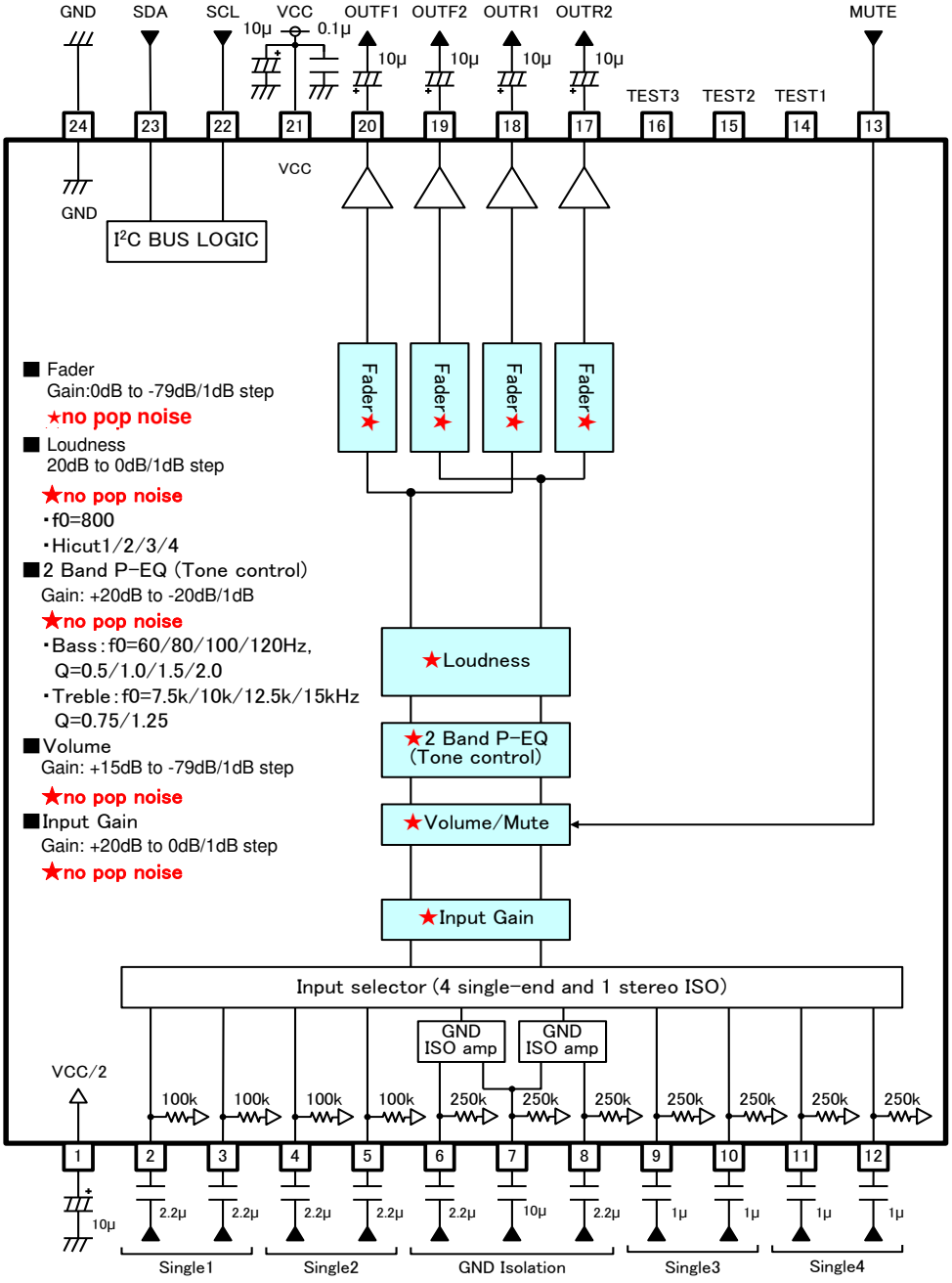
2. Volume/Fader Volume Attenuation of the Details

(dB)	D7	D6	D5	D4	D3	D2	D1	D0		(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+15	0	1	1	1	0	0	0	1		-33	1	0	1	0	0	0	0	1
+14	0	1	1	1	0	0	1	0		-34	1	0	1	0	0	0	1	0
+13	0	1	1	1	0	0	1	1		-35	1	0	1	0	0	0	1	1
+12	0	1	1	1	0	1	0	0		-36	1	0	1	0	0	1	0	0
+11	0	1	1	1	0	1	0	1		-37	1	0	1	0	0	1	0	1
+10	0	1	1	1	0	1	1	0		-38	1	0	1	0	0	1	1	0
+9	0	1	1	1	0	1	1	1		-39	1	0	1	0	0	1	1	1
+8	0	1	1	1	1	0	0	0		-40	1	0	1	0	1	0	0	0
+7	0	1	1	1	1	0	0	1		-41	1	0	1	0	1	0	0	1
+6	0	1	1	1	1	0	1	0		-42	1	0	1	0	1	0	1	0
+5	0	1	1	1	1	0	1	1		-43	1	0	1	0	1	0	1	1
+4	0	1	1	1	1	1	0	0		-44	1	0	1	0	1	1	0	0
+3	0	1	1	1	1	1	0	1		-45	1	0	1	0	1	1	0	1
+2	0	1	1	1	1	1	1	0		-46	1	0	1	0	1	1	1	0
+1	0	1	1	1	1	1	1	1		-47	1	0	1	0	1	1	1	1
0	1	0	0	0	0	0	0	0		-48	1	0	1	1	0	0	0	0
-1	1	0	0	0	0	0	0	1		-49	1	0	1	1	0	0	0	1
-2	1	0	0	0	0	0	1	0		-50	1	0	1	1	0	0	1	0
-3	1	0	0	0	0	0	1	1		-51	1	0	1	1	0	0	1	1
-4	1	0	0	0	0	1	0	0		-52	1	0	1	1	0	1	0	0
-5	1	0	0	0	0	1	0	1		-53	1	0	1	1	0	1	0	1
-6	1	0	0	0	0	1	1	0		-54	1	0	1	1	0	1	1	0
-7	1	0	0	0	0	1	1	1		-55	1	0	1	1	0	1	1	1
-8	1	0	0	0	1	0	0	0		-56	1	0	1	1	1	0	0	0
-9	1	0	0	0	1	0	0	1		-57	1	0	1	1	1	0	0	1
-10	1	0	0	0	1	0	1	0		-58	1	0	1	1	1	0	1	0
-11	1	0	0	0	1	0	1	1		-59	1	0	1	1	1	0	1	1
-12	1	0	0	0	1	1	0	0		-60	1	0	1	1	1	1	0	0
-13	1	0	0	0	1	1	0	1		-61	1	0	1	1	1	1	0	1
-14	1	0	0	0	1	1	1	0		-62	1	0	1	1	1	1	1	0
-15	1	0	0	0	1	1	1	1		-63	1	0	1	1	1	1	1	1
-16	1	0	0	1	0	0	0	0		-64	1	1	0	0	0	0	0	0
-17	1	0	0	1	0	0	0	1		-65	1	1	0	0	0	0	0	1
-18	1	0	0	1	0	0	1	0		-66	1	1	0	0	0	0	1	0
-19	1	0	0	1	0	0	1	1		-67	1	1	0	0	0	0	1	1
-20	1	0	0	1	0	1	0	0		-68	1	1	0	0	0	1	0	0
-21	1	0	0	1	0	1	0	1		-69	1	1	0	0	0	1	0	1
-22	1	0	0	1	0	1	1	0		-70	1	1	0	0	0	1	1	0
-23	1	0	0	1	0	1	1	1		-71	1	1	0	0	0	1	1	1
-24	1	0	0	1	1	0	0	0		-72	1	1	0	0	1	0	0	0
-25	1	0	0	1	1	0	0	1		-73	1	1	0	0	1	0	0	1
-26	1	0	0	1	1	0	1	0		-74	1	1	0	0	1	0	1	0
-27	1	0	0	1	1	0	1	1		-75	1	1	0	0	1	0	1	1
-28	1	0	0	1	1	1	0	0		-76	1	1	0	0	1	1	0	0
-29	1	0	0	1	1	1	0	1		-77	1	1	0	0	1	1	0	1
-30	1	0	0	1	1	1	1	0		-78	1	1	0	0	1	1	1	0
-31	1	0	0	1	1	1	1	1		-79	1	1	0	0	1	1	1	1
-32	1	0	1	0	0	0	0	0		-∞	1	1	1	1	1	1	1	1

Fader Volume only 0dB to -∞dB are available.

: Initial condition

3. Application Circuit



Unit
R : [Ω]
C : [F]

Notes on Wiring

① Please connect the decoupling capacitor of the power supply in the shortest possible distance to GND.
② GND Lines should be one-point connected.
③ Wiring pattern of Digital should be away from that of analog unit and crosstalk should not be acceptable.
④ Lines of SCL and SDA of I²C BUS should not be in parallel if possible.
The lines should be shielded, if they are adjacent to each other.
⑤ Lines of analog input should not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.
⑥ TEST pins (Pin 14,15,16) should be OPEN.

Power Dissipation

About the thermal design of the IC

Characteristics of an IC are greatly affected by the temperature at which it is used. Exceeding absolute maximum ratings may degrade and destroy the device. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.

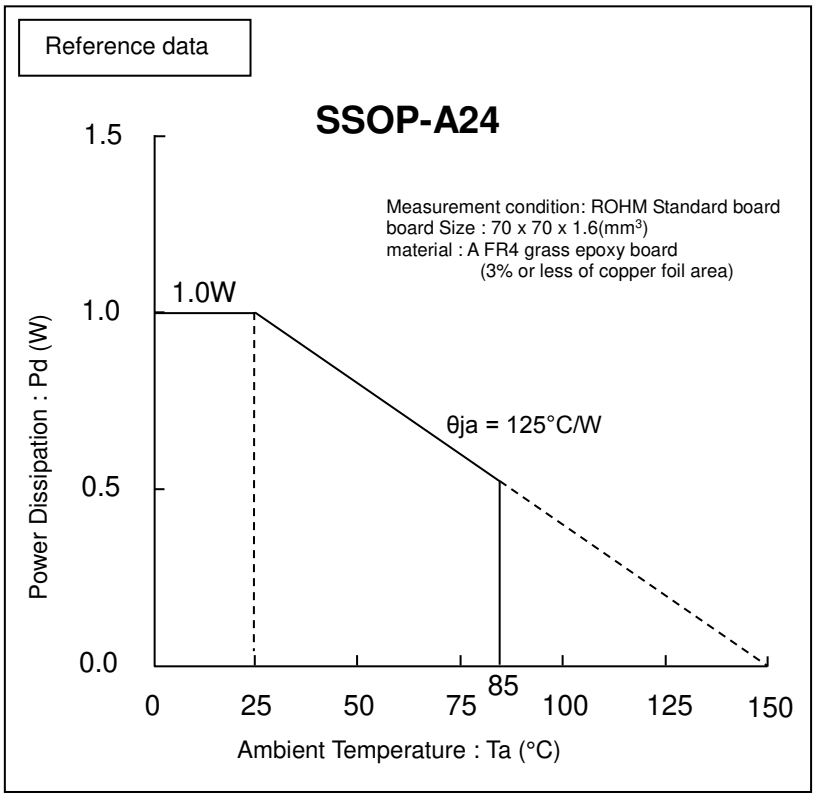
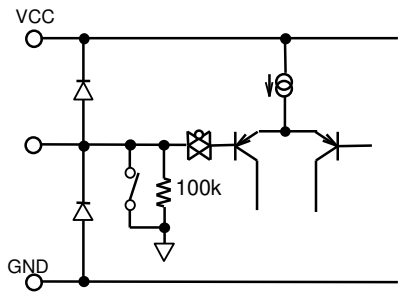
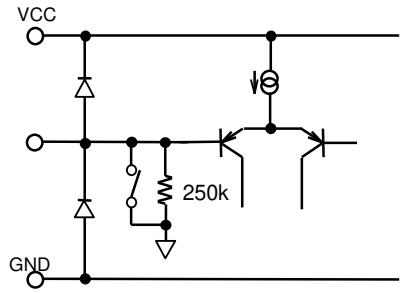
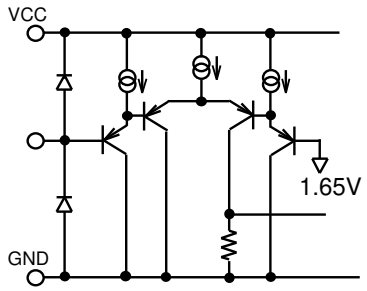
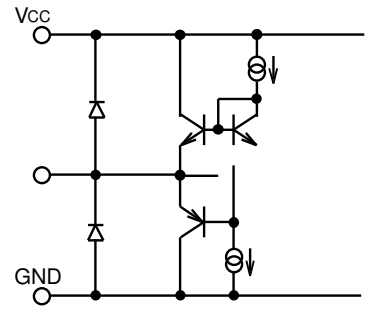


Figure 19. Temperature Derating Curve

(Note) Values are actual measurements and are not guaranteed.

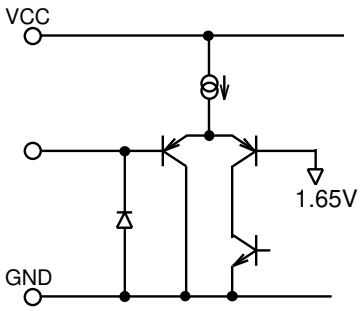
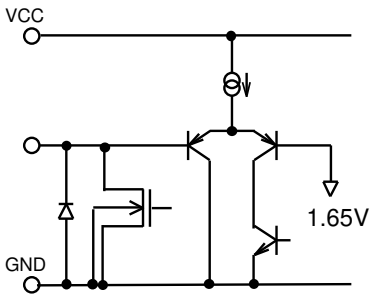
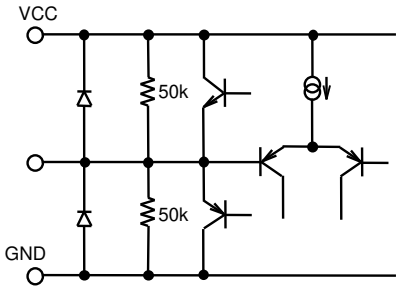
Power dissipation values vary according to the board on which the IC is mounted.

I/O Equivalent Circuits

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
2 3 4 5	A1 A2 B1 B2	4.25		A terminal for signal input. The input impedance is 100kΩ (typ).
6 7 8 9 10 11 12	CP1 CN CP2 D1 D2 E1 E2	4.25		A terminal for signal input. The input impedance is 250kΩ (typ).
13	MUTE	-		A terminal for external compulsory mute. If terminal voltage is High level, the mute is off. If the terminal voltage is Low level, the Mute is ON.
17 18 19 20	OUTR2 OUTR1 OUTF2 OUTF1	4.25		A terminal for fader and Subwoofer output.

The values in the pin explanation and input/output equivalent circuit are for reference purposes only. It is not a guaranteed value.

I/O Equivalent Circuits – continued

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
21	VCC	8.5		Power supply terminal.
22	SCL	-		A terminal for clock input of I²C BUS communication.
23	SDA	-		A terminal for data input of I²C BUS communication.
24	GND	0		Ground terminal.
1	FIL	4.25		Voltage for reference bias of analog signal system. The simple pre-charge circuit and simple discharge circuit for an external capacitor are built in.
14 15 16	TEST	-		TEST terminal

The Values in the pin explanation and input/output equivalent circuit are for reference purposes only. It is not a guaranteed value

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

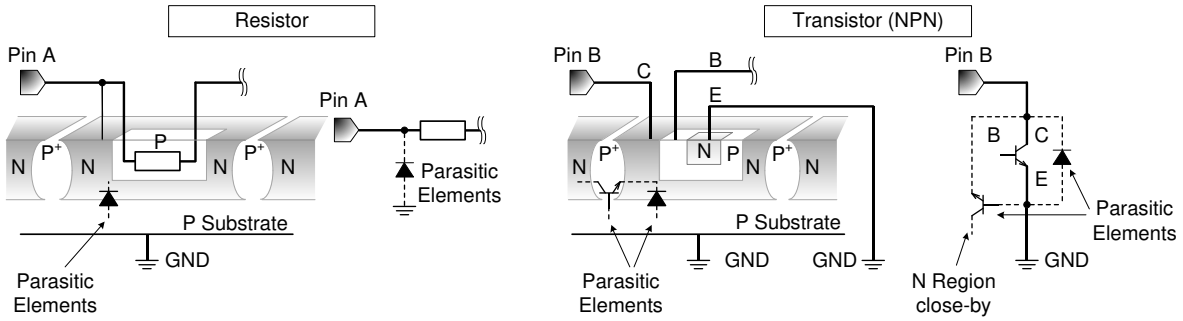
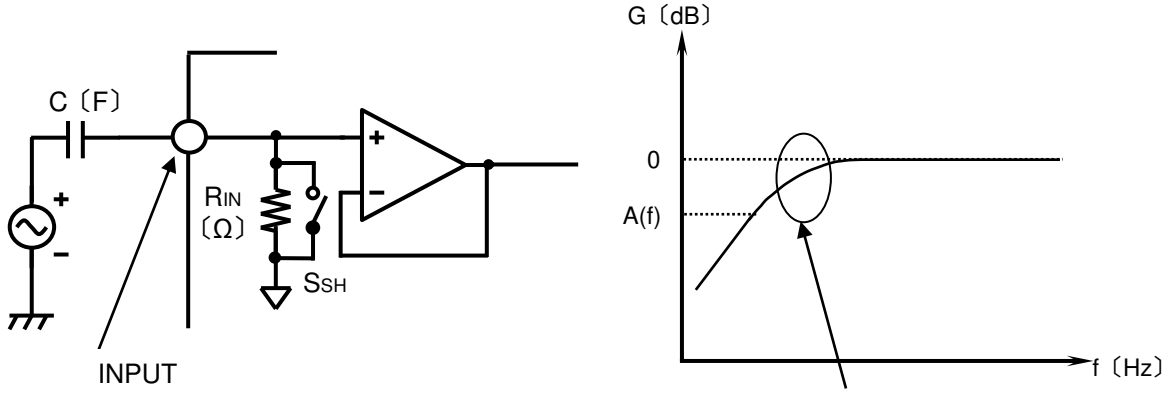


Figure 20. Example of monolithic IC structure

13. About a Signal Input Part

(a) About Input Coupling Capacitor Constant Value

In the input signal terminal, please decide the constant value of the input coupling capacitor C(F) that would be sufficient to form an RC characterized HPF with input impedance R_{IN}(Ω) inside the IC.



$$A(f) = \sqrt{\frac{(2\pi fCR_{IN})^2}{1+(2\pi fCR_{IN})^2}}$$

(b) About the Input Selector SHORT

SHORT mode is the command which makes switch S_{SH} =ON of input selector part so that the input impedance R_{IN} of all terminals becomes small. Switch S_{SH} is OFF when SHORT command is not selected.
The constant time brought about by the small resistance inside and the capacitor outside the LSI becomes small when this command is used. The charge time of the capacitor becomes short. Since SHORT mode turns ON the switch of S_{SH} and makes it low impedance, please use it at no signal condition.

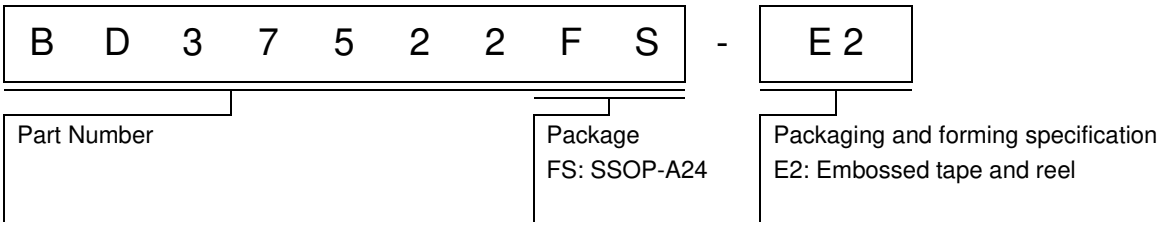
14. About Mute Terminal(Pin 13) when power supply is OFF

There should be no applied voltage across the Mute terminal (Pin 13) when power-supply is OFF.
A resistor (about 2.2kΩ) should be connected in series to Mute terminal in case a voltage is supplied to Mute terminal. (Please refer Application Circuit Diagram.)

15. About TEST Pin

TEST Pin, should be OPEN.
Pin 14,15,16 are TEST Pins.

Ordering Information



Marking Diagram