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Power Management IC for Automotive Microcontroller

Buck-Boost Switching Regulator + LDO + Step-down Switching Regulator + Reset + Watch Dog Timer

BD39001EKV-C

General Description

BD39001EKV-C is a power management IC with buck-boost switching regulator controller (DC / DC1), secondary step-down switching regulator (DC / DC2), LDO, reset and WDT.
The BD39001EKV-C includes protection circuits, such as Under voltage, Over voltage, Over current and TSD.

Features

- AEC-Q100 Qualified(Note 1)
- Automatically controlled buck-boost switching regulator with 40 V rated V_{CC}, DC / DC2 and LDO input
- 3.3 V fixed output secondary step-down switching regulator with built-in FET
- 5 V fixed output secondary LDO
- Configurable Sequence control
- Over Current protection
  DC / DC1: Adjustable voltage with external resistors
  DC / DC2: Integrated
  LDO: Integrated
- Over voltage / Under voltage detection
- Reset for LDO and DC / DC2
- Window Watchdog Timer
- HTQFP48V package
  (Note 1: Grade 1)

Applications

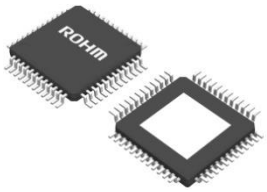
- Microcontroller for Automotive

Key Specifications

- Input voltage range 4.0 V to 30 V
  (Startup voltage needs to be above 4.5V.)
- Output voltage
  - Buck-Boost DC / DC1 FB Voltage 0.8 V
  - Secondary DC / DC2 3.3 V
  - Secondary LDO 5.0 V
- Reference voltage accuracy
  - Buck-Boost DC / DC1 FB Voltage ±2 %
  - Secondary DC / DC2 ±2 %
  - Secondary LDO ±2 %
- Oscillation frequency 200 to 550 kHz
- Max output current
  - Secondary Buck DC / DC2 900 mA
  - Secondary LDO 600 mA
- Stand-by Current 0 μA (Typ)
- Operating temperature range -40 °C to 125 °C
- AEC-Q100 Qualified

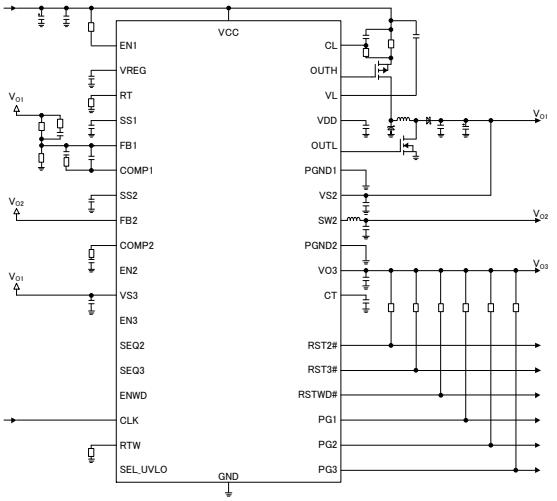
Package

	W (Typ) × D (Typ) × H (Max)
HTQFP48V	9.00 mm × 9.00 mm × 1.00 mm



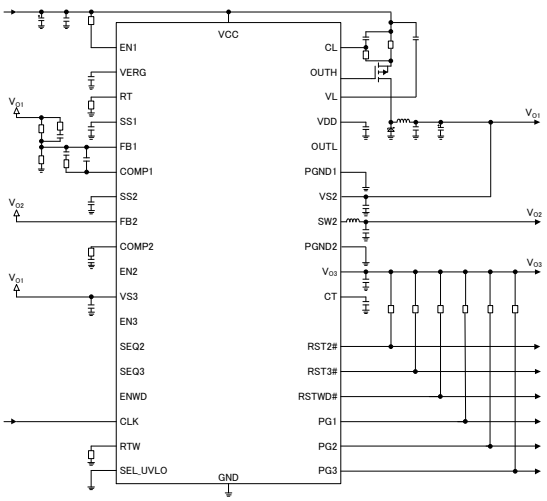
Typical Application Circuit

Simplified Circuit1



Buck-Boost Switching Regulator
+ Secondary Switching Regulator
+ Secondary LDO

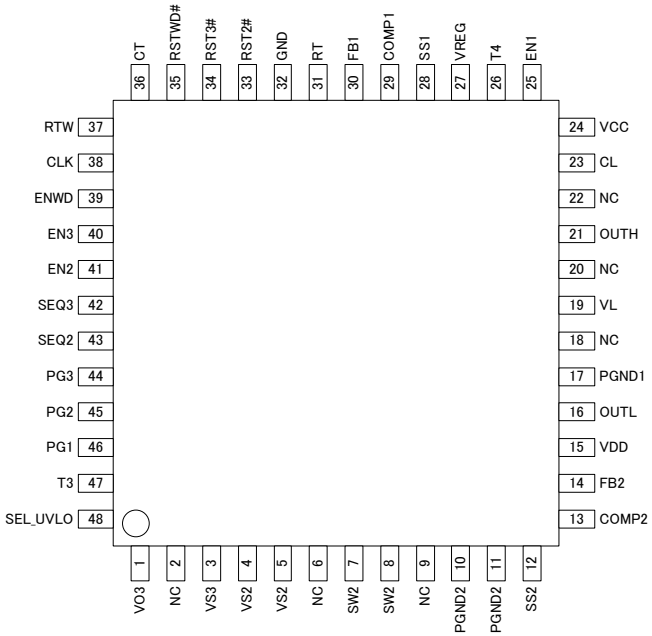
Simplified Circuit2



Buck Switching Regulator
+ Secondary Switching Regulator
+ Secondary LDO

Pin Configuration

(TOP VIEW)

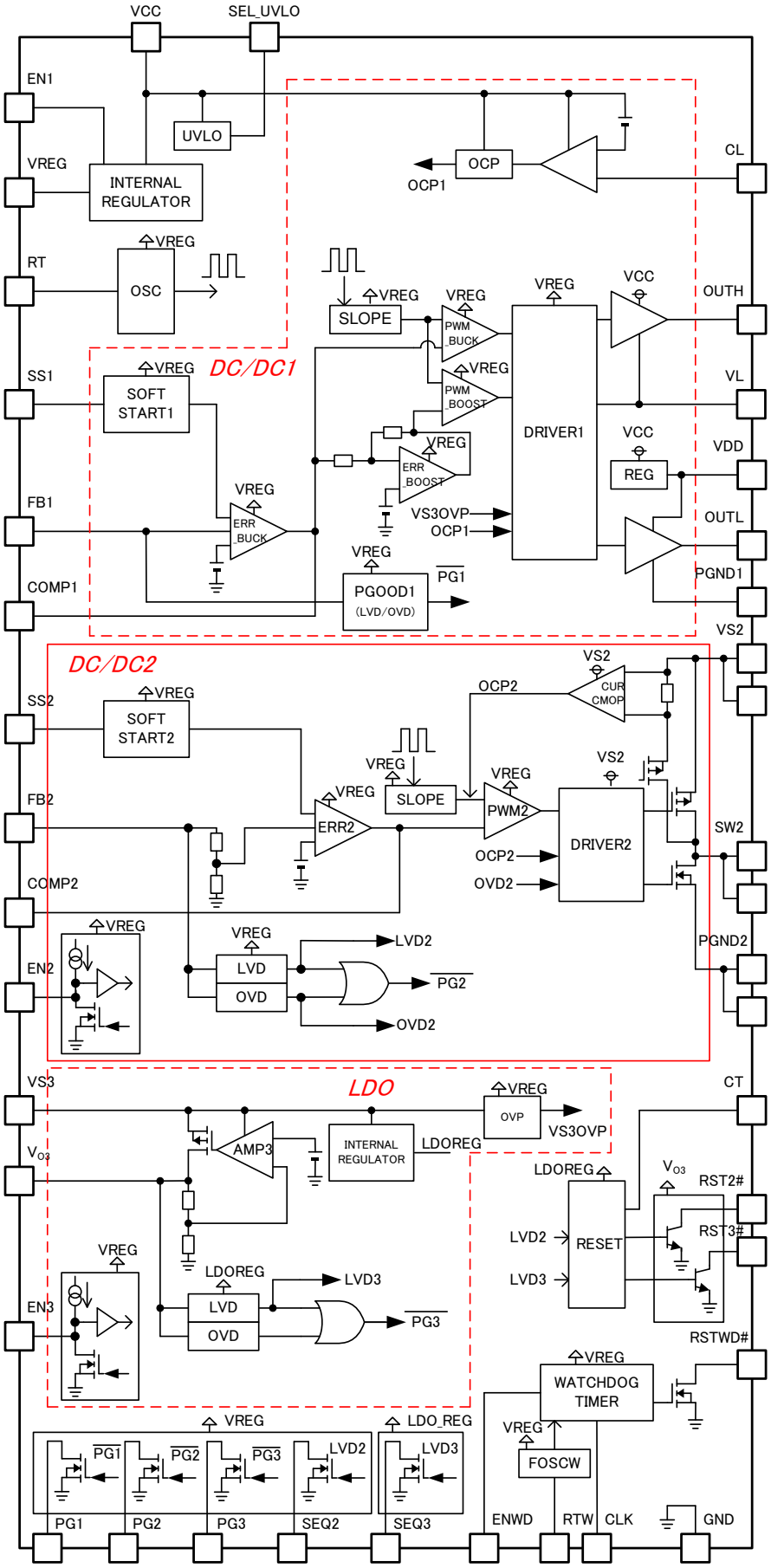


Pin Description

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	VO3	5 V Output	25	EN1	Output ON / OFF
2	N.C.	Not connected	26	T4 (Note 1)	Test pin
3	VS3	Supply Voltage Input for LDO	27	VREG	Internal power supply
4	VS2	Supply Voltage Input for DC / DC2	28	SS1	Soft start time setting for DC / DC1
5	VS2	Supply Voltage Input for DC / DC2	29	COMP1	Error-amp output for DC / DC1
6	N.C.	Not connected	30	FB1	Feedback for DC / DC1
7	SW2	DC / DC2 SW pin	31	RT	Frequency setting
8	SW2	DC / DC2 SW pin	32	GND	Ground
9	N.C.	Not connected	33	RST2#	Reset Output for DC / DC2
10	PGND2	Power Ground	34	RST3#	Reset Output for LDO
11	PGND2	Power Ground	35	RSTWD#	Reset Output for WDT
12	SS2	Soft start time setting for DC / DC2	36	CT	Reset Delay
13	COMP2	Error-amp output for DC / DC2	37	RTW	Frequency setting for WDT
14	FB2	Feedback for DC / DC2	38	CLK	Clock input
15	VDD	N-channel MOSFET drive supply	39	ENWD	WDT ON / OFF
16	OUTL	N-channel MOSFET drive	40	EN3	Output ON / OFF for LDO
17	PGND1	Power Ground	41	EN2	Output ON / OFF for DC / DC2
18	N.C.	Not connected	42	SEQ3	Sequence setting for LDO
19	VL	Pch FET gate clamp for DC / DC1	43	SEQ2	Sequence setting for DC / DC2
20	N.C.	Not connected	44	PG3	Power good output for LDO
21	OUTH	N-channel MOSFET drive	45	PG2	Power good output for DC / DC2
22	N.C.	Not connected	46	PG1	Power good output for DC / DC1
23	CL	Overcurrent detection setting for DC / DC1	47	T3 (Note 1)	Test pin
24	VCC	Supply Voltage Input	48	SEL_UVLO	Select Pin for VCC UVLO

(Note 1) Short with GND

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
VCC Voltage (Note 1)	V_{CC}	40	V
VS2 Voltage (Note 1)	V_{S2}	40	V
VS3 Voltage (Note 1)	V_{S3}	40	V
CL Voltage	V_{CL}	VCC	V
EN1 Voltage	V_{EN1}	VCC	V
VREG Voltage	V_{REG}	7	V
VDD Voltage	V_{DD}	7	V
SS1, SS2 Voltage	V_{SS1}, V_{SS2}	VREG	V
RST2#, RST3#, RSTWD#	$V_{RST2\#}$, $V_{RST3\#}$, $V_{RSTWD\#}$	7	V
CLK, RTW, CT, ENWD	V_{CLK}, V_{RTW}, V_{CT}, V_{ENWD}	7	V
PG1, PG2, PG3	V_{PG1}, V_{PG2}, V_{PG3}	7	V
EN2, EN3	V_{EN2}, V_{EN3}	VREG	V
SEQ2, SEQ3	V_{SEQ2}, V_{SEQ3}	7	V
Power Dissipation (Note 2)	Pd	5.00	W
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	150	°C

(Note 1) Pd should not be exceeded.
(Note 2) If mounted on a standard ROHM 4 layer PCB (copper foil area: 70 mm × 70 mm) (Standard ROHM PCB size: 70mm × 70 mm ×1.6mm)
Reduce by 9.6 mW / °C (Ta ≥ 25 °C)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Rating

Parameter	Symbol	Maximum ratings		Unit
		Min	Max	
Voltage Power Supply	V_{CC} (Buck Boost mode)	4 (Note 1)	30	V
	V_{CC} (Buck mode)	6	30	V
	V_{S2}	5	10	V
	V_{S3}	5	10	V
Oscillation Frequency	F_{OSC}	200	550	kHz
WDT Oscillation Frequency	F_{OSCW}	50	250	kHz
OUTH Current Ability	I_{OUTH}	-	1.5	A
OUTL Current Ability	I_{OUTL}	-	1.5	A
SW2 Current Ability	I_{SW2}	-	900 (Note 2)	mA
V_{O3} Current Ability	I_{VO3}	-	600 (Note 2)	mA
Operating Temperature Range	Topr	-40	+125	°C

(Note 1) Initial startup is over 4.5 V
(Note 2) Pd should not be exceeded.

Electrical Characteristic

(Unless otherwise specified: -40 °C ≤ Ta ≤ +125 °C, 4 V ≤ V_{CC} ≤ 30 V, 5 V ≤ V_{S2} ≤ 10 V, 5 V ≤ V_{S3} ≤ 10 V)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
All						
Standby Current 1	I_{STB1}	-	0	10	μA	Ta = 25 °C
Standby Current 2	I_{STB2}	-	-	30	μA	Ta = 125 °C
Circuit Current	I_{VCC}	5	8	12	mA	R_{RT} = 33 kΩ, V_{FB1} = 1.0 V
Oscillation Frequency	F_{OSC}	315	350	385	kHz	R_{RT} = 33 kΩ
VREG Output Voltage	V_{REG}	3.0	3.5	4.0	V	
VDD Output Voltage	V_{DD}	4.5	5	5.5	V	V_{CC} = 12 V
UVLO_VCC Detection Voltage 1	$V_{UVLOVCC1}$	3.30	3.60	3.90	V	SEL_UVLO = OPEN
UVLO_VCC Release Voltage 1	$V_{UVVCCRE1}$	3.50	4.00	4.50	V	SEL_UVLO = OPEN
UVLO_VCC Hysteresis Voltage 1	$V_{UVVCCHYS1}$	200	400	600	mV	SEL_UVLO = OPEN
UVLO_VCC Detection Voltage 2	$V_{UVLOVCC2}$	5.27	5.58	5.89	V	SEL_UVLO = GND
UVLO_VCC Release Voltage 2	$V_{UVVCCRE2}$	5.35	5.67	6.0	V	SEL_UVLO = GND
UVLO_VCC Hysteresis Voltage 2	$V_{UVVCCHYS2}$	50	75	-	mV	SEL_UVLO = GND
EN1 L Voltage	V_{EN1L}	-	-	0.5	V	
EN1 H Voltage	V_{EN1H}	2.5	-	-	V	
EN1 Input Resistance	R_{EN1}	180	375	570	kΩ	V_{EN1} = 5 V
SEL_UVLO Threshold	V_{SEL_UVLO}	-	V_{REG} / 2	-	V	
SEL_UVLO Output Current	I_{SEL_UVLO}	5	14	23	μA	V_{SEL_UVLO} = 0V
DC / DC1 (Buck - Boost DC / DC Controller)						
FB1 Voltage	VREF08	0.784	0.800	0.816	V	FB1 = COMP1
FB1 Input Bias Current	I_{FB1}	-1	0	+1	μA	V_{FB1} = 0.8 V
Soft Start Quick Charge Current	I_{SS0}	55	110	165	μA	
Soft Start Charge Current	I_{SS1}	5	10	15	μA	
Soft Start selected Voltage	V_{SS0}	0.3	0.7	1.5	V	
Soft Start End Voltage 1	V_{SS1}	-	V_{SS0}+ V_{REF08}	-	V	
Soft Start Cramp Voltage	V_{SSCL1}	2.2	2.8	3.3	V	SS1 = OPEN
VCC - VL Voltage	V_L	8	10	12	V	V_{CC} ≥ 12 V, V_{CC} - V_{VL}
Hi - Side OUTH ON - Resistance	R_{ONHH}	-	1.7	-	Ω	V_{CC} = 12 V, OUTH - VCC
Lo - Side OUTH ON - Resistance1	R_{ONHL1}	-	3	-	Ω	V_{CC} = 12 V, OUTH - VL
Lo - Side OUTH ON - Resistance2	R_{ONHL2}	-	-	30	Ω	V_{CC} = 4 V, OUTH - PGND
Hi - Side OUTL ON - Resistance	R_{ONLH}	-	18	-	Ω	V_{CC} = 12 V
Lo - Side OUTL ON - Resistance	R_{ONLL}	-	22	-	Ω	V_{CC} = 12 V
Over current detection CL voltage (Low)	V_{CL_L}	86	100	114	mV	V_{CC} - V_{CL}, V_{CC} = 12 V
Over current detection CL voltage (High)	V_{CL_H}	172	200	228	mV	V_{CC} - V_{CL}, V_{CC} = 12 V
Maximum ON Duty (OUTL)	T_{ON}	-	92	-	%	F_{OSC} = 550 kHz

Electrical Characteristic

(Unless otherwise specified: -40 °C ≤ Ta ≤ +125 °C, 4 V ≤ V_{CC} ≤ 30 V, 5 V ≤ V_{S2} ≤ 10 V, 5 V ≤ V_{S3} ≤ 10 V)

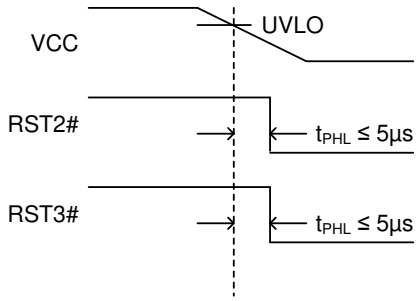
Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
DC / DC2 (Secondary DC / DC)						
Output Voltage 2	V_{O2}	3.23	3.30	3.37	V	
Under voltage detection voltage	V_{RST2}	3.00	3.07	3.14	V	
Under voltage hysteresis voltage	V_{RSTH2}	20	-	80	mV	
Soft Start Charge Current	I_{SS2}	5	10	15	µA	V_{SS2} = 0.2 V
Soft Start end voltage 2	V_{SS2}	0.6	0.8	1.0	V	
SW2 ON - Resistance H	R_{ONH2}	-	0.3	0.6	Ω	
SW2 ON - Resistance L	R_{ONL2}	-	0.3	0.6	Ω	
EN2 L Voltage	V_{EN2L}	-	-	0.6	V	
EN2 H Voltage	V_{EN2H}	1.0	-	-	V	
EN2 Charge Current	I_{EN2}	4	8	12	µA	V_{EN2} = 0.2 V
UVLO_VS2 Detection Voltage	$V_{UVLOVS2}$	3.5	3.9	4.3	V	
UVLO_VS2 Hysteresis Voltage	$V_{UVVS2HYS}$	0.2	0.35	0.5	V	
LDO (5.0 V Output LDO)						
Output Voltage 3	V_{O3}	4.90	5.00	5.10	V	6.0 V ≤ V_{S3} ≤ 10 V, 5 mA ≤ I_{VO3} ≤ 600 mA
Drop Voltage	ΔV_{O3}	-	-	0.6	V	V_{S3} = 4.65 V, I_{VO3} = 600 mA
Under voltage detection voltage	V_{RST3}	4.50	4.625	4.75	V	
Under voltage hysteresis voltage	V_{RSTH3}	30	-	150	mV	
VCC UVLO - LDO LVD difference voltage	ΔV_{LVD3}	0.7	0.9	1.5	V	$V_{UVLOVVCC2}$ - V_{RST3}
EN3 L Voltage	V_{EN3L}	-	-	0.6	V	
EN3 H Voltage	V_{EN3H}	1.0	-	-	V	
EN3 Charge Current	I_{EN3}	4	8	12	µA	V_{EN3} = 0.2 V
UVLO_VS3 Detection Voltage	$V_{UVLOVS3}$	3.5	3.9	4.3	V	
UVLO_VS3 Hysteresis Voltage	$V_{UVVS3HYS}$	0.2	0.35	0.5	V	
VS3 Over voltage detection voltage	V_{OVVS}	12.5	14	15.5	V	
RST2#, RST3#, RSTWD#						
Reset Delay Time	t_{RST}	30	56	160	ms	C_{CT} = 0.47 µF
Reset L Voltage 1	V_{RSTL1}	-	-	0.25	V	V_{O3} = 1.0 V, I_{RST} = 100 µA
Reset L Voltage 2	V_{RSTL2}	-	-	0.4	V	I_{RST} = 1 mA
Reset Response Time	t_{PHL}	-	-	5	µs	RST# pull up resistance 4.7 kΩ
WDT Oscillation Frequency	F_{OSCW}	75	100	125	kHz	R_{TW} = 51 kΩ
CLK FAST NG Threshold	t_{WF}	$\frac{507}{F_{OSCW}}$	$\frac{512}{F_{OSCW}}$	$\frac{517}{F_{OSCW}}$	s	
CLK SLOW NG Threshold	t_{WS}	$\frac{6635}{F_{OSCW}}$	$\frac{6655}{F_{OSCW}}$	$\frac{6675}{F_{OSCW}}$	s	
WDT Reset Time	t_{WRES}	$\frac{123}{F_{OSCW}}$	$\frac{128}{F_{OSCW}}$	$\frac{133}{F_{OSCW}}$	s	
CLK L Voltage	V_{CLKL}	-	-	0.8	V	
CLK H Voltage	V_{CLKH}	2.0	-	-	V	
ENWD L Voltage	V_{ENWDL}	-	-	0.8	V	
ENWD H Voltage	V_{ENWDH}	2.0	-	-	V	
RSTWD ON Resistance	R_{RSTWD}	50	100	200	Ω	I_{RSTWD} = 100 µA
CLK Input Current	I_{CLK}	10	22	55	µA	V_{CLK} = 5 V
ENWD Input Current	I_{ENWD}	5	11	28	µA	V_{ENWD} = 5 V
RST Leak Current	I_{LRST}	-	-	10	µA	V_{RST} = 5V
RSTWD Leak Current	I_{LRSTWD}	-	-	10	µA	V_{RSTWD} = 5V

Electrical Characteristic

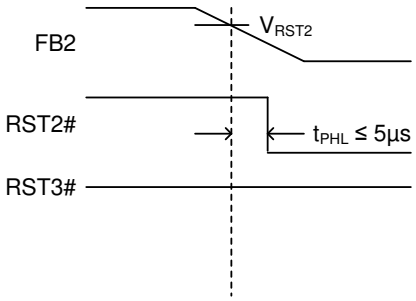
(Unless otherwise specified: -40 °C ≤ Ta ≤ +125 °C, 4 V ≤ V_{CC} ≤ 30 V, 5 V ≤ V_{S2} ≤ 10 V, 5 V ≤ V_{S3} ≤ 10 V)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
PG1, PG2, PG3						
PG ON - Resistance	R_{PG1} R_{PG2} R_{PG3}	0.5	1.0	2.0	kΩ	
PG1 Under Voltage Detection voltage	V_{LVPG1}	0.62	0.67	0.72	V	V_{FB1} Voltage
PG1 Under Voltage Hysteresis	V_{LVPH1}	20	-	100	mV	V_{FB1} Voltage
PG1 Over Voltage Detection Voltage	V_{OVPG1}	0.88	0.94	1.00	V	V_{FB1} Voltage
PG1 Over Voltage Hysteresis	V_{OVPH1}	20	-	100	mV	V_{FB1} Voltage
PG2 Under Voltage Detection Voltage	V_{LVPG2}	3.00	3.07	3.14	V	V_{FB2} Voltage
PG2 Under Voltage Hysteresis	V_{LVPH2}	20	-	80	mV	V_{FB2} Voltage
PG2 Over Voltage Detection Voltage	V_{OVPG2}	3.45	3.53	3.60	V	V_{FB2} Voltage
PG2 Over Voltage Hysteresis	V_{OVPH2}	20	-	80	mV	V_{FB2} Voltage
PG3 Under Voltage Detection Voltage	V_{LVPG3}	4.50	4.625	4.75	V	V_{O3} Voltage
PG3 Under Voltage Hysteresis	V_{LVPH3}	30	-	150	mV	V_{O3} Voltage
PG3 Over Voltage Detection Voltage	V_{OVPG3}	5.25	5.38	5.50	V	V_{O3} Voltage
PG3 Over Voltage Hysteresis	V_{OVPH3}	30	-	150	mV	V_{O3} Voltage
PG Leak Current	I_{LPG}	-	-	10	μA	V_{PG} = 5V
SEQ 2, SEQ 3						
SEQ2 ON Resistance	R_{SEQ2}	0.5	1.0	2.0	kΩ	I_{SEQ2} = 100 μA
SEQ3 ON Resistance	R_{SEQ3}	0.5	1.0	2.0	kΩ	I_{SEQ3} = 100 μA
SEQ Leak Current	I_{LSEQ}	-	-	10	μA	V_{SEQ} = 5V

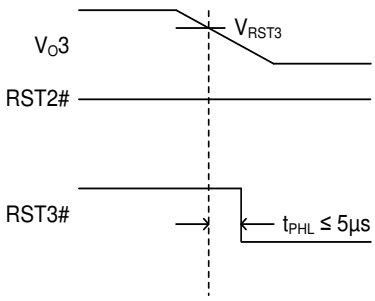
Reset response time (t_{PHL})



UVLO, RST# Delay time



FB2, RST2# Delay time



VO3, RST3# Delay time

Typical Performance Curves

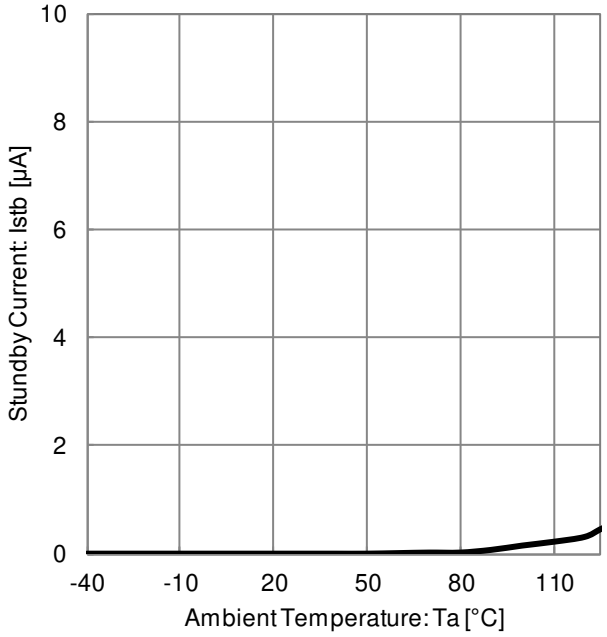


Figure 1. Standby Current vs. Temperature

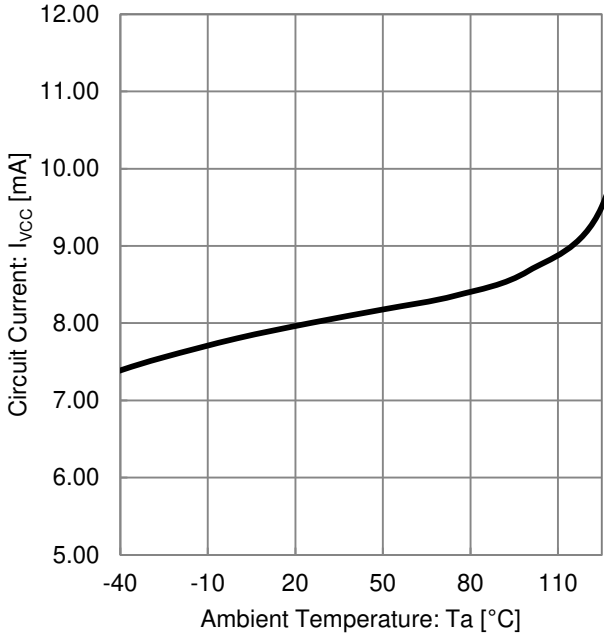


Figure 2. Circuit Current vs. Temperature

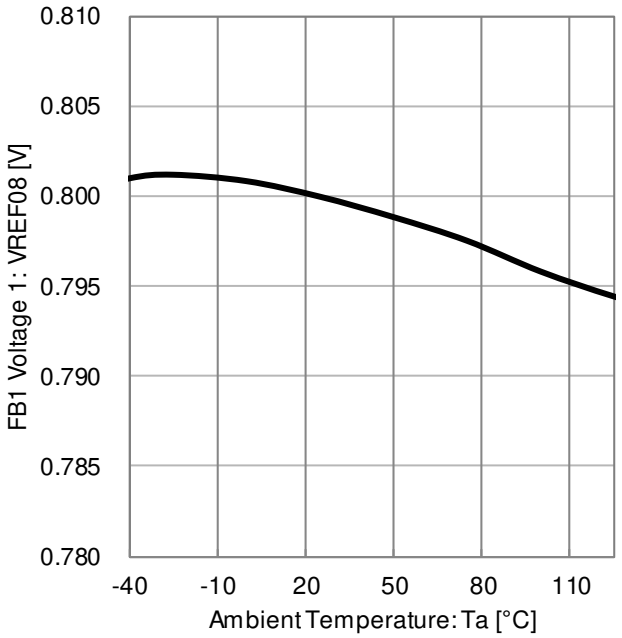


Figure 3. FB1 Voltage vs. Temperature

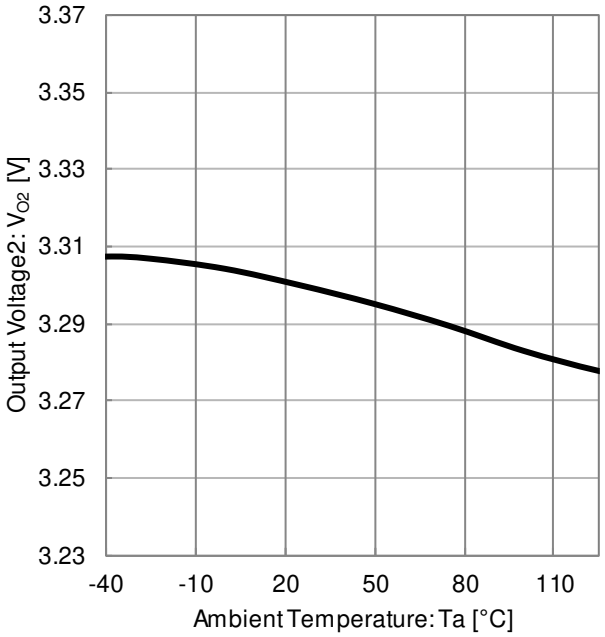


Figure 4. Output Voltage2 vs. Temperature

Typical Performance Curves

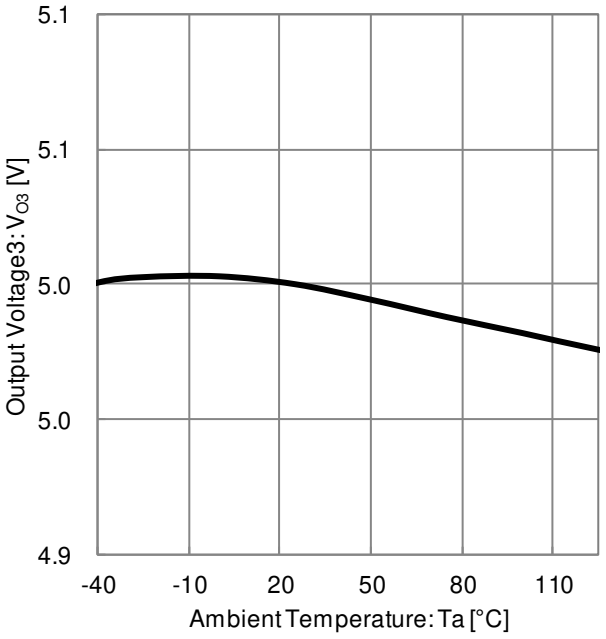


Figure 5. Output Voltage3 vs. Temperature

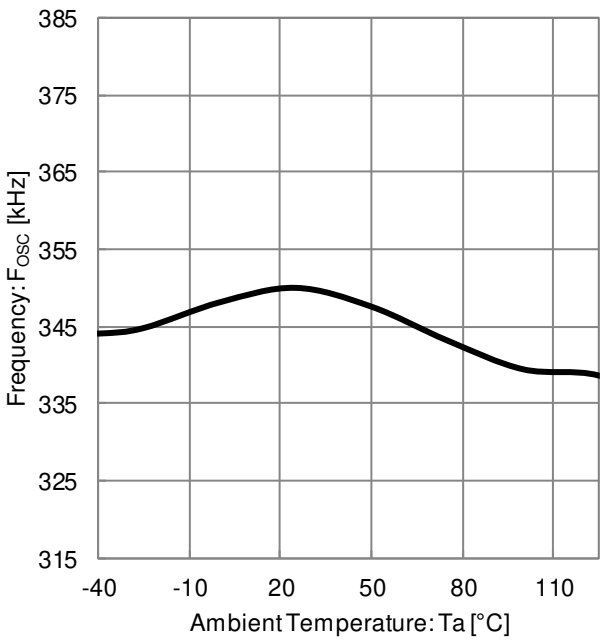


Figure 6. Frequency vs. Temperature

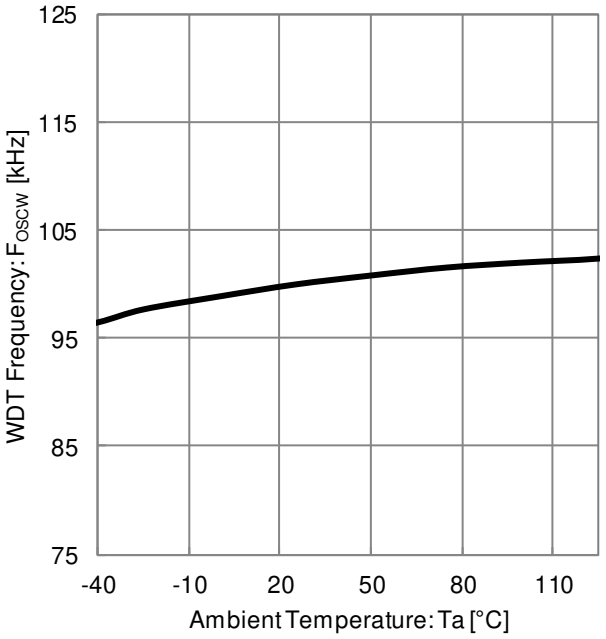


Figure 7. WDT Frequency vs. Temperature

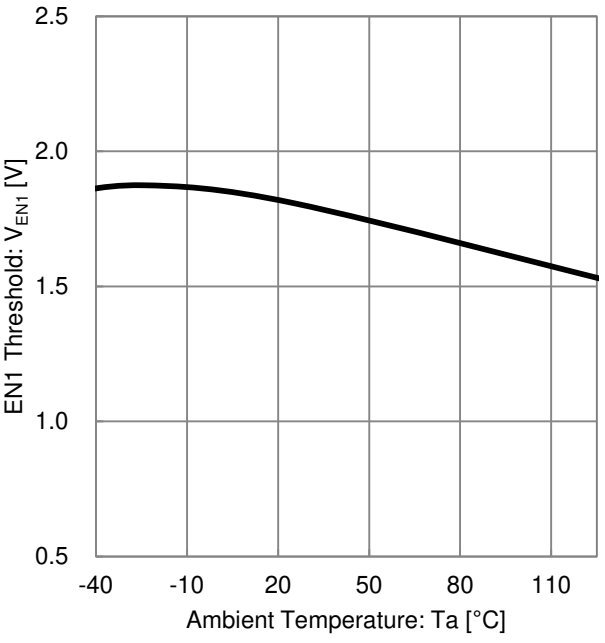


Figure 8. EN1 Threshold vs. Temperature

Typical Performance Curves

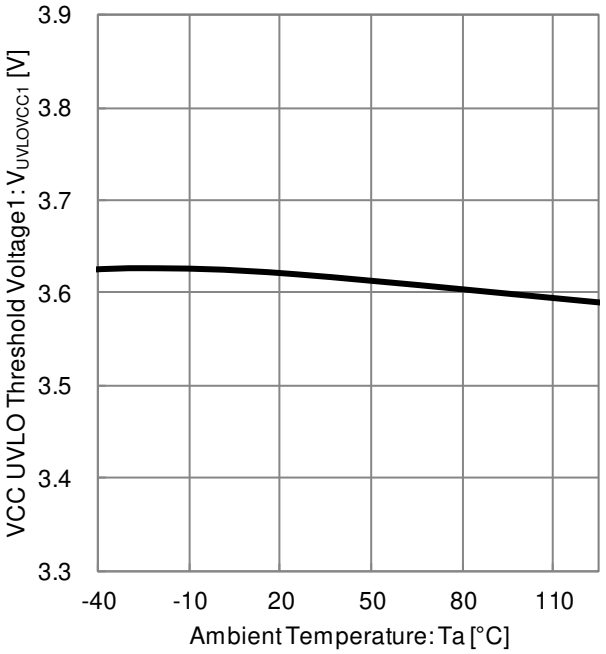


Figure 9. VCC UVLO Threshold Voltage1 vs. Temperature

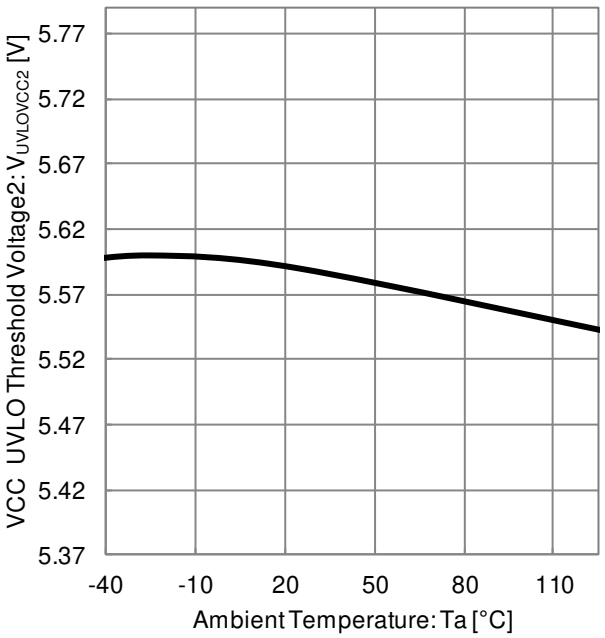


Figure 10. VCC UVLO Threshold Voltage2 vs. Temperature

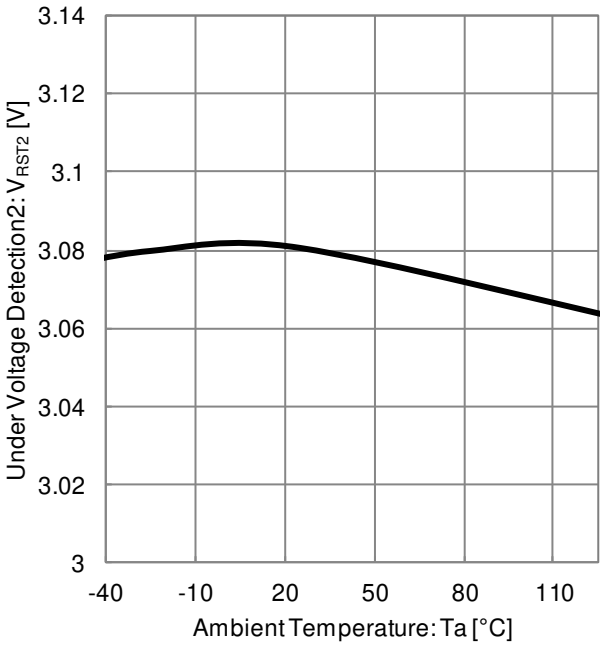


Figure 11. Under Voltage Detection2 vs. Temperature

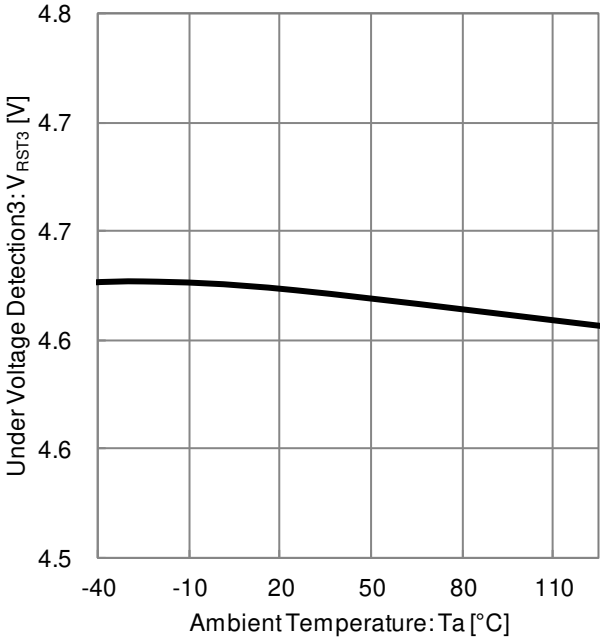


Figure 12. Under Voltage Detection3 vs. Temperature

Typical Performance Curves

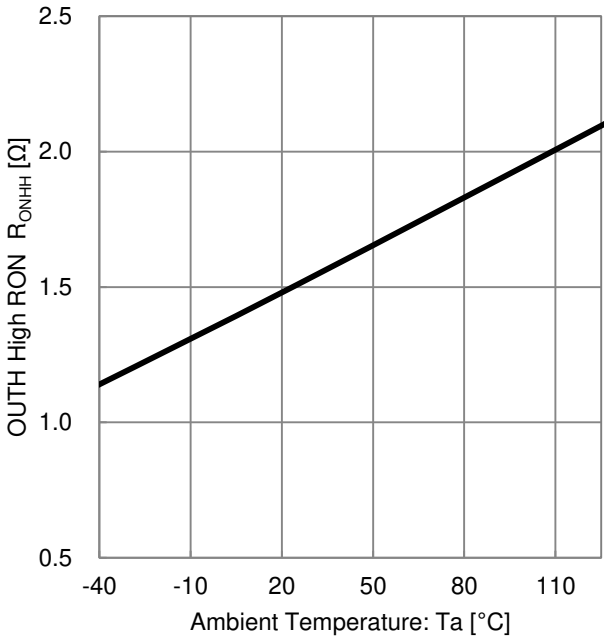


Figure 13. OUTH High RON vs. Temperature

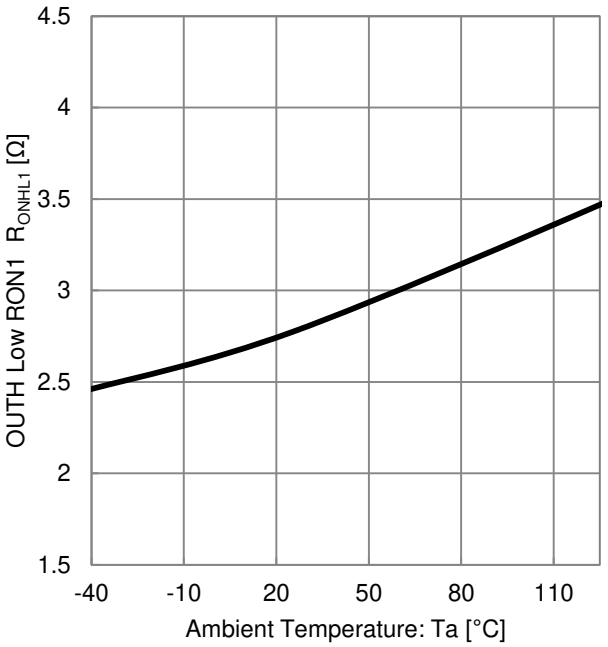


Figure 14. OUTH Low RON1 vs. Temperature

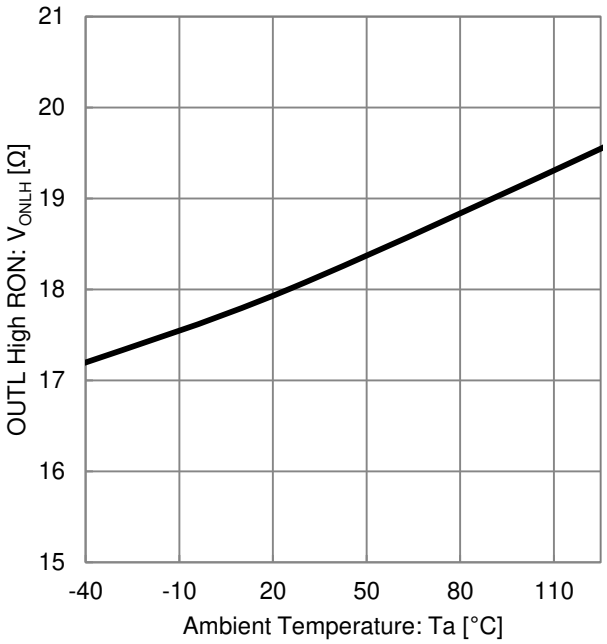


Figure 15. OUTL High RON vs. Temperature

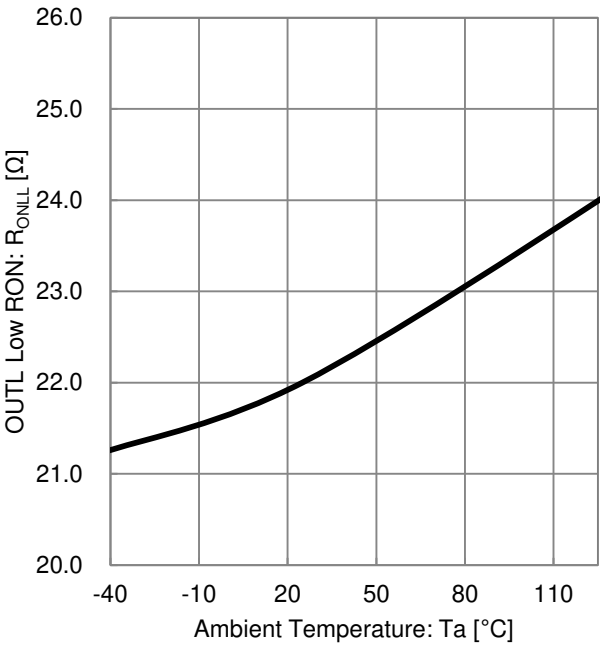


Figure 16. OUTL Low RON vs. Temperature

Typical Performance Curves

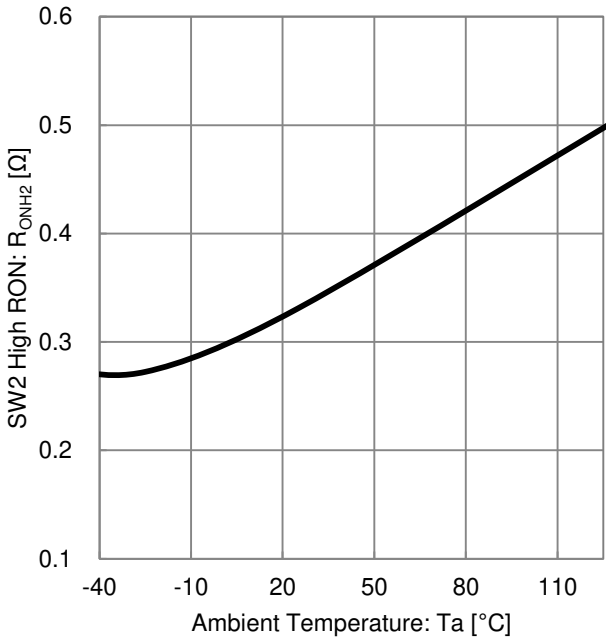


Figure 17. SW2 High RON vs. Temperature

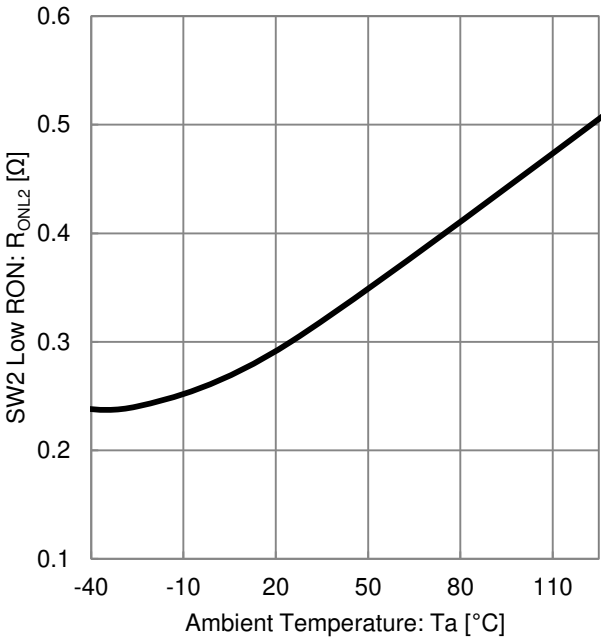


Figure 18. SW2 Low RON vs. Temperature

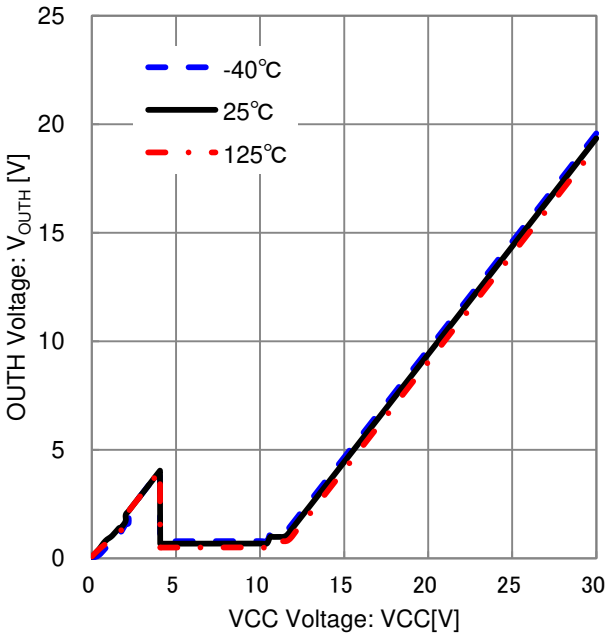


Figure 19. OUTH Voltage vs. VCC

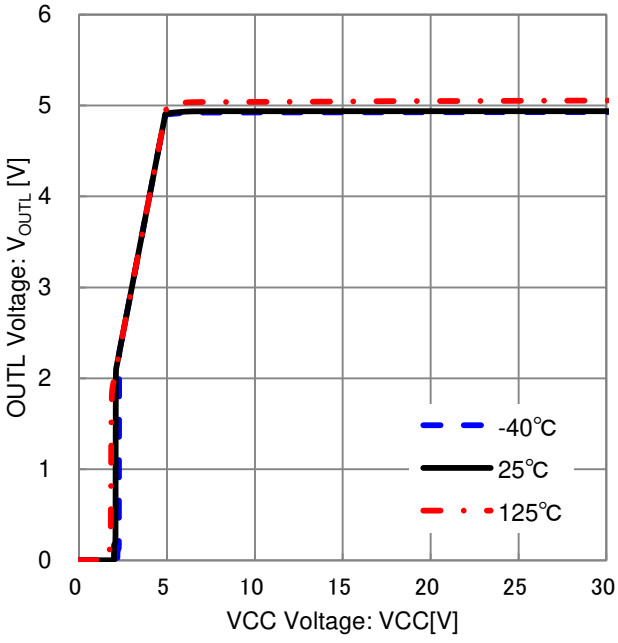


Figure 20. OUTL Voltage vs. VCC

Description of Blocks

■ Under Voltage Lockout circuit (VCC_UVLO)
This is a Low Voltage Error Prevention Circuit.
In case of SEL_UVLO = OPEN, if the VCC drops below 3.6 V (Typ), the VCC_UVLO is activated and the output circuit shuts down. In case of SEL_UVLO = GND, if the VCC drops below 5.58 V (Typ), the VCC_UVLO is activated and the output circuit shuts down. When Vcc power supply off, Vcc voltage drop down low enough and make UVLO detect function, then the voltage of OUTH is same as VCC and OUTL is same as VDD.

■ Thermal Shut Down (TSD)
The TSD protects the device from overheating.
If the chip temperature (Tj) reaches 175 °C (Typ), the circuit shuts down

■ Oscillation Frequency (OSC)
The oscillator frequency is fixed by RT pull-down resistance value. Switching frequency of DC / DC1 and DC / DC2 are as same as OSC, but with a 180 °C difference in phase angle.

■ Over Voltage Detection (OVD)
If DC / DC1, DC / DC2 and LDO output voltage exceed OVD, each PGOOD Pin turns Low.
DC / DC1 OVD monitors FB1 voltage, DC / DC2 OVD monitors FB2 voltage and LDO OVD monitors V_{O3} voltage.
PGOOD pin is an open drain output. And the pull up resistor should be connected to PGOOD for using this function.

■ Low Voltage Detection (LVD)
If DC / DC1, DC / DC2 and LDO output voltage below LVD, each PGOOD Pin turns Low.
DC / DC1 LVD monitors FB1 voltage, DC / DC2 LVD monitors FB2 voltage and LDO LVD monitors V_{O3} voltage.
PGOOD pin is an open drain output, and the pull up resistor should be connected to PGOOD for using this function.

■ Under Voltage Lockout (VS_UVLO)
VS_UVLO prevents Error function at low VS voltage.
If the VS2 or VS3 drops below 3.9 V (Typ), the VS_UVLO is activated and the DC / DC2 or LDO is turned off.

■ Over Current Protection (OCP1_L, OCP1_H)
DC / DC1 has two levels over current protection with different control system as shown below.

1) OCP1 low level operations
In case the voltage between VCC and CL exceeds 100 mV (Typ), OCP1 (low level operation) is activated and the switching pulse width of OUTH and the switching pulse width of OUTL are limited. Also, if this pulse limited status continues during 256 clock times where the FB1 pin voltage drops below the under voltage detection level, the SS1 pin capacitor is discharged and the output is turned OFF during 8192 clock times.
During the 8192 clock in which the output is turned OFF, the logic of OUTH and OUTL pin changes as follows; OUTH = H and OUTL = H. After the 8192 clock the chip returns to normal operations and the SS1 pin is recharged. The clk is the same frequency as OSC.

2) OCP1 high level operations
In case the inter VCC - CL pin voltage exceeds 200 mV (Typ), the chip goes into OCP1 high level operations, the SS1 pin capacitor is discharged and the output is turned OFF for 8192 clk. During the 8192 clock in which the output is turned OFF, the logic of OUTH and OUTL pin changes as follows; OUTH = H and OUTL = H. After the 8192 clock the chip returns to normal operations and the SS1 pin is recharged. clk and OSC has the same frequency.

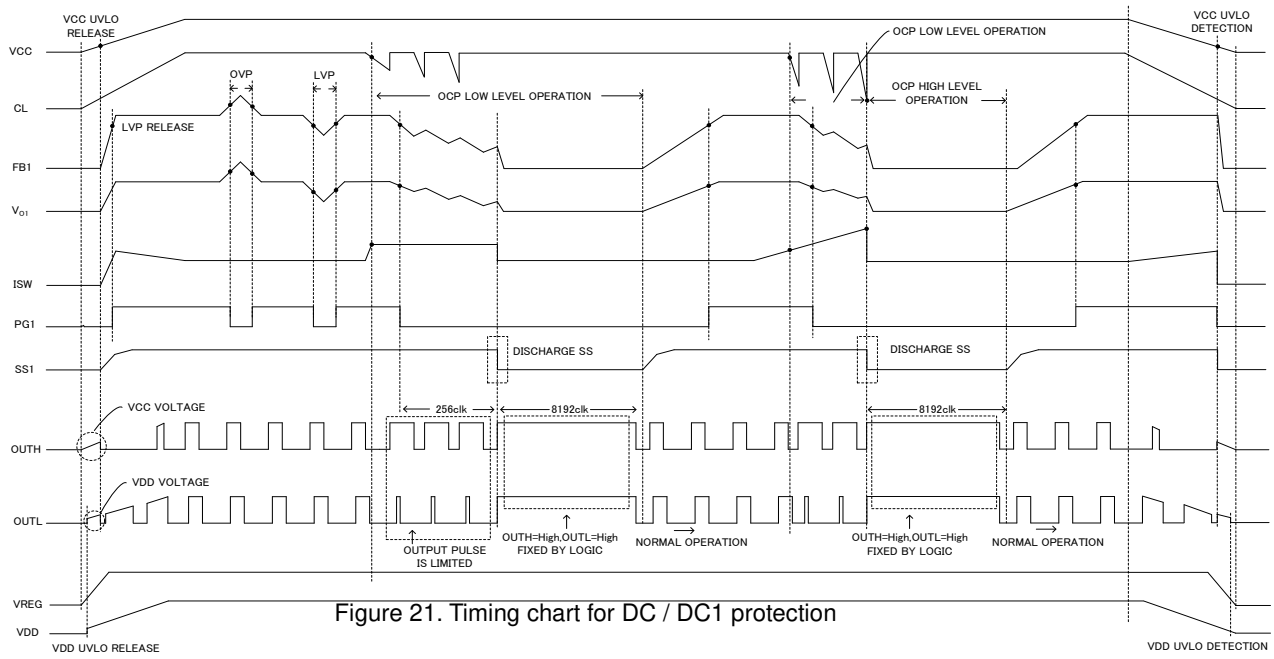


Figure 21. Timing chart for DC / DC1 protection

・DC / DC2

If output current of SW2 exceeds OCP, SW2 ON duty is limited and the output voltage is lowered.
If FB2 voltage is below SCP and after 256 clk, DC / DC2 is turned off. After 256 clk, DC / DC2 return to normal operation. The clk is the same frequency as OSC.

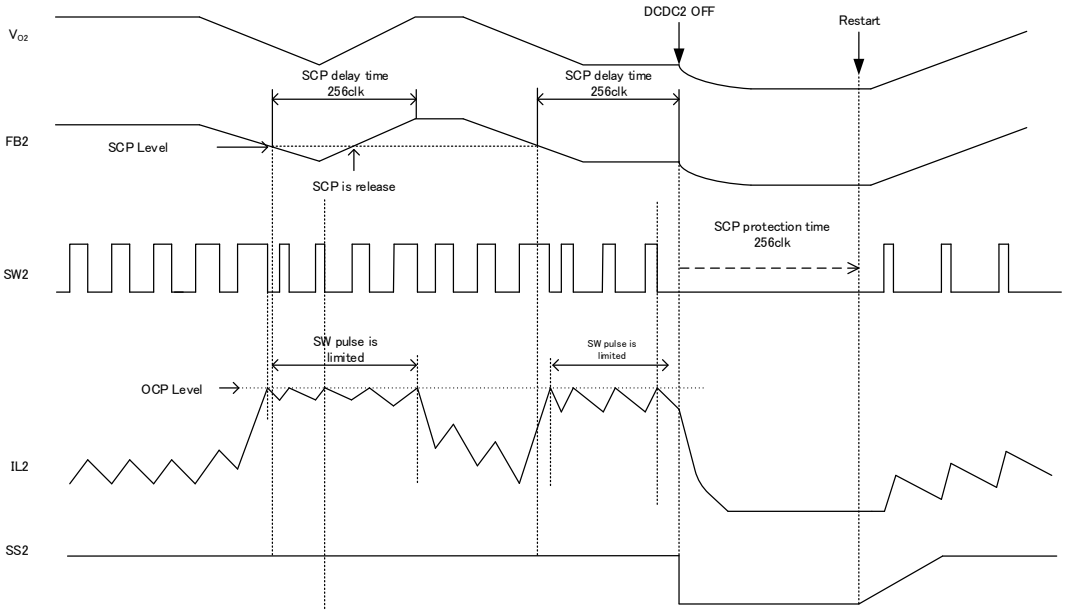
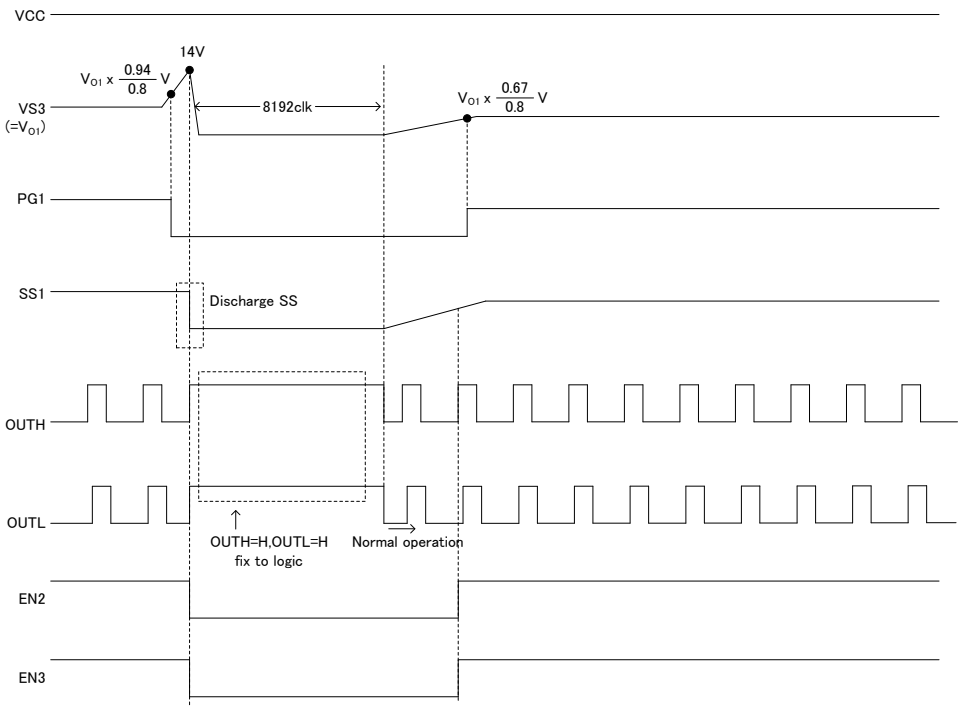


Figure 22. DC / DC2 Over current protection

・If the output current of LDO exceed OCP, the output current is limited and the output voltage is lowered. (fold-back OCP)

■ Over Voltage Protection (VS3 OVP)

・In case the VS3 voltage exceeds 14 V (Typ), the chip goes into VS3 OVP, the SS1 capacitor is discharged and the output is turned OFF for 8192 clock. During the 8192 clock in which the output is turned OFF, the logic of OUTH and OUTL changes as follows; OUTH = H and OUTL = H. After the 8192 clock the chip returns to normal operations and the SS1 is recharged. The clk is the same frequency as OSC.



All numerical values are Typical.

Figure 23. VS3 Over voltage protection

■ RST#, RSTWD# pin

In case of ENWD = L, RSTWD# voltage is pull up voltage.
In case of ENWD = H, WDT operation starts. If WDT is in abnormal condition, RSTWD# outputs 'L'.
If V_{O2} or V_{O3} voltage is below the LVD, reset voltage (RST#) output is low.
If both of V_{O2} and V_{O3} exceed the reset release voltage, CT is charged. After tPOR, reset voltage outputs high.

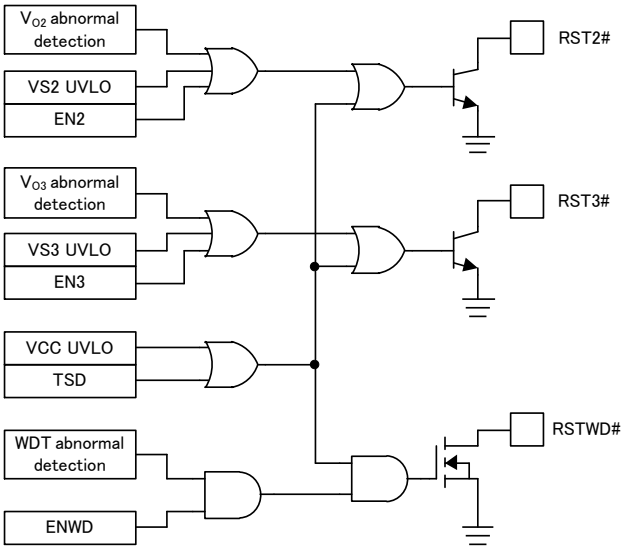


Figure 24. RST#, RSTWD# Logic Circuit

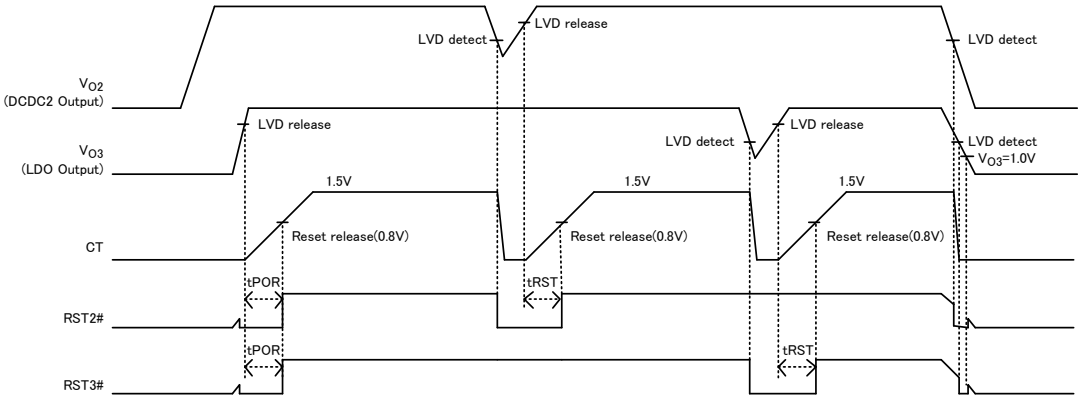


Figure 25. RST2#, RST3# Timing Chart

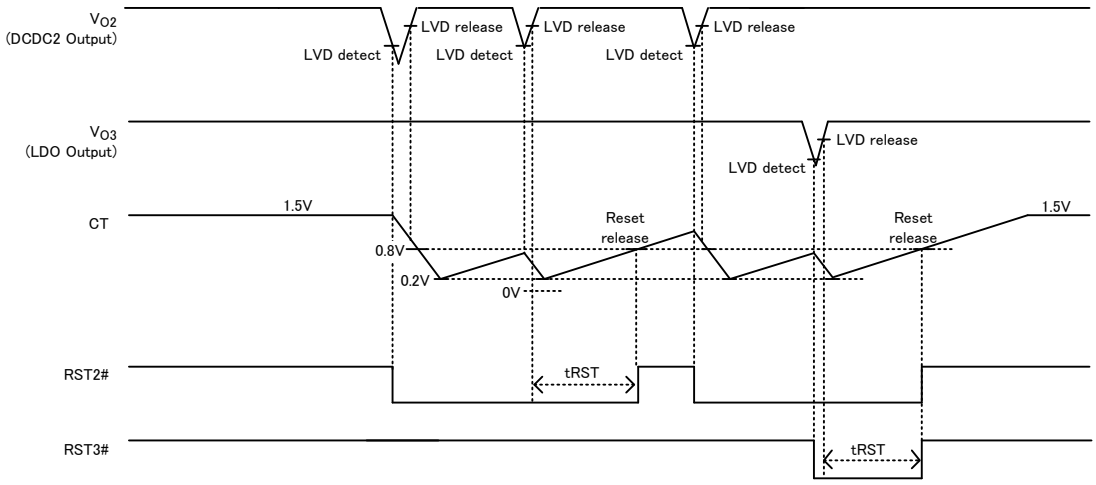


Figure 26. Timing chart (detection of LVD between reset)

■ Oscillator for Watch Dog Timer (FOSCW)

This block creates a reference frequency of the Watch Dog Timer. The oscillation frequency is determined by the RTW resistance. The oscillation frequency can be set in the range of 50 kHz to 250 kHz.

■ WATCH DOG TIMER

Microcontroller (μC) operation is monitored with CLK pin. Window watch dog timer is included to enhance the assurance of the system. WDT starts operating when ENWD becomes high. CLK pin voltage must be Low when ENWD switches to High.

WDT monitors both edges of CLK pin (rising edge and falling edge). If width of both edges are shorter than Fast NG or longer than Slow NG, R_{STWD} turns low for a WDT reset time (t_{WRES}). Since the width of Fast NG and Slow NG depends on a number of F_{OSCW}, Fast NG and Slow NG are variable by frequency of F_{OSCW}. If F_{OSCW} is unusual (ex. RTW is short to ground), R_{STWD} turns low. In case of using RSTWD, pull-up resister is needed because RSTWD is an open drain.

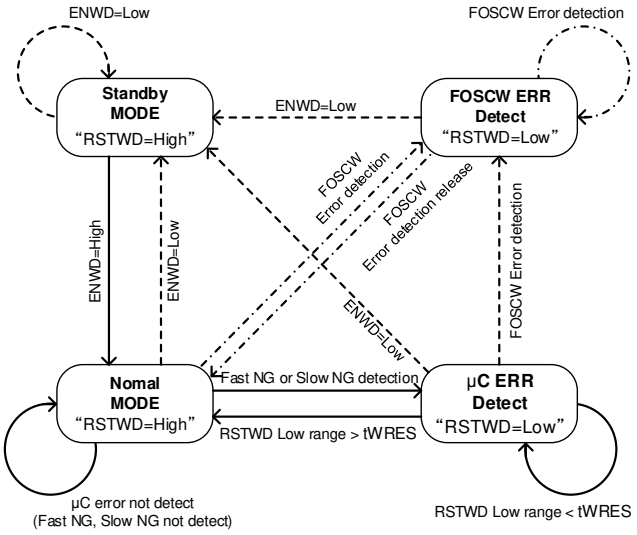
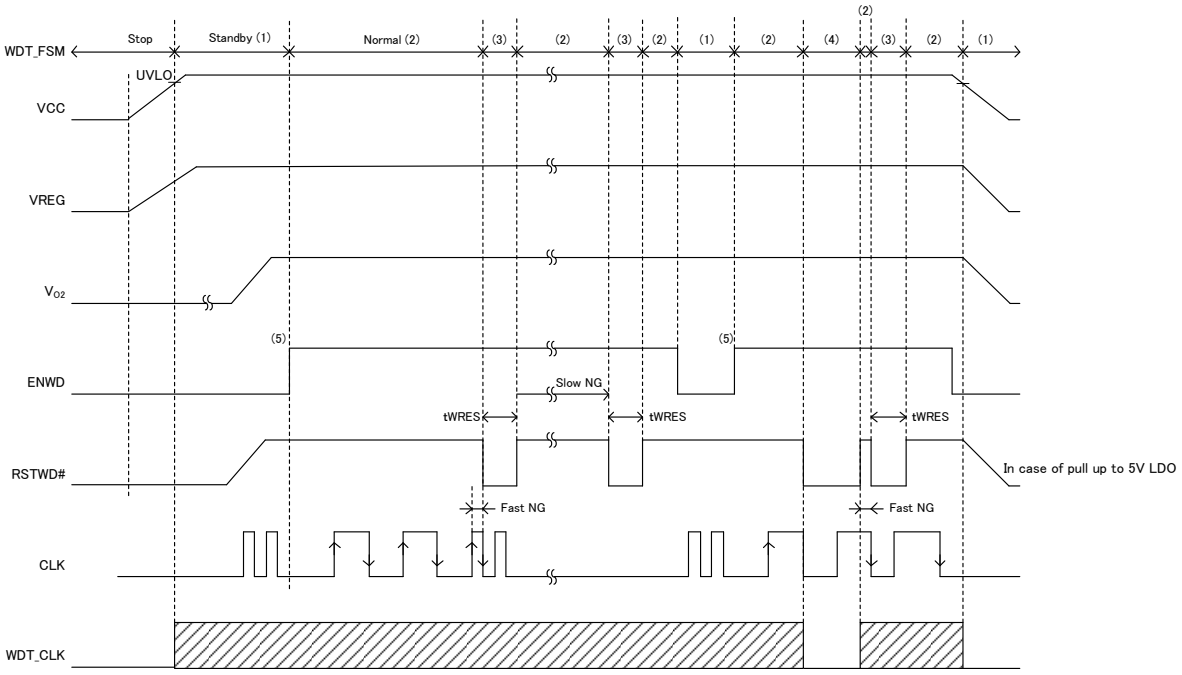


Figure 27. Witch Dog Timer State Change Diagram (WDT FSM)



(1): Standby Mode, (2): Normal Mode, (3): Microcontroller Error Detect, (4): OSC_WDT Error Detect (See Figure 27 WDT FSM)
(5): When ENWD is changed Low to High, it is necessary that CLK is Low.

Figure 28. WDT Timing Chart

External Components Selection

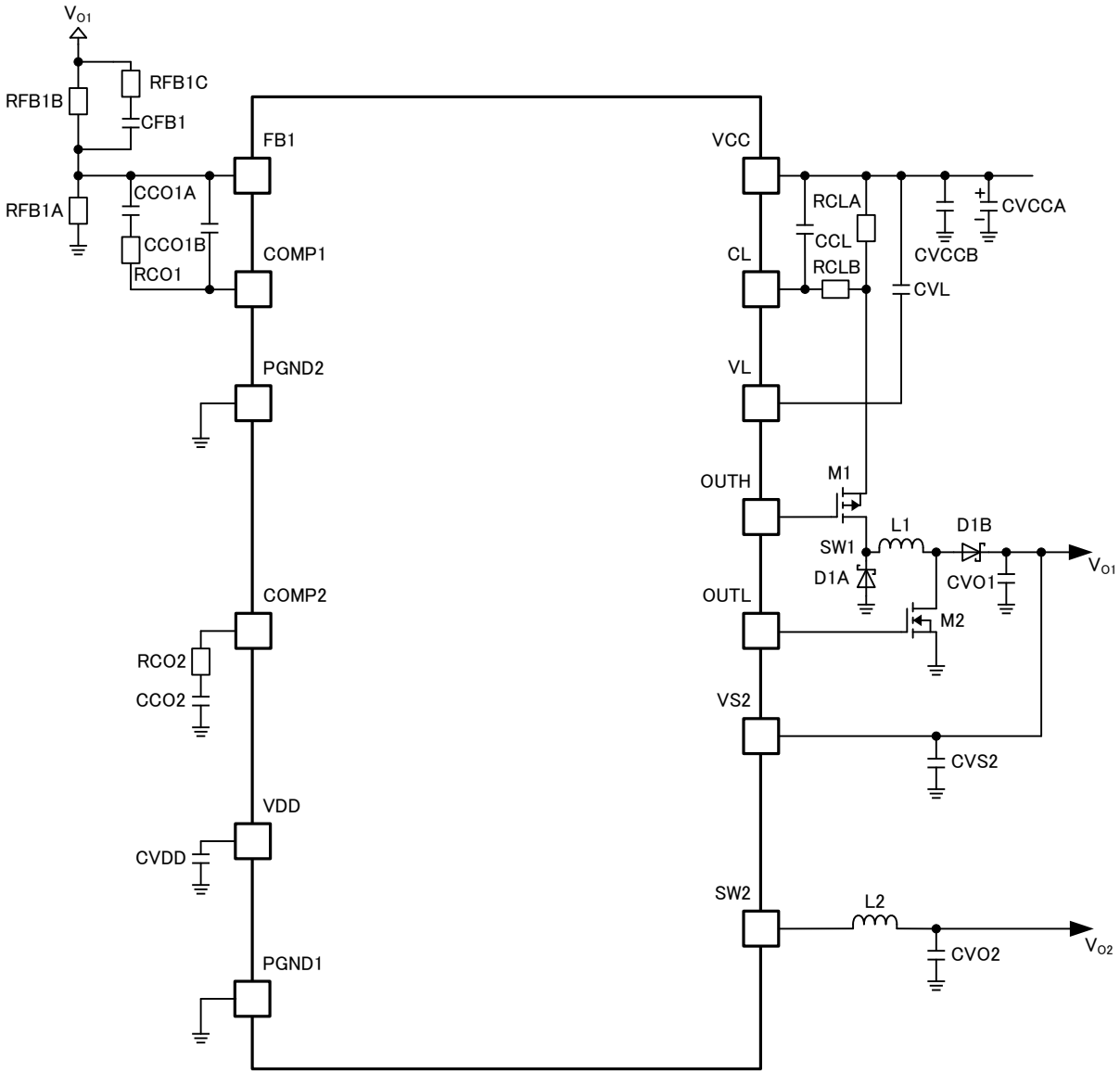


Figure 29. Application Example 1

(1) Buck mode (V_{CC}>>V_{O1})
In case the input voltage is high compared to the output voltage, the chip will go into buck mode, resulting OUTH to repeatedly switch between H and L and that the OUTL will go to L (= OFF).
This operation is the same as that of standard step-down switching regulators.
Shown below are the OUTH and OUTL waveforms on the right.
ON duty of PMOS (D_{pon}), VCC and V_{O1} are shown in the following equation.

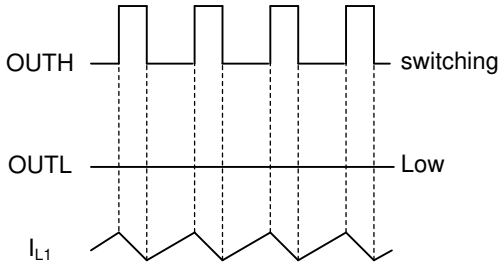


Figure 30

$$V_{cc} \times D_{pon} = V_{O1} \quad \text{(eq. 1)}$$

(2) Buck-Boost mode (V_{CC} ≈ V_{O1})
In case the input voltage is close to the output voltage, the chip will go into buck-boost mode, resulting both the OUTH and OUTL to repeatedly switch between H and L. Concerning the OUTH, OUTL timing, the chip internally controls where the following sequence is upheld; when OUTH: H → L, OUTL: H → L.
Shown below are the OUTH and OUTL waveforms.

① V_{CC} > V_{O1}

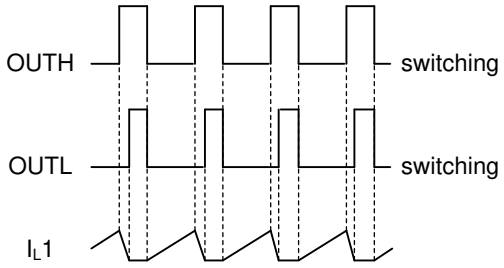


Figure 31

② V_{CC} < V_{O1}

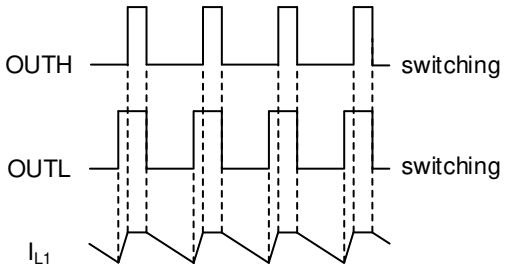


Figure 32

*The timing excludes the SW delay

The relationship between ON duty of PMOS (D_{pon}), ON duty of NMOS (D_{non}), V_{CC} and V_{O1} is shown in the following equation.

$$\frac{V_{cc} \times D_{pon}}{(1-D_{non})} = V_{O1} \quad \text{(eq. 2)}$$

The calculation formula of D_{pon} and D_{non} are shown in page 20.

(3) Boost mode (V_{CC} << V_{O1})
In case the input voltage is low compared to the output voltage, the chip will go into boost mode, resulting OUTH to go to L (= ON) and OUTL will repeatedly switch between H and L. This operation is the same as that of standard step-up switching regulators.
Max duty of OUTL is limited by internal circuit.
ON duty of NMOS (D_{non}), V_{CC} and V_{O1} are shown in the following equation.

$$V_{O1} \times (1 - D_{non}) = V_{cc} \quad \text{(eq. 3)}$$

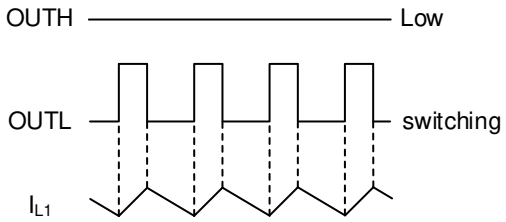


Figure 33

(4) Voltage for Mode Switching and Duty Control
In the event of mode switching from Boost to Buck-Boost or vice versa, mode switching input voltage is dependent on output voltage, the gain of inverting amplifier and the cross duty. The general description is shown below.

The duty of OUTH is controlled by output of error amp (COMP1) and SLOPE voltage.
Also, OUTL duty is controlled by the output voltage of the inverting amplifier in chip (BOOSTCOMP) and SLOPE voltage.
In case VCC = V_{O1}, COMP1 voltage becomes equal to BOOSTCOMP voltage, and switching control timing of OUTH and OUTL becomes identical accordingly.

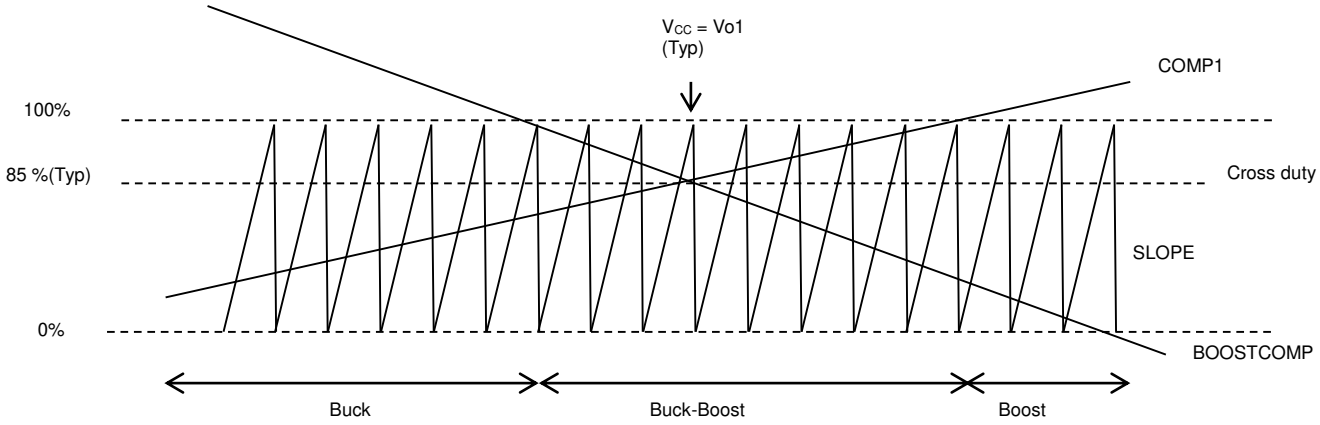


Figure 34. Buck-Boost operation controlled by COMP1, BOOSTCOMP and SLOPE voltage

ON duty of PMOS in this condition is called the cross duty (Dx = 0.85, Typ). D_{pon} and D_{non} can be calculated by the following equation, assuming the gain of the inverting amplifier as A (1.5, Typ).

$$D_{non} = 1 - D_X + A(D_{pon} - D_X)$$
$$= 1.5D_{pon} - 1.125 \quad \text{(Note 1)} \quad \text{(eq. 4)}$$

From eq.3, eq.4 and D_{pon} = 1, the input voltage at transition between buck - boost and boost mode is calculated as follows;

$$V_{CC} = \{D_X - A(1 - D_X)\}V_{O1}$$
$$= 0.625 \times V_{O1} \quad \text{(Note 1)} \quad \text{(eq. 5)}$$

Also, from eq.1, eq.4 and D_{non} = 0, the input voltage at transition between buck - boost and buck mode is calculated as follows;

$$V_{CC} = \frac{V_{O1} \times A}{\{(1+A)D_X - 1\}} = 1.333 \times V_{O1} \text{ (Note 1)}$$

Be sure to confirm Dx and A value under the actual application because these parameters vary depending on conditions of use and external components selected.
Dx varies with oscillating frequency shown in Figure 35.
In addition, 'A' value can be calculated by D_{non} / D_{pon}.

(Note 1) A = 1.5 (Typ), Dx = 0.85 (Typ)

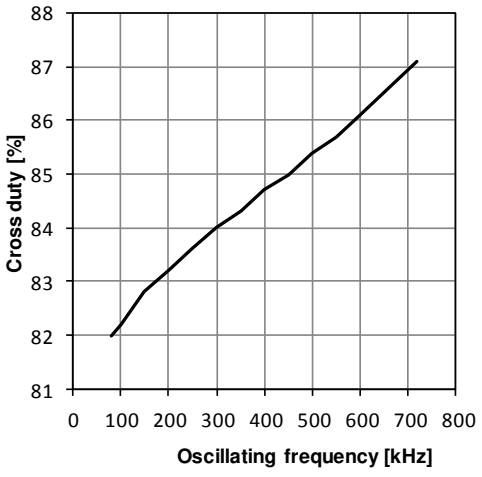


Figure 35. Cross duty vs. frequency characteristics

1. Setting the output L1, L2 value (DC / DC1, DC / DC 2)

It is necessary to use LC filter. The use of a big inductor helps lower the inductor ripple current and output ripple voltage, even though cost is higher and the size is bigger.
The inductance is shown in the following equation.
The coil value significantly influences the output ripple current. Thus, as seen bellow, the larger coil and the higher switching frequency, the lower ripple current it becomes. The optimal output ripple current setting is 30 % of maximum current.

・DC / DC1 (at Buck - Boost)

Buck mode	Buck-Boost mode		Boost mode
$\Delta I_{L1} = \frac{(V_{CC} - V_{O1}) \times V_{O1}}{L1 \times V_{CC} \times f}$	VCC > V_{O1} $\Delta I_{L1} = \frac{(V_{CC} - V_{O1}) \times D_{pon}}{L1 \times f}$	VCC < V_{O1} $\Delta I_{L1} = \frac{(V_{O1} - V_{CC}) \times D_{noff}}{L1 \times f}$	$\Delta I_{L1} = \frac{(V_{O1} - V_{CC}) \times V_{CC}}{L1 \times V_{O1} \times f}$
$\overline{I_{L1}} = I_{O1}$	$\overline{I_{L1}} = \frac{I_{O1}}{D_{noff}}$		

ΔI_L: Ripple current, $\overline{I}_L$: Average coil current, f: Oscillating frequency

$$D_{pon}: \text{PMOS ON } duty = V_{O1} \times Dx\,(1+A) \,/\, (V_{CC} + A \times V_{O1}) = 2.13 \times V_{O1} \,/\, (V_{CC} + 1.5 \times V_{O1}) \quad (Typ)$$

$$D_{noff}: \text{NMOS OFF } duty = (1+A) \times Dx - A \times Dpon = 2.13 - 1.5 \times Dpon \quad (Typ)$$

・DC / DC1 (at Buck)

$$\Delta I_{L1} = \frac{(V_{CC(MAX)} - V_{O1}) \times V_{O1}}{V_{CC(MAX)} \times f_{SW} \times L1}$$

($V_{CC\,(MAX)}$: Maximum input voltage, ΔI_{L1}: Inductor ripple current, V_{O1}: Output voltage 1, f_{SW}: Oscillating frequency)

・DC / DC2 (at Boost)

$$\Delta I_{L2} = \frac{(V_{S2(MAX)} - V_{O2}) \times V_{O2}}{V_{S2(MAX)} \times f_{SW} \times L2}$$

($V_{S2\,(MAX)}$: Maximum input voltage, ΔI_{L2}: Inductor ripple current, V_{O2}: Output voltage 2, f_{SW}: Oscillating frequency)

An output current in excess of the coil current rating will cause magnetic saturation to the coil and decrease efficiency.
The following equation shows the peak current I_{LMAX} assuming the efficiency as η.
It is recommended to secure sufficient margin to ensure that the peak current does not exceed the coil current rating.

$$I_{LMAX} = \frac{1}{\eta}\left(\overline{I_L} + \frac{\Delta I_L}{2}\right)$$

Use low resistance (DCR, ACR) coils to minimize coil loss and increase efficiency.

When load current is low, DC / DC1 operates discontinuously so set ΔI_L in a way it operates continuously (I_{L1} keeps continuously flowing).
The condition of continuous operation is shown in the following equation.

・DC / DC1

$$I_{O1} > \frac{(V_{CC} - V_{O1}) \times V_{O1}}{2 \times V_{CC} \times f_{SW} \times L1}$$

(I_{O1}: Load current)

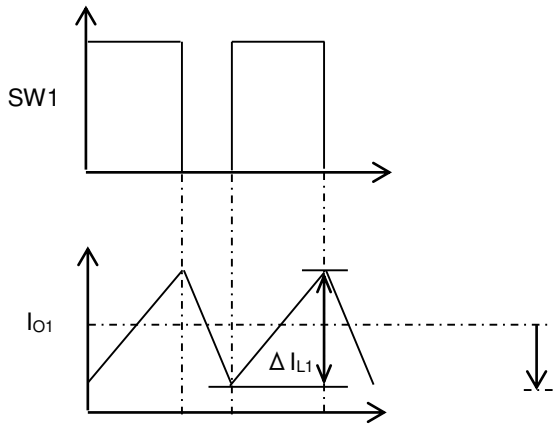


Figure 36. Continuous operation

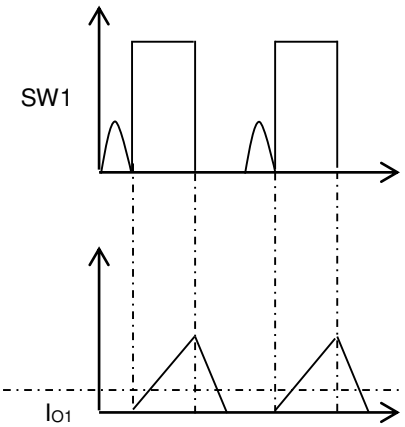


Figure 37. Discontinuous operation

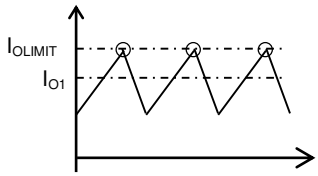


Figure 38. Over current detection

Shielded type inductor (closed magnetic circuit) is recommended. Open magnetic circuit type inductor can be used for low cost applications if noise is not of concern. But in this case, there is magnetic field radiation between the parts and thus keep enough spacing between the parts.

For ferrite core inductor type, please note that magnetic saturation may occur. Saturation needs to be avoided at all times. Precautions must be taken into account on the given provisions of the current rating because it differs according to each manufacturer.

Please confirm the rated current at the maximum ambient temperature of the application to the coil manufacturer.

2. Setting the output capacitor C_{VO1}, C_{VO2} value (DC / DC1, DC / DC 2)

The maximum output current is limited by the over current protect operation current as shown in below equation.

$$I_{O(MAX)} = I_{LIMIT(MIN)} - \frac{\Delta I_L}{2}$$

$I_{O\,(MAX)}$: Maximum output current, $I_{LIMIT\,(MIN)}$: Minimum over current protect operation level (0.9 A) (1ch is external set)
When the ΔI_L is low, the Inductor core loss (iron loss), the loss due to ESR of the output capacitor and the ΔV_{PP} will become low. ΔV_{PP} is expressed as follows:

Buck mode	Boost mode
$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{8 \times C_{VO} \times f_{SW}}$	$\Delta V_{PP} = I_{LMAX} \times R_{ESR} + \frac{I_O}{C_{VO} \times f_{SW}} \times \frac{V_O - V_{CC}}{V_O}$

(*ESR*: Output capacitor equivalence series resistance, C_O: Output capacitor volume)

By using small ESR capacitor, ΔV_{PP} voltage level can be lowered. The benefit of ceramics capacitor is low ESR and small form factor.

The frequency characteristic of ESR from the datasheet of the manufacturer should be confirmed. Choose the ceramic capacitor which exhibits low ESR in the switching frequency range that is used On the other hand, DC biasing characteristics of the ceramic capacitor is significant so it needs to be carefully examined. For the voltage rating of the ceramic capacitor, twice or more than the maximum output voltage is usually required. By selecting these high voltages rating, it is possible to reduce the influence of DC bias characteristics. Moreover, in order to maintain good temperature characteristics, the one with the characteristic of X7R or better, is recommended.

Because the voltage rating of ceramic capacitor is low, the selection becomes difficult in the application with high output voltage. In that case, select electrolytic capacitor.

When using electrolytic capacitors, the voltage rating should be 1.2 times or more than the output voltage. Electrolytic capacitors have a high voltage rating, large capacity, small amount of DC biasing characteristic, and are generally inexpensive. Because typical failure mode is OPEN, it is effective to use electrolytic capacitor for applications where high reliability is required such as automotive. On the other hand, disadvantages are relatively high ESR and capacitance value drop at low temperatures. In this case, please take note that ΔV_{PP} may increase at low temperature conditions. Moreover, consider the lifetime characteristic of this capacitor.

When it comes to the capacitance C_O, the value needs to be less than the value calculated by the equations below.

・DC / DC 1

$$C_{O1\,(MAX)} = \frac{0.5\,ms \times (I_{L1imit\,(MIN)} - I_{O1\,(MAX)})}{V_{O1}}$$

・DC / DC 2

$$C_{O2\,(MAX)} = \frac{0.4\,ms \times (I_{L2imit\,(MIN)} - I_{O2\,(MAX)}}{V_{O2}}$$

($I_{LIMIT\,(MIN)}$: Minimum over current protect operation current (1ch is external set). 2ch = 0.9 A.
Soft start Min time DC / DC1: 0.5 ms, DC / DC2: 0.4 ms, Soft start setting refer to page 34)

Boot failure may occur if the capacitance value exceeds the limits explained above. If the capacitance value is extremely large, over-current protection may be activated by the inrush current at startup, and the output may not start.
Please confirm this on the actual circuit.

Capacitance values are critical parameter to determine the LC oscillation frequency. Transient response and loop stability are dependent on the C_{VO}. Please select after confirming the setting of the phase compensation circuit.

3. Setting the input capacitor C_{VCCA} / C_{VCCB}, C_{VS2} value (VCC, VS2)

Input capacitors reduce the power output impedance that is connected to VCC. Two types of capacitors are needed for input capacitor, i.e., decoupling capacitor C_{VCCB} and bulk capacitor C_{VCCA}. The decoupling capacitors of VCC and VS2 need to be 1 μF to 10 μF ceramics. More than 22 μF are necessary for the bulk capacitor of VCC. The ceramic capacitors are most effective when placed as close to VCC and VS2 as possible. At VCC, the ceramic capacitors need to be placed between VCC and GND and close to PMOS and the ground of schottky barrier diode. At VS2, the ceramic capacitor needs to be placed between VS2 and GND. Voltage rating is recommended to be more than 1.2 times the maximum input voltage and twice the normal input voltage.

The bulk capacitor prevents line voltage drop and serves as a backup power supply to maintain the input voltage. The low ESR electrolytic capacitor with large capacitance is suitable for the bulk capacitor. It is necessary to select the capacitance value which best fits to each application. In case impedance of input side is high such as long wiring between the power supply and VCC, input voltage gets unstable when output impedance of the power supply increases resulting in oscillation or degraded ripple rejection characteristics. Large capacitor is needed in this case. It is necessary to verify that the output does not turn off in the event of Vcc drop due to transient in the actual circuit.
Make sure not to exceed the rated ripple current of the capacitor in this case. The RMS of the input ripple current can be obtained from the following equation.

・DC / DC 1

$$I_{CVCCB\,(RMS)} = I_{O1} \times \frac{\sqrt{V_{O1}\,(V_{CC} - V_{O1})}}{V_{CC}}$$

($I_{CVCCB\,(RMS)}$: Input ripple current RMS value)

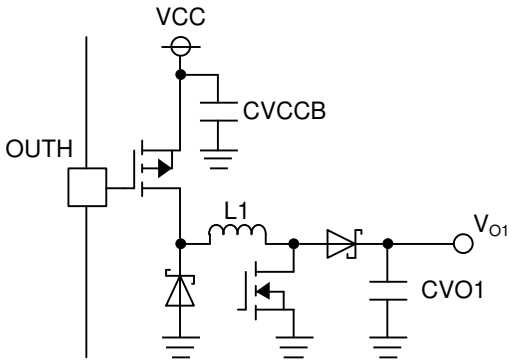


Figure 39. VCC pin

・DC / DC 2

$$I_{CVS2\,(RMS)} = I_{O2} \times \frac{\sqrt{V_{O2}\,(V_{S2} - V_{O2})}}{V_{S2}}$$

($I_{CVS2\,(RMS)}$: Input ripple current RMS value)

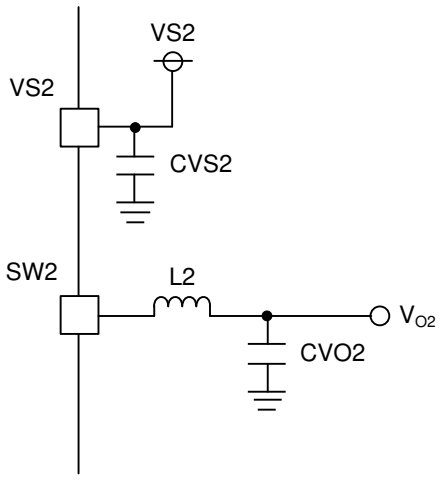


Figure 40. VS2 pin

In automotive and other applications requiring high reliability, it is recommended that capacitors are connected in parallel to reduce the risk of electrolytic capacitors drying out. In case of ceramic capacitors, it is recommended make it two in series and two in parallel structures to reduce the risk of destruction due to short circuit event. Currently capacitors containing two in series or two in parallel in one package are available in the market so please contact suppliers.

4. Setting the input capacitor C_{VS3} value
   Place a capacitor which is greater than 0.1 µF between VS3 and GND. Select the capacitor considering filter circuit for power supply and VS3. Since the capacitance value is dependent on the board layout and pattern, secure enough margin when selecting the capacitor. Capacitors that have good voltage and temperature characteristics are recommended.

5. Setting the output capacitor C_{VREG} value
   Place a capacitor between the VREG pin and GND to avoid oscillation. 0.47 µF or greater capacitance is recommended. C_{VREG} can be electrolytic capacitor or ceramic capacitor. Secure the capacitance of 0.47 µF or greater in the voltage and temperature range in actual operating conditions. The change in capacitance value by temperature may cause oscillation. Select the capacitors which have good temperature characteristics (X7R or better), good DC bias characteristics with high voltage rating. In case significant voltage swing and load transient are expected, make sure to carry out thorough evaluation before making a decision on the capacitance value.

6. Setting the output capacitor C_{VDD} value
   Place a capacitor between VDD and GND. The capacitance needs to be 0.01 µF or greater (OUTL = open) and1 µF or greater (OUTL in use). C_{VDD} can be electrolytic or ceramic. Secure high enough capacitance in the voltage and temperature range in actual operating conditions. The change in capacitance value by temperature may cause oscillation. Select the capacitors which have good temperature characteristics (X7R or better), good DC bias characteristics with high voltage rating. In case significant voltage swing and load transient are expected, make sure to carry out thorough evaluation before making a decision on the capacitance value.

7. Setting the internal drive circuit supply capacitor C_{VL} value
   Add the capacitor greater than 0.1 µF between VCC and VL. Select the capacitor considering the filter circuit for power supply and VL. Since the capacitance value is dependent on the board layout and pattern, secure enough margin when selecting the capacitor.

8. Setting output voltage (V_{O1})

V_{O2} and V_{O3} are fixed output while V_{O1} is adjustable.
V_{O1} output voltage is determined by the following equation.

$$V_{O1} = 0.8 \times \frac{R_{FB1A} + R_{FB1B}}{R_{FB1A}}$$

Please set feedback resistor RFB1A below 30 kΩ to reduce the error margin by the bias current. In addition, since power efficiency is reduced when RFB1A + RFB1B is small, please set the current flowing through the feedback resistor small enough as compared to the output current I_{O1}.

9. Selection of the MOSFET (M1, M2)

In case of Buck-Boost DC / DC, DC / DC1 needs 2 external MOSFET (PMOS = M1 and NMOS = M2). In case of Buck DC / DC, DC / DC1 needs 1 external MOSFET (PMOS). Key parameters in choosing MOSFET are voltage and current rating.

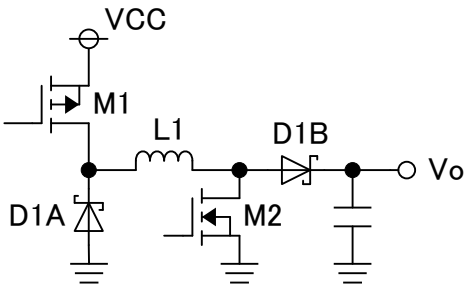


Figure 41. Select MOSFET

(i) PMOS

- V_{ds} maximum rating > VCC
- V_{gs} maximum rating > Lower value of 13 V or VCC

  * The voltage between VCC - VL is kept at 10 V (Typ), 12 V (Max).
  VL become 0 V when VCC become less than 10.3 V (Typ)
- Allowable current > coil peak current I_{LMAX}

  * A value above the over current protection setting is recommended.
  * Choosing a low ON Resistance FET results in high efficiency.

(ii) NMOS

- V_{ds} maximum rating > V_O
- V_{gs} maximum rating > V_{DD}
- Allowable current > Coil peak current I_{LMAX}

  * A value above the over current protection setting is recommended.
  * Choosing a low ON Resistance FET results in high efficiency.