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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Management IC for Automotive Microcontroller

System Regulator for microcontroller for automotive

BD39012EFV-C

General Description

BD39012EFV-C is a power management IC with 1 ch DC / DC convertor, 1 ch LDO, reset and watch dog timer. It can supply the power supply to module from battery directly. LDO has reset built-in and always watches that it supplies stable power supply to module. In addition, window watch dog timer is provided to detect the abnormality of the microcomputer. BD39012EFV-C enables a superior heat dissipation and a compact PCB design by HTSSOP-B24 package.

Features

- Synchronous rectifier step-down DC / DC converter with built-in FET (Adjustable output)
- Secondary LDO with built-in 5 V output FET
- Monitoring function
  Output over voltage / under voltage detection (PG output), Reset function (LDO)
  Window Watchdog Timer
- Built-in protection function
  Input under voltage protection (UVLO)
  Thermal shut down (TSD)
  Output over current protection (OCP)
- Independent enable control
- HTSSOP-B24 package

Applications

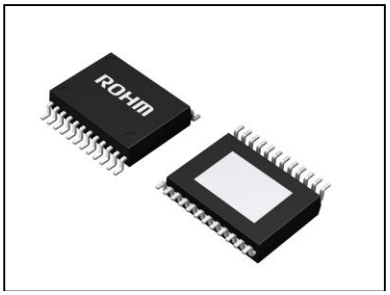
- Microcontroller for Automotive

Key Specifications

- Input voltage range: 4 V to 45 V
  (Startup voltage needs to be above 4.5V.)
- Output Voltage Accuracy
  Step-down DC / DC Converter FB Voltage: 0.8 V ±2 %
  Secondary LDO: 5.0 V ±2 %
- Output Maximum Current
  Step-down DC / DC Converter: 1.0 A
  Secondary LDO: 0.4 A
- Operating Frequency
  Step-down DC / DC Converter: 200 k to 600 kHz (Typ)
- Standby Current: 0 µA (Typ)
- Operating Temperature Range: -40 °C to +125 °C

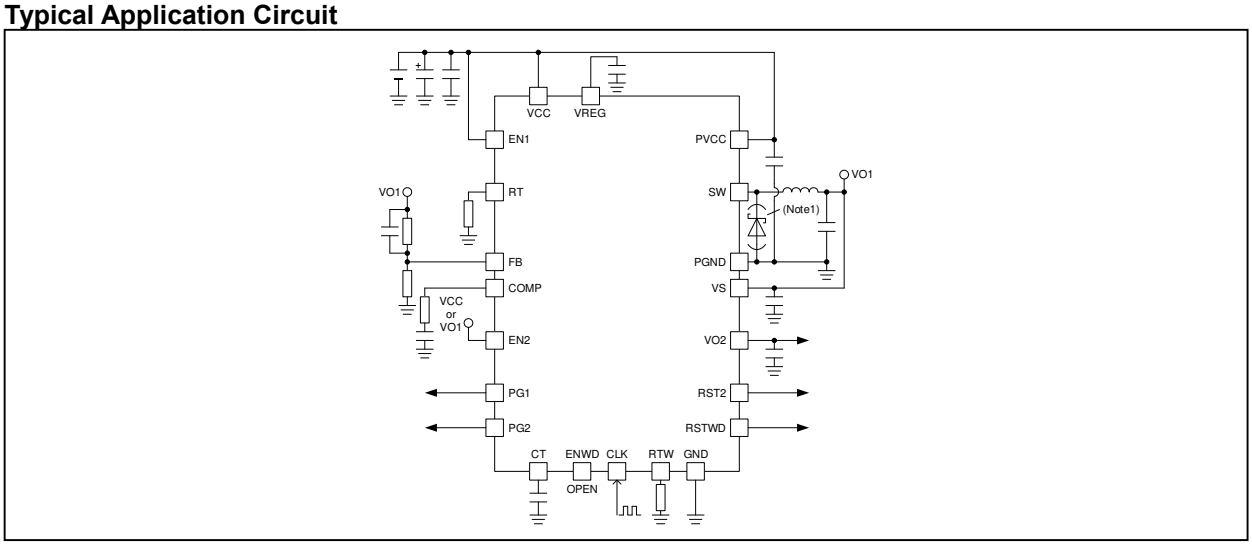
Package

Package	W(Typ) x D(Typ) x H(Max)
HTSSOP-B24	7.80 mm x 7.60 mm x 1.00 mm



HTSSOP-B24

Typical Application Circuit



☆These specifications may be changed without a notice.

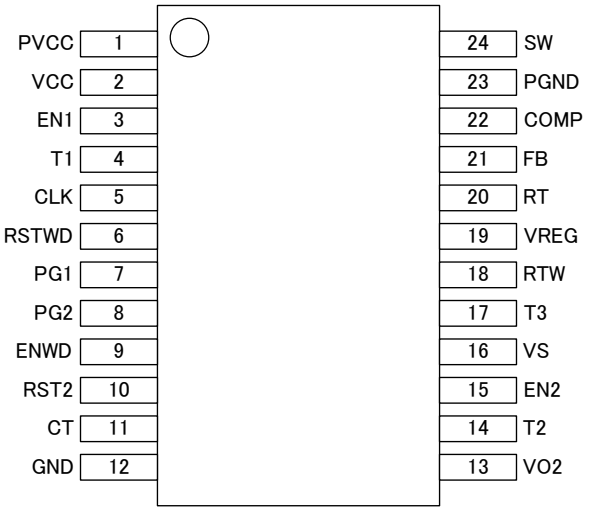
(Note 1) Please connect when the application is that the load current of VO1 output exceed in 500 mA.

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Contents

Pin Configuration

(TOP VIEW)

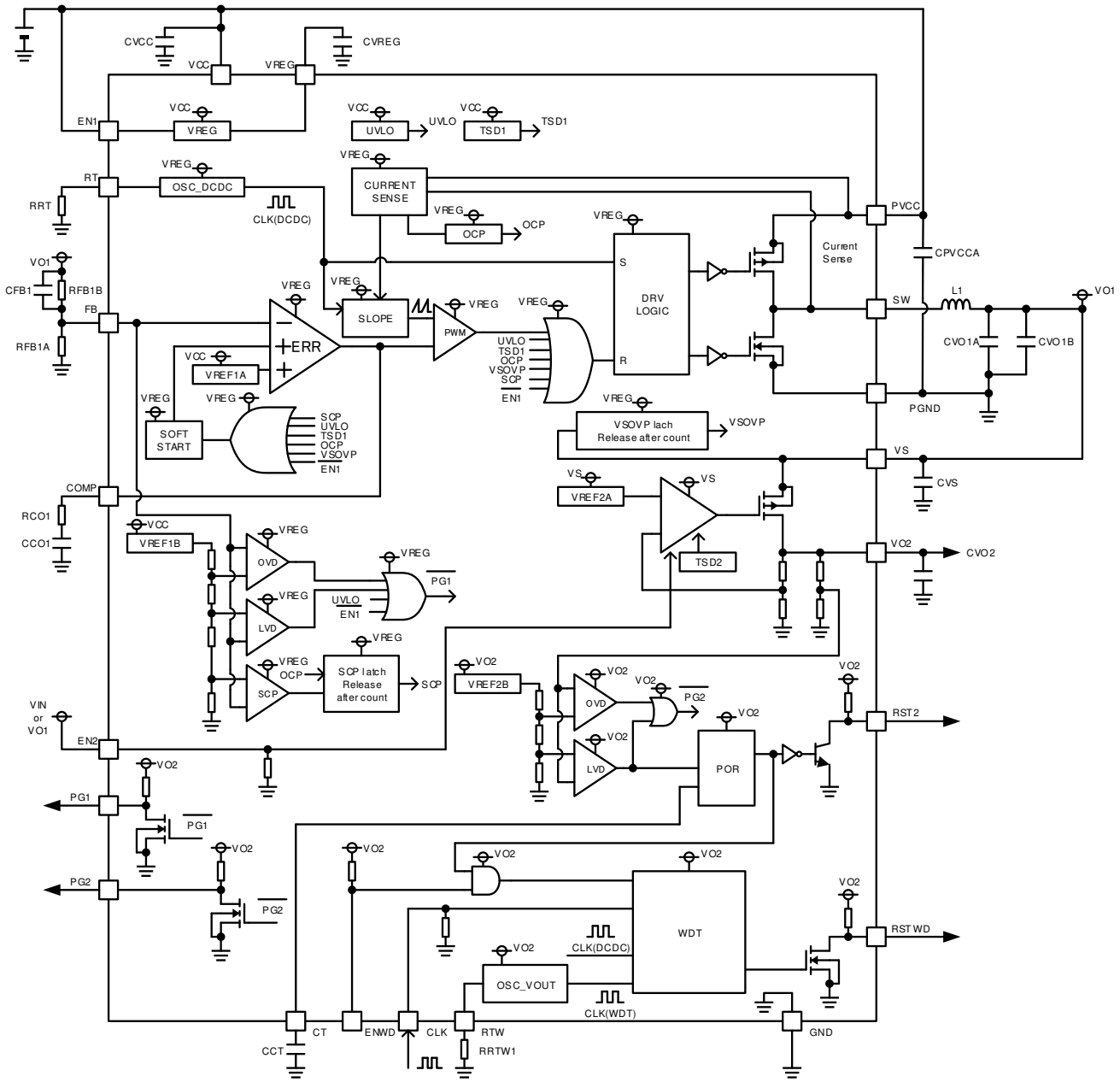


Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	PVCC	Power VCC supply terminal	13	VO2	LDO output terminal
2	VCC	Signal VCC supply terminal	14	T2	Test terminal (Note1)
3	EN1	Enable terminal (DC / DC)	15	EN2	Enable terminal (LDO)
4	T1	Test terminal (Note1)	16	VS	Power supply input terminal for LDO
5	CLK	WDT CLK input terminal	17	T3	Test terminal (Note1)
6	RSTWD	Reset output terminal (WDT monitoring)	18	RTW	Frequency setting terminal for WDT
7	PG1	Power good output terminal (DC / DC monitoring)	19	VREG	Internal power supply terminal
8	PG2	Power good output terminal (LDO monitoring)	20	RT	Frequency setting terminal for DC / DCl
9	ENWD	Enable terminal (WDT)	21	FB	DC / DC output voltage feed buck terminal
10	RST2	Reset output terminal (LDO monitoring)	22	COMP	DC / DC error amp output terminal
11	CT	Power on reset time setting capacitor connect terminal	23	PGND	Power GND terminal
12	GND	Signal GND terminal	24	SW	DC / DC output terminal

(Note 1) Be sure to connect to ground.

Block Diagram



Description of Blocks

- Internal Power Supply (VREG)
  It is the block which generates 4.0 V internal power supply voltage. It is a power supply to supply to the IC inside.
  Please do not be connected to the outside circuit.
  VREG needs to outside capacitor more than 1 µF. Low capacitor of the ESR is recommended.

- Enable (EN1)
  The circuit becomes standby state when EN1 pin becomes less than 0.8 V. Internal power supply and DC / DC convertor are OFF and consumption current from VCC becomes 0 µA (25 °C, Typ) when standby state.
  It can be used when connected to VCC or inputted into the signal from a microcomputer.

- Soft Start (SOFT START)
  The Soft start is a block to prevent over short of the output voltage in the startup and inrush current to an output step.
  With controlling error amp input voltage and increasing switching pulse width gradually, it prevents then.
  Because the soft start time operate an internal counter by oscillation frequency and decides time, it depends on the oscillation frequency setting of the DC / DC converter. It becomes 3.28 ms (Typ) when oscillation frequency is 500 kHz.
  It reboots after an internal SS pin is discharged when VSOVP, TSD1, and SCP are detected.

- Error Amp (ERR)
  The error amp compares the output feedback voltage to the 0.8V reference voltage. This comparison result is output to COMP pin as current. By the voltage of the COMP pin, switching duty is decided. In the startup because soft start is taken, COMP voltage is limited by SOFT START voltage. In addition, COMP pin needs to outside resistance and capacitor for phase compensation.

- PWM COMP (PWM)
  PWM comparator makes a conversion to a continuous duty cycle to control an output transistor in the voltage of COMP pin. The duty becomes 100 % and the high-side output transistor becomes ON state if input voltage becomes less than setting output voltage.

- Oscillation frequency for DC / DC convertor (OSC_DCDC)
  Oscillation frequency is decided by the current which is caused by resistance connected to RT pin.
  The range of oscillation frequency can be set 200 kHz to 600 kHz.
  Short circuit protection starts operating and oscillator stops when RT pin is short-circuited to ground.

- Short Circuit Protection (SCP)
  DC / DC convertor stores with short circuit protection. The short circuit protection starts operation after the short circuit protection circuit considers that the output is in short state when the over current protection starts operation in a state with FB pin voltage less than 0.45 V (Typ) (Except during soft start).
  DC / DC convertor output is OFF when the short circuit protection starts operation. In addition, SOFT START is initialized and COMP pin is discharged. Afterwards, it reboots after 1,024 cycles of the oscillation frequency.

- Reference Voltage of 2 systems
  DC / DC convertor and LDO have a reference voltage which is made from an independent block in both output voltage part and abnormal detection part.
  In this way, even if there was an abnormality in reference voltage of whichever it is suitable for a safe design because abnormality can be informed from PG pin
  Each reference voltage is used as follows.
    VREF1A: Reference of DC / DC convertor output voltage and VREG voltage.
    VREF1B: Reference of DC / DC convertor OVD, LVD, SCP, VSOVP and OCP.
    VREF2A: Reference of LDO output voltage.
    VREF2B: Reference of LDO OVD and LVD.

- Over Voltage Detection (OVD)
  PG1 pin becomes L when reference voltage of DC / DC convertor exceeds 0.95 V (Typ).
  PG2 pin becomes L when output voltage of LDO exceeds 5.38 V (Typ).

- Low Voltage Detection (LVD)
  PG1 pin becomes L when reference voltage of DC / DC convertor is less than 0.65 V (Typ).
  PG2 pin becomes L when output voltage of LDO is less than 4.62 V (Typ).

- Over Current Protection Circuit (OCP, SCP)
  DC / DC convertor and LDO store with over current protection. Current limit is taken in the over current detection of the DC / DC converter, and ON duty cycle is limited, and output voltage decreases. In addition, when it becomes overloaded and FB pin voltage decreases and is less than 0.45 V (Typ), SCP is detected. Afterwards, it reboots after 1,024 cycles of the oscillation frequency. Current limit is taken in the over current detection of the LDO, and output voltage decreases (foldback current limiting characteristic). When it load-short-circuited, it prevents the destruction of the IC, but this protection circuit is effective for prevention of destruction by the sudden accident. It is not supported use at the continuous protection circuit operation and a transitional period.

- DRV LOGIC
  This is the driver block of FET. It drives SW pin.

- Over Voltage Protection Circuit (VSOVP_latch)
  VS pin possesses over voltage protection. If the voltage of the VS pin becomes more than over voltage detection level 13.5 V (Typ), it starts operation. SS and COMP is discharged after DC / DC output is OFF when the over voltage protection circuit starts operation. Afterwards, it reboots after 1,024 cycles of the oscillation frequency from release when VS returned to 13.0 V (Typ). VSOVP is effective for prevention of destruction by the sudden accident. VSOVP is effective for prevention of the destruction by the sudden accident. Please avoid using it at continuous protection circuit operation.

- Under Voltage malfunction prevention circuit (UVLO_VCC)
  DC / DC convertor circuit shuts down after UVLO starts operating when VCC voltage is less than 3.5 V (Typ).
  It starts normal operating after UVLO is released when VCC voltage is more than 4.0 V (Typ).
  Please apply more than 4.45 V to the VCC voltage in initial startup.

- Thermal Shut Down (TSD1, TSD2)
  DC / DC convertor (TSD1) and LDO (TSD2) of BD39012EFV-C, each has thermal shutdown and operates individually.
  The protection is taken when chip temperature Tj exceeds 175 °C (Typ). DC / DC convertor lets the switching OFF.
  The Output is OFF in LDO. In addition, it returns if it becomes less than 150 °C (Typ).

- SLOPE, CURRENT SENCE
  This block is a block to give slope compensation of the current mode of DC / DC convertor and current return.

- LDO Block
  LDO operates by full independence. Even if it is the state that does not contain the voltage in PVCC pin and VCC pin, power on reset (POR), watch dog timer (WDT), PG2 pin, RST pin, RSTWD pin and ENWD pin become effective when a power supply is spent to VS pin.
  But OSC_WDT ERR Detect informing abnormality does not function. (Timing chart 6 (*4))

- Power On Reset (POR)
  POR starts charge to the outside capacitor of CT pin (= CCT) when VO2 of LDO output releases under voltage detect. RST2 pin outputs `H` when CT pin voltage becomes more than 1.18 V (Typ). CCT is discharged and RST2 pin outputs `L` when VO2 detects low voltage. Please set the setting range of CCT in the range of 0.001 µF from 10 µF

- Oscillator for Watch Dog Timer (OSC_VOUT)
  This block creates a reference frequency of the Watch Dog Timer. The oscillation frequency is determined by the RTW resistance. The oscillation frequency can be set in the range of 50 kHz to 250 kHz.
  Short circuit protection starts operating and oscillator stops when RTW pin is short-circuited to ground.

- Watch Dog Timer (WDT)
  Microcontroller (µC) operation is monitored with CLK pin. Window watch dog timer is included to enhance the assurance of the system. WDT starts operating when POR and ENWD becomes high. It watches both edges (rising edge, falling edge) of the CLK pin. When the width of both edges is lower than the watch dog lower limit (Fast NG) or more than the watch dog upper limit (Slow NG), RSTWD is made low during WDT reset time (tWRES) (µC ERR Detect).
  Fast NG and Slow NG are decided by the number of the counts of OSC_WDT. Therefore a time change of Fast NG and Slow NG is possible by changing frequency of OSC_WDT. In addition, it lets RSTWD low and informs abnormality when abnormality occurs in OSC_WDT (including the RTW pin ground) (OSC_WDT ERR Detect).

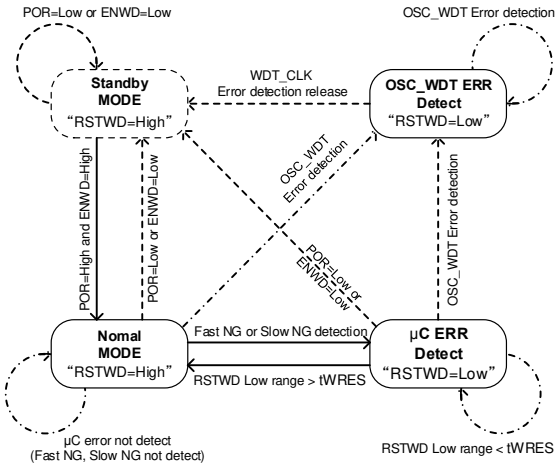


Figure 1. Witch Dog Timer State Change Diagram (WDT FSM)

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VCC	-0.3 to 45 (Note 1)	V
Output Switch Pin Voltage	VSW	-0.3 to VCC	V
EN1 Pin Voltage	VEN1	-0.3 to 45	V
VREG Pin Voltage	VREG	-0.3 to 7	V
RT, FB, COMP Pin Voltage	VRT, VFB, VCOMP	-0.3 to 7	V
VS Pin Voltage	VS	-0.3 to 45*1	V
EN2 Pin Voltage	VEN2	-0.3 to 45	V
VO2 Pin Voltage	VO2	-0.3 to 7	V
PG1, PG2 Pin Voltage	VPG1, VPG2	-0.3 to VO2	V
RST2, RSTWD Pin Voltage	VRST2, VRSTWD	-0.3 to VO2	V
CT Pin Voltage	VCT	-0.3 to 7 (Note 2)	V
RTW Pin Voltage	VRTW	-0.3 to 7	V
ENWD Pin Voltage	VENWD	-0.3 to VO2	V
CLK Pin Voltage	VCLK	-0.3 to 7	V
Power Dissipation (Note 3)	Pd	4.0	W
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	150	°C

(Note 1) Pd, should not be exceeded
(Note 2) VS+0.3 V, should not be exceeded.
(Note 3) Derating in done 32.0 mW / °C for operating above Ta ≥ 25 °C (Mount on 4-layer 70.0mm x 70.0mm x 1.6mm board)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Operating Power Supply Voltage	VCC	4 (Note 4)	-	36 (Note 5)	V
VS Operating Voltage	VS	6.0	-	10	V
Switch Current	ISW	0	-	1	A
Oscillation Frequency	FOSC	200	-	600	kHz
WDT Oscillation Frequency	FOSCW	50	-	250	kHz
LDO Output Current	IVO2	0	-	0.4 (Note 5)	A
Operating Temperature Range	Topr	-40	-	125	°C

(Note 4) Initial startup is over 4.45 V
(Note 5) Pd, should not be exceeded

Electrical Characteristics (Unless otherwise specified Ta = -40 to 125 °C, VCC = 4 to 36 V)

Parameter	Symbol	Min	Typ	Max	Unit	Function
< The Whole >						
Standby Circuit Current 1	ISTB1	-	0	10	μA	VEN1 = 0 V, Ta = 25 °C
Standby Circuit Current 2	ISTB2	-	-	50	μA	VEN1 = 0 V
VCC Circuit Current	IQVCC	-	2	4	mA	FB = 0 V
VS Circuit Current	IQVS	-	505	1100	μA	VS = 6 V, VEN2 = 5 V, ENWD = 0 V, RTW = 24 kΩ, CLK = 0 V, PG1, PG2, RST2, RSTWD = H
UVLO Detection Voltage	VUVLO	3.3	3.5	3.7	V	VCC detection
UVLO Hysteresis Voltage	VUVLOHYS	0.25	0.5	0.75	V	VCC detection
VREG Output Voltage	VVREG	3.6	4.0	4.4	V	
EN1L Threshold Voltage	VEN1L	-	-	0.8	V	
EN1H Threshold Voltage	VEN1H	3.5	-	-	V	
EN1 Inflow Current	IEN1	-	13	26	μA	VEN1 = 5 V
< DCDC >						
Pch MOSFET ON Resistance	RONSWP	-	0.4	1	Ω	ISW = 300 mA
Nch MOSFET ON Resistance	RONSWN	-	0.4	1	Ω	ISW = -300 mA
Over Current Protection	IOLIM	1	-	-	A	
Output Leak Current 1	ISWLK1	-	0	10	μA	VEN1 = 0 V, Ta = 25 °C
Output Leak Current 2	ISWLK2	-	-	50	μA	VEN1 = 0 V
Reference Voltage	VREF	0.784	0.800	0.816	V	VCOMP = VFB
FB Input Bias Current	IFBB	-1	-	1	μA	FB = 0.8 V
Soft Start Time	TSS	2.70	3.28	4.00	ms	RT = 24 kΩ
Oscillation Frequency	FOSC	450	500	550	kHz	RT = 24 kΩ
VS Over Voltage Detection	VVSOVP	11	13.5	16	V	
PG1 Pull-up Resistance	RPUPG1	30	50	75	kΩ	Internal Resistance (VO2 Pull-up)
PG1 Output L Voltage	VPG1L	-	-	0.3	V	PG1, PG2, RST2, RSTWD pin short (Note 1)
PG1 Low Voltage Detection Voltage	VLVD1	0.60	0.65	0.70	V	VFB monitor, PG1 output
PG1 Over Voltage Detection Voltage	VOVD1	0.90	0.95	1.00	V	VFB monitor, PG1 output

(Note 1) PG1, PG2, RST2, RSTWD pin is shorted. In the case of ON, it is met only Tr of PG1.

Electrical Characteristics – Continued (Unless otherwise specified Ta = -40 to 125 °C, VCC = 4 to 36 V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
< LDO / Reset >						
Output Voltage	VO2	4.90	5.00	5.10	V	5 mA to 400 mA, VS = 6.0 V to 10 V
Drop Voltage 1	ΔVdd1	-	0.17	0.33	V	VS = 4.75 V, Io = 200 mA
Drop Voltage 2	ΔVdd2	-	0.33	0.67	V	VS = 4.75 V, Io = 400 mA
EN2L Threshold Voltage	VEN2L	-	-	0.8	V	
EN2H Threshold Voltage	VEN2H	2.8	-	-	V	
EN2 Inflow Current	IEN2	-	25	50	μA	VEN2 = 5 V
Under Voltage Detection Detection Voltage	VRST2DET	4.50	4.62	4.75	V	
Under Voltage Detection Hysteresis	VRST2DETH	20	60	100	mV	
Power On Reset Time	tPOR0	10	14	18	ms	CCT = 0.1 μF (Note 2)
RST2 Pull-up Resistance	RPURST2	30	50	75	kΩ	Internal Resistance (VO2 Pull-up)
RST2 Output L Voltage	VRST2L	-	0.15	0.30	V	VO2 ≥ 1 V, PG1, PG2, RST2, RSTWD pin short (Note 3)
PG2 Pull-up Resistance	RPUPG2	30	50	75	kΩ	Internal Resistance (VO2 Pull-up)
PG2 Output L Voltage	VPG2L	-	-	0.3	V	PG1, PG2, RST2, RSTWD pin short (Note 4)
PG2 Low Voltage Detection Voltage	VLVD2	4.50	4.62	4.75	V	VO2 monitor, PG2 output
PG2 Over Voltage Detection Voltage	VOVD2	5.25	5.38	5.50	V	VO2 monitor, PG2 output

(Note 2) Power on reset time tPOR can be changed by capacity of the capacitor to connect to CT. (Available range 0.001 to 10 μF)
tPOR (ms) ≒ tPOR0 (Reset delay time at the time of the 0.1 μF connection) × CCT (μF) / 0.1 CT capacity: 0.1 ≤ CCT ≤ 10 μF
tPOR (ms) ≒ tPOR0 (Reset delay time at the time of the 0.1 μF connection) × CCT (μF) / 0.1 (±0.1) CT capacity: 0.001 ≤ CCT ≤ 0.1 μF
(Note 3) PG1, PG2, RST2, RSTWD pin is shorted. In the case of ON, it is met only Tr of RST2.
(Note 4) PG1, PG2, RST2, RSTWD pin is shorted. In the case of ON, it is met only Tr of PG2.

Electrical Characteristics – Continued (Unless otherwise specified Ta = -40 to 125 °C, VCC = 4 to 36 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
< WDT >						
WDT Oscillation Frequency	FOSCW	75	100	125	kHz	RTW = 24 kΩ, VO2 = 4.9 V to 5.1 V
CLK FAST NG Threshold	tWF	123 / FOSCW	128 / FOSCW	133 / FOSCW	s	CLK edge time
CLK SLOW NG Threshold	tWS	865 / FOSCW	870 / FOSCW	875 / FOSCW	s	
WDT Reset Time	tWRES	123 / FOSCW	128 / FOSCW	133 / FOSCW	s	
CLK Detection Minimum Pulse Width	WCLK	1	-	-	µs	
CLK L Threshold Voltage	VCLKL	-	-	0.8	V	
CLK H Threshold Voltage	VCLKH	2.6	-	-	V	
CLK Inflow Current	ICLK	-	25	50	µA	VCLK = 5 V
ENWD L Threshold Voltage	VENWDL	-	-	0.2 × VO2	V	VO2 = 4.9 V to 5.1 V
ENWD H Threshold Voltage	VENWDH	0.8 × VO2	-	-	V	VO2 = 4.9 V to 5.1 V
ENWD Pull-up Resistance	RPURENWD	100	200	300	kΩ	
RSTWD Pull-up Resistance	RPURSTWD	30	50	75	kΩ	Internal Resistance (VO2 Pull-up)
RSTWD Output L Voltage	VRSTWDL	-	-	0.3	V	PG1, PG2, RST2, RSTWD pin short (Note 5)

(Note 5) PG1, PG2, RST2, RSTWD pin is shorted. In the case of ON, it is met only Tr of RSTWD.

Typical Performance Curves

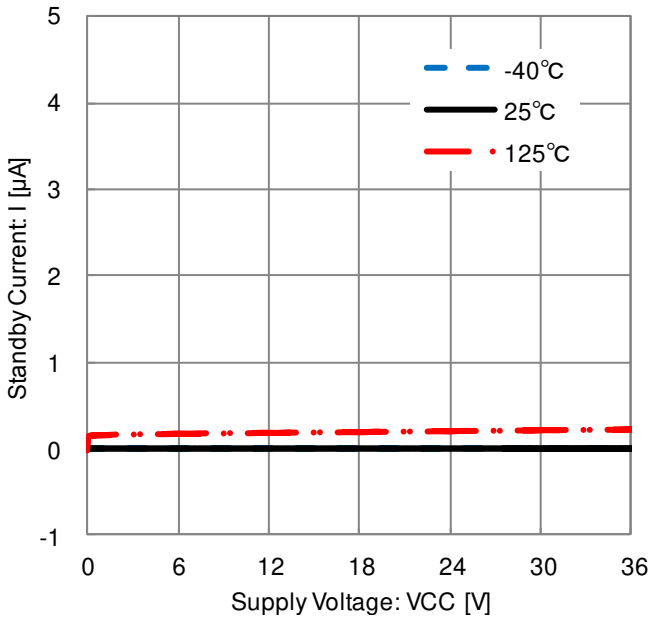


Figure 2. Standby Current vs Supply Voltage
(Standby Circuit Current)

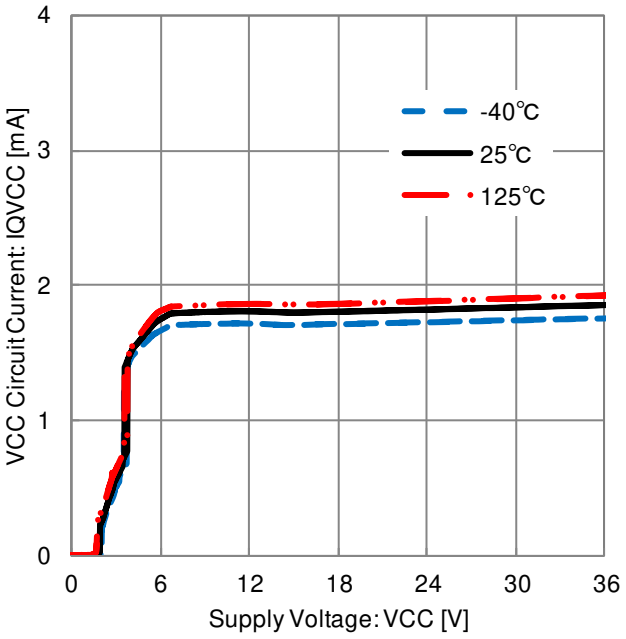


Figure 3. VCC Circuit Current vs Supply Voltage
(VCC Circuit Current)

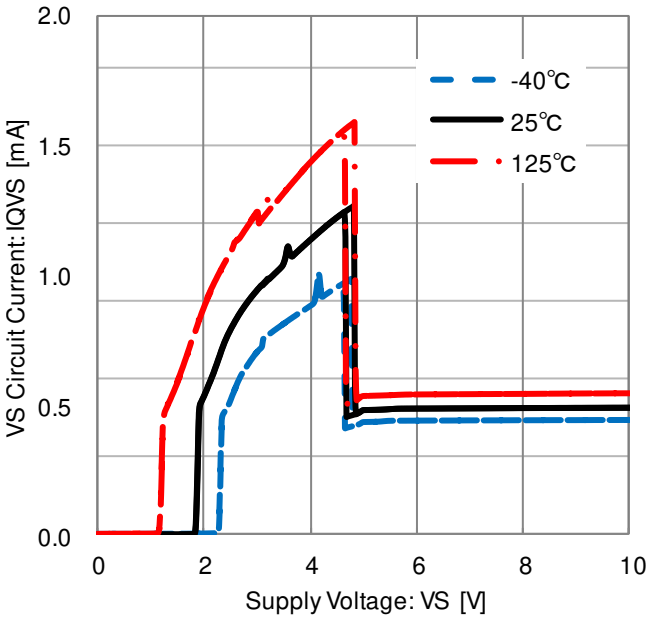


Figure 4. VS Circuit Current vs VS Supply Voltage
(VS Circuit Current)

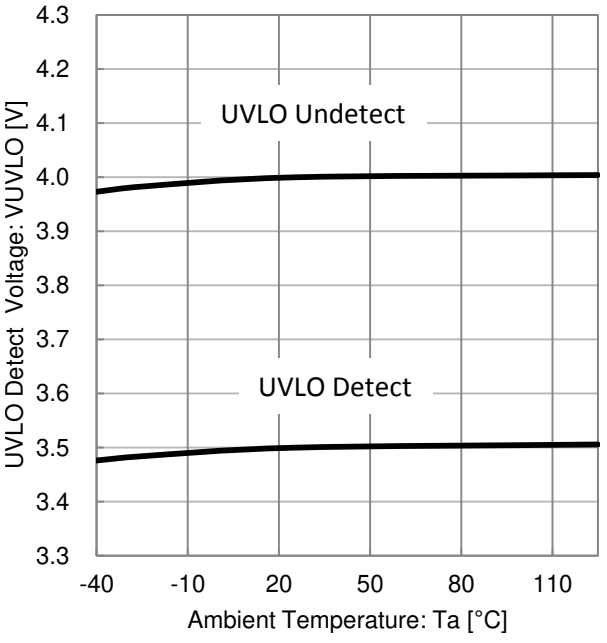


Figure 5. UVLO Detect Voltage vs Ambient Temperature
(UVLO Detection Voltage)

Typical Performance Curves - continued

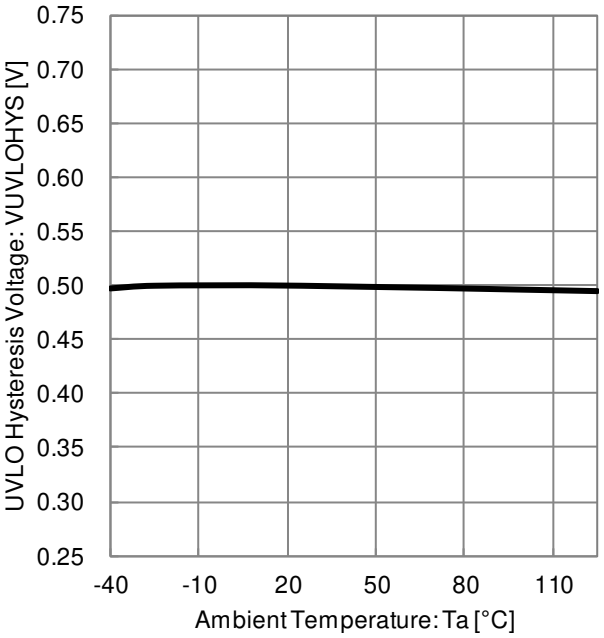


Figure 6. UVLO Hysteresis Voltage vs Ambient Temperature (UVLO Hysteresis Voltage)

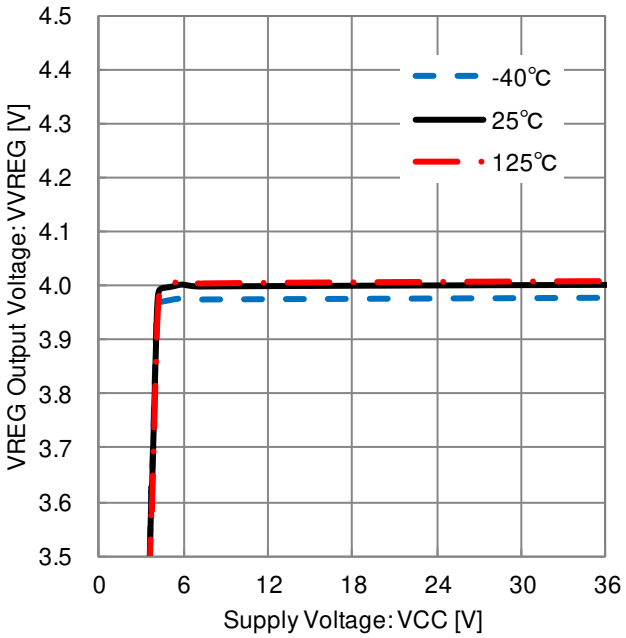


Figure 7. VREG Output Voltage vs Supply Voltage (VREG Output Voltage)

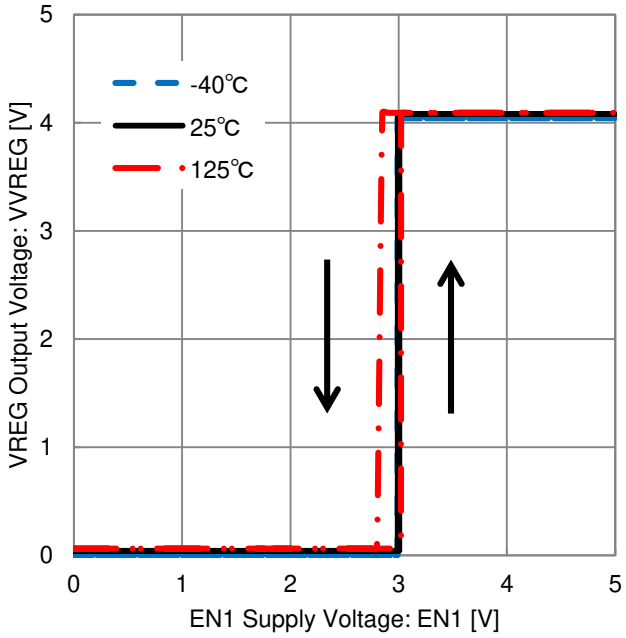


Figure 8. VREG Output Voltage vs EN1 Supply Voltage (EN Threshold Voltage)

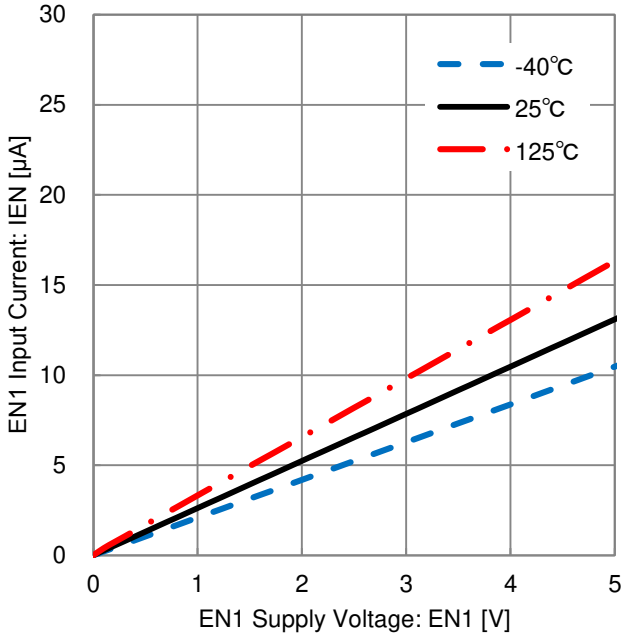


Figure 9. EN1 Input Current vs EN1 Supply Voltage (EN Inflow Current)

Typical Performance Curves - continued

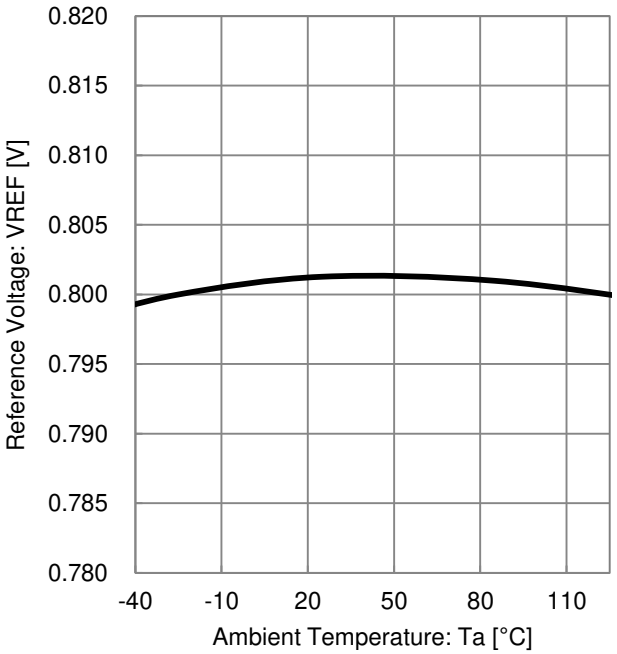


Figure 10. Reference Voltage vs Ambient Temperature
(Reference Voltage)

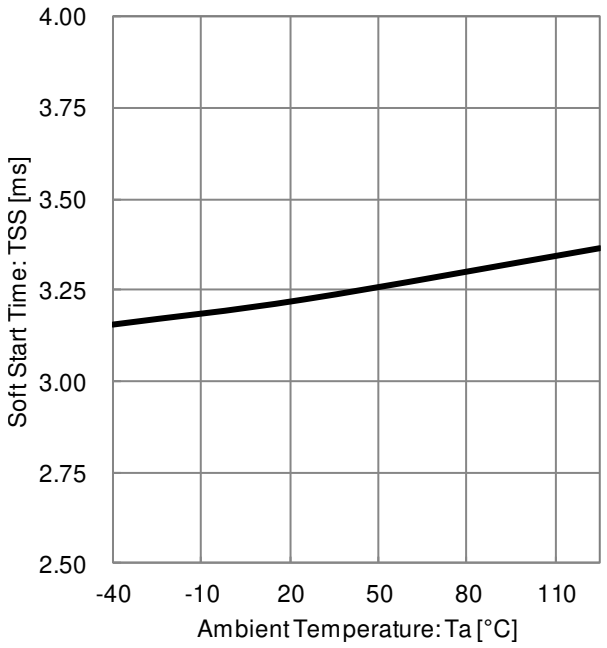


Figure 11. Soft Start Time vs Ambient Temperature
(Soft Start Time)

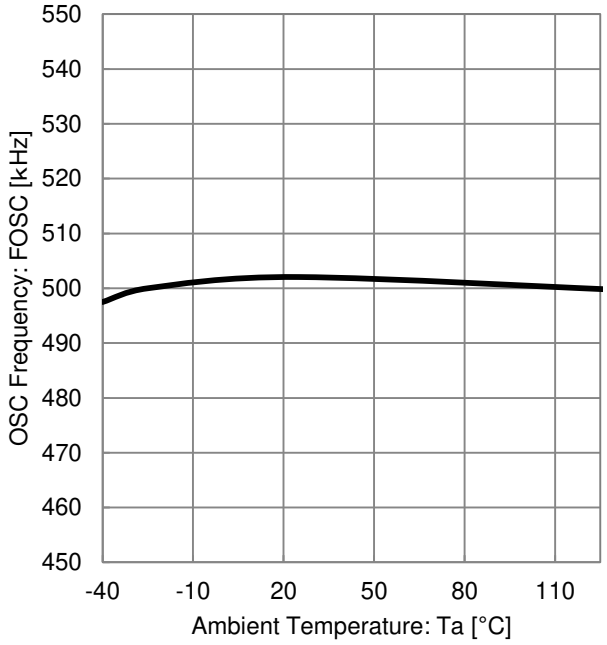


Figure 12. OSC Frequency vs Ambient Temperature
(Oscillation Frequency)

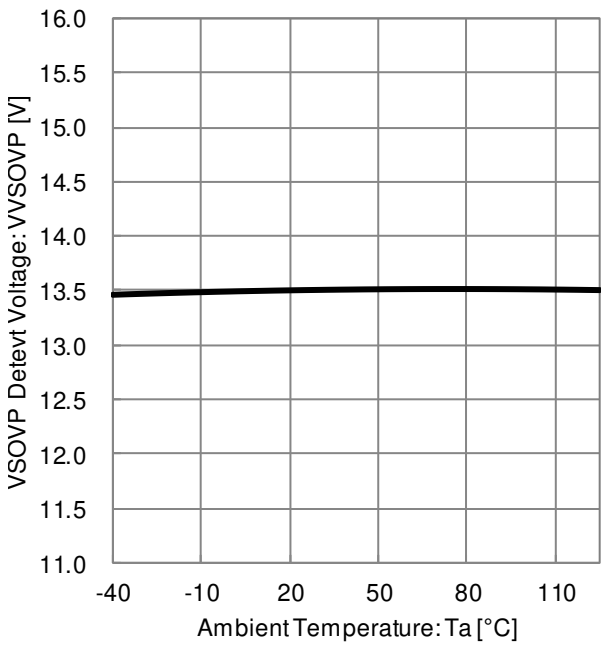


Figure 13. VSOVP Detect Voltage vs Ambient Temperature
(VS Over Voltage Detection)

Typical Performance Curves - continued

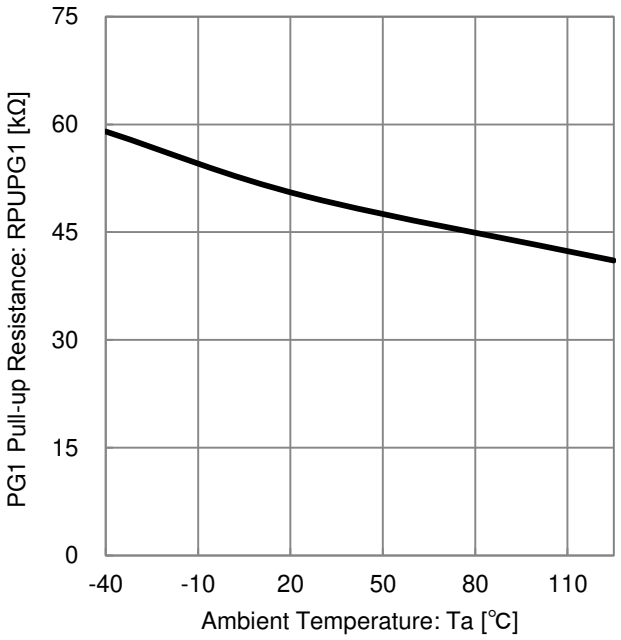


Figure 14. PG1 Pull-up Resistance vs Supply Voltage
(PG1 Pull-up Resistance)

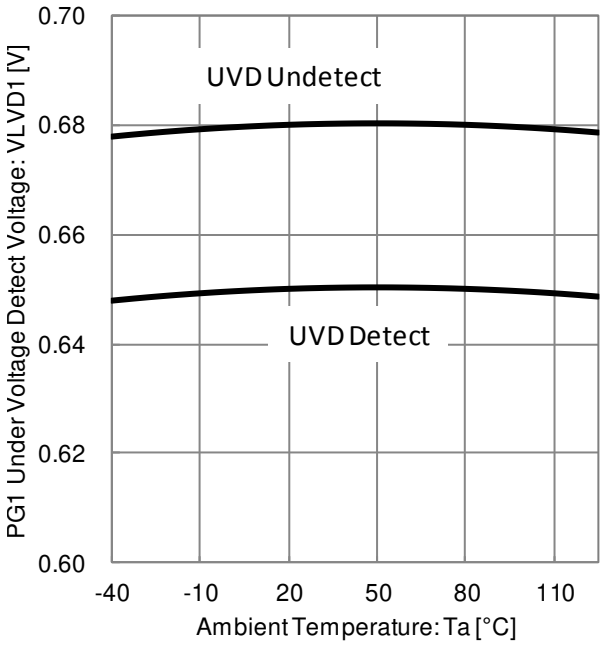


Figure 15. PG1 Under Voltage Detect Voltage
vs Ambient Temperature
(PG1 Low Voltage Detection Voltage)

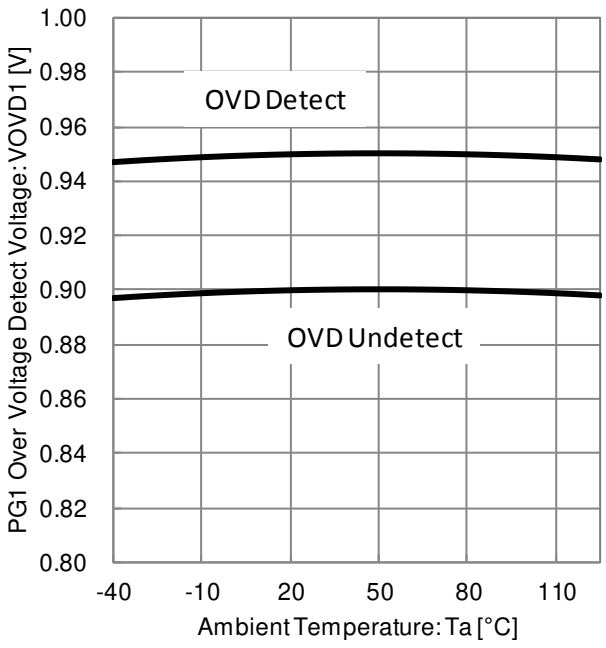


Figure 16. PG1 Over Voltage Detect Voltage
vs Ambient Temperature
(PG1 Over Voltage Detection Voltage)

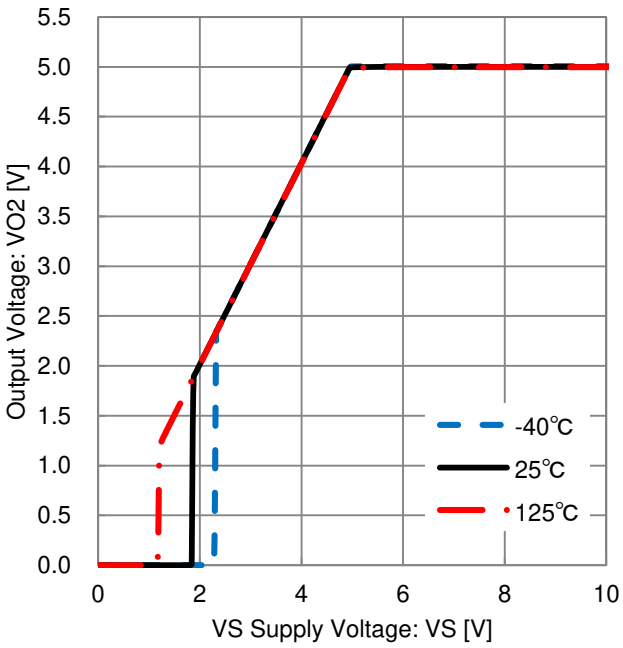


Figure 17. Output Voltage vs VS Supply Voltage
(Output Voltage)

Typical Performance Curves - continued

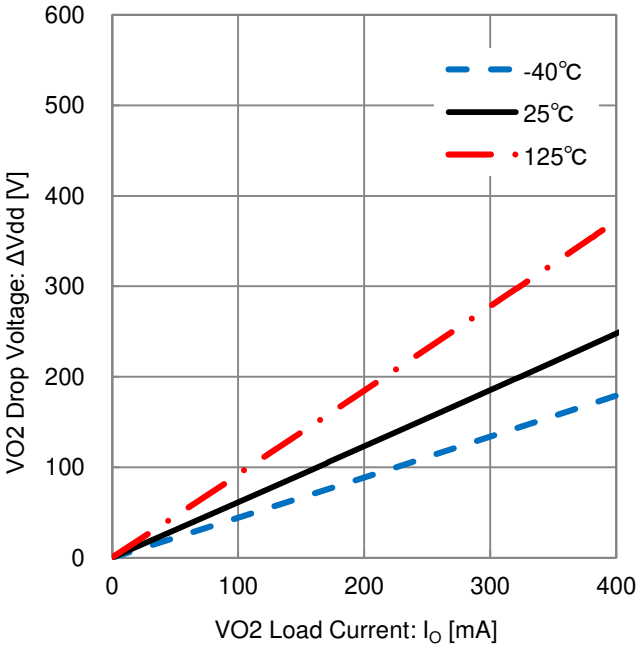


Figure 18. VO2 Drop Voltage vs VO2 Load Current (Drop Voltage)

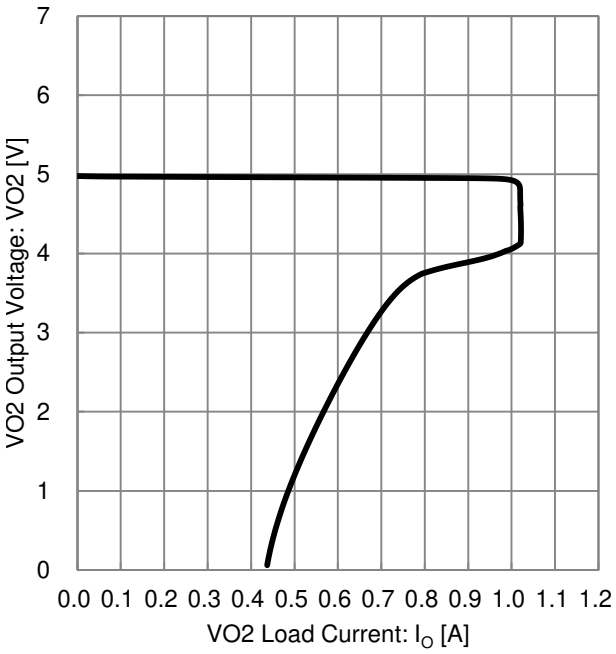


Figure 19. VO2 Output Voltage vs VO2 Load Current (LDO OCP)

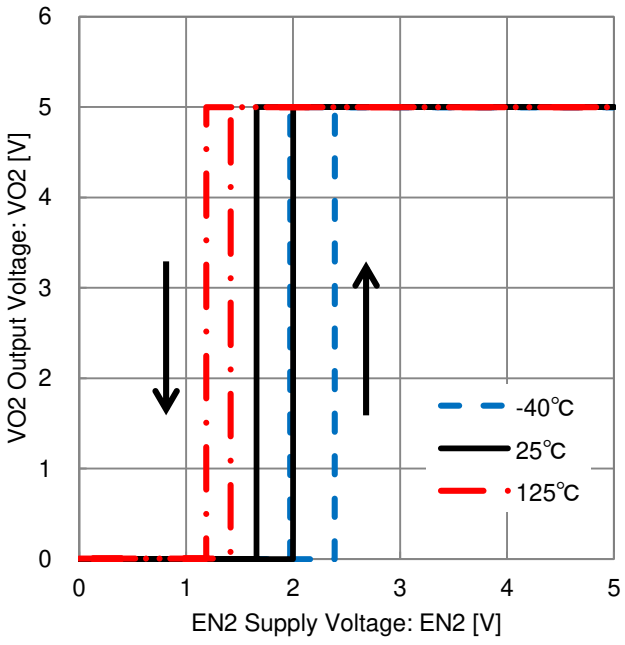


Figure 20. VO2 Output Voltage vs EN2 Supply Voltage (EN2 Threshold Voltage)

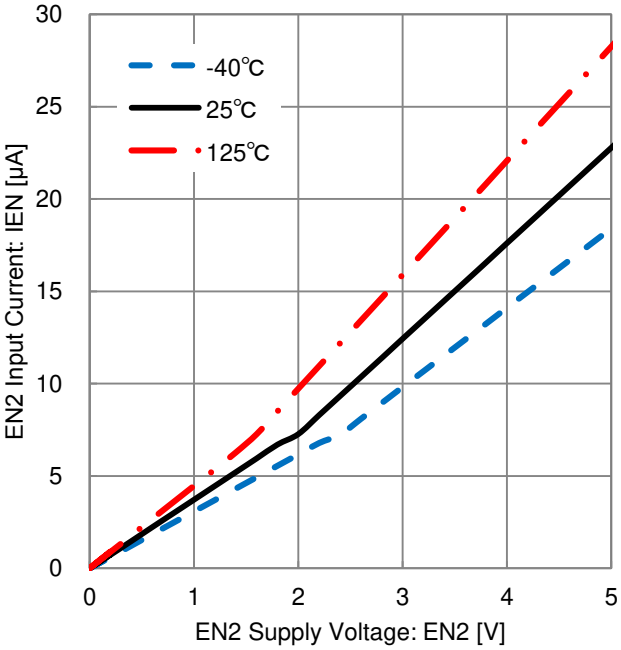


Figure 21. EN2 Input Current vs EN2 Supply Voltage (EN2 Inflow Current)

Typical Performance Curves - continued

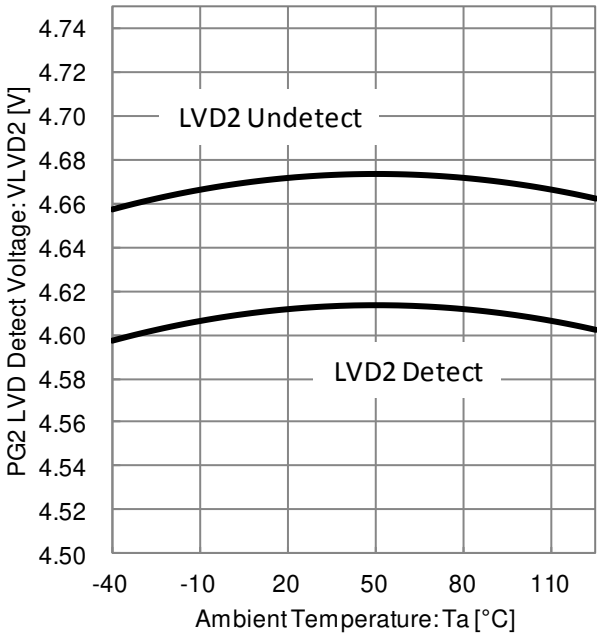


Figure 22. PG2 LVD Detect Voltage vs Ambient Temperature
(PG2 Low Voltage Detection Voltage)

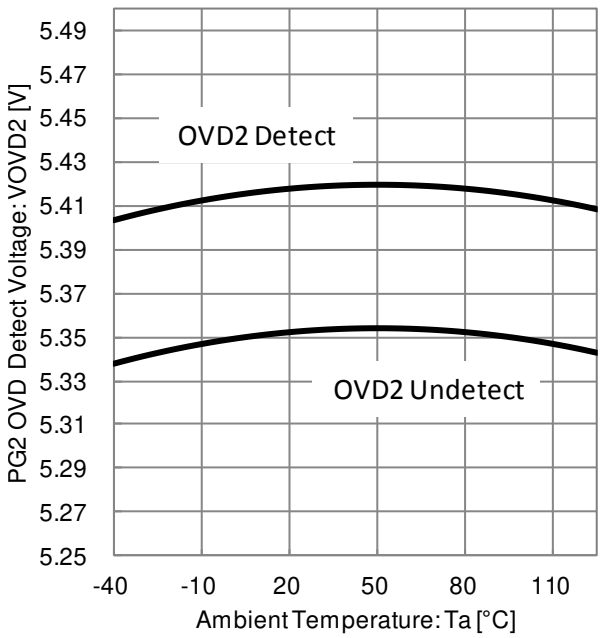


Figure 23. PG2 OVD Detect Voltage vs Ambient Temperature
(PG2 Over Voltage Detection Voltage)

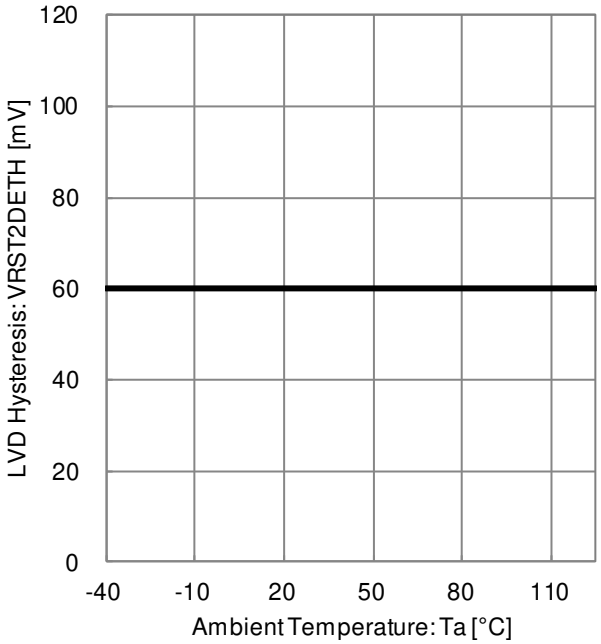


Figure 24. LVD Hysteresis vs Ambient Temperature
(Under Voltage Detection Hysteresis)

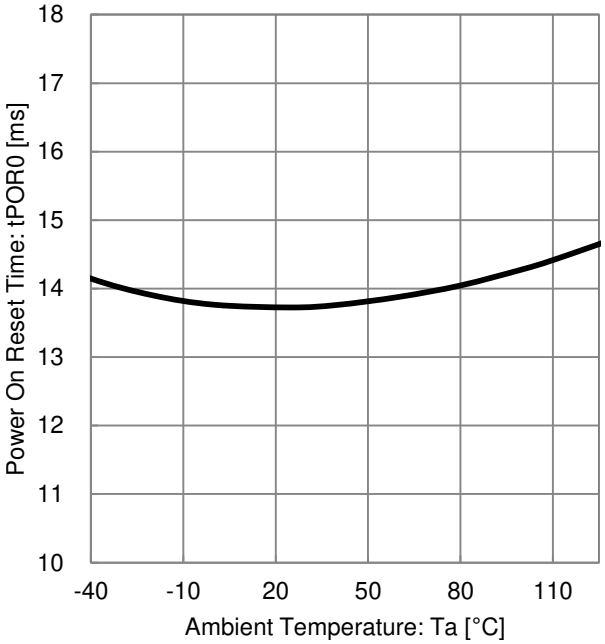


Figure 25. Power On Reset Time vs Ambient Temperature
(Power On Reset Time)

Typical Performance Curves - continued

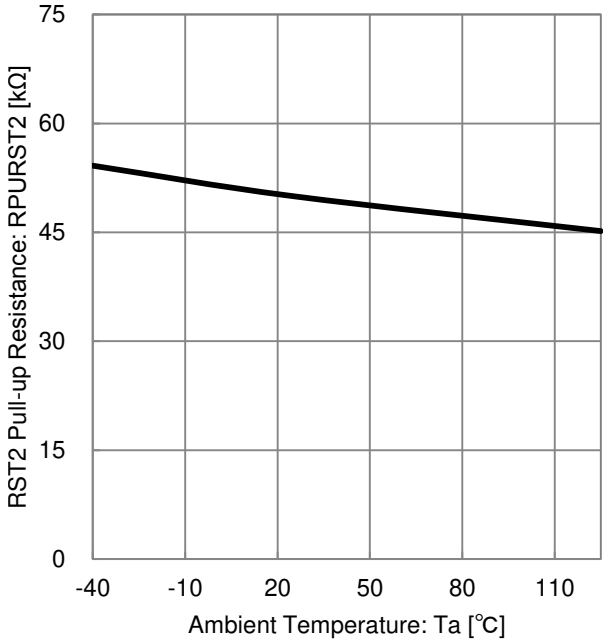


Figure 26. RST2 Pull-up Resistance vs Ambient Temperature
(RST2 Pull-up Resistance)

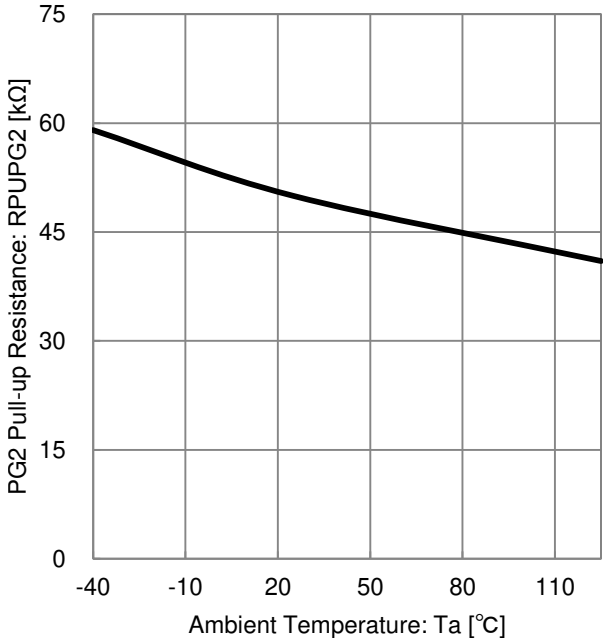


Figure 27. PG2 Pull-up Resistance vs Ambient Temperature
(PG2Pull-up Resistance)

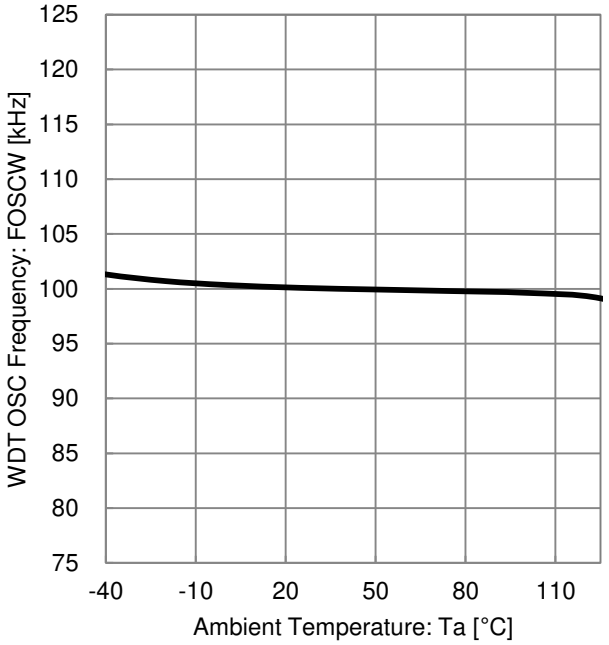


Figure 28. WDT OSC Frequency vs Ambient Temperature
(WDT Oscillation Frequency)

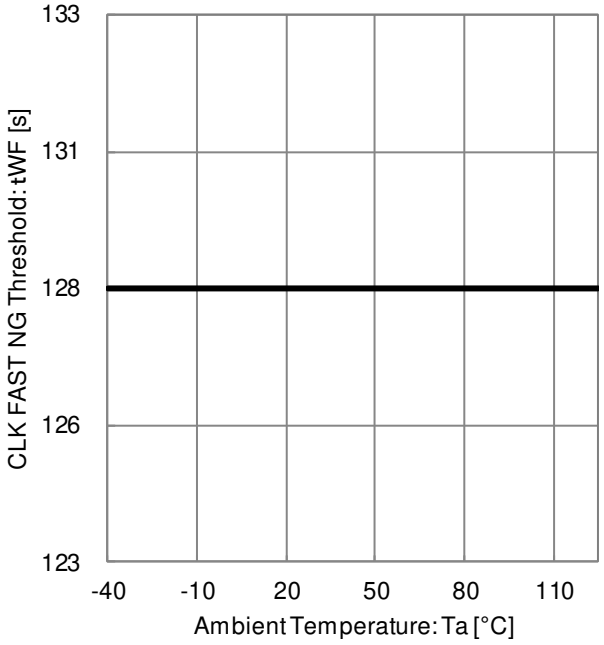


Figure 29. CLK FAST NG Threshold vs Ambient Temperature
(CLK FAST NG Threshold)

Typical Performance Curves - continued

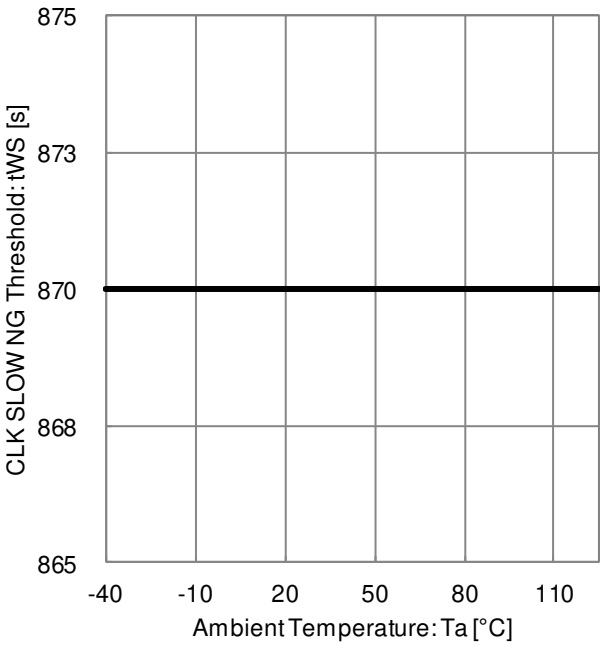


Figure 30. CLK SLOW NG Threshold vs Ambient Temperature (CLK SLOW NG Threshold)

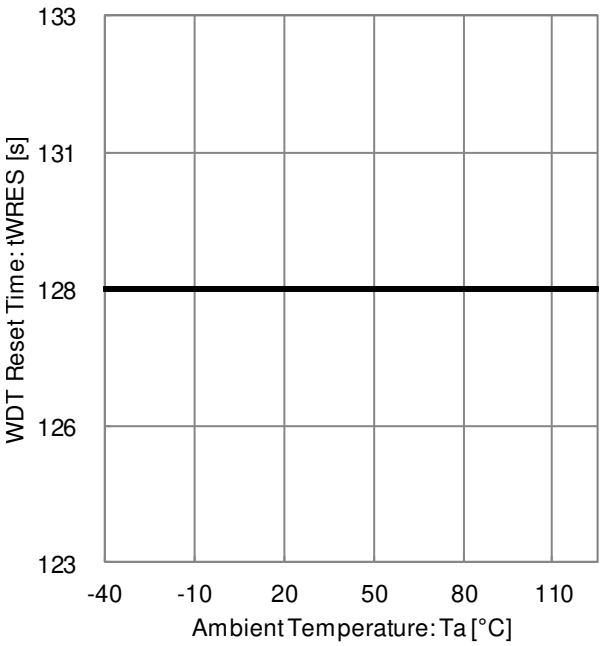


Figure 31. WDT Reset Time vs Ambient Temperature (WDT Reset Time)

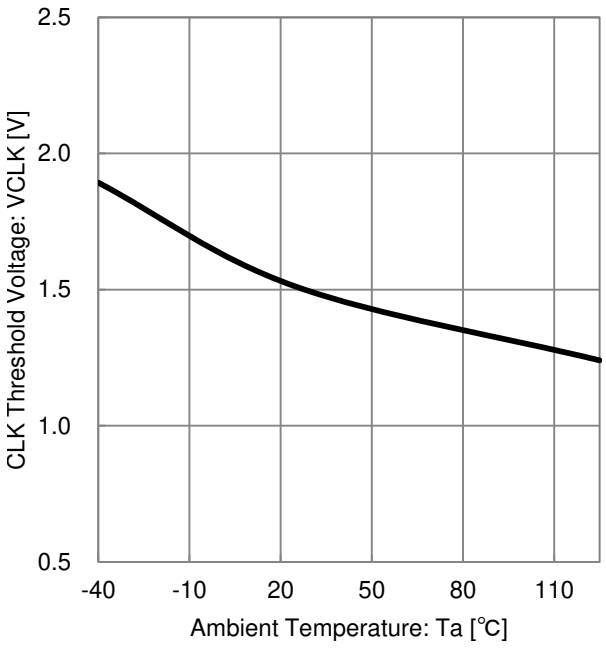


Figure 32. CLK Threshold Voltage vs Ambient Temperature (CLK Threshold Voltage)

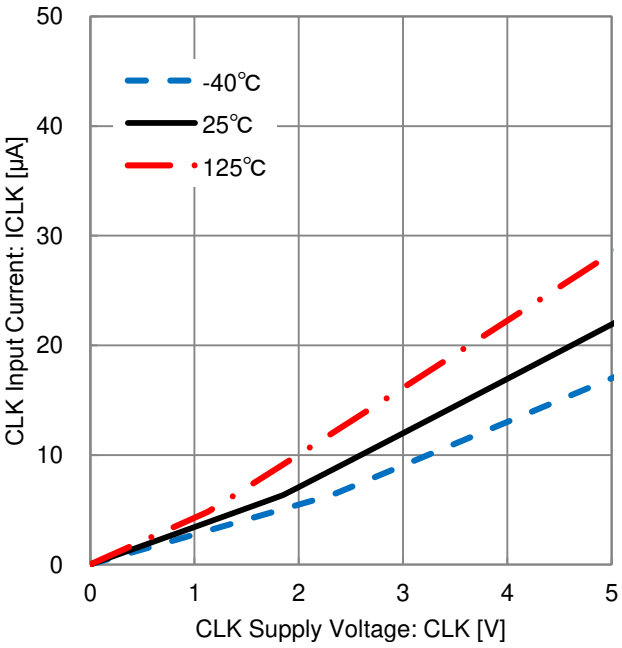


Figure 33. CLK Input Current vs CLK Supply Voltage (CLK Inflow Current)

Typical Performance Curves - continued

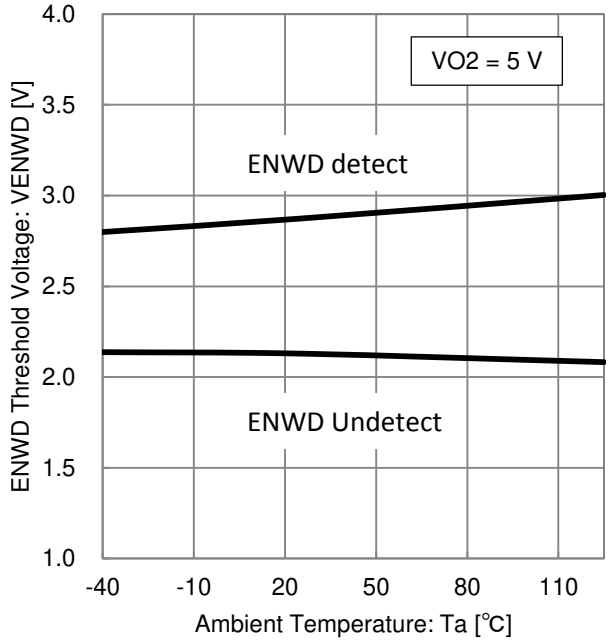


Figure 34. ENWD Threshold Voltage vs Ambient Temperature
(ENWD Threshold Voltage)

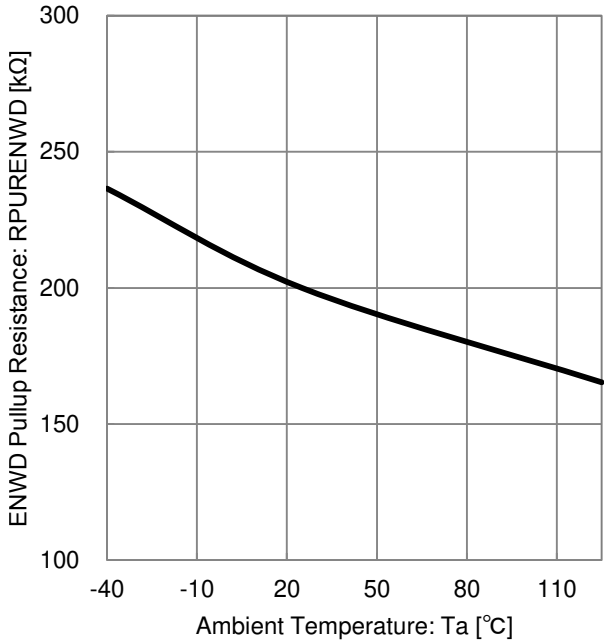


Figure 35. ENWD Pull-up Resistance
vs Ambient Temperature
(ENWD Pull-up Resistance)

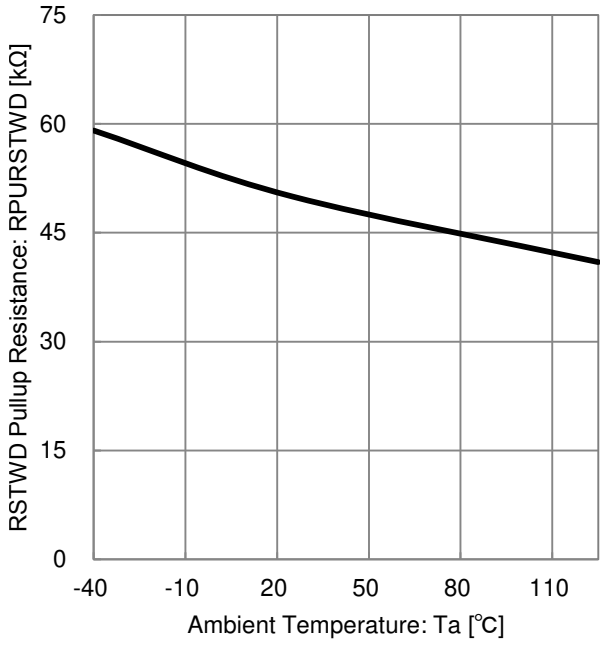
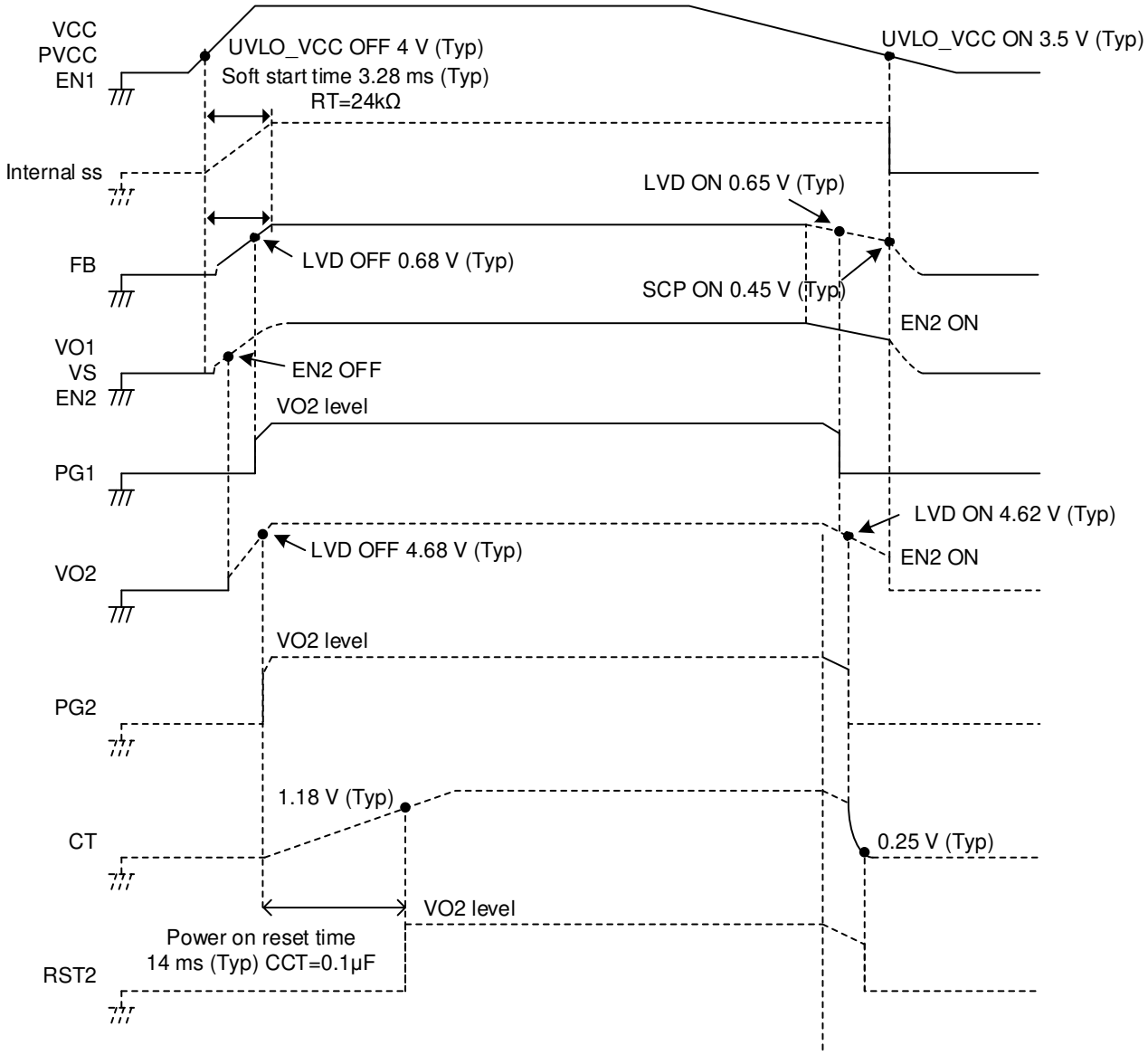


Figure 36. RSTWD Pull-up Resistance
vs Ambient Temperature
(RSTWD Pull-up Resistance)

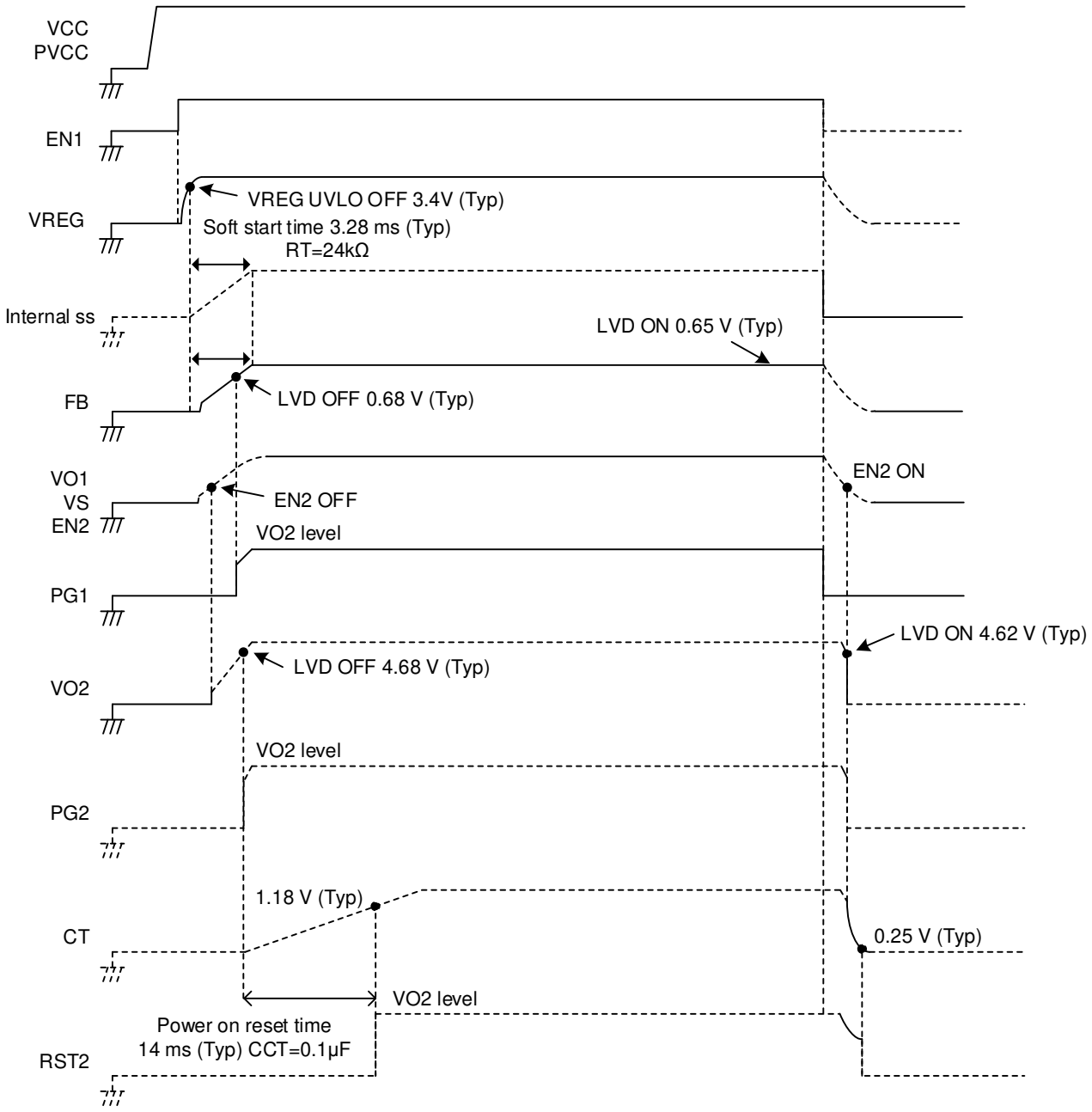
Timing Chart

1. Start up・Stop

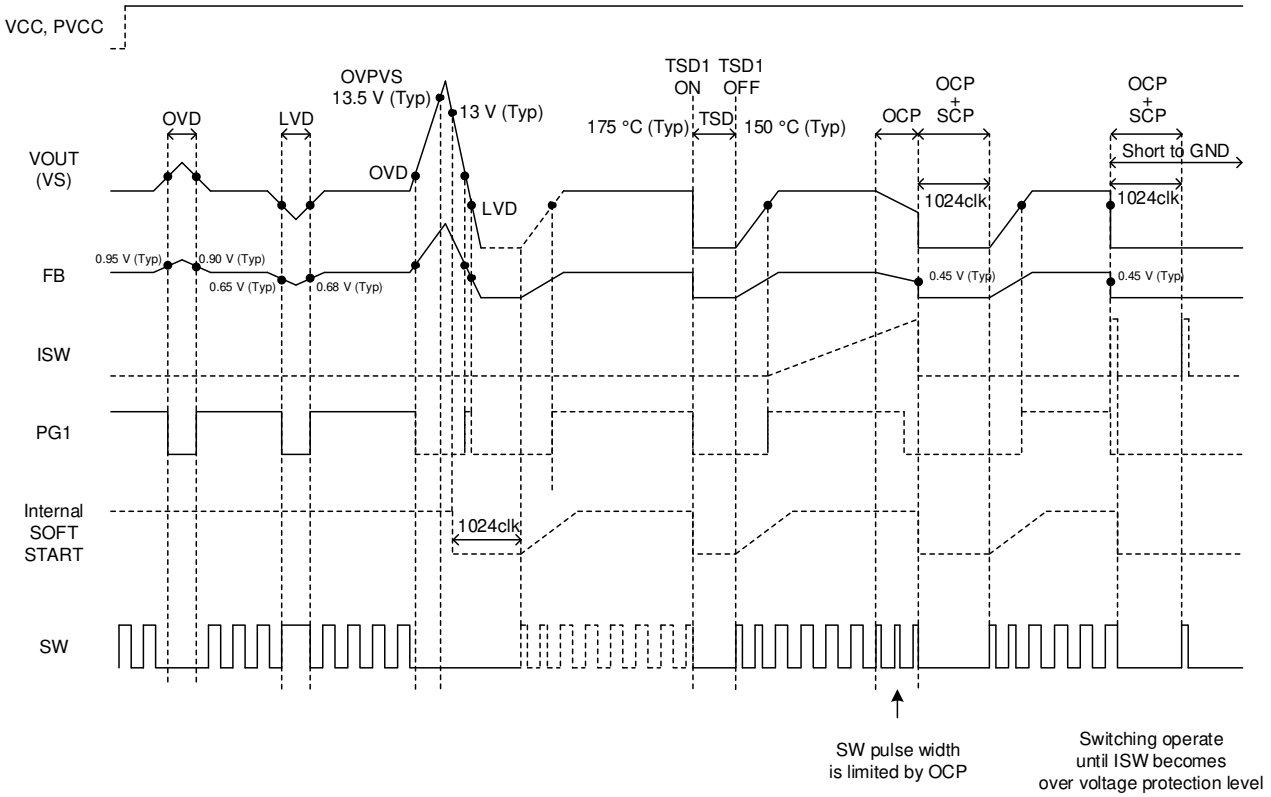
EN1 short to VCC, EN2 short to VS, VOUT = 6 V, load from VO2 is 400 mA.



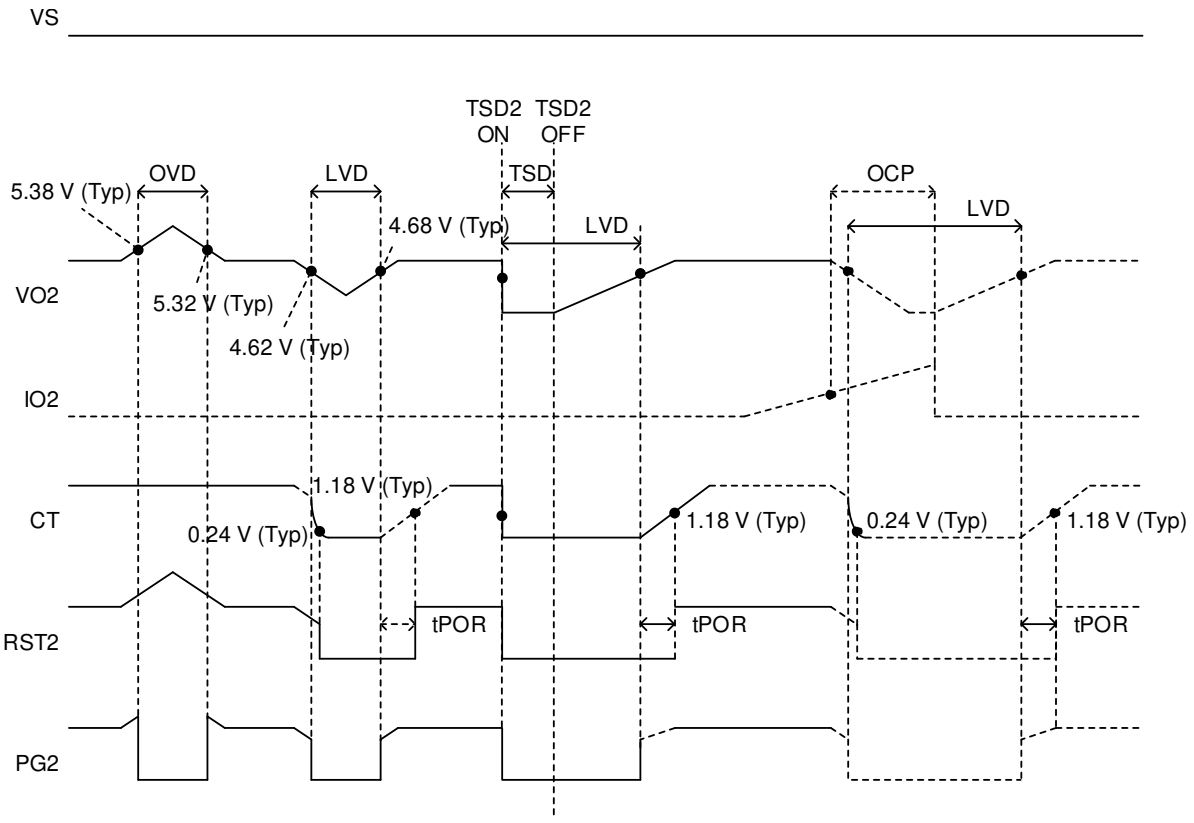
2. Start up・Stop
EN1 is controlled, EN2 short to VS, VOUT = 6 V, load from VO2 is 400 mA after VCC starts up.



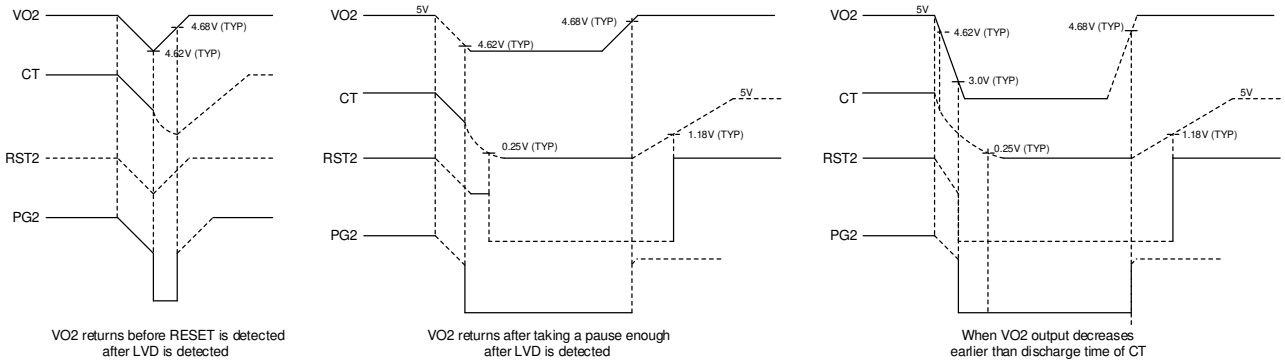
3. DCDC Converter Protection Operations



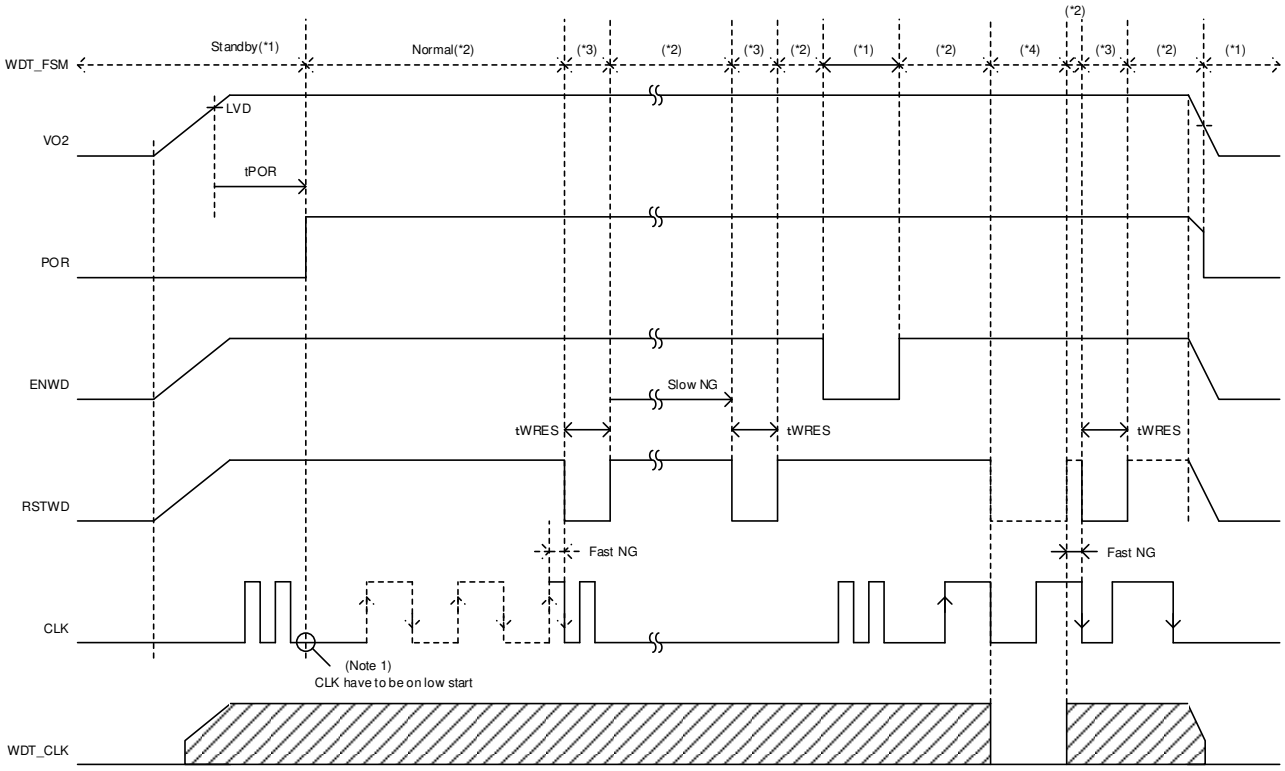
4. LDO Protection Operations (The Whole)



5. LDO Protection Operations (RESET timing)



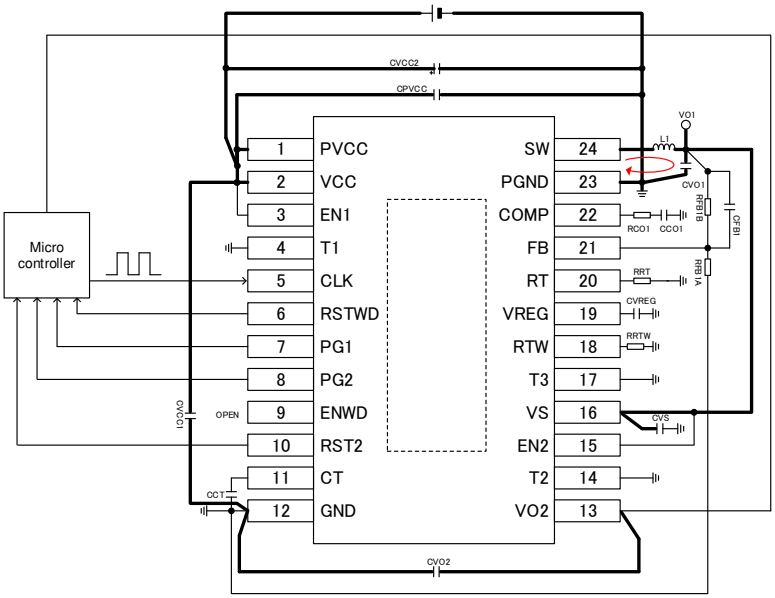
6. WDT



*1 : Standby Mode, *2 : Normal Mode, *3 : µC ERR Detect, *4 : OSC_WDT ERR Detect (See Figure 1. WDT FSM)
(Note 1) Please release power on reset in a state of CLK = LOW by all means.

Application Example

*There are many factors (Board layout, variation of the part, etc.) that can affect the characteristics.
Please verify and confirm using practical applications.
*Be sure to connect the T1, T2 and T3 pin to ground.
*In the case of high current application (About more than 500 mA from DC / DC convertor), please insert the schottky barrier diode between SW and PGND



Example of Constant Setting

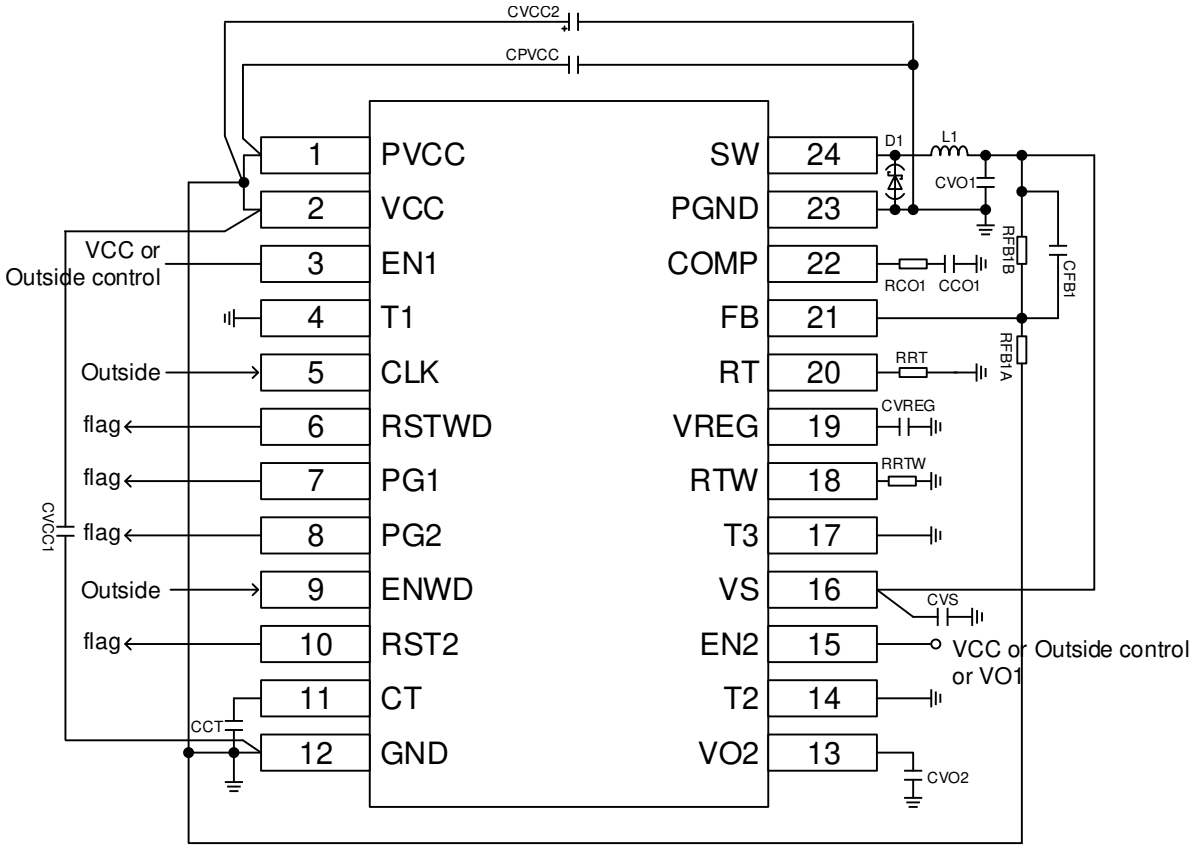
VCC = 13.5 V, VO1 = 6.5 V, fsw = 500 kHz, ILOAD (VO2) = 400 mA, fwdt = 100 kHz

name	Value	Unit	Parts No	size	manufacture
IC	-	-	BD39012EFV-C	7.8mm × 7.6mm	ROHM
L1	4.7	uH	3N1CDH74NP470KC	7.0mm × 7.0mm	SUMIDA
CVCC1	4.7	uF	GCM32ER71H475KA40L	3225	murata
CVCC2	47	uF	-	-	-
CPVCC	4.7	uF	GCM32ER71H475KA40L	3225	murata
CVO1	10 // 2	uF	GCM31CR71C106K	3216	murata
CVS	1	uF	GCM188R71C105K	1608	murata
CCT	0.1	uF	GCM188R11H104K	1608	murata
CVREG	1	uF	GCM188R71C105K	1608	murata
CFB1	100	pF	GCM1882C1H101JA01	1608	murata
CCO1	4700	pF	GCM2162C1H472JA01	1608	murata
CVO2	10	uF	GCM31CR71C106K	3216	murata
RFB1B	22	kΩ	MCR03	1608	ROHM
RFB1A	6.2 // 6.2	kΩ	MCR03	1608	ROHM
RRT	24	kΩ	MCR03	1608	ROHM
RRTW	24	kΩ	MCR03	1608	ROHM
RCO1	12	kΩ	MCR03	1608	ROHM

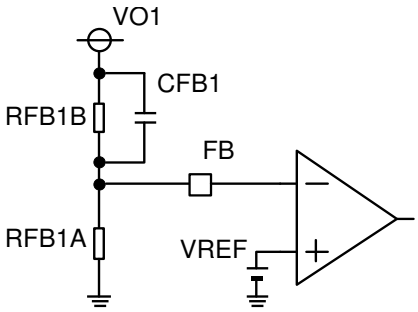
Notes for pattern layout of PCB

1. Design the wirings shown in bold line as short as possible.
2. Place the input ceramic capacitor CVCC1, CVCC2, CPVCC, CVO1, CVS and CVO2 as close to IC as possible.
3. Place RRT and RRTW in GND pin nearest IC not to receive a noise.
4. Place the RFB1A and RFB1B as close to FB pin as possible and provide the shortest wiring from FB pin. In addition, be careful not to arrange it in parallel with SW pin and high current line of L1 because it is the high Impedance line.
5. The loop of the red arrow is the line which high current line. Please layout with the shortest loop as much as possible, and wire with the 1-layer without pass the through hall.
6. Please connect to GND thermal plate of IC back.

Selection of Components Externally Connected



1) Setting the output voltage (RFB1A, RFB1B, CFB1B)
In BD39012EFV-C, VO1 voltage can be set from reference voltage 0.8 V (Typ) and the resistance division ratio of feed buck resistance RFB1A and RFB1B. Output voltage can be calculated as follow.



$$VO1 = 0.8 \times \left(1 + \frac{RFB1B}{RFB1A}\right)[V]$$

[Output voltage setting resistance]

Use of highly precise resistance less than ±1 % is recommended for output voltage setting. It is recommended that it is set around 1 kΩ to 100 kΩ for resistor value. The FB pin is very high impedance and easy to be affected by the noise. By all means connect resistance to nearest an IC. In addition, please layout it not to be affected by the noise of the SW pin without layout nearness. As needed, 0 point is made by assembling CFB1 beside RFB1B, and the stable ratio of the control system can be planned.
The equation of 0 points is as follows.

$$f_{zcf} = \frac{1}{2\pi \times RFB1B \times CFB1}\ [Hz]$$