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LDO Regulators with Watch Dog and Timer Voltage Detector

550 mA Output LDO Regulator with WDT and Voltage Detector

BD4271HFP-C BD4271FP2-C

General Description

BD4271HFP-C is automotive voltage regulator with watchdog timer and offers the output current of 550mA while limiting the quiescent current low. A logical "HIGH" at the CTL pin enables the LDO regulator and "LOW" disables the LDO regulator and keeps current consumption low.
A reset signal is generated for an output voltage V_O of Typ 4.65V.
The reset delay time and watchdog time (WDT) can be programmed by the external capacitor.

Key Specifications

- AEC-Q100 qualified (Note 1)
- Qualified for Automotive Applications
- Wide Temperature Range (Tj): -40 °C to +150 °C
- Wide Operating Input Range: -0.3 V to 45 V
- Low Quiescent Current: 75 µA (Typ)
- Output Load Current: 550 mA
- Output Voltage: 5.0 V (Typ) ± 2 %
- Reset Detect Voltage Accuracy: 4.53 V to 4.77 V
  4.65 V (Typ)
- Enable input
- Over Current Protection (OCP)
- Thermal Shut Down(TSD)

(Note1: Grade 1)

Features

- Low ESR ceramic capacitors applicable for output
- Low drop voltage: PDMOS output transistor
- Power on and under-voltage reset
- Programmable reset delay and watchdog time by external capacitor

Package

	W(Typ) × D(Typ) × H(Max)
HFP: HRP7	9.395 mm × 10.540 mm × 2.005 mm
FP2: TO263-7	10.00 mm x 14.95 mm x 4.50 mm

HRP7

TO263-7

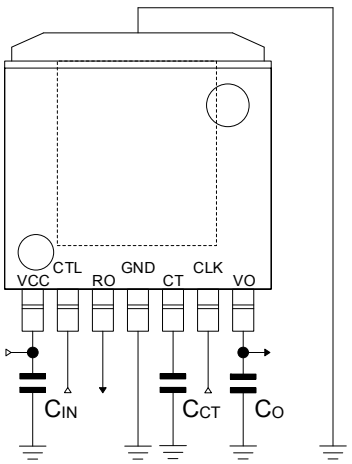
Applications

- Onboard vehicle device

(Engine ECU, Body-control, Car Stereos, Satellite Navigation System, etc.)

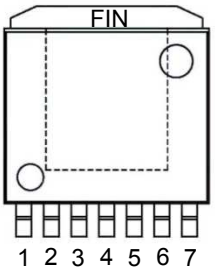
Typical Application Circuit

C_{IN} ≥ 0.1µF, C_{CT} = 0.001 µF to 10 µF, C_O ≥ 6 µF

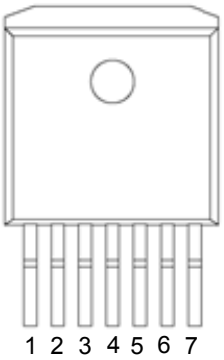


Pin Configurations

HRP7
(TOP VIEW)



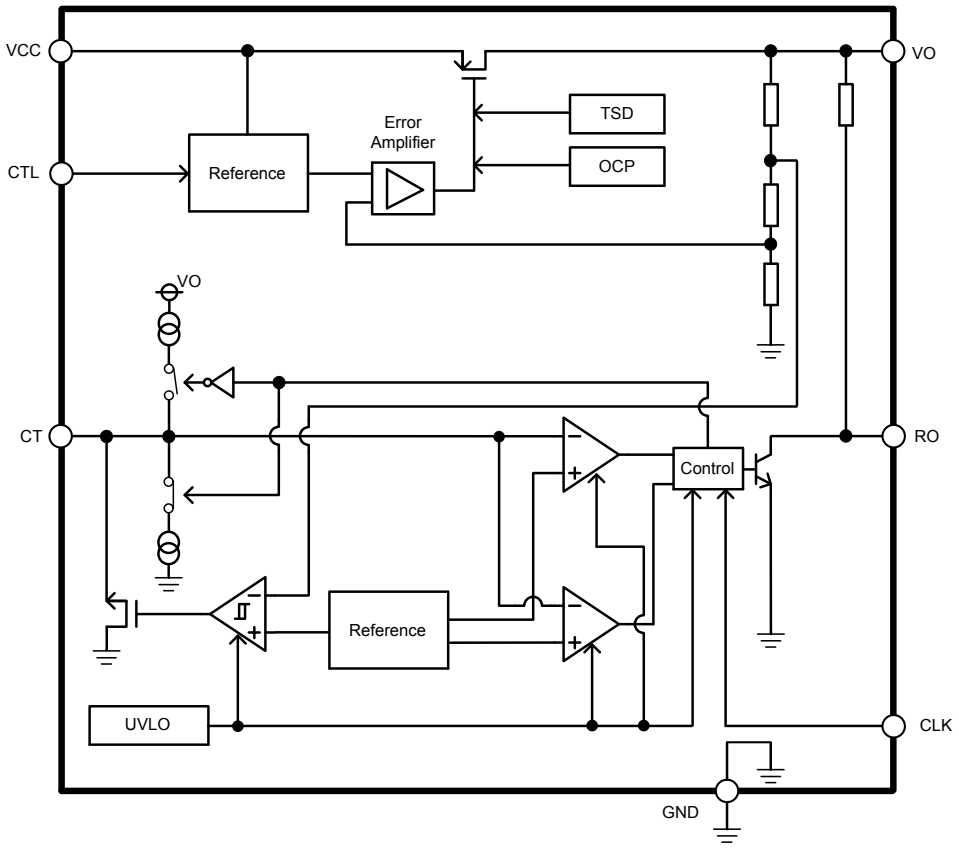
TO263-7
(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function
1	VCC	Input
2	CTL	Output control
3	RO	Reset output
4	GND	Ground
5	CT	Setting Reset Delay Time and WDT time
6	CLK	Input CLK from Microcomputer
7	VO	Output
FIN	GND	Ground

Block Diagram



Block Descriptions

Block Name	Function	Description of Blocks
TSD	Thermal shutdown protection	The TSD protects the device from overheating. If the chip temperature (Tj) reaches ca. 175 °C (Typ), the output is turned off.
Reference	Reference voltage	The Reference generates the Reference Voltage.
OCP	Over current protection	The OCP protects the device from damage caused by over current.
UVLO	Under voltage lock out	The UVLO prevents malfunction of the reset block in case of very low output voltage.
Error Amplifier	Error amplifier	The Error Amplifier amplifies the difference between the feed back voltage of the output voltage and the reference voltage.
Control	RESET + WDT time control	The reset delay time and watchdog time can be programmed.

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	-0.3 to +45.0	V
Output Control Voltage	V_{CTL}	-0.3 to +45.0	V
RO Voltage	V_{RO}	-0.3 to +7.0 (≤ V_O + 0.3)	V
Output Voltage	V_O	-0.3 to +7.0	V
CLK Voltage	V_{CLK}	-0.3 to V_O	V
Junction Temperature Range	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

Caution: Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters can result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc.). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.

Recommended Operating Conditions (-40°C ≤ Tj ≤ +150°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (I_O ≤ 300 mA)	V_{CC}	5.5	45.0	V
Supply Voltage (I_O ≤ 550 mA)	V_{CC}	6.0	45.0	V
Output Control Voltage	V_{CTL}	0	45.0	V
Start -Up Voltage (Note 1)	V_{CC}	3.0	—	V
Output Current	I_O	0	550	mA
Operating Ratings Temperature	Ta	-40	+125	°C

(Note 1) When I_O = 0 mA.

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
HRP7				
Junction to Ambient	θ_{JA}	96.0	22.0	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	6	2	°C/W
TO263-7				
Junction to Ambient	θ_{JA}	80.7	20.3	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	8	2	°C/W

(Note 1)Based on JESD51-2A(Still-Air)
(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4)Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Electrical Characteristics (LDO)
(Unless otherwise specified, Tj = -40 °C to +150 °C, V_{CC} = 13.5 V, V_{CTL} = 5 V, I_O = 0 mA, the typical value is defined at Tj = 25 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I_{CC}	—	75	150	μA	I_O = 0 mA
Standby Current	I_{ST}	—	2.0	9.0	μA	V_{CTL} = 0 V Tj ≤ 125 °C
Output Voltage	V_O	4.90	5.00	5.10	V	6 V ≤ V_{CC} ≤ 40 V 0 mA ≤ I_O ≤ 300 mA
Output Voltage	V_O	4.90	5.00	5.10	V	8 V ≤ V_{CC} ≤ 26 V I_O ≤ 550 mA
Dropout Voltage	ΔV_d	—	0.2	0.5	V	V_{CC} = 4.75 V I_O = 300 mA
Ripple Rejection	R.R.	—	60	—	dB	f = 120 Hz, ein = 1 Vrms I_O = 100 mA
Line Regulation	Reg.I	-30	—	30	mV	8 V ≤ V_{CC} ≤ 16 V
Load Regulation	Reg.L	—	10	40	mV	10 mA ≤ I_O ≤ 300 mA
Thermal Shut Down	TSD	—	175	—	°C	Tj at TSD ON
Over Current Protection	I_O	550	—	—	mA	
CTL ON Mode Voltage	V_{thH}	2.7	—	—	V	Active Mode
CTL OFF Mode Voltage	V_{thL}	—	—	0.8	V	Off Mode
CTL Input Current	I_{CTL}	—	15	30	μA	V_{CTL} = 5 V

Electrical Characteristics (Reset, WDT Function)

(Unless otherwise specified, Tj = -40 °C to +150 °C, V_{CC} = 13.5 V, V_{CTL} = 5 V, I_O = 0 mA, the typical value is defined at Tj = 25 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Reset Detection Voltage	V_{RT}	4.53	4.65	4.77	V	—
Reset Detection Hysteresis	V_{RHY}	25	60	100	mV	3.5 V ≤ Vo ≤ 4.4 V
Reset Pull-up Resistance	R_{RO}	18	30	46	kΩ	—
Reset Low Voltage	V_{RO}	—	—	0.4	V	—
CT Upper-side Threshold	V_{CTH}	—	1.80	—	V	—
CT Lower-side Threshold	V_{CTL}	—	0.45	—	V	—
CT Charge Current	I_{CT}	—	16	—	μA	V_{CT} = 0.15 V
CT Discharge Current	I_{CT}	—	3	—	μA	V_{CT} = 1.35 V
Delay Time L→H	t_d	8	11.5	16	ms	C_{CT} = 0.1 μF (Note 1)
WDT Monitor Time	t_{WH}	30	45	66	ms	C_{CT} = 0.1 μF (Note 1)
WDT Reset Time	t_{WL}	5	9	15	ms	C_{CT} = 0.1 μF (Note 1)
WDT OFF threshold Voltage	V_{HCLK}	V_O × 0.8	—	V_O	V	
WDT ON threshold Voltage	V_{LCLK}	0	—	V_O × 0.3	V	CLK is pulled down inside the IC when CLK open.
CLK Input Current	I_{CLK}	1.5	5	15	μA	V_{CLK} = 5 V
CLK Input Pulse Width	t_{PCLK}	3	—	—	μs	
Minimum Operation Voltage	V_{OPR}	1	—	—	V	RO < 0.5 V

(Note 1) t_d, t_{WH}, and t_{WL} can be varied by changing the CT capacitance value. (0.001μF to 10 μF available)

t_d (ms) ≈ t_d (the Deley Time at 0.1μF) × C_{CT} (μF) / 0.1 — CT Capacitor: 0.1μF ≤ C_{CT} ≤ 10 μF
for example: when C_{CT} = 1μF, 80ms ≤ t_d ≤ 160 ms
t_{WH} (ms) ≈ t_{WH} (the WDT Monitor Time at 0.1μF) × C_{CT} (μF) / 0.1 — CT Capacitor: 0.1μF ≤ C_{CT} ≤ 10 μF
for example: when C_{CT} = 1μF, 300ms ≤ t_d ≤ 660 ms
t_{WL} (ms) ≈ t_{WL} (the WDT Reset Time at 0.1μF) × C_{CT} (μF) / 0.1 — CT Capacitor: 0.1μF ≤ C_{CT} ≤ 10 μF
for example: when C_{CT} = 1μF, 50ms ≤ t_d ≤ 150 ms

t_d (ms) ≈ t_d (the Delay Time at 0.1μF) × C_{CT} (μF) / 0.1 ± 0.1 — CT Capacitor: 0.001μF ≤ C_{CT} < 0.1 μF
for example: when C_{CT} = 0.01μF, 0.7ms ≤ t_d ≤ 1.7 ms
t_{WH} (ms) ≈ t_{WH} (the WDT Monitor Time at 0.1μF) × C_{CT} (μF) / 0.1 — CT Capacitor: 0.001μF ≤ C_{CT} < 0.1 μF
for example: when C_{CT} = 0.01μF, 2.9ms ≤ t_d ≤ 6.7 ms
t_{WL} (ms) ≈ t_{WL} (the WDT Reset Time at 0.1μF) × C_{CT} (μF) / 0.1 — CT Capacitor: 0.001μF ≤ C_{CT} < 0.1 μF
for example: when C_{CT} = 0.01μF, 0.4ms ≤ t_d ≤ 1.6 ms

Typical Performance Curves (Unless otherwise specified, Tj = 25 °C, V_{CC} = 13.5 V, V_{CTL} = 5 V)

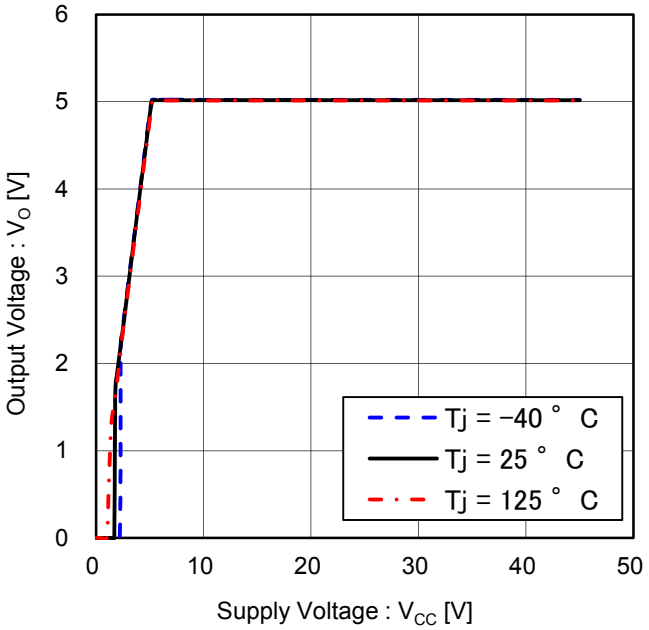


Figure 1. Output Voltage vs Supply Voltage
(R_L = 25 Ω)

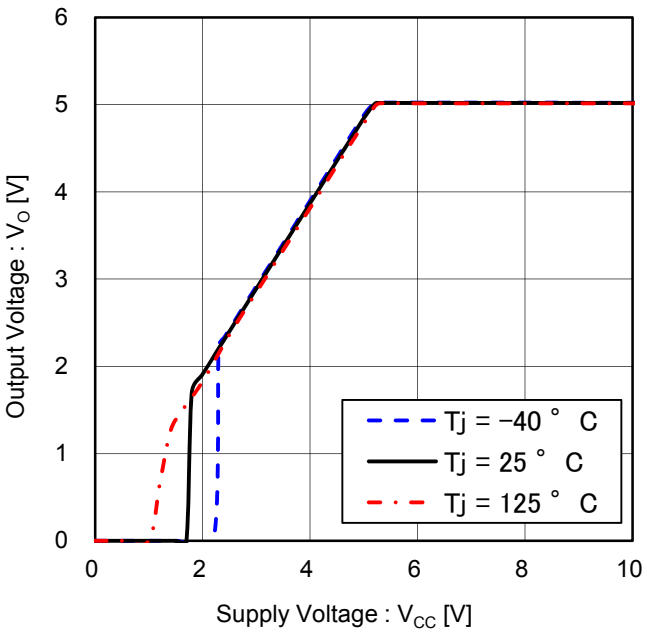


Figure 2. Output Voltage vs Supply Voltage
(R_L = 25 Ω)

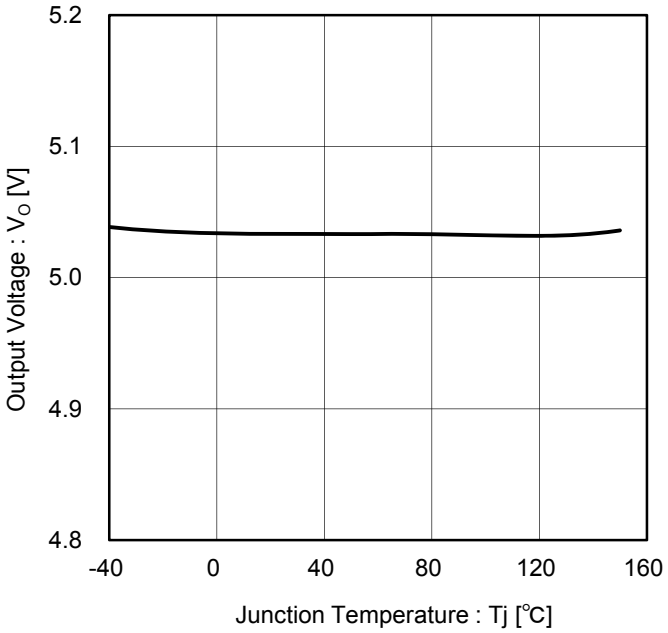


Figure 3. Output Voltage vs Junction Temperature
(R_L = 1 kΩ)

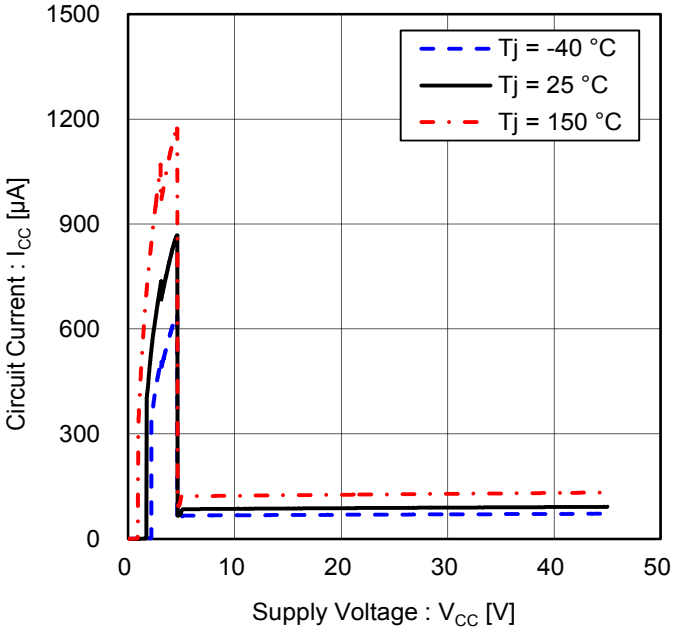


Figure 4. Circuit Current vs Supply Voltage

Typical Performance Curves - continued

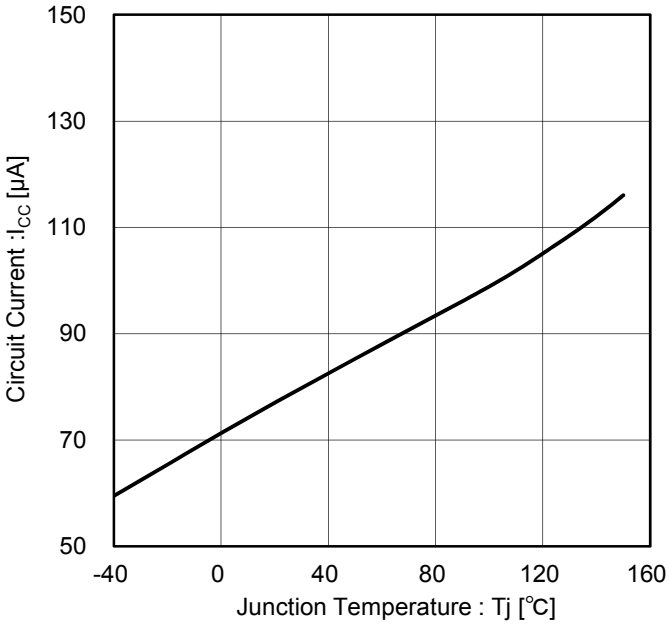


Figure 5. Circuit Current vs Junction Temperature

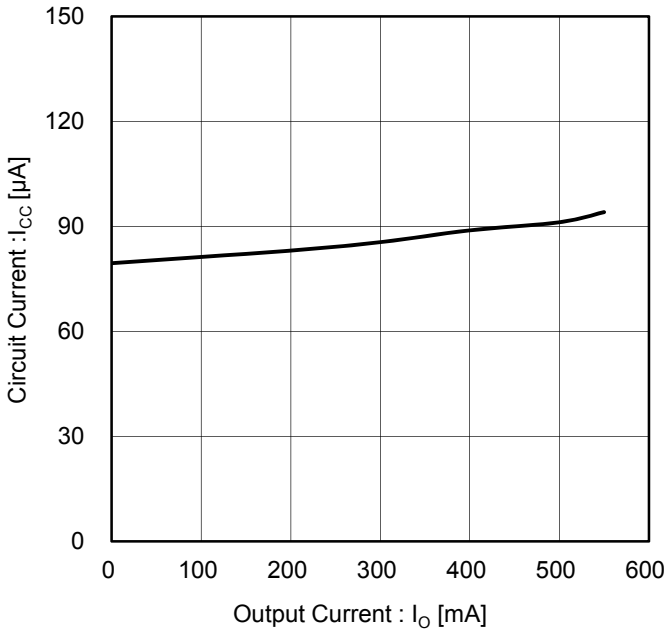


Figure 6. Circuit Current vs Output Current

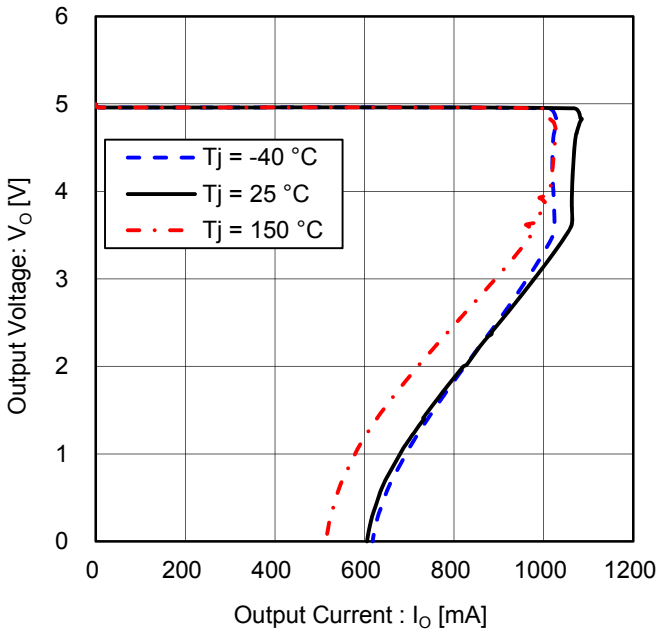


Figure 7. Output Voltage vs. Output Current
(Over Current Protection)

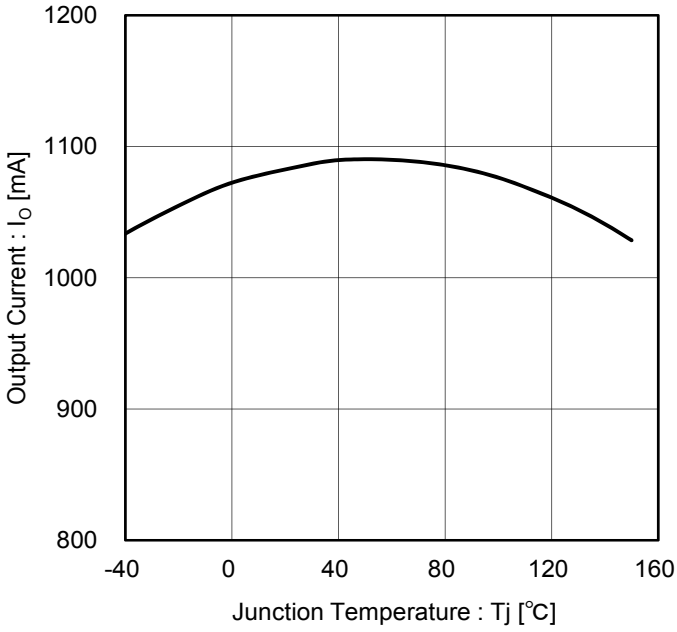


Figure 8. Output Current vs Junction Temperature

Typical Performance Curves - continued

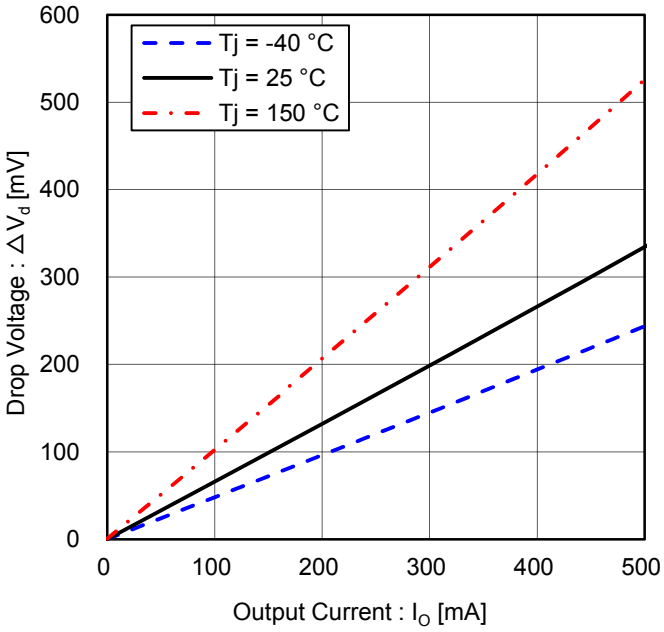


Figure 9. Drop Voltage vs Output Current
(V_{CC} = 4.75 V)

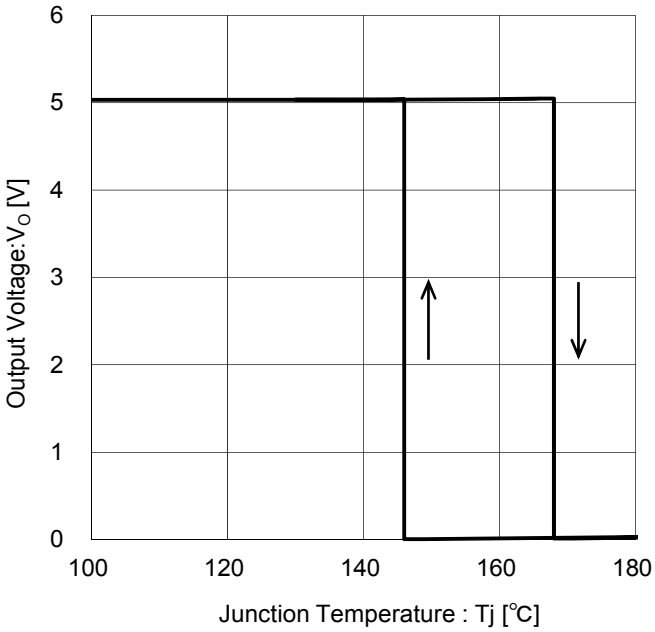


Figure 10. Output Voltage vs Junction Temperature
(Thermal Shut Down)

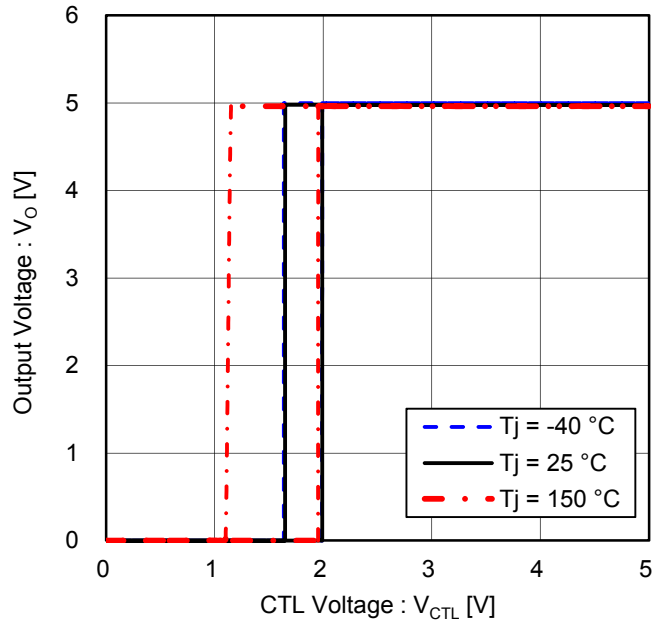


Figure 11. Output Voltage vs CTL Voltage

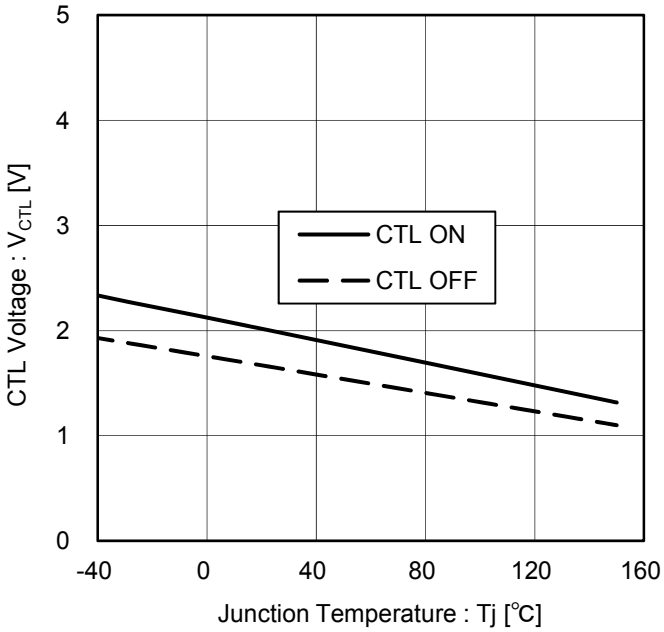


Figure12. CTL Voltage vs Junction Temperature

Typical Performance Curves - continued

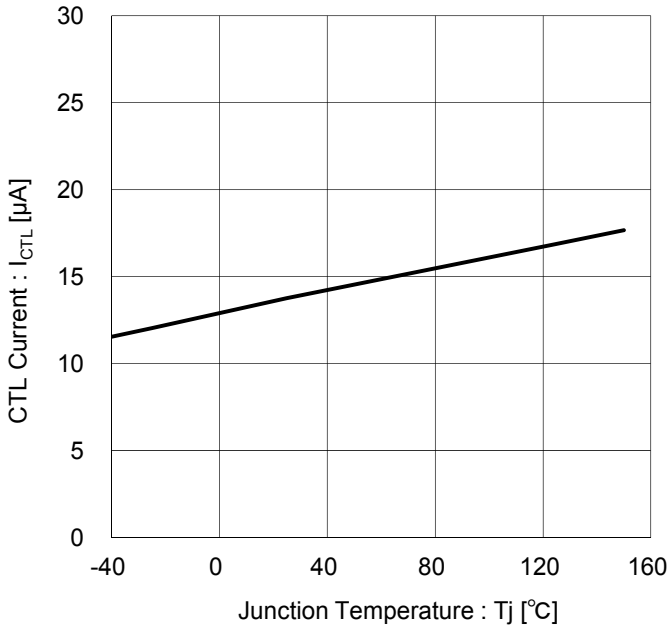


Figure 13. Output Voltage vs CTL Current

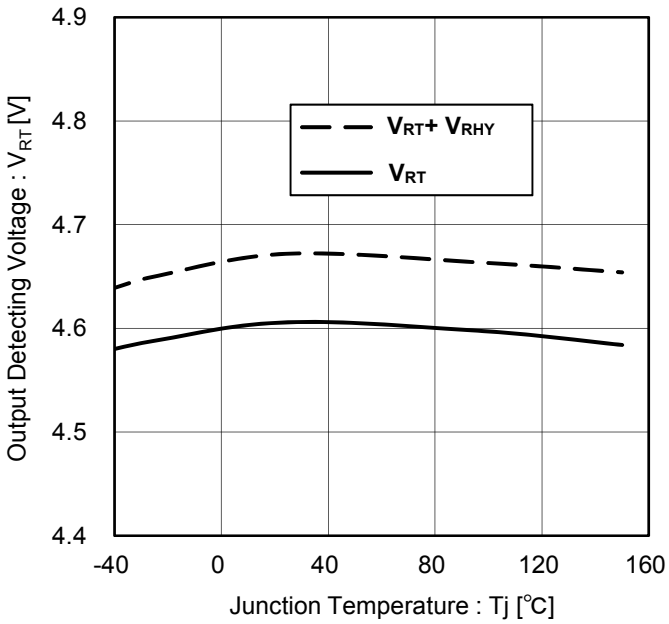


Figure 14. Output Detecting Voltage vs Junction Temperature

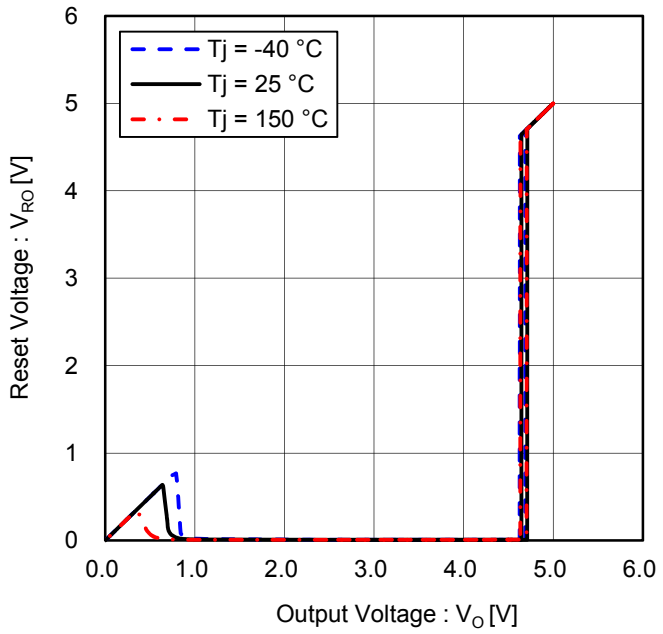


Figure 15. RO Voltage vs Output Voltage

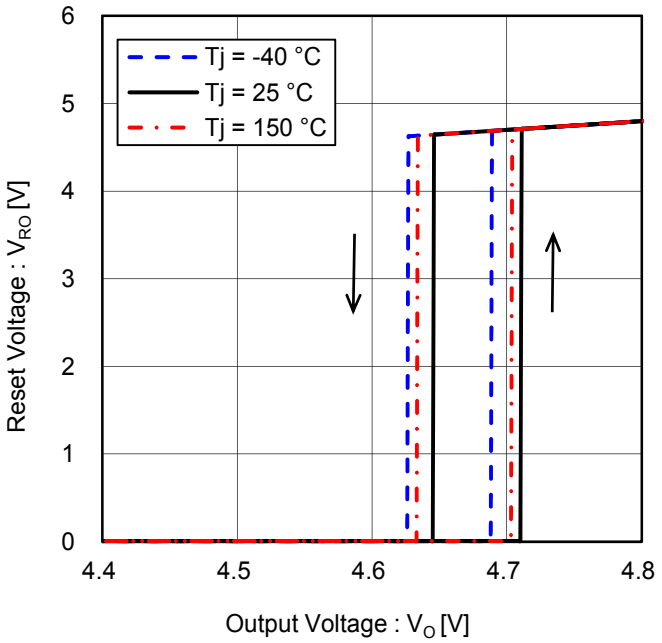


Figure 16. RO Voltage vs Output Voltage

Typical Performance Curves - continued

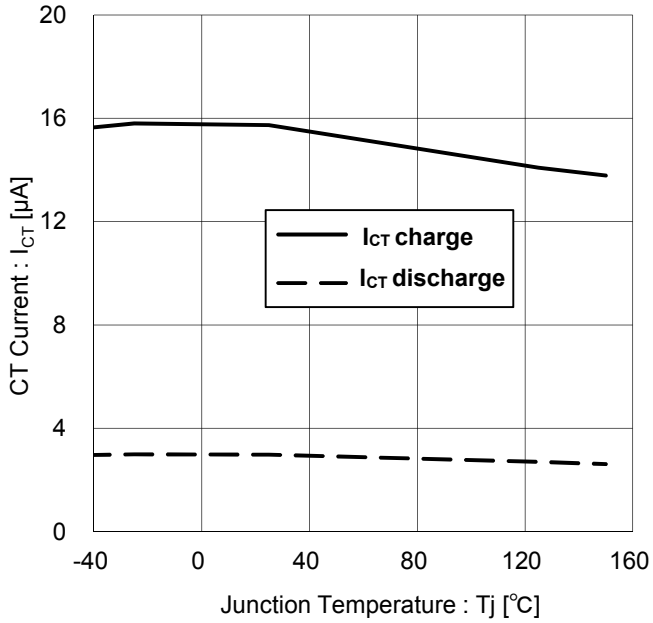


Figure 17. CT Current vs Junction Temperature

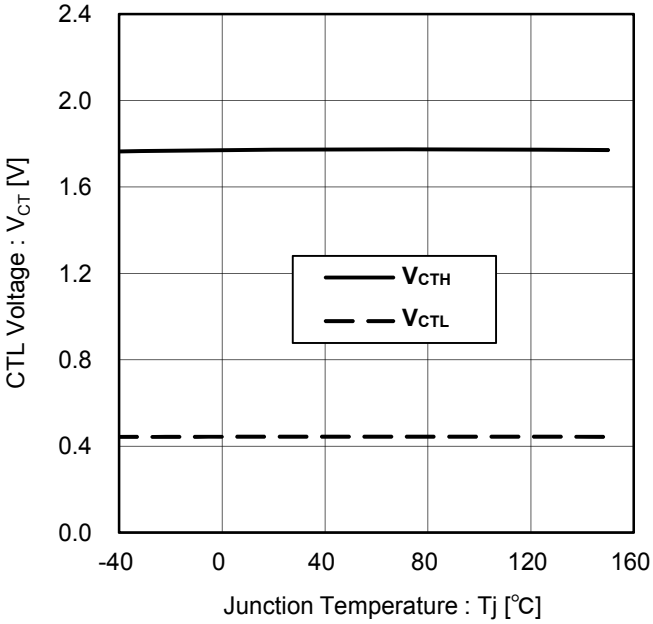


Figure 18. CT Voltage vs Junction Temperature

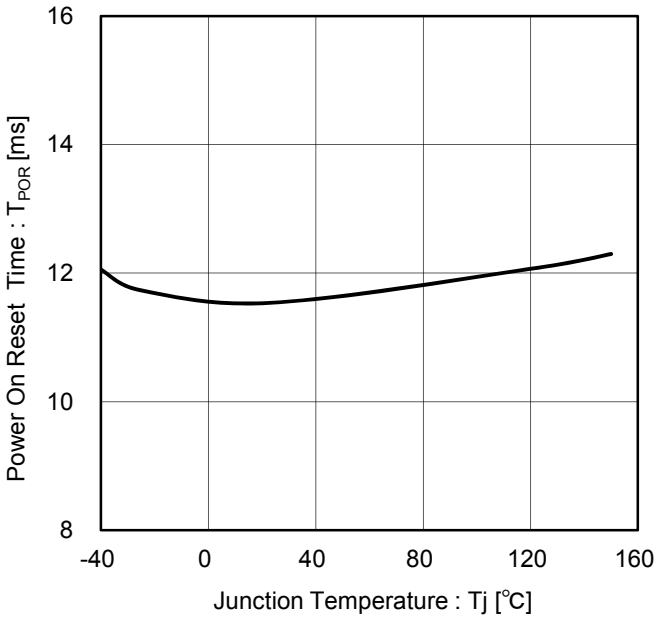


Figure 19. Power on Reset Time vs Junction Temperature
(C_{CT} = 0.1 μF)

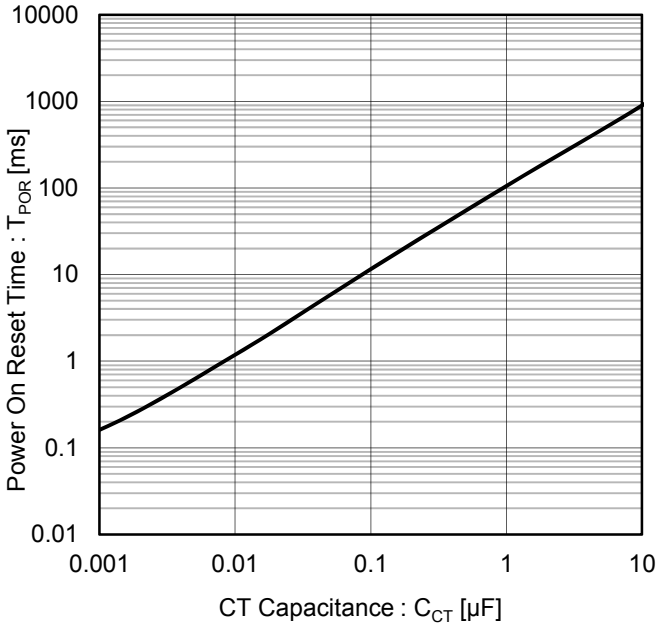


Figure 20. Power on Reset Time vs CT Capacitance

Typical Performance Curves - continued

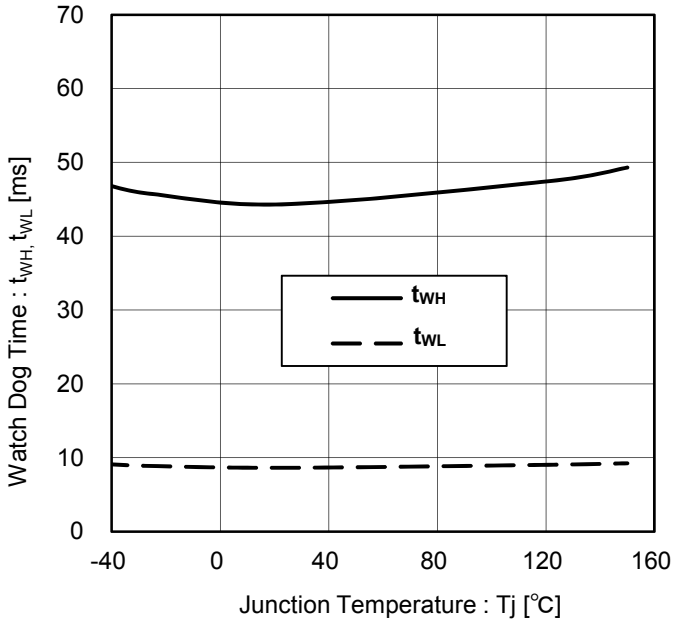


Figure 21. Watch Dog Time vs Junction Temperature

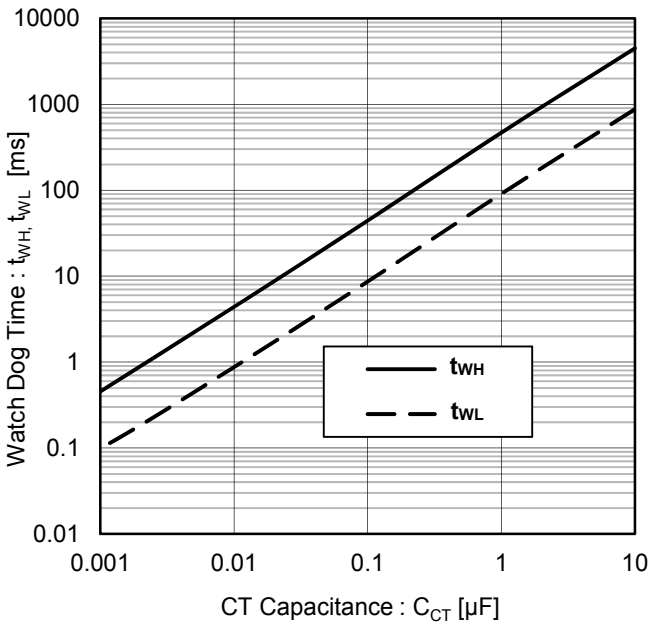
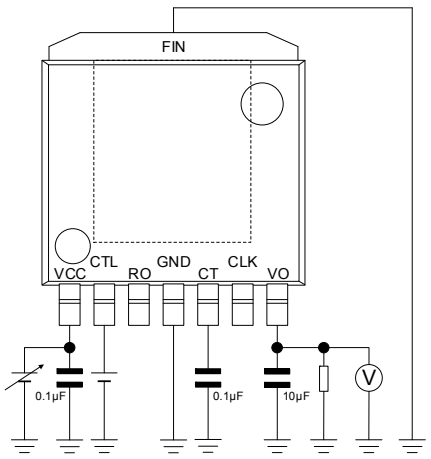
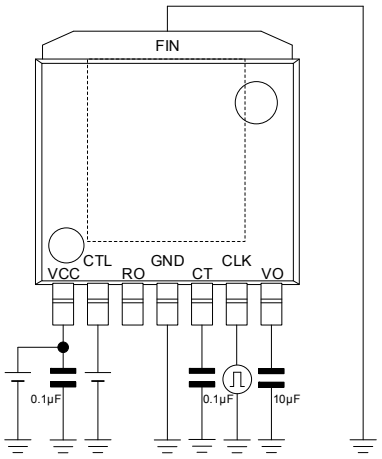


Figure 22. Watch Dog Time vs CT Capacitance

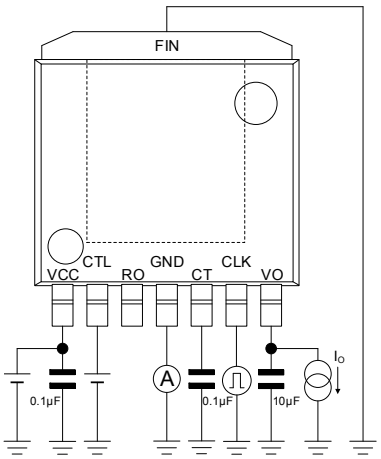
Measurement Circuit



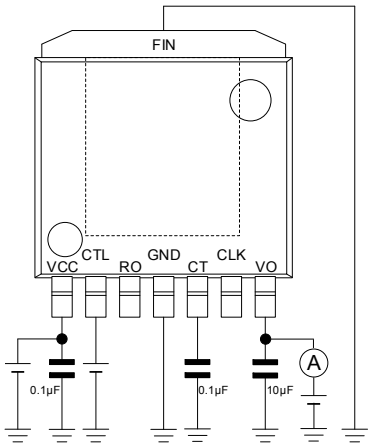
Measurement setup for Figure 1,2,3,10.



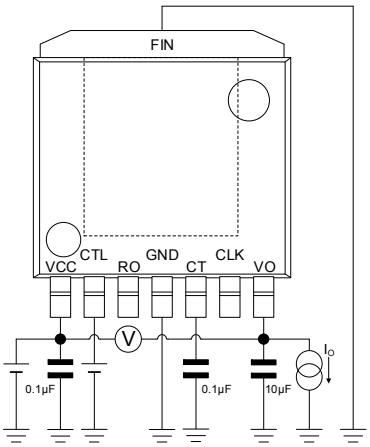
Measurement setup for Figure 4,5.



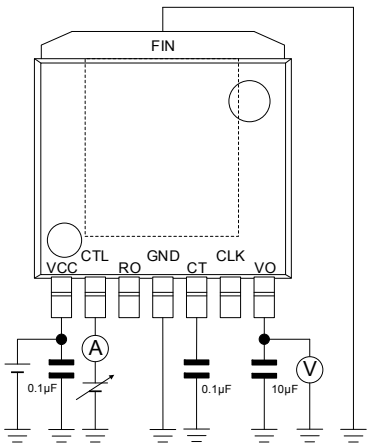
Measurement setup for Figure 6.



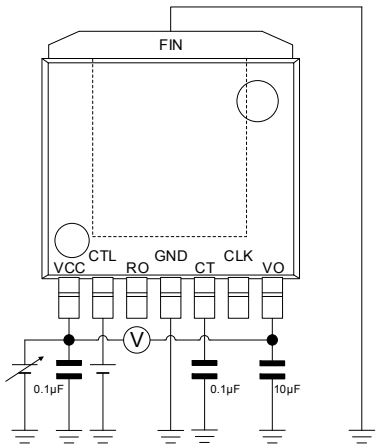
Measurement setup for Figure 7,8.



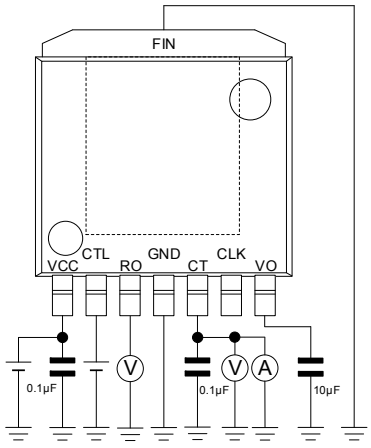
Measurement setup for Figure 9.



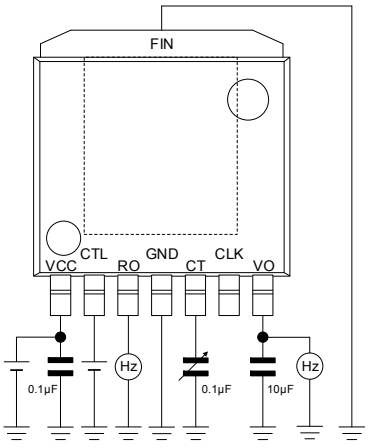
Measurement setup for Figure 11,12,13.



Measurement setup for Figure 14,15,16.



Measurement setup for Figure 17,18.



Measurement setup for Figure 19,20,21,22.

Figure 23. Measurement Circuit

Timing Chart

1. When supply voltage V_{CC} is ON ⇔ OFF (Not to input CLK voltage V_{CLK} when output voltage V_O = Low)

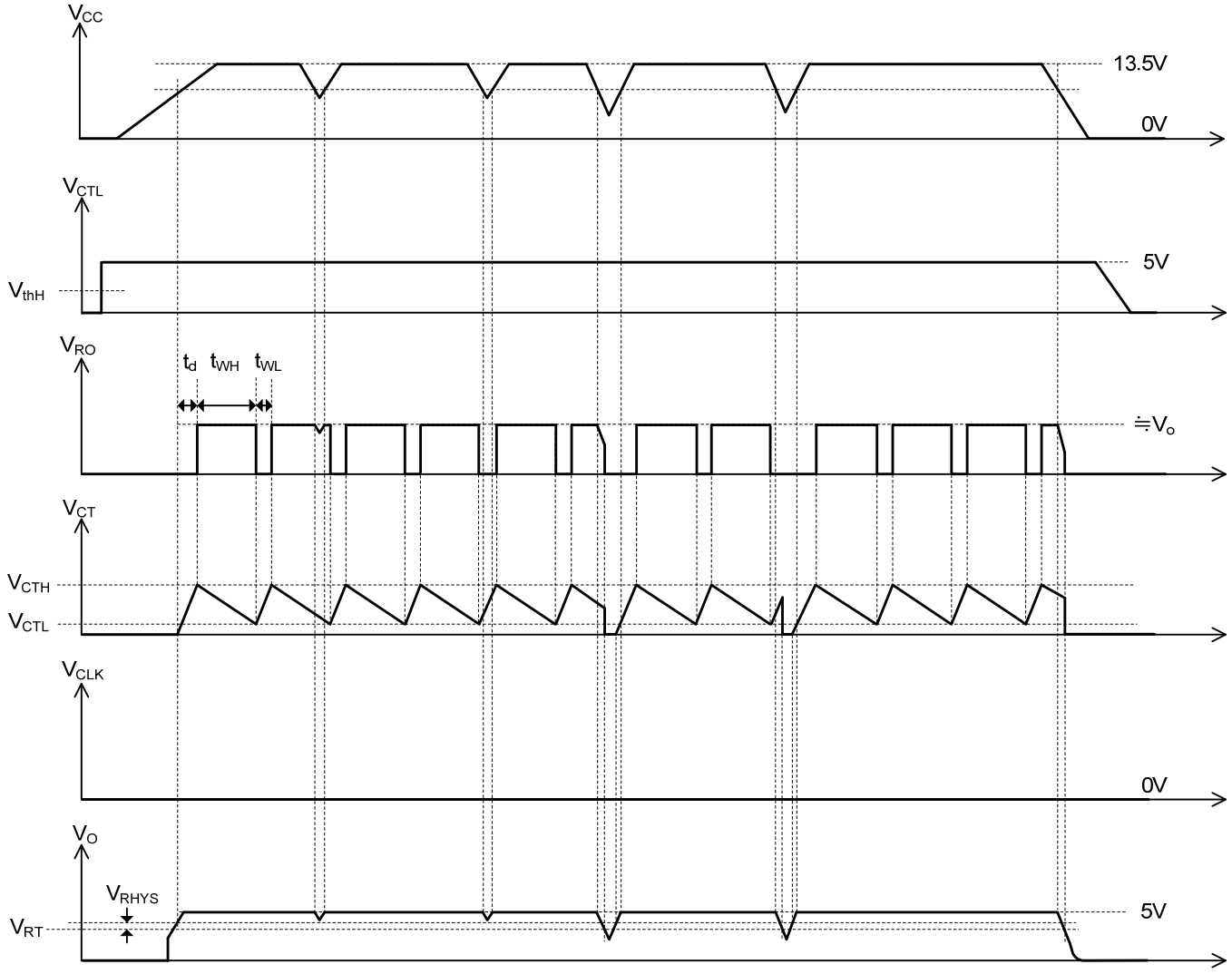


Figure 24. Timing Chart 1

Timing Chart – continued

2. When output control voltage V_{CTL} is ON ⇔ OFF (Not to input CLK voltage V_{CLK} when output voltage V_O = Low)

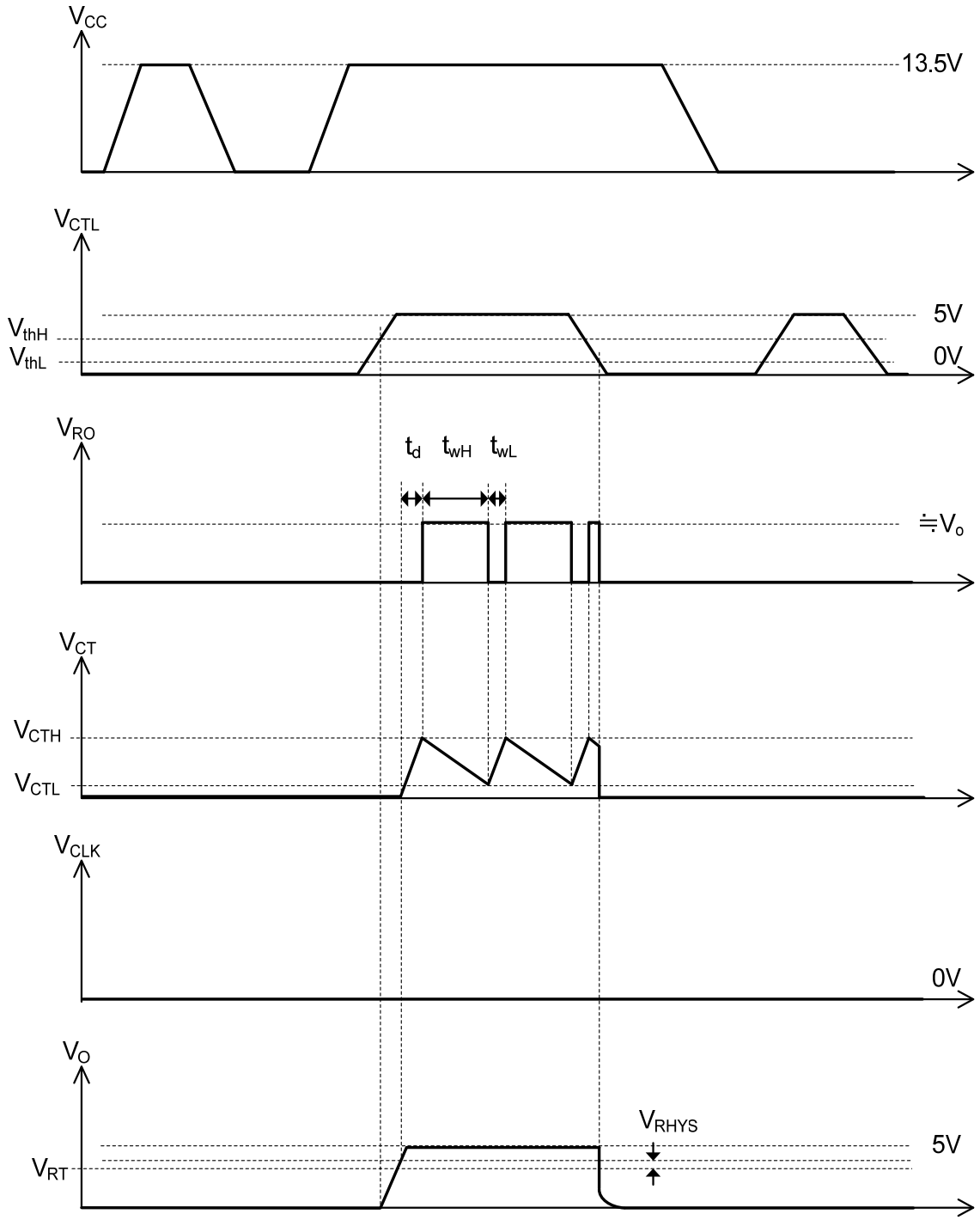


Figure 25. Timing Chart 2

The Delay Time (t_d) is estimated roughly by following calculation.

$$t_d[s] \approx \frac{V_{CTH}[V] \times C_{CT}[F]}{I_{CT}(charge)[A]}$$

Basically, verify the Delay Time (t_d) by the ratio of the value at C_{CT} = 0.1μF specified in datasheet and the actual C_{CT} capacitance used to calculate.

Timing Chart – continued

3. When WDT threshold Voltage V_{CLK} is ON ⇔ OFF

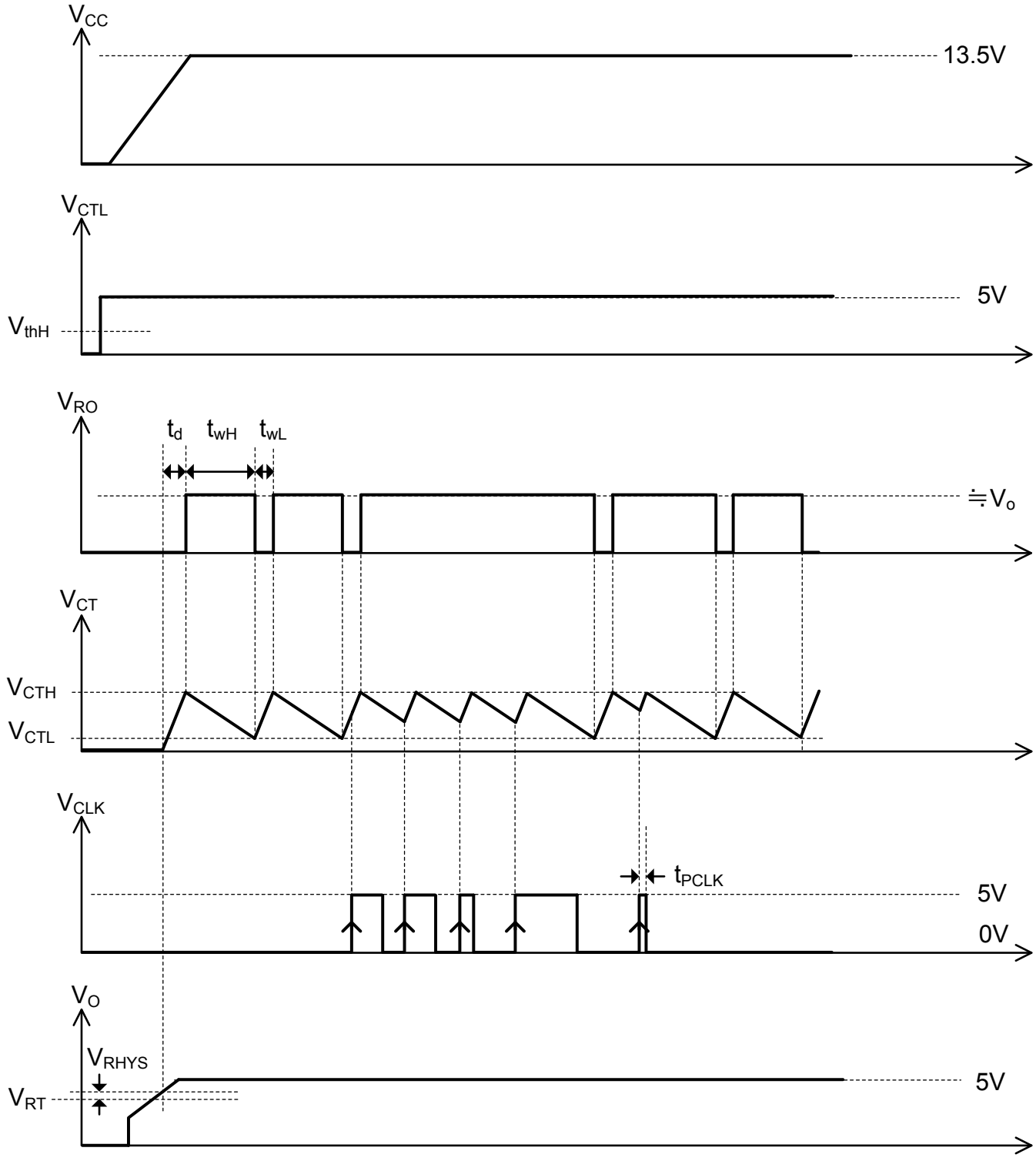


Figure 26. Timing Chart 3

The WDT Monitor Time (t_{WH}) and the WDT Reset Time (t_{WL}) is estimated roughly by following calculation.

$$t_{WH}[s] \approx \frac{|V_{CTH} - V_{CTL}|[V] \times C_{CT}[F]}{I_{CT}(\text{discharge})[A]} \qquad t_{WL}[s] \approx \frac{|V_{CTL} - V_{CTH}|[V] \times C_{CT}[F]}{I_{CT}(\text{charge})[A]}$$

Basically, verify the WDT Monitor Time (t_{WH}) and the WDT Reset Time (t_{WL}) by the ratio of the value at C_{CT} = 0.1μF specified in datasheet and the actual C_{CT} capacitance used to calculate

Selection of Components Externally Connected

・VCC pin capacitor

Insert capacitors with a capacitance of 0.1 µF or higher between the VCC and GND pin. We recommend using ceramic capacitor generally featuring good high frequency characteristic. When selecting a ceramic capacitor, please be consider about temperature and DC - biasing characteristics. Place capacitors closest possible to VCC - GND pin. When input impedance is high, e.g. in case there is distance from battery, line voltage drop needs to be prevented by large capacitor. Choose the capacitance according to the line impedance between the power smoothing circuit and the VCC pin. Selection of the capacitance also depends on the applications. Verify the application and allow sufficient margins in the design. We recommend using a capacitor with excellent voltage and temperature characteristics.

・Output pin capacitor

In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND pin. We recommend using a ceramic capacitor with a capacitance of 6 µF or higher. In selecting the capacitor, ensure that the capacitance of 6 µF or higher is maintained at the intended applied voltage and temperature range. Due to changes in temperature the capacitor's capacitance can fluctuate possibly resulting in oscillation.

In actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore verification of the final operating environment is needed. When selecting a ceramic capacitor, we recommend using X7R or better components with excellent temperature and DC - biasing characteristics and high voltage tolerance.

In case of the transient input voltage and the load current fluctuation, output voltage may fluctuate. In case this fluctuation can be problematic for the application, connect low ESR capacitor (capacitance > 6 µF, ESR < 1 Ω) in paralleled to large capacitor with a capacitance of 13 µF or higher and ESR of 5 Ω or lower. Electrolytic and tantalum capacitors can be used as large capacitor. When selecting an electrolytic capacitor, please consider about increasing ESR and decreasing capacitance at cold temperature.

Place the capacitor closest possible to output pin.

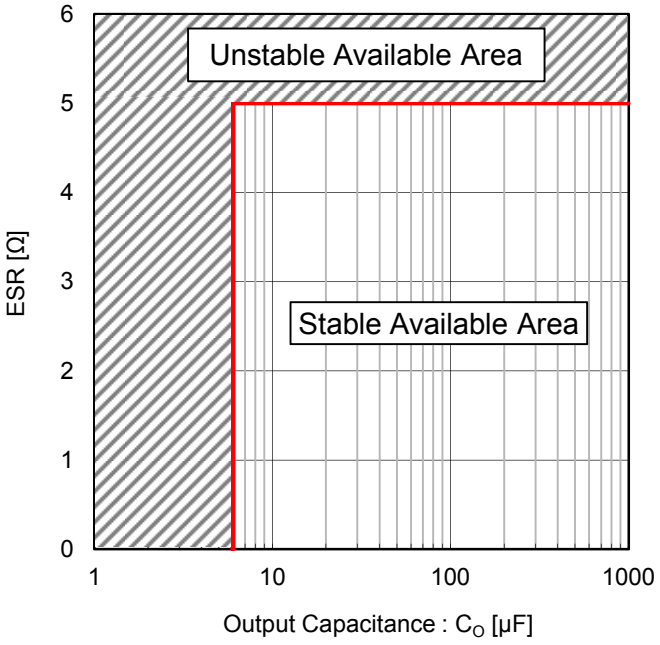


Figure 27. Output Capacitance ESR Available Area

-40 °C ≤ Tj ≤ +150 °C, 6V ≤ V_{CC} ≤ 45 V, V_{CTL} = 5 V, I_O = 0 mA to 550mA

Power Dissipation

■HRP7

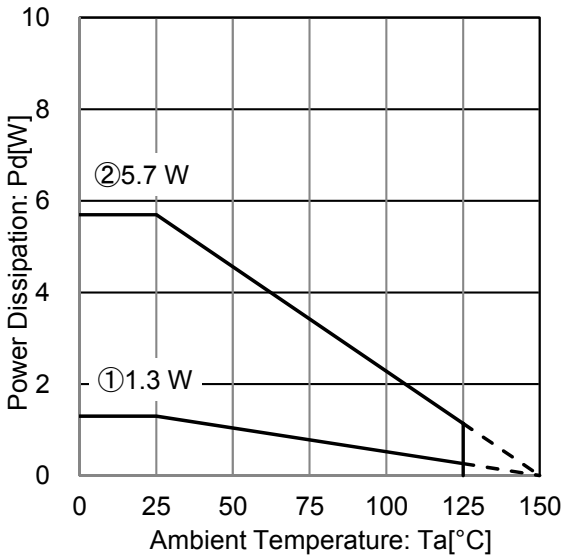


Figure 28. HRP7 Package Data

IC mounted on ROHM standard board based on JEDEC.
① : 1 - layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.

② : 4 - layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB:
74.2 mm x 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB:
74.2 mm x 74.2 mm, 2 oz. copper.

Condition①: θ_{JA} = 96.0 °C/W、Ψ_{JT} (top center) = 6 °C/W
Condition②: θ_{JA} = 22.0 °C/W、Ψ_{JT} (top center) = 2 °C/W

■TO263-7

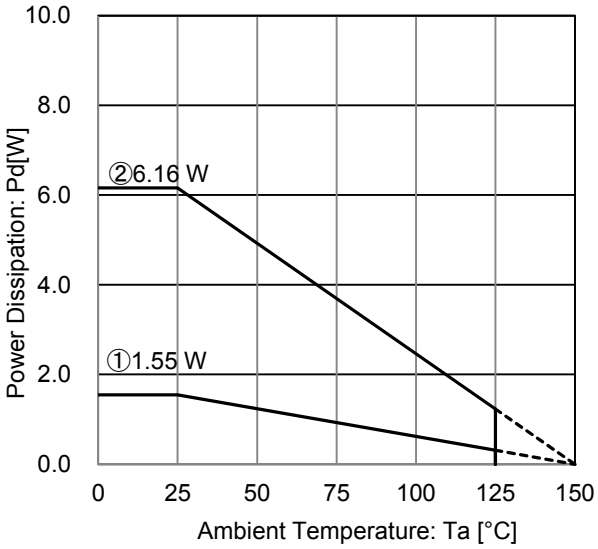


Figure 29. TO263-7 Package Data

IC mounted on ROHM standard board based on JEDEC.
① : 1 - layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.

② : 4 - layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB:
74.2 mm x 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB:
74.2 mm x 74.2 mm, 2 oz. copper.

Condition①: θ_{JA} = 80.7 °C/W、Ψ_{JT} (top center) = 8 °C/W
Condition②: θ_{JA} = 20.3 °C/W、Ψ_{JT} (top center) = 2 °C/W

Thermal Design

This product exposes a frame on the back side of the package for thermal efficiency improvement.
Within this IC, the power consumption is decided by the dropout voltage condition, the load current and the circuit current. Refer to power dissipation curves illustrated in Figure 28, 29 when using the IC in an environment of Ta ≥ 25 °C. Even if the ambient temperature Ta is at 25 °C, depending on the input voltage and the load current, chip junction temperature can be very high. Consider the design to be Tj ≤ Tjmax = 150 ℃ in all possible operating temperature range.
Should by any condition the maximum junction temperature Tjmax = 150℃ rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature Tj.
Tj can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature Tj.
   $Tj = Ta + P_C \times \theta_{JA}$

Tj	: Junction Temperature
Ta	: Ambient Temperature
P_C	: Power Consumption
θ_{JA}	: Thermal Impedance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature Tj.
   $Tj = T_T + P_C \times \Psi_{JT}$

Tj	: Junction Temperature
T_T	: Top Center of Case's (mold) Temperature
P_C	: Power Consumption
Ψ_{JT}	: Thermal Impedance (Junction to Top Center of Case)

The following method is used to calculate the power consumption P_c (W).
$P_C = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC}$

P_C	: Power Consumption
V_{CC}	: Supply Voltage
V_O	: Output Voltage
I_O	: Load Current
I_{CC}	: Circuit Current

・Calculation Example

If V_{CC} = 13.5 V、V_O = 5.0 V、I_O = 200 mA、I_{CC} = 85 μA, the power consumption P_c can be calculated as follows:

$P_C = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC}$
= (13.5 V – 5.0 V) × 200 mA + 13.5 V × 85 μA
= 1.7 W

At the ambient temperature Tamax = 85°C, the thermal impedance (Junction to Ambient)θ_{JA} = 22.0 °C / W(4-layer PCB),

$Tj = Tamax + P_C \times \theta_{JA}$
= 85 °C + 1.7 W × 22.0 °C / W
= 122.4 °C

When operating the IC, the top center of case's (mold) temperature T_T = 100℃、Ψ_{JT} = 6 °C / W(1-layer PCB),

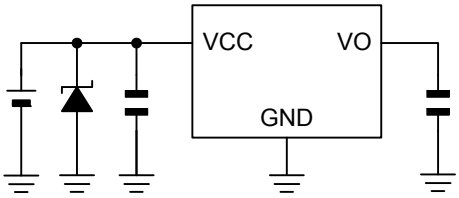
$Tj = T_T + P_C \times \Psi_{JT}$
= 100 °C + 1.7 W × 6 °C / W
= 110.2 °C

For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad.

Application Examples

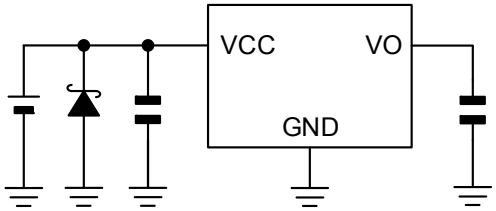
・Applying positive surge to the VCC

If the possibility exists that surges higher than 45 V will be applied to the VCC, a Zener Diode should be placed between the VCC and GND as shown in the figure below.



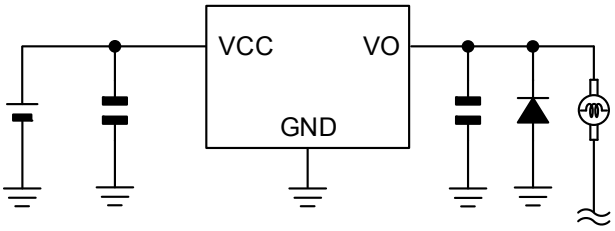
・Applying negative surge to the VCC

If the possibility exists that negative surges lower than the GND are applied to the VCC, a Shottky Diode should be place between the VCC and GND as shown in the figure below.



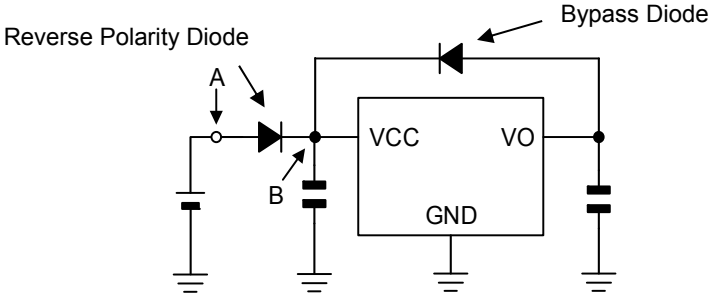
・Implementing a Protection Diode

If the possibility exists that a large inductive load is connected to the output pin resulting in back-EMF at time of startup and shutdown, a protection diode should be placed as shown in the figure below.



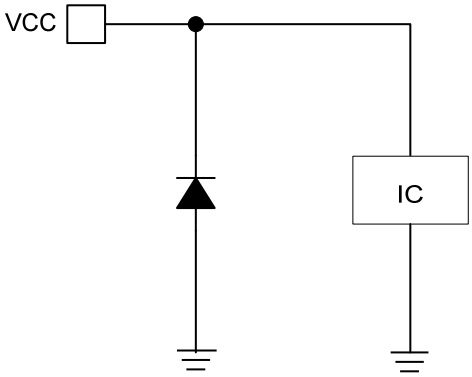
・Reverse Polarity Diode

In some applications, the VCC and the VO potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, the accumulated charge in the output pin capacitor flowing backward from the VO to the VCC when the VCC shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 1000 μF. Also by inserting a reverse polarity diode in series to the VCC, it can prevent reverse current from reverse battery connection or the case. When the point A is short-circuited GND, if there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VCC and the VO.

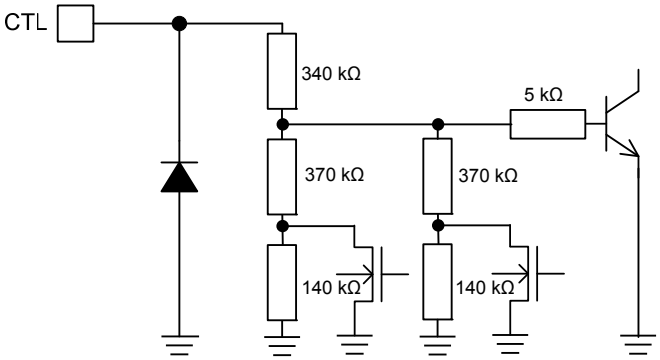


I/O Equivalence Circuits (Note 1)

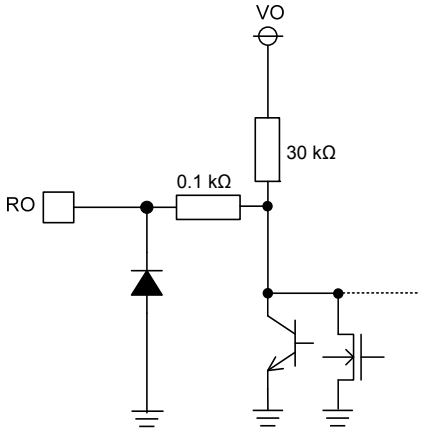
1 VCC



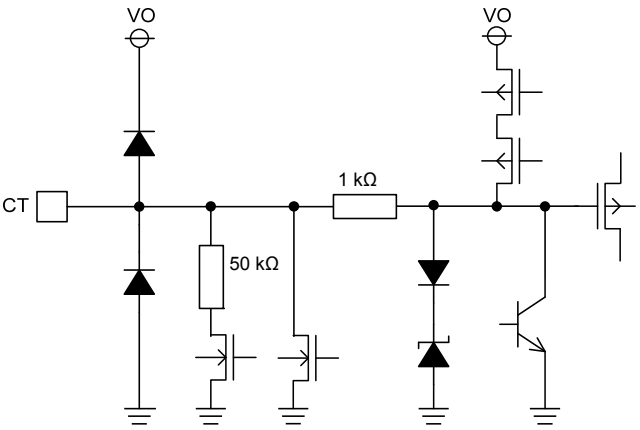
2 CTL



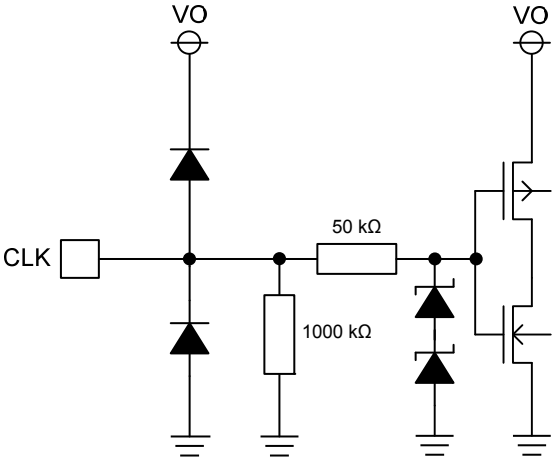
3 RO



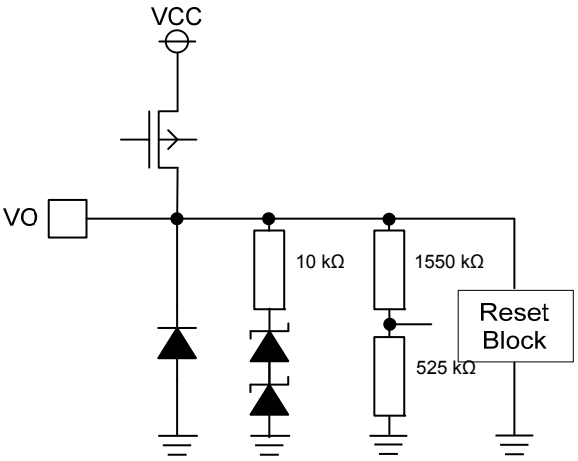
5 CT



6 CLK



7 VO



(Note 1) Resistance value is Typical.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed for in the thermal design. On the reverse side of the package this product has an exposed heat pad for improving the heat dissipation. Use both the front and reverse side of the PCB to increase the heat dissipation pattern as far as possible. The amount of heat generated depends on the voltage difference across the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating.
   Should by any condition the maximum junction temperature Tjmax = 150℃ rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

10. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

11. Regarding the Input Pin of the IC

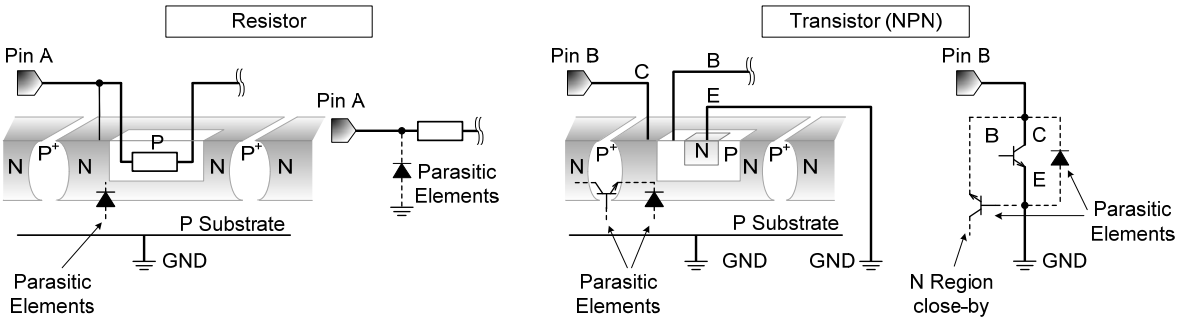
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, in case a resistor and a transistor are connected to the pins as shown in the figure below then:

○ The P/N junction functions as a parasitic diode when the GND > pin A for the resistor, or the GND > pin B for the transistor.

○ Also, when the GND > pin B for the transistor (NPN), the parasitic diode described above combines with the N layer of the other adjacent elements to operate as a parasitic NPN transistor.

Parasitic diodes inevitably occur in the structure of the IC. Their operation can result in mutual interference between circuits and can cause malfunctions and, in turn, physical damage to or destruction of the chip. Therefore do not employ any method in which parasitic diodes can operate such as applying a voltage to an input pin that is lower than the (P substrate) GND.



12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Thermal Shutdown Circuit (TSD)

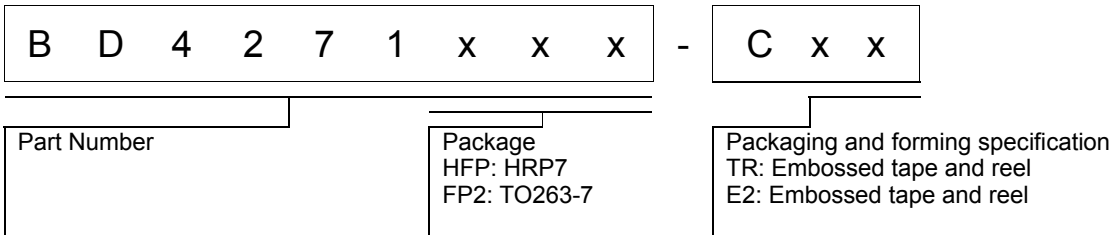
This IC incorporates and integrated thermal shutdown circuit to prevent heat damage to the IC. Normal operation should be within the power dissipation rating, if however the rating is exceeded for a continued period, the junction temperature (Tj) will rise and the TSD circuit will be activated and turn all output pins OFF. After the Tj falls below the TSD threshold the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

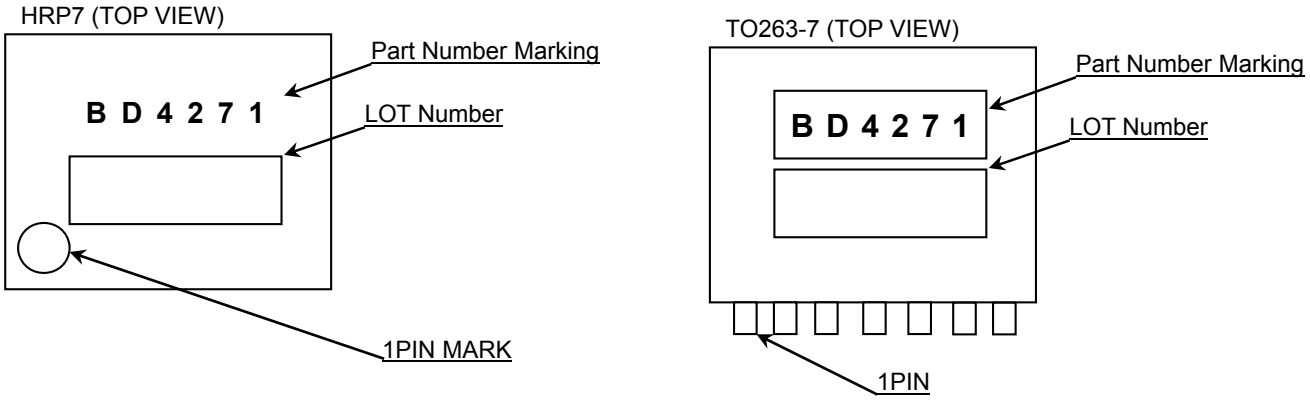
14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information



Marking Diagram



Part Number Marking	Package	Orderable Part Number
BD4271	HRP7	BD4271HFP-CTR
BD4271	TO263-7	BD4271FP2-CE2