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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Datasheet

Multi-Channel Power Supply LSI Series for Car Electronics

Multi-channel Power Supply IC for Car Audio Systems

BD49101ARFS-M

General Description

The BD49101ARFS-M LSI is a multi-channel power supply IC that can provide all necessary supply voltages for automobile audio systems. The IC has two Switching Power Supplies (DCDC), five Regulators (REG) and a High Side switch. This single power supply system can provide the required voltages to all systems including the MCU, CD, tuner, USB, illumination, audio circuits and others.

The IC system is based on switching regulator which has high efficiency then you can suppress heat of IC than before. And it has low power mode operation or voltage control function so that you can get ①High Efficiency ②Low IQ and ③easiness of power supply design.

Features

- AEC-Q100 Qualified(Note1)
- Integrated 7 channels of Power Supply for Car Audio
  - 2 DCDC (Integrated 1 Controller)
  - 5 REG
- 1 High Side Switch channel
- Integrated Low Power Standby REG for MCU Power Supply
- REG4 Cable Impedance Compensation
- I^2C Interface
- Selectable Oscillator Frequency using External Resistance
- External Clock Synchronization
- Power Supply Control Function (Power on/off Sequencer).
- Low Voltage, Over Voltage and REG4 Over Current Detect Flag
- Integrated Protection Circuitry:
  - Over Voltage Input Protection
  - Over Current Protection
  - Thermal Shutdown

(Note1:Grade3)

Applications

- Car Audio and Infotainment

Key Specifications

- Input Voltage Range: 5.5V to 25V(VIN0=BCAP)
- DCDC1(controller):
- DCDC2(with low power mode for MCU): 1A
- REG1(output voltage variable): 500mA
- REG2(output voltage variable): 100mA
- REG3(output voltage variable): 300mA
- REG4(output voltage variable for USB): 1.5A
- REG5(output voltage variable): 50mA
- High side SW: 500mA
- Standby Current: 100μA(Typ)
- REG4 Over Current Detect Accuracy: ±20%
- Operating Temperature Range: -40°C to +85°C
- DCDC Switching Frequency: 200kHz to 500kHz

Package	W(Typ) x D(Typ) x H(Max)
HTSSOP-A44R	18.50mm x 9.50mm x 1.00mm

HTSSOP-A44R

Pin Configuration

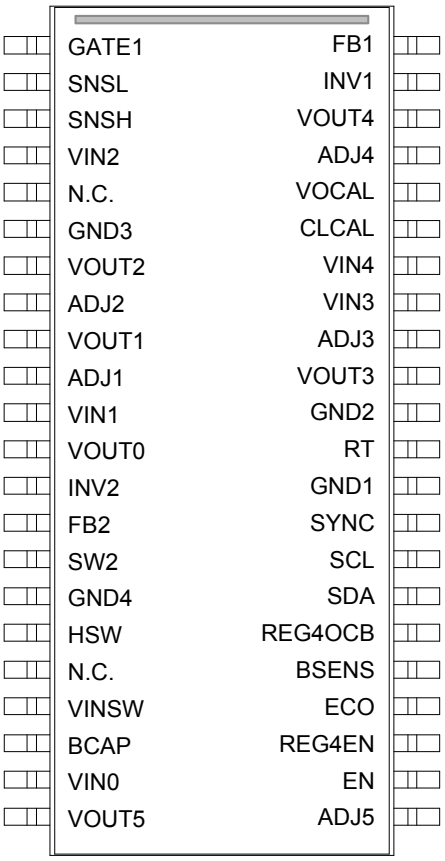

Figure 1. Pin Configuration(s)

Pin Description

Pin NO	Symbol	Function	Pin NO	Symbol	Function
1	GATE1	DCDC1 outside FET gate drive	23	ADJ5	REG5 output voltage adjustment
2	SNSL	DCDC1 current detection	24	EN	Enable
3	SNSH	DCDC1 current detection	25	REG4EN	REG4 Enable
4	VIN2	Power supply for built-in FET REG2	26	ECO	Low power mode switch
5	N.C.	—	27	BSENS	Error flag output
6	GND3	Ground	28	REG4OCB	Error flag output
7	VOUT2	REG2 voltage output	29	SDA	I^2C-bus data input
8	ADJ2	REG2 output voltage adjustment	30	SCL	I^2C-bus clock input
9	VOUT1	REG1 voltage output	31	SYNC	External synchronization signal input
10	ADJ1	REG1 output voltage adjustment	32	GND1	Ground
11	VIN1	Power supply for built-in FET REG1	33	RT	Oscillator frequency setting
12	VOUT0	STBREG voltage output	34	GND2	Ground
13	INV2	DCDC2 Error Amp Input	35	VOUT3	REG3 voltage output
14	FB2	DCDC2 Error Amp output	36	ADJ3	REG3output voltage adjustment
15	SW2	DCDC2 switching output	37	VIN3	Power supply for built-in FET REG3
16	GND4	Ground	38	VIN4	Power supply for built-in FET REG4
17	HSW	High side switch output	39	CLCAL	REG4 over current protection setting
18	N.C.	—	40	VOCAL	REG4 output USB cable impedance calibration setting
19	VINSW	Power supply for high side switch	41	ADJ4	REG4 output voltage adjustment
20	BCAP	Back-up capacity connection pin	42	VOUT4	REG4 voltage output
21	VIN0	Battery power supply connection pin	43	INV1	DCDC1 Error Amp Input
22	VOUT5	REG5 voltage output	44	FB1	DCDC1 Error Amp output

"N.C" pins are not connected into internal circuits.

Block Diagram

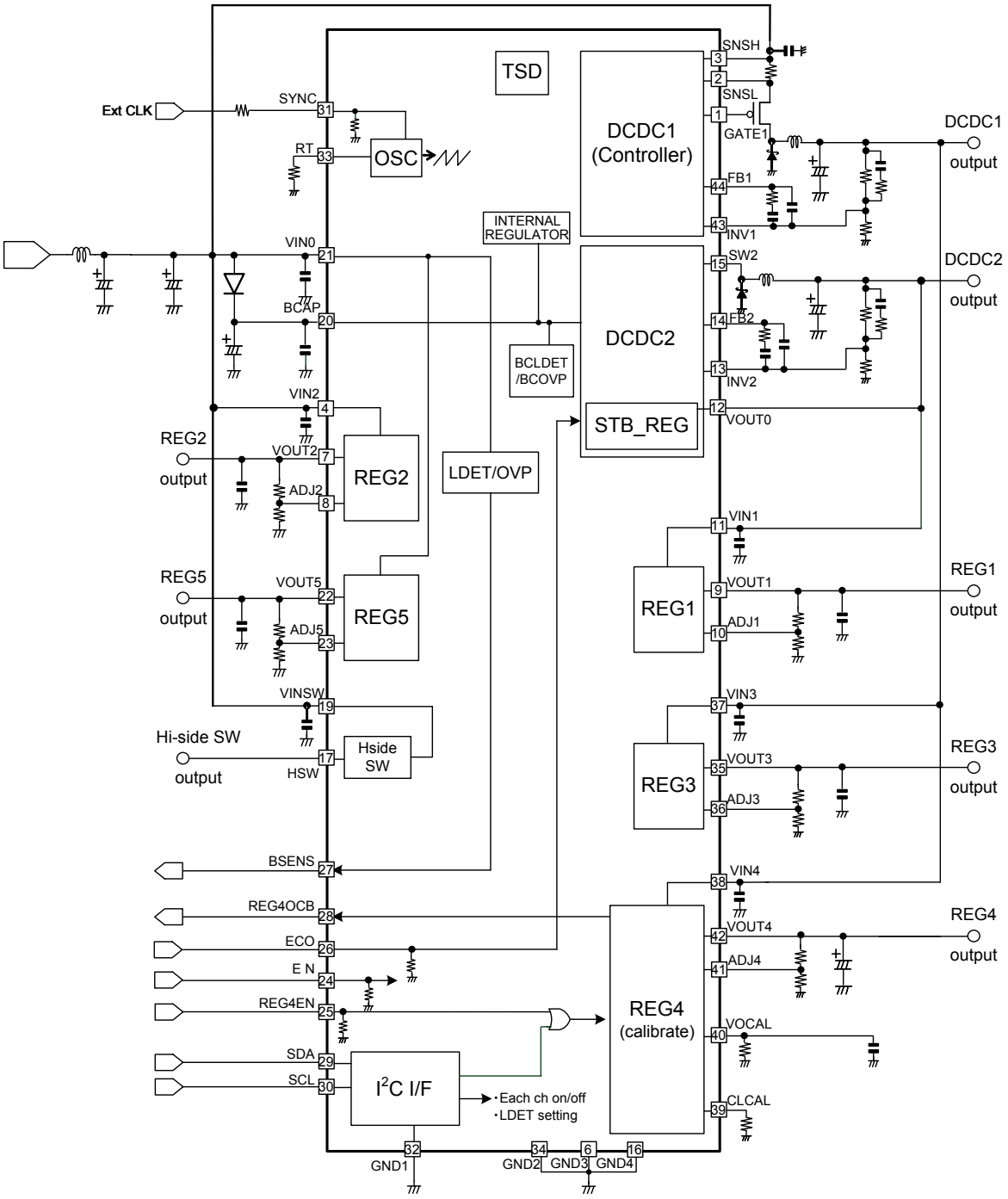

Figure 2. Block Diagram

Description of Blocks

・DCDC2 – STBREG Switch Function

The ECO input is used to switch between operating mode and low power standby mode.
(This function is for a 3.3V I/O microcomputer because of the 3.3V fixed STBREG output)
The function of the ECO input is as follows:

- ECO = H – Normal Operating Mode (DCDC2 operating).
- ECO = L – Low Power Standby Mode (STBREG operating).

・Sequence of VIN0 start up, Low Power Standby mode

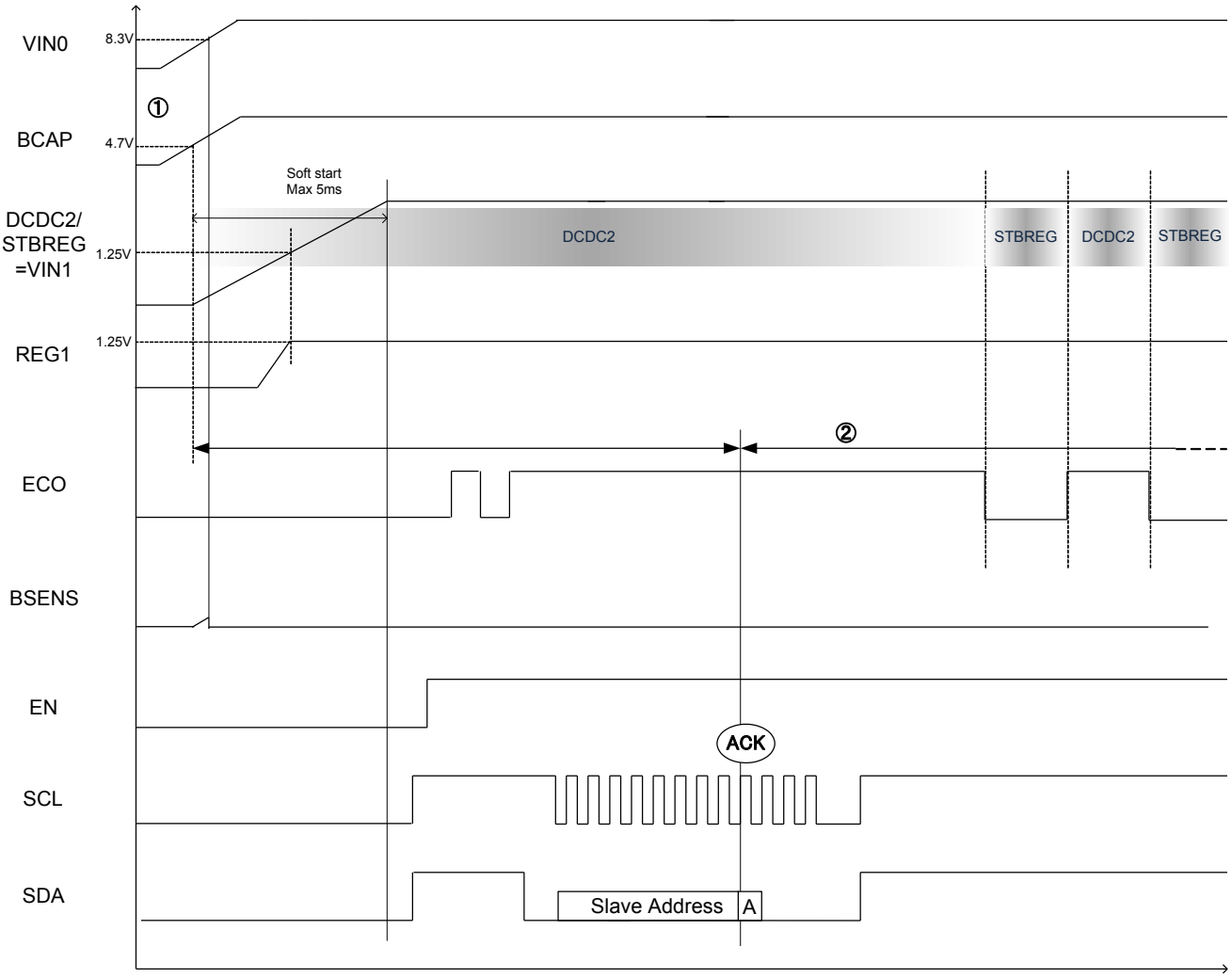

Figure 3. Timing Chart of VIN0 start up, Low Power Standby Mode

① When BD49101ARFS starts up, it starts in the normal operation mode (DCDC2 operation), independent of ECO setting. An internal regulator, the reference voltage circuit, and the OSC circuit start up when the voltage of the BCAP pin exceeds low voltage protection release voltage (4.7V).

② Following the first access to the I^2C interface, the ECO input is able to control the operating mode (normal or low power standby). ECO must be set to the desired operating mode prior to accessing the I^2C interface for the first time.

③ The conditions of independent of ECO setting is shown below.

- Input power supply for VIN0 at the first time
- BCAP voltage becomes under 4.5V
- DCDC2 detects over current and DCDC2 restarts

At each condition ECO setting become effective after you send I^2C command and receive ACK.

・Relations of BCAP Voltage and Operating Mode

When the voltage of the BCAP pin decreases under BCAP low voltage detection voltage (4.5V), the registers are initialized and the ECO pin setting becomes invalid and forcibly changed to low power mode. Afterwards, when BCAP voltage increases over BCAP low detection release voltage (4.7V) without under POWER ON reset voltage (3.1V), the mode change to DCDC2 mode. (ECO pin setting is invalid.) If BCAP voltage increases with under POWER ON reset voltage, the operation is same as VIN0 start up.

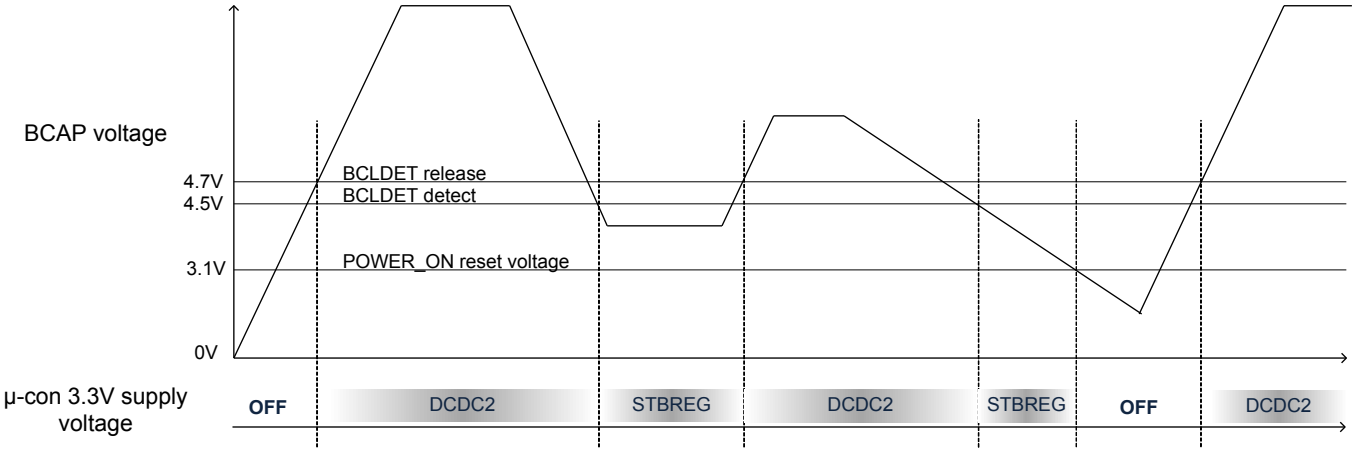

Figure 4. Relation of BCAP Voltage and Operating Mode

・Mode Changing (Normal Operation Mode ⇔ Low Power Mode)

When the ECO pin is changed from “L” to “H”, it changes from the low power mode to the normal operation mode. When it changes from the low power mode to the normal operation mode, the output voltage drops according to the load current. (Figure 5)
(ex.) ：Supply Voltage 14.4V, Output Capacitor 100μF, Load Current 200mA: Output Drop Voltage= -80mV(Typ)
We recommend that you save consumption current of the microcomputer in 200mA within 1ms when the mode is changed to normal operation mode (Figure 6).

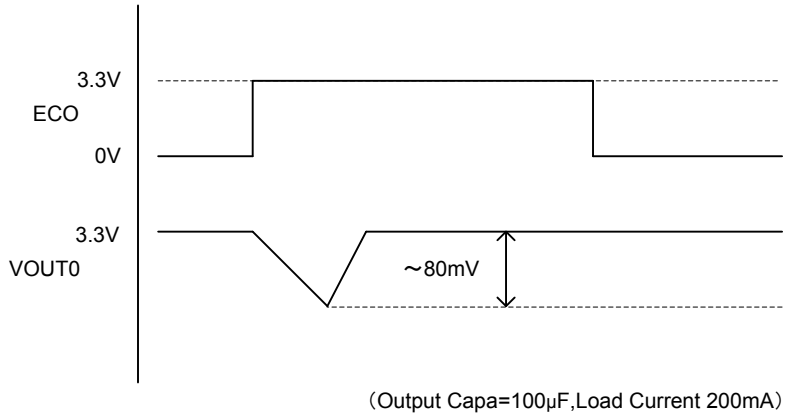

Figure 5. Timing Chart of Mode Changing (Normal Operation Mode ⇔ Low Power Mode)

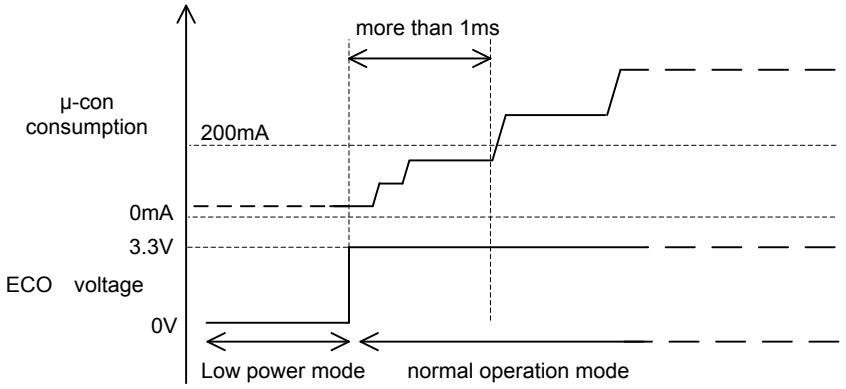

Figure 6. Image of Increasing Consumption Current when Switching from Low Power Mode to Normal Operation Mode

USB Supply Calibration (REG4).

The VOCAL input is used to adjust for cable impedance between the supply and USB connector. This adjustment will correct for voltage drop across the cable as a function of the current flow thus maintaining a constant voltage at the connector. Compensation of up to 0.5Ω of cable impedance can be achieved.
The CLCAL input is used to set the over current threshold, up to a maximum of 1.5A.Please refer 2-(3)-② Setting of cable impedance calibration

Over Current Protection (OCP)

All regulators and high side switch have over current protection. When OCP is detected, the following conditions will apply:

- DCDC1: After disabled for a certain period, it will attempt to restart automatically.
- DCDC2 : After disabled for a certain period, it will attempt to restart automatically and the register will be initialized.
- REG4 – Current limit circuit will operate and REG4OCB is activated (Low).
- Other regulators and a high side switch – Current limit circuit will operate.

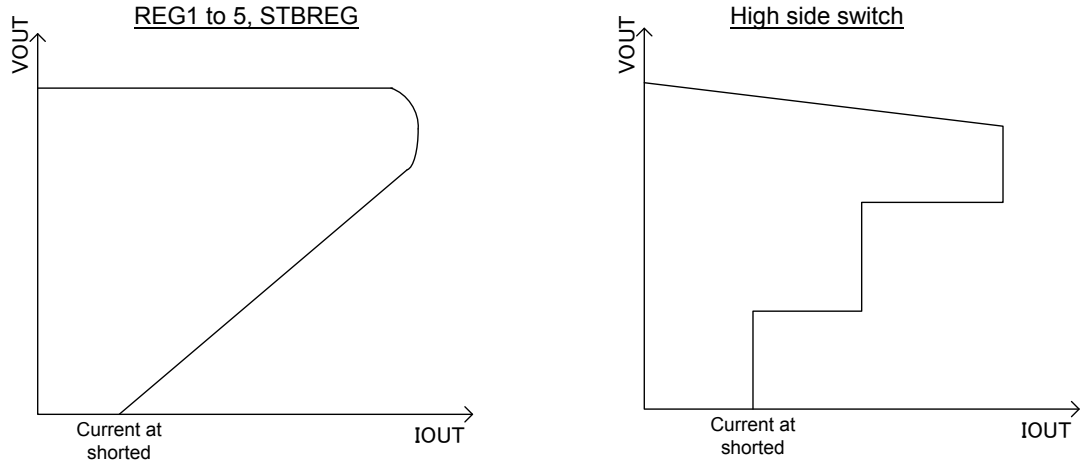

Figure 7. REG, High Side Switch Example of the Characteristics about Output Voltage vs Output Current

Battery Voltage Monitoring Function and BSENS Output

The BSENS output is active (High) when over voltage protection(OVP) is active. OVP becomes active when VIN0 exceeds 20.2V(Typ) OVP is cleared when VIN0 falls below 18.2V(Typ).
BSENS is also active (High) when VIN0 falls below 7.8V(Typ, initial register condition), afterwards BSENS is cleared when VIN0 exceeds 8.3V (Typ, initial register condition).
This low detection (LDET) voltage can change from 5.7V to 6.4V, and from 7.7V to 8.4V with writing register (Initial setting is 7.8V).

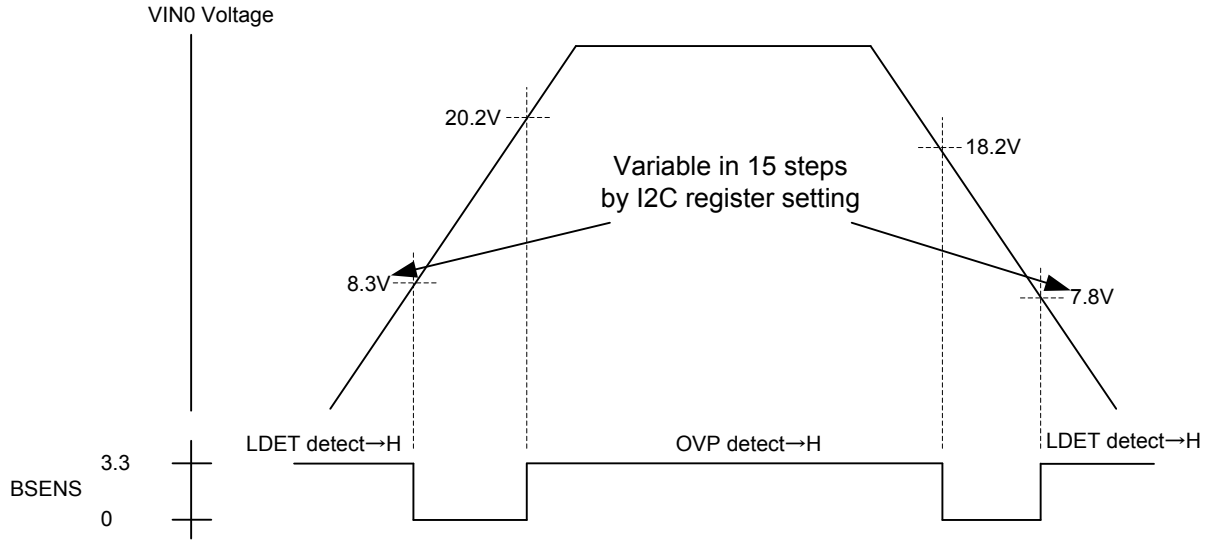

Figure 8. Timing Chart of OVP/LDET Detection

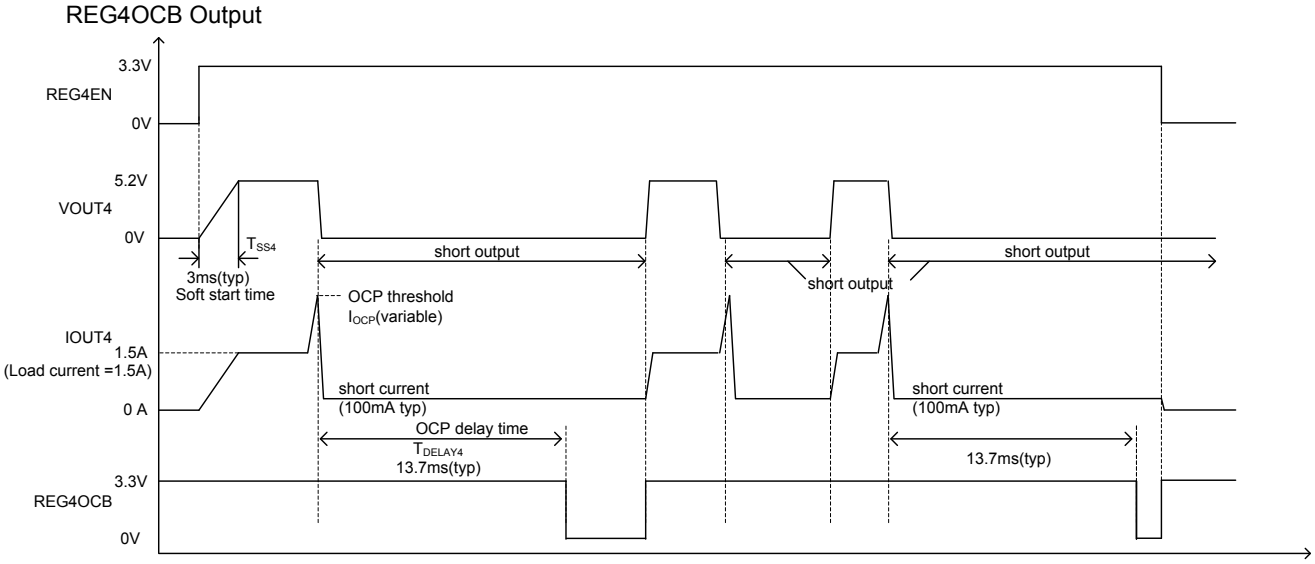

Figure 9. Timing Chart of REG4OCB Output

REG4 starts by a soft start in 3ms(Typ). And when detecting over current detection the REG4OCB output is active (Low) after 13.7ms continuous over current condition.

External Synchronization

The SYNC input is used to synchronize the switching frequency of DCDC1 and DCDC2. A signal in the range of 200kHz – 500kHz can be input. The input signal must be at a higher frequency than that set by the resistor on RT input and should be configured between 0.6 to 1.5 times the set frequencies.(when SYNC Duty=45 to 55%)

When it changes from internal oscillation mode to external synchronization mode, it changes after it is inputted continuously 3 pulses.

When it changes from external synchronization mode to internal oscillation mode, it changes within a period of internal oscillator frequency after SYNC input sets L. When SYNC input sets H, it doesn't change to internal oscillation mode. The high pulse within 50ns(like unexpected noise etc.) input could stop DCDC operation. In that case you can take measure by inserting damping resister etc. to reduce the pulse.

At first applying of power on VIN0(BCAP), SYNC pin must be under "input L level" max value until VODC2 rises up. If it is not so, the IC could not start normally.

It can adjust to the phase of switching pulse between DCDC1 and DCDC2 by the duty of SYNC input.

The switching positive edge timing of DCDC1,2 is below.

- DCDC1: synchronized the negative edge of SYNC input.
- DCDC2: synchronized the positive edge of SYNC input

The EN and the REG4EN pins

When the EN pin is set to H, I2C register setting is available, and when set to L, all register reset.
This function enable all REG and HSW channel expect DCDC2/STBREG and REG1 to OFF.
REG4EN is the enable pin of REG4 and can control REG4 through REG4_EN register or REG4EN.
When the EN pin is set to L, REG4 becomes OFF even if the REG4EN pin is set to H.

Input Pin	Output Conditions							Register
	STBREG	DCDC2	REG1	DCDC1	REG2,3,5	REG4	HSW	
EN	–	–	L=ON	L=OFF need resetting when turning ON				Reset (input"L")
REG4EN	–	–	–	–	–	L=OFF H=ON(Note 1)	–	–
ECO	L=STBREG H=DCDC2		–	–	–	–	–	–

(Note 1) When the EN pin input H.

Figure 10. Table of EN control

I^2C Interface

The I^2C interface allows access to the internal registers. The internal registers are used for the following functions:

- Enable the high side switch and power supplies except for DCDC2-STBREG.
- Setting LDET – VIN0 low voltage detection threshold.
- Detecting high side switch over current condition (address 0x04)

For Protect and Detect Functions and Enable Function

		Output Conditions							Error Flag		Register
		STBREG	DCDC2	REG1	DCDC1	REG2,3,5	REG4	HSW	BSENS	REG4OCB	
over current detection	STBREG	fold back limit	–	–	–	–	–	–	–	–	–
	DCDC2	–	restart (Note 1)	–	OFF(Note 2)				–	–	Reset
	REG1	–	–	fold back limit	–	–	–	–	–	–	–
	DCDC1	–	–	–	restart (Note 1)	–	–	–	–	–	–
	REG2,3,5	–	–	–	–	fold back limit	–	–	–	–	–
	REG4	–	–	–	–	–	fold back limit		–	○	–
	HSW	–	–	–	–	–	–	fold back limit	–	–	–
tharmal power supply voltage detection	TSD	–	–	–	OFF(Note 3)				–	–	–
	LDET	–	–	–	–	–	–	–	○	–	–
	OVP	–	–	–	–	–	–	–			
	BCLDET	ON (Note 4)	OFF (Note 4)	–	OFF(Note 2)				–	–	Reset
	BCOVP	–	–	–	OFF(Note 3)				–	–	–

(Note 1) When detecting each output is limited in minimum duty and dropping output and INV voltage then restarts after 1024clk.
(Note 2) When detecting each output doesn't restart.
(Note 3) When detecting each output restarts.
(Note 4) When detecting BCAP low voltage the operation mode switches to standby mode without depending on the ECO setting.

Figure 11. Table of EN Protect and Detect Functions

Absolute Maximum Ratings(Ta=25°C)

Parameter	Symbol	Limits	Unit
Power Supply Voltage (PIN4,19,20,21)	V_{CC}	-0.3 to +42	V
Input Voltage(PIN24,25,26,29,30,31)	Vin	-0.3 to +7	V
Pin Voltage 1(PIN1,7,15,17,22)	V_{PIN1}	-0.3 to +42	V
Pin Voltage 2(PIN2,3)	V_{PIN2}	VIN0 – 7 to VIN0	V
Pin Voltage 3(PIN8-14,23,27,28,33,35-44)	V_{PIN3}	-0.3 to +7	V
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Ratings

Parameter	Symbol	Limits	Unit
Operating Power Supply Voltage1(VIN0,BCAP)	V_{INopr}	5.5 to 25	V
Output Voltage Range 1(DCDC1/2)	$V_{OUTopr1}$	0.8 to V_{INopr}	V
Output Voltage Range 2(REG1/3/4)	$V_{OUTopr2}$	0.8 to 2.4 (REG1) 0.8 to VIN3,4 - $VSAT_{RG3,4}$ (REG3.4)	V
Output Voltage Range 3(REG2/5)	$V_{OUTopr3}$	0.8 to 10.5 (REG2) 0.8 to 8.5 (REG5)	V
DCDC Switching Frequency	f_{SW}	200 to 500	kHz
Oscillator Frequency Setting Resistance	R_T	27 to 82	kΩ
External Sync Frequency	f_{CLK}	200 to 500	kHz
External Synchronization Pulse Duty	D_{CLK}	20 to 80	%
REG4 Over Current Detection Set Resistance	R_{CLCAL}	5 to 50	kΩ
REG4 Cable Impedance Compensation Set Resistance	R_{VOCAL}	0 to 230	Ω

Electrical Characteristics

(Unless otherwise specified, Ta= 25°C, VIN0=BCAP=14.4V, EN=3.3V, VOUT1=1.25V, VOUT2=5.78V, VOUT3=3.3V, VOUT4=5.2V, VOUT5=5.0V)

Parameter	Symbol	Spec Values			Unit	Conditions
		Min	Typ	Max		
【Consumption Current】						
Standby Current	I_{STB}	—	100	150	μA	ECO=0V, EN=0V
Circuit Current	I_Q	—	5.0	7.5	mA	ECO=3.3V, EN=3.3V, Io=0A ENABLE=0x7F
【Over Voltage Detection】						
Detection Threshold Voltage	V_{OVPON}	18.2	20.2	22.2	V	
Release Threshold Voltage	V_{OVPOFF}	16.2	18.2	20.2	V	
【Low Voltage Detection】						
Detection Threshold Voltage	V_{LDETON}	7.5	7.8	8.1	V	LDET_SETTING=0x09
Release Threshold Voltage	$V_{LDETOFF}$	8.0	8.3	8.6	V	
【OSC】						
Oscillator Frequency	F_{OSC}	285	300	315	kHz	RT=51kΩ
【DCDC1】						
Reference Voltage	V_{REF1_DC1}	0.784	0.800	0.816	V	
Over Current Detection Threshold Voltage	$V_{OCP\_TH\_DC1}$	-	0.1	-	V	SNSH-SNSL
Maximum FB1 Voltage	V_{FB1H}	-	3.0	-	V	INV1=0V
Minimum FB1 Voltage	V_{FB1L}	-	0.8	-	V	INV1=2V
FB1 Sink Current	$I_{FB1SINK}$	-800	-400	-200	μA	FB1=1V, INV1=1V
FB1 Source Current	$I_{FB1SOURCE}$	50	100	200	μA	FB1=1V, INV1=0.6V
Maximum GATE1 Voltage	V_{GT1H}	-	-	VIN +0.3V	V	INV1=2V
Minimum GATE1 Voltage	V_{GT1L}	8.1	-	-	V	INV1=0V
Soft Start	TSS1	-	-	5	ms	
【DCDC2】						
Reference Voltage	V_{REF1_DC2}	0.784	0.800	0.816	V	
Output Current Capacity	IO_{DC2}	1	-	-	A	
Maximum FB2 Voltage	V_{FB2H}	-	3.0	-	V	INV2=0V
Minimum FB2 Voltage	V_{FB2L}	-	0.8	-	V	INV2=2V
FB2 Sink Current	$I_{FB2SINK}$	-800	-400	-200	μA	FB2=1V, INV2=1V
FB2 Source Current	$I_{FB2SOURCE}$	50	100	200	μA	FB2=1V, INV2=0.6V
Soft Start	TSS2	-	-	5	ms	
Power MOS FET ON Resistance	R_{ON}	125	250	500	mΩ	IO=800mA

Parameter	Symbol	Spec Values			Unit	Conditions
		Min	Typ	Max		
【STBREG】						
Reference Voltage	V_{REF_STLD}	3.234	3.300	3.366	V	
Load Current Capacity	IO_{STLD}	200	-	-	mA	
Line Regulation	ΔVI_{STLD}	-	-	15	mV	VIN0=7 to 18V, Io=5mA
Load Regulation	ΔVL_{STLD}	-	-	30	mV	IO=5m to 200mA
Ripple Rejection	RR_{STLD}	-	70	-	dB	Frp=100Hz, VIN0rp=1Vpp
I/O Voltage Difference	$VSAT_{STLD}$	-	-	0.6	V	IO=100mA
【REG1】						
Reference Voltage	V_{REF_LD1}	0.588	0.600	0.612	V	
Load Current Capacity	IO_{LD1}	500	-	-	mA	VIN1=3.3V
Line Regulation	ΔVI_{LD1}	-	-	10	mV	VIN1=3 to 6V, Io=5mA
Load Regulation	ΔVL_{LD1}	-	-	20	mV	IO=5m to 500mA
Ripple Rejection	RR_{LD1}	-	70	-	dB	Frp=100Hz, VIN1rp=1Vpp
I/O Voltage Difference	$VSAT_{LD1}$	-	-	1.0	V	IO=250mA
【REG2】						
Reference Voltage	V_{REF_LD2}	0.777	0.793	0.809	V	
Load Current Capacity	IO_{LD2}	100	-	-	mA	
Line Regulation	ΔVI_{LD2}	-	-	25	mV	VIN2=9 to 18V, Io=5mA
Load Regulation	ΔVL_{LD2}	-	-	50	mV	IO=5mA to 100mA
Ripple Rejection	RR_{LD2}	-	70	-	dB	Frp=100Hz, VIN2rp=1Vpp
I/O Voltage Difference	$VSAT_{LD2}$	-	-	0.65	V	IO=50mA
【REG3】						
Reference Voltage	V_{REF_LD3}	0.784	0.800	0.816	V	
Load Current Capacity	IO_{LD3}	300	-	-	mA	VIN3=6V
Line Regulation	ΔVI_{LD3}	-	-	20	mV	VIN3=4.0 to 6.5V, Io=5mA
Load Regulation	ΔVL_{LD3}	-	-	40	mV	IO=5m to 300mA
Ripple Rejection	RR_{LD3}	-	70	-	dB	Frp=100Hz, VIN3rp=1Vpp
I/O Voltage Difference	$VSAT_{LD3}$	-	-	0.6	V	IO=150mA

Parameter	Symbol	Spec Values			Unit	Conditions
		Min	Typ	Max		
【REG4】						
Reference Voltage	V_{REF_RG4}	0.784	0.800	0.816	V	
Load Current Capacity	IO_{RG4}	1.5	—	—	A	VIN4=6V,VOCAL=0Ω
Line Regulation	ΔVI_{RG4}	—	—	50	mV	VIN4=5.6 to 6.5V, Io=5mA
Load Regulation	ΔVL_{RG4}	—	—	40	mV	Io=5m to 1.5A
Ripple Rejection	RR_{RG4}	—	55	—	dB	Frp=100Hz, VIN4rp=1Vpp
I/O Voltage Difference	$VSAT_{RG4}$	—	—	0.4	V	Io=1.5A
Over Current Detection Threshold 1	I_{OCP1}	1.18	1.47	1.76	A	VIN4=6V, CLCAL= 6.8kΩ, VOCAL=0Ω
Over Current Detection Threshold 2	I_{OCP2}	534	667	800	mA	VIN4=6V, CLCAL= 15kΩ, VOCAL=0Ω
Voltage Adjusted For Cable Impedance(0.26Ω)	V_{cal}	5.32	5.46	5.60	V	VIN4=6.5V,Io=1.0A, VOCAL=120Ω
Soft Start Time	T_{SS4}	—	3	—	ms	
OCP Delay Time	T_{DELAY4}	8.7	13.7	18.7	ms	f_{sw} = 300kHz
【REG5】						
Reference Voltage	V_{REF_RG5}	0.784	0.800	0.816	V	
Load Current Capacity	IO_{RG5}	50	—	—	mA	
Line Regulation	ΔVI_{RG5}	—	—	25	mV	VIN0=9 to 18V, Io=5mA
Load Regulation	ΔVL_{RG5}	—	—	50	mV	Io=5mA to 50mA
Ripple Rejection	RR_{RG5}	—	70	—	dB	Frp=100Hz, VIN5rp=1Vpp
I/O Voltage Difference	$VSAT_{RG5}$	—	—	0.65	V	Io=25mA
【High Side SW】						
Output Current Capacity	IO_{SW1}	500	-	-	mA	
ON Resistance	R_{ON_SW1}	—	-	3	Ω	IO=500mA
【Digital IO】 (EN,REG4EN,ECO,SYNC,BSENS,REG4OCB)						
Input H level	V_{IH}	2.6	-	-	V	For pin EN, REG4EN, ECO,SYNC
Input L level	V_{IL}	-	-	0.8	V	For pin EN, REG4EN, ECO,SYNC
Input Pulldown Resistance1	R_{IND1}	—	100k	—	Ω	For pin REG4EN, ECO,SYNC
Input Pulldown Resistance2	R_{IND2}	—	660k	—	Ω	For pin EN
Output H level	V_{OH}	2.6	-	-	V	For pin BSENS,REG4OCB IO=1mA
Output L level	V_{OL}	-	-	0.8	V	For pin BSENS,REG4OCB IO= -1mA

Typical Performance Curves(reference)

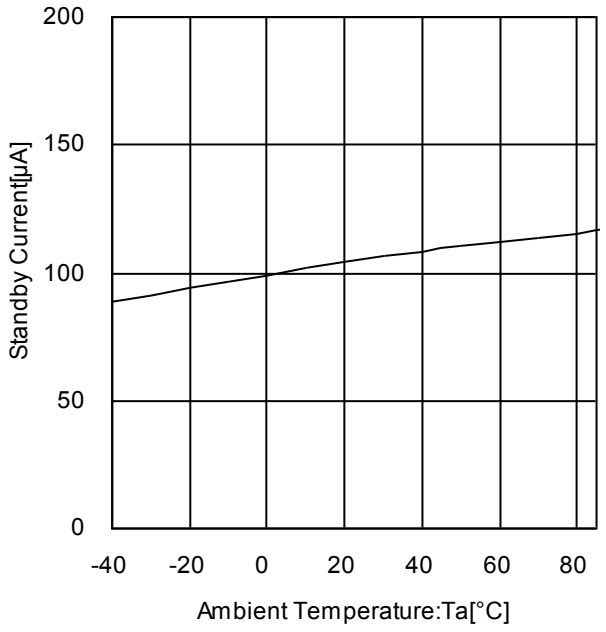

Figure 12. Standby Current vs Temperature

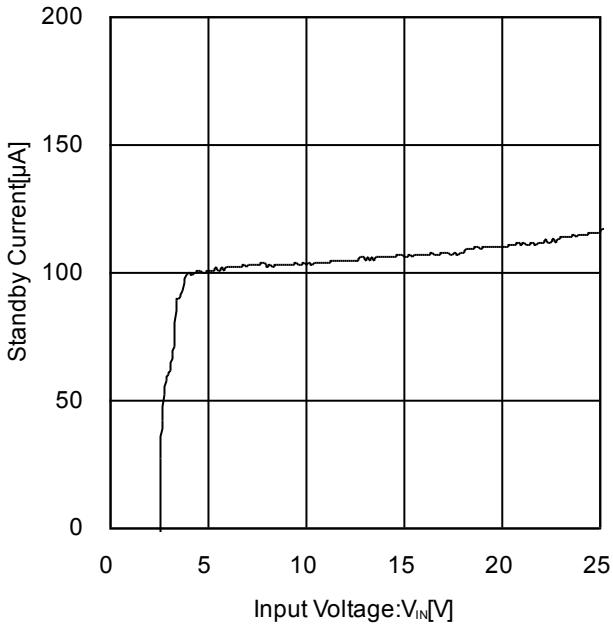

Figure 13. Standby Current vs Input Voltage

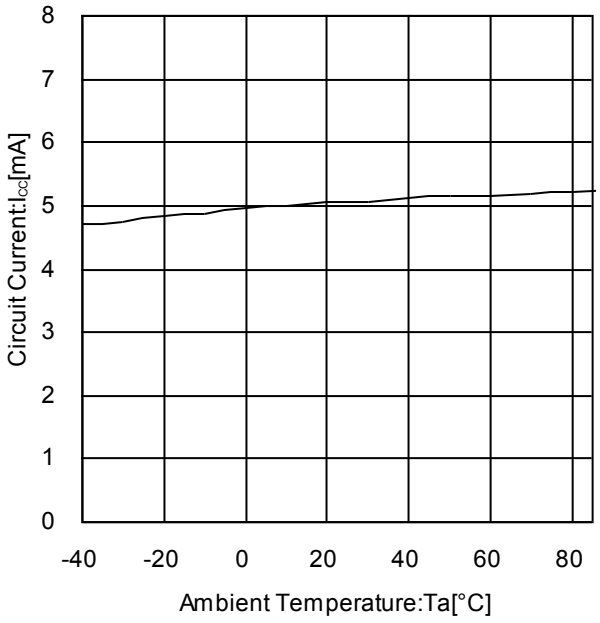

Figure 14. Circuit Current vs Temperature

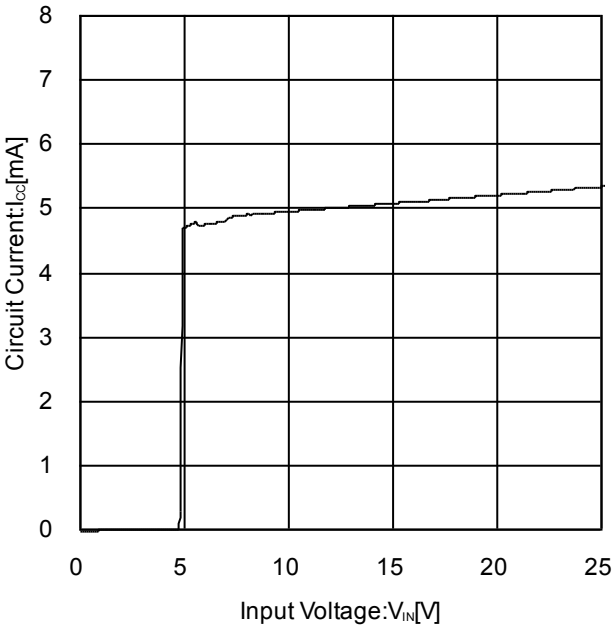

Figure 15. Circuit Current vs Input Voltage

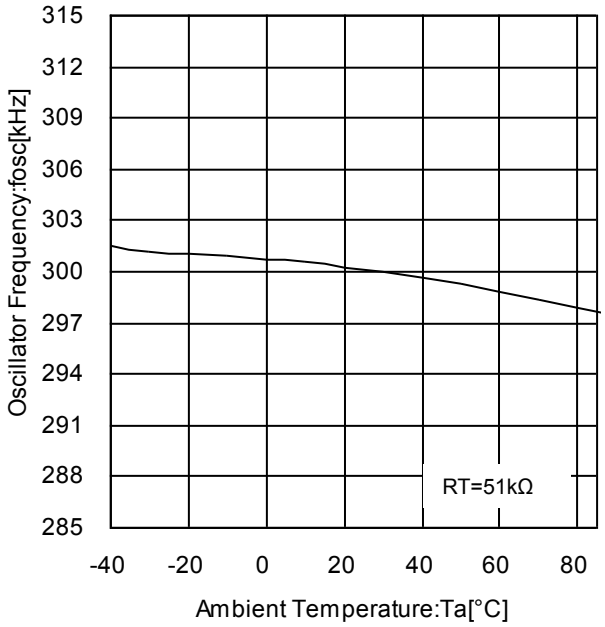

Figure 16. Oscillator Frequency vs Temperature

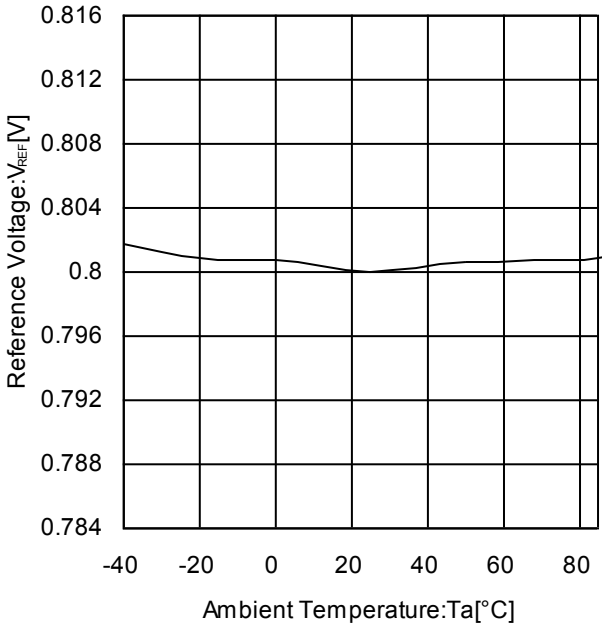

Figure 17. DCDC1 Reference Voltage vs Temperature

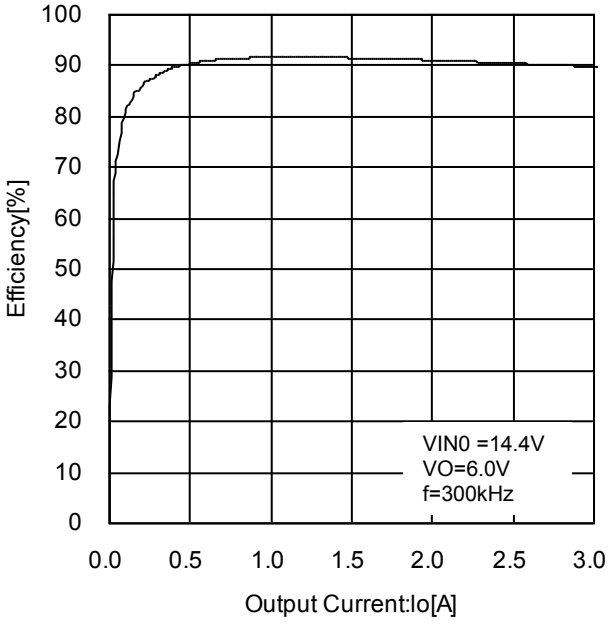

Figure 18. DCDC1 Efficiency vs Output Current

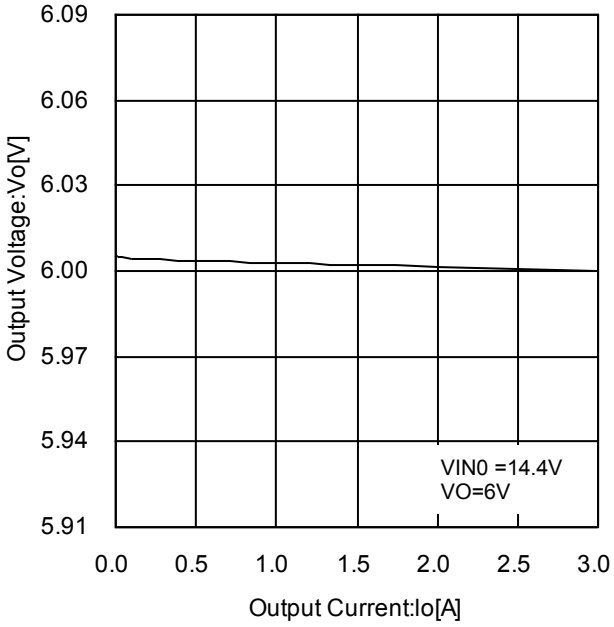

Figure 19. DCDC1 Output Voltage vs Output Current

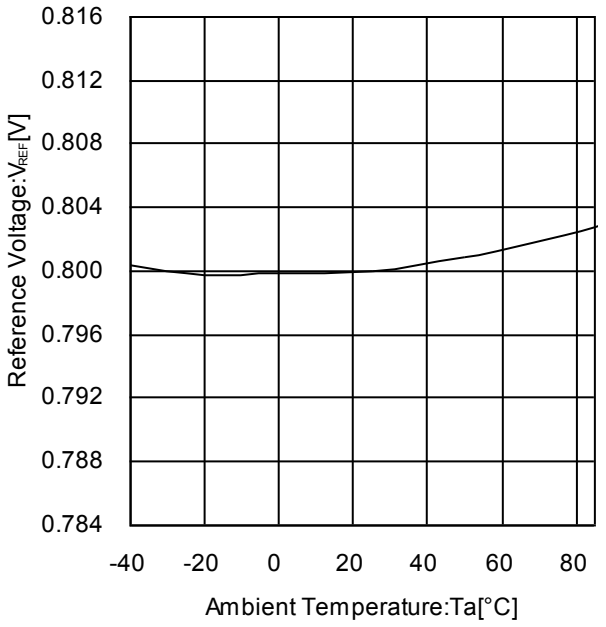

Figure 20. DCDC2 Reference Voltage vs Temperature

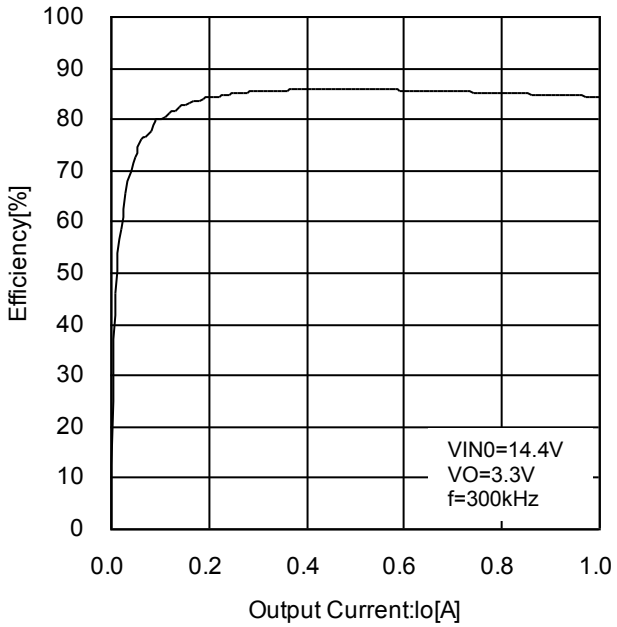

Figure 21. DCDC2 Conversion Efficiency vs Output Current

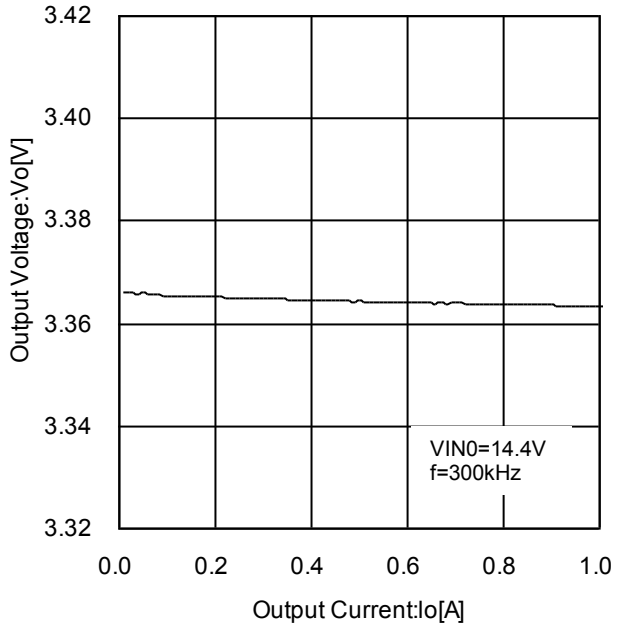

Figure 22. DCDC2 Output Voltage vs Output Current

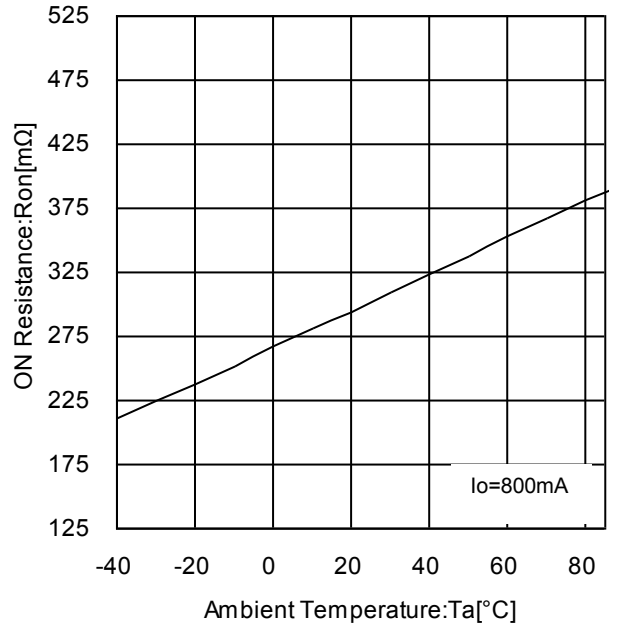

Figure 23. DCDC2 FET ON Resistance vs Temperature

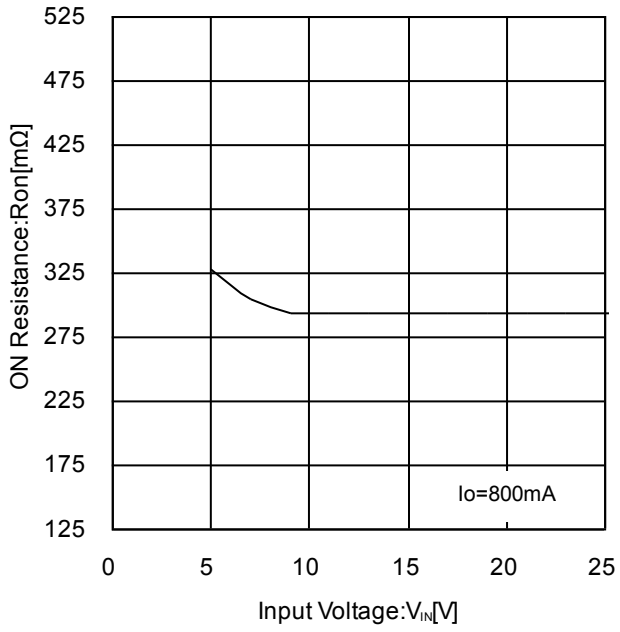

Figure 24. DCDC2 FET ON Resistance vs Input Voltage

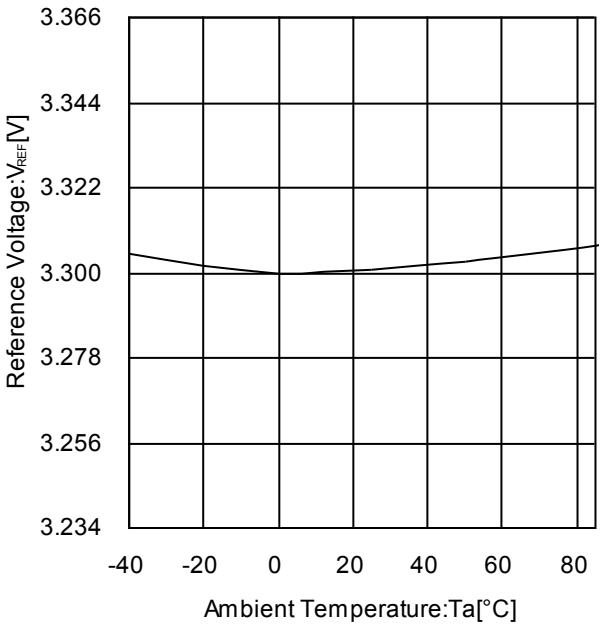

Figure 25. STBREG Reference Voltage vs Temperature

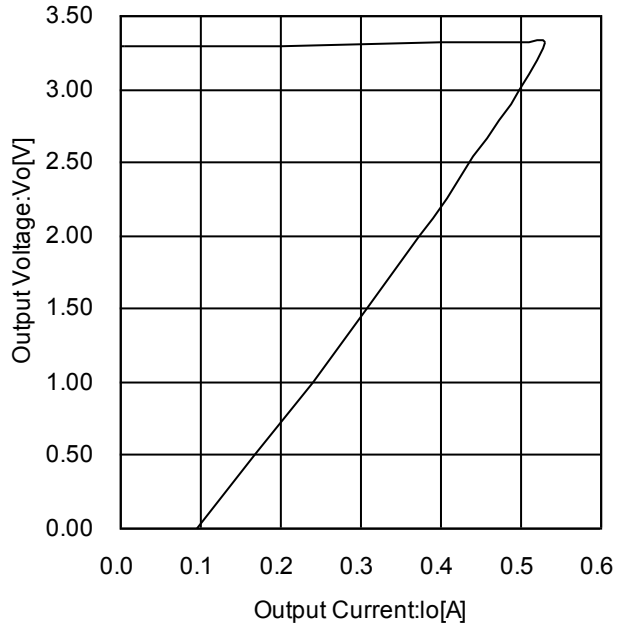

Figure 26. STBREG Output Voltage vs Output Current

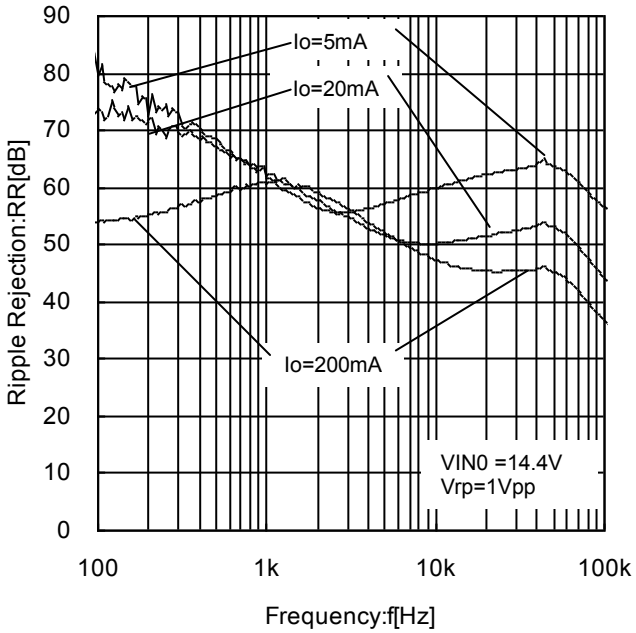

Figure 27. STBREG Ripple Rejection vs Frequency

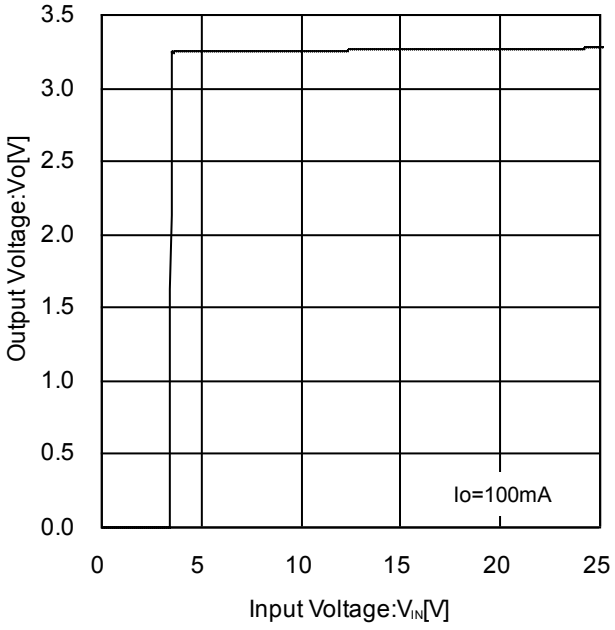

Figure 28. STBREG Output Voltage vs Input Voltage

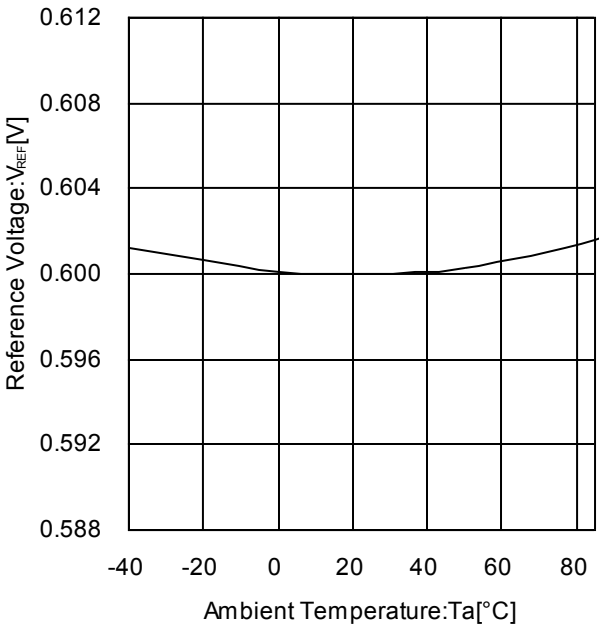

Figure 29. REG1 Reference Voltage vs Temperature

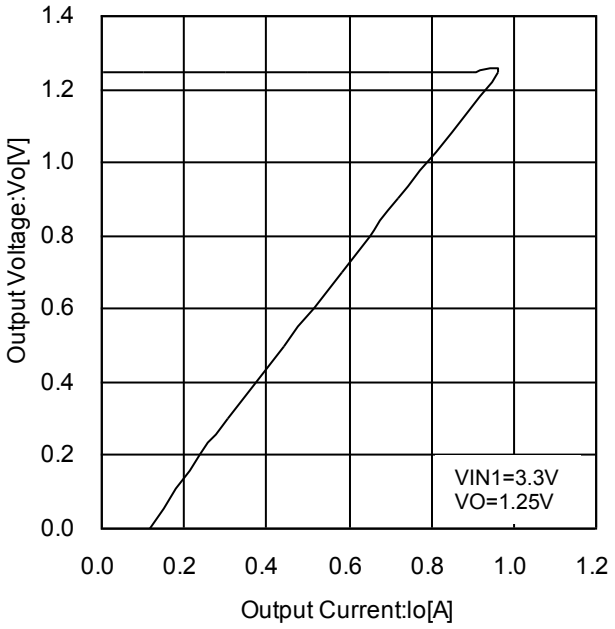

Figure 30. REG1 Output Voltage vs Output Current

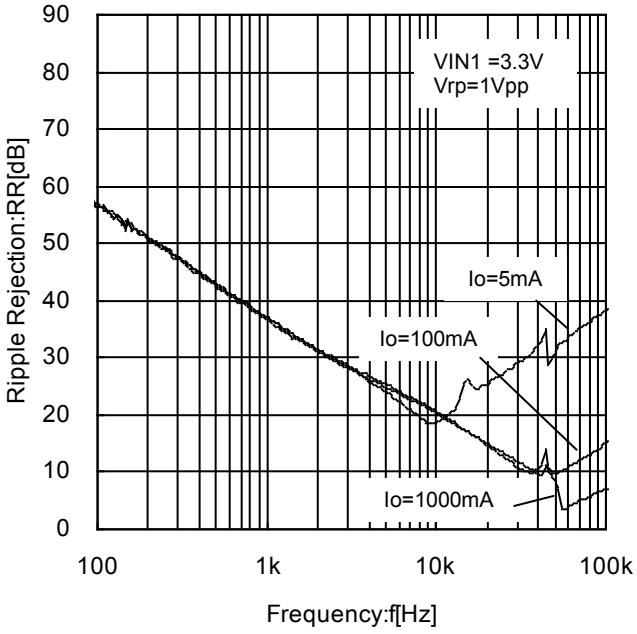

Figure 31. REG1 Ripple Rejection vs Frequency

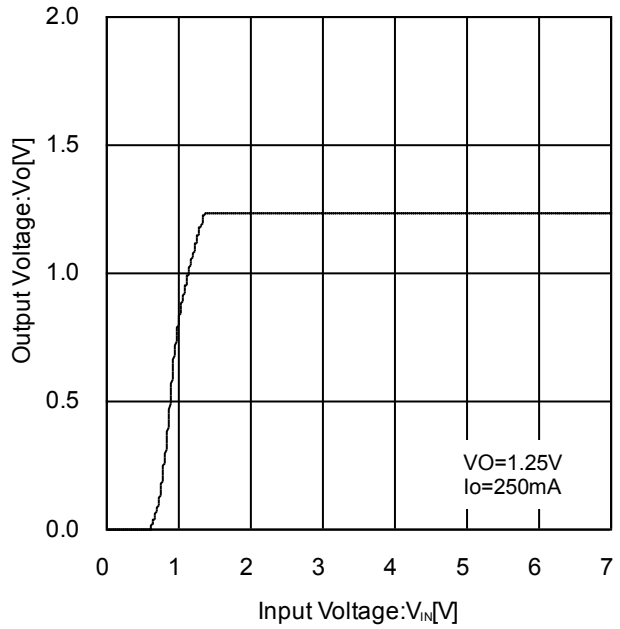

Figure 32. REG1 Output Voltage vs Input Voltage

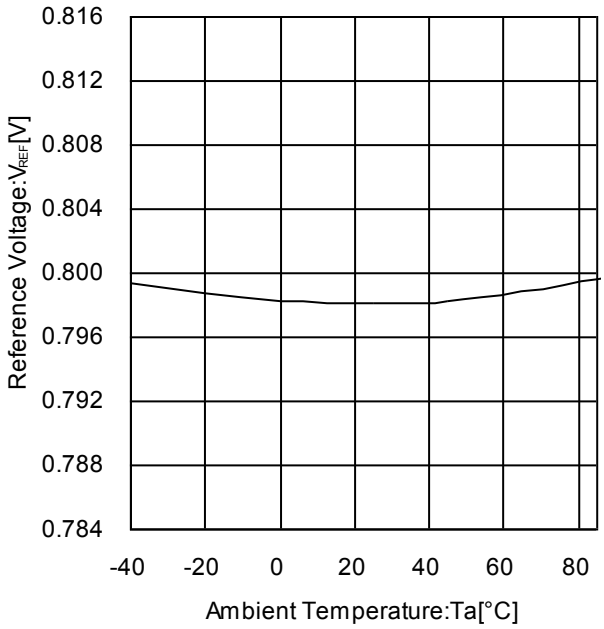

Figure 33. REG2 Reference Voltage vs Temperature

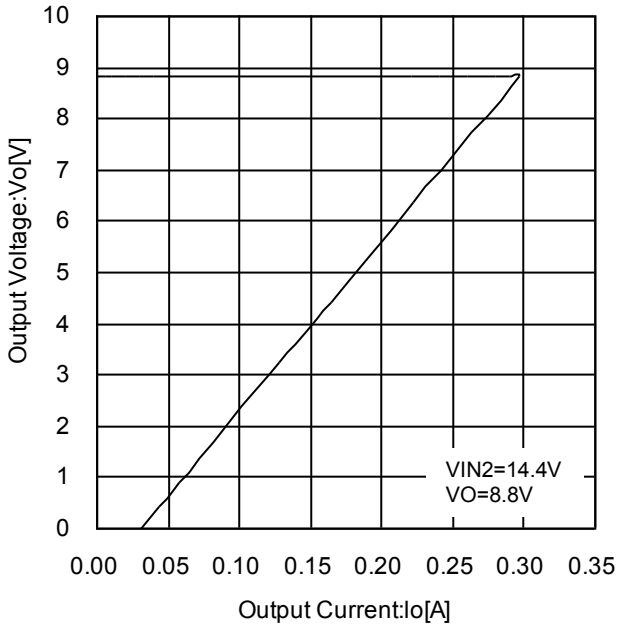

Figure 34. REG2 Output Voltage vs Output Current

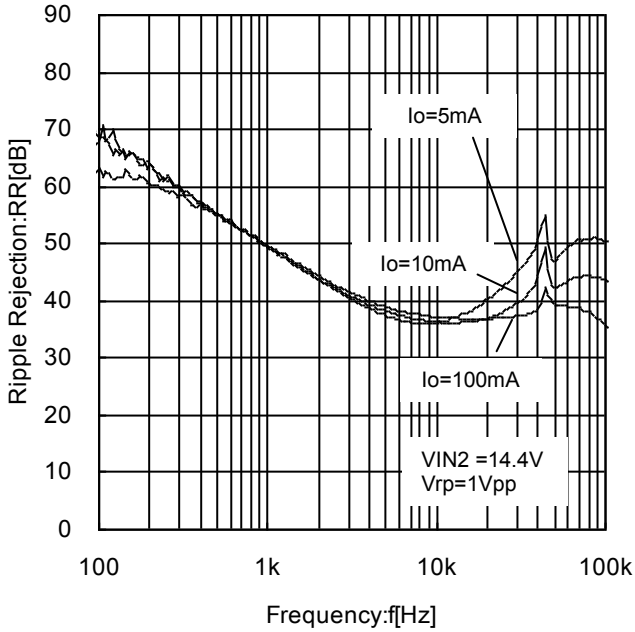

Figure 35. REG2 Ripple Rejection vs Frequency

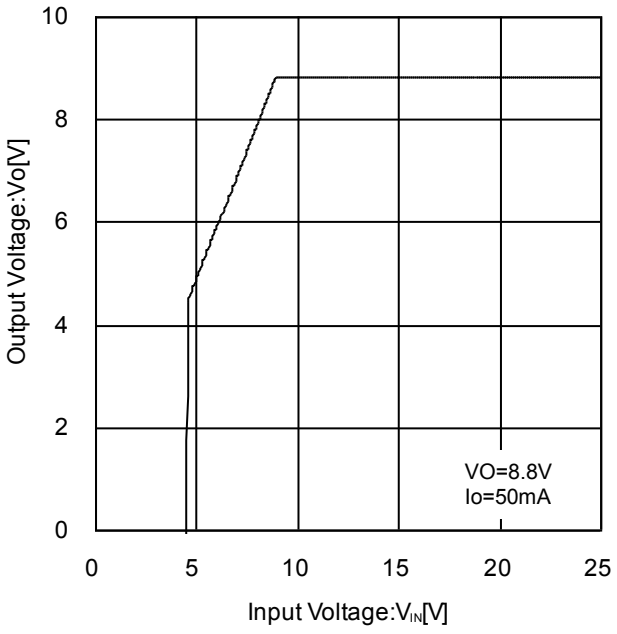

Figure 36. REG2 Output Voltage vs Input Voltage

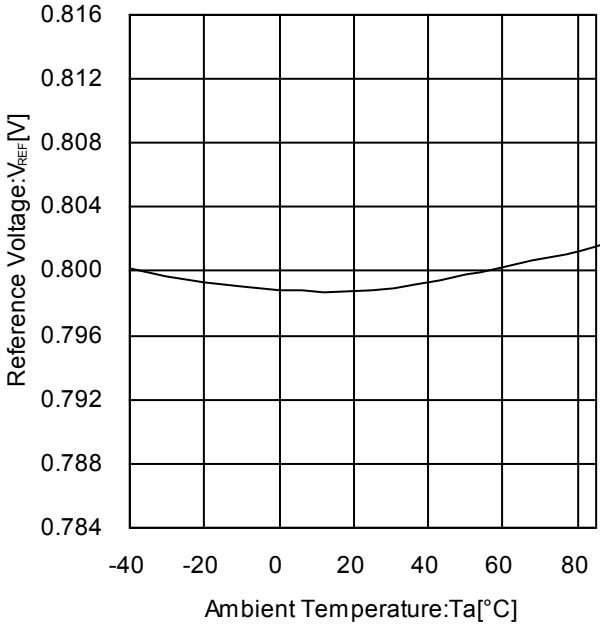

Figure 37. REG3 Reference Voltage vs Temperature

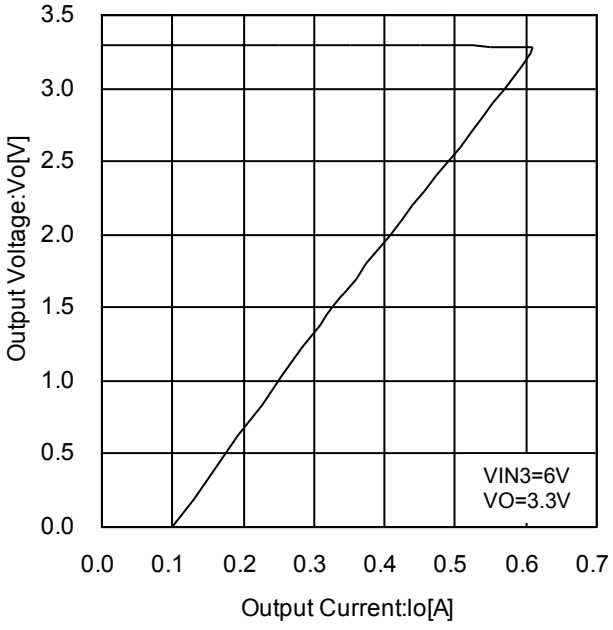

Figure 38. REG3 Output Voltage vs Output Current

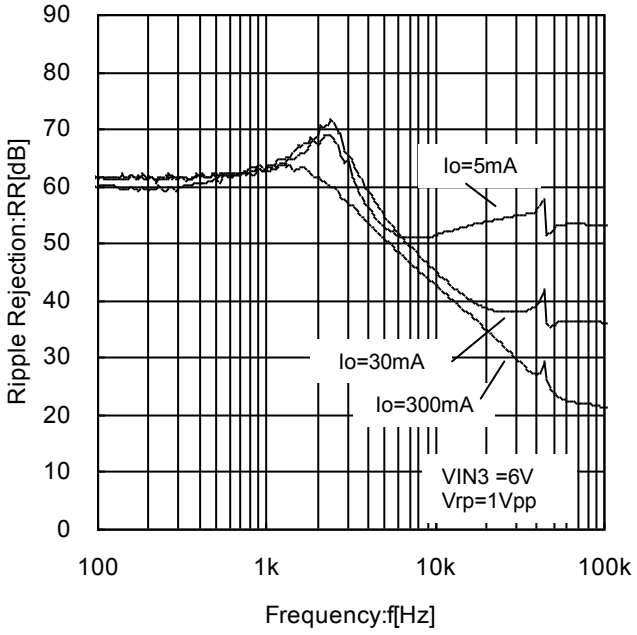

Figure 39. REG3 Ripple Rejection vs Frequency

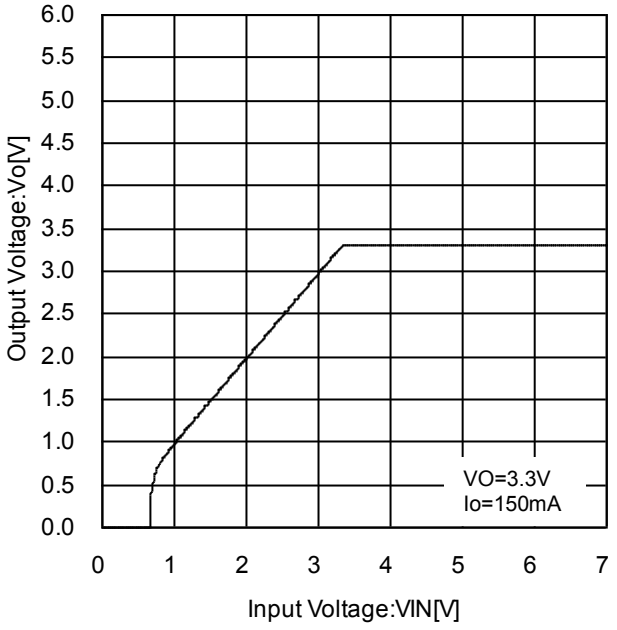

Figure 40. REG3 Output Voltage vs Input Voltage

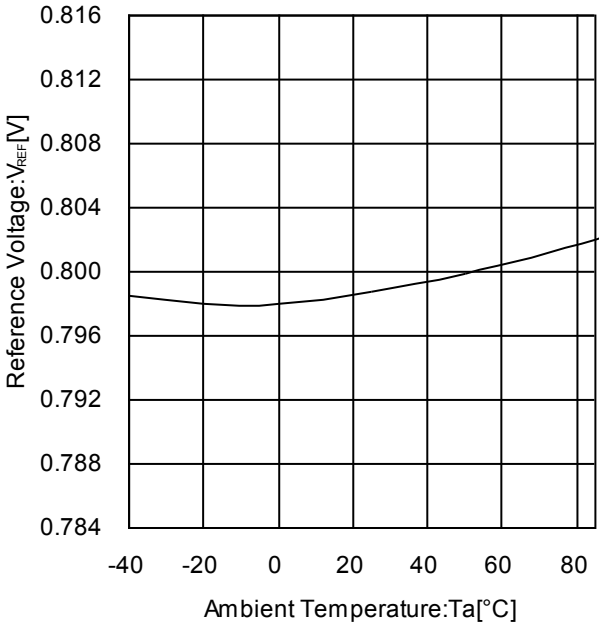

Figure 41. REG4 Reference Voltage vs Temperature

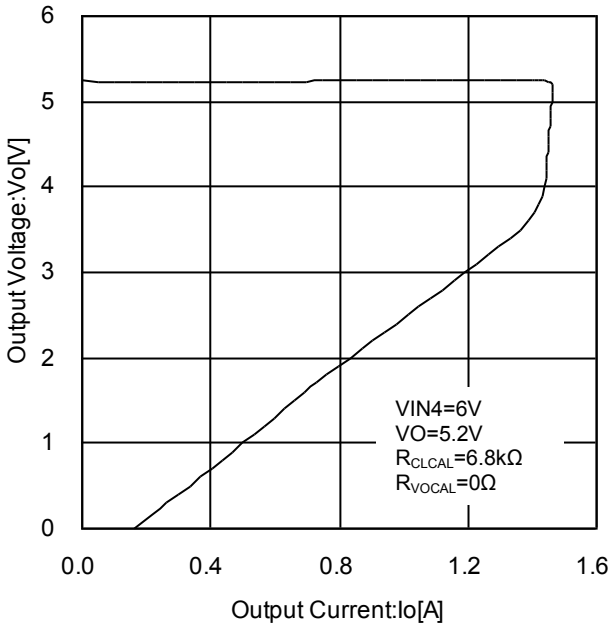

Figure 42. REG4 Output Voltage vs Output Current

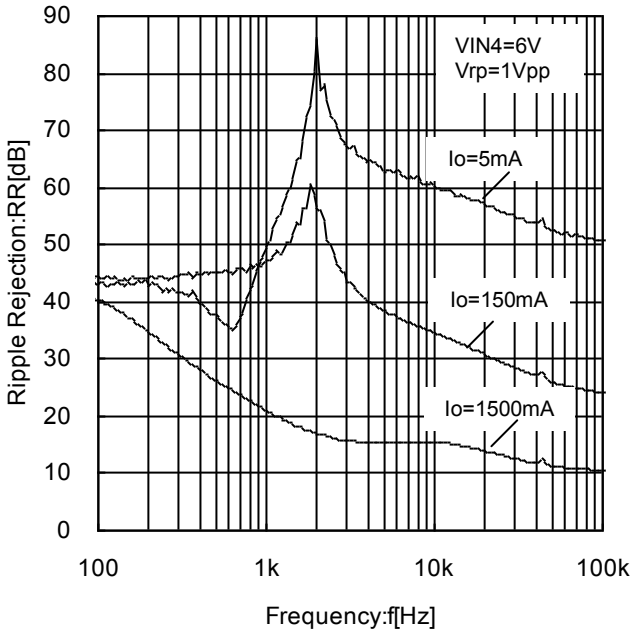

Figure 43. REG4 Ripple Rejection vs Frequency

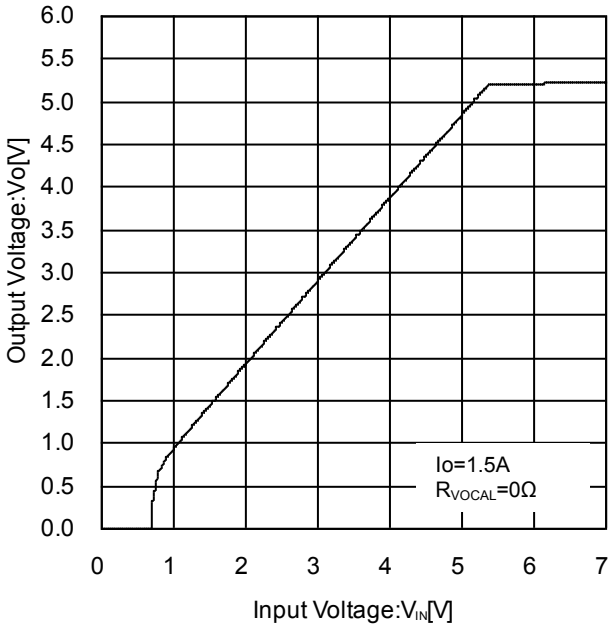

Figure 44. REG4 Output Voltage vs Input Voltage

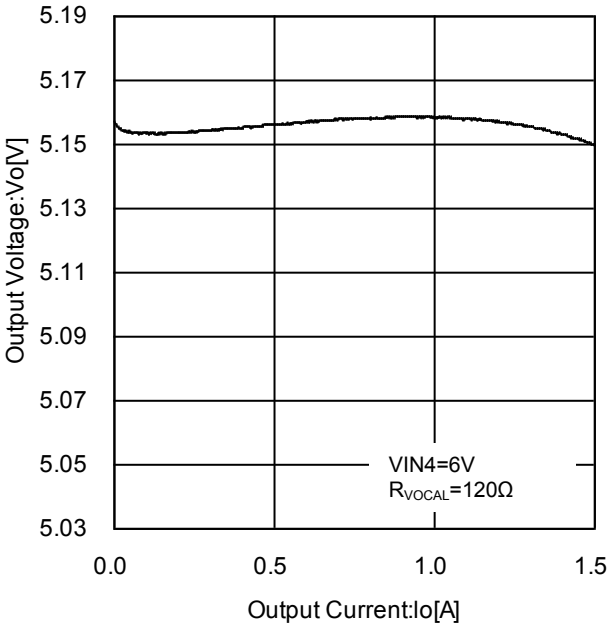

Figure 45. Voltage Adjusted for Cable Impedance vs Output Current

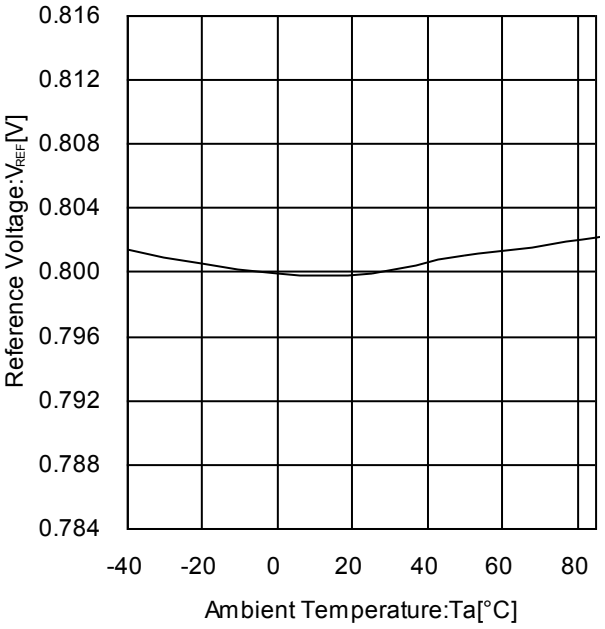

Figure 46. REG5 Reference Voltage vs Temperature

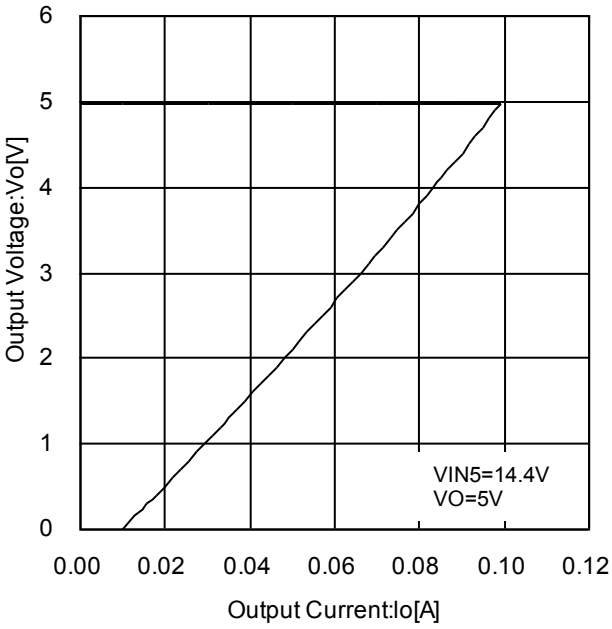

Figure 47. REG5 Output Voltage vs Output Current

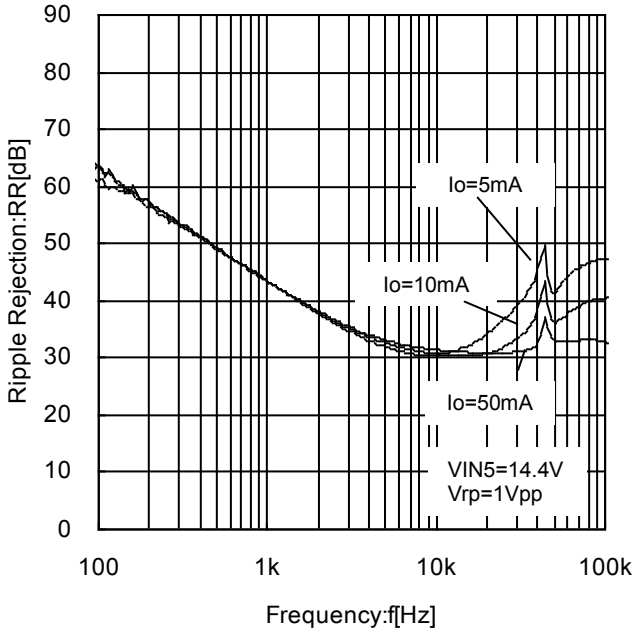

Figure 48. REG5 Ripple Rejection vs Frequency

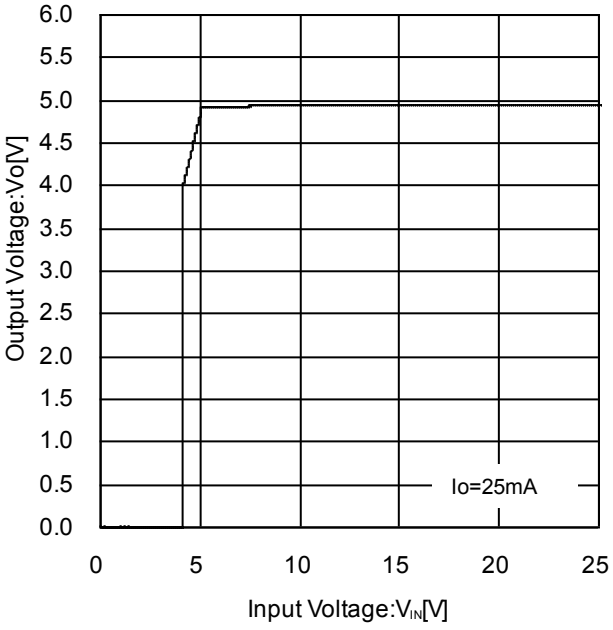

Figure 49. REG5 Output Voltage vs Input Voltage

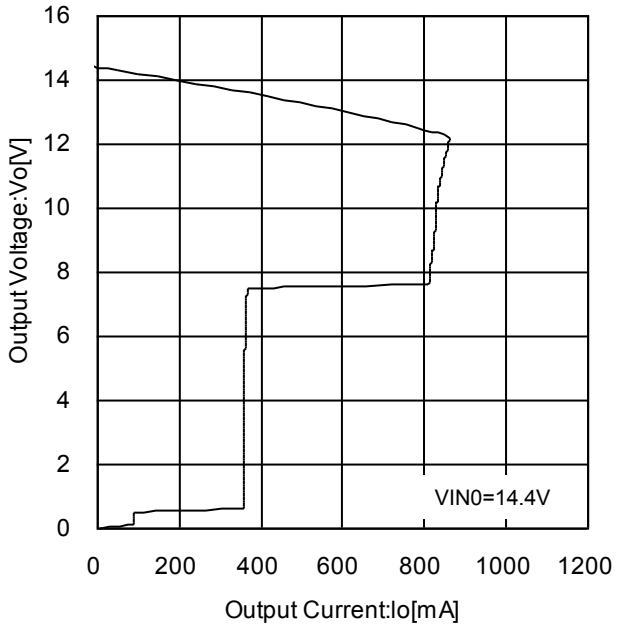

Figure 50. HSW Output Voltage vs Output Current

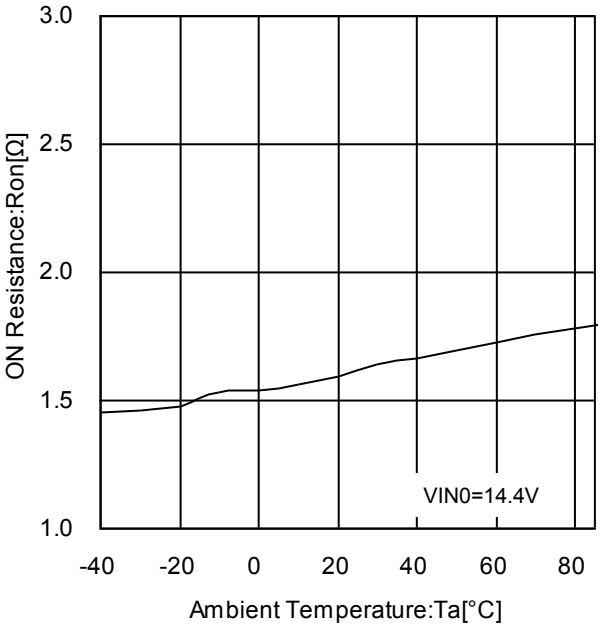

Figure 51. HSW ON Resistance vs Temperature

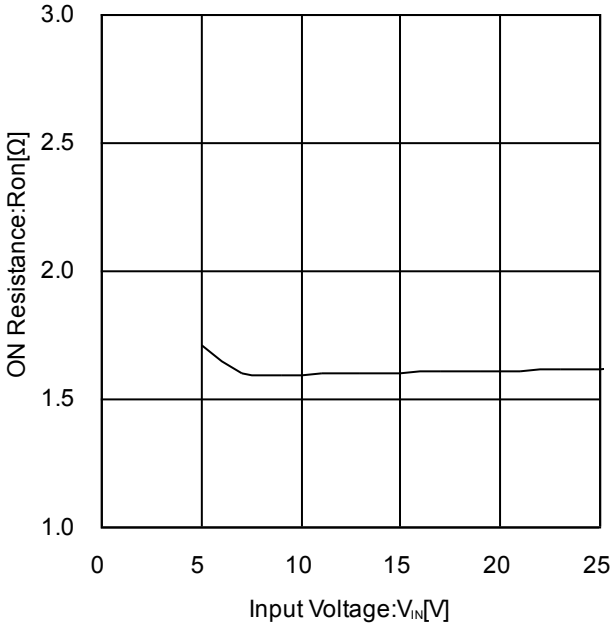

Figure 52. HSW ON Resistance vs Input Voltage

I²C-bus Block

(1) Electrical Specifications and Timing for Bus Lines and I/O Stages

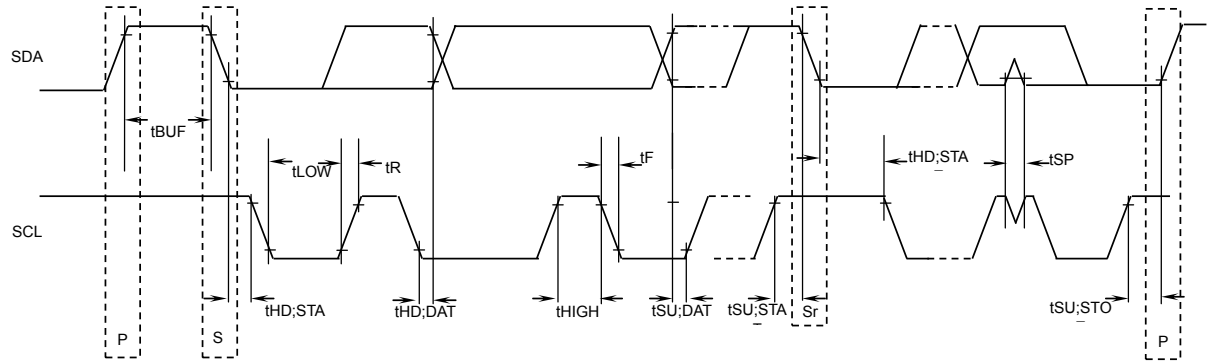

Figure 53. Definition of timing on the I²C-bus

Table 1. Characteristics of the SDA and SCL Bus Lines for I²C-bus Devices
(Unless specified particularly, Ta=25°C, VIN0=14.4V)

Parameter		Symbol	Fast-mode I²C-bus		Unit
			Min	Max	
1	SCL Clock Frequency	fSCL	0	400	kHz
2	Bus Free Time between a STOP and START Condition	tBUF	1.3	—	µs
3	Hold Time (repeated) Start Condition (After this period, the first clock pulse is generated.)	tHD;STA	0.6	—	µs
4	LOW Period of the SCL Clock	tLOW	1.3	—	µs
5	HIGH Period of the SCL Clock	tHIGH	0.6	—	µs
6	Set-up Time for a Repeated START Condition	tSU;STA	0.6	—	µs
7	Data Hold Time	tHD;DAT	0.06 (Note 1)	—	µs
8	Data Setup Time	tSU;DAT	120	—	ns
9	Setup Time for STOP Condition	tSU;STO	0.6	—	µs

All values referred to VIH min and VIL max levels (see Table 2).

(Note 1) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH min. of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
About 7(tHD;DAT), 8(tSU;DAT), make it the setup which a margin is fully in .

Table 2. Characteristics of the SDA and SCL I/O stages for I²C-bus Devices

Parameter		Symbol	Fast-mode devices		Unit
			Min	Max	
10	LOW Level Input Voltage:	VIL	-0.3	+1	V
11	HIGH Level Input Voltage:	VIH	2.3	5	V
12	Pulse Width of Spikes which must be suppressed by the input filter.	tSP	0	50	ns
13	LOW Level Output Voltage: at 3mA sink current	VOL1	0	0.4	V
14	Input Current each I/O pin with an input voltage between 0.4V and 4.5V.	Ii	-10	+10	µA

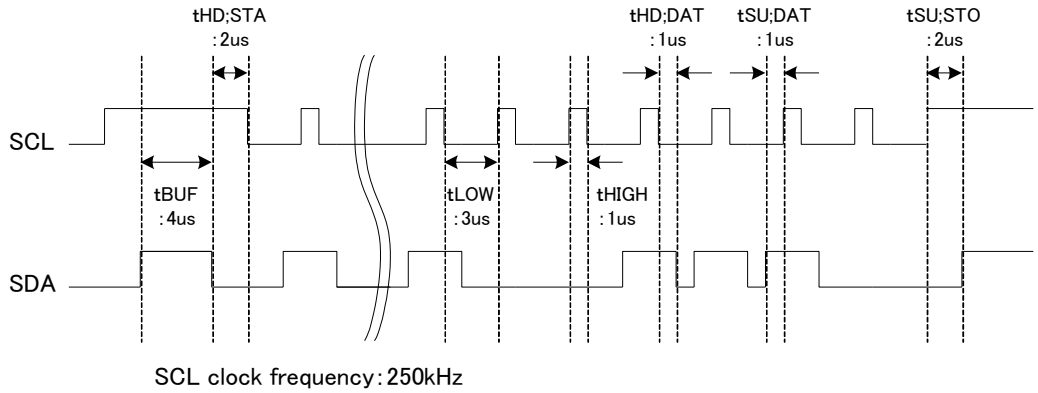

Figure 54. A Command Timing Example in the I²C Data Transmission

(2)I²C-bus Format

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S = Start Conditions (Recognition of Start Bit)
Slave Address = Recognition of Slave Address. 7 bits in upper order are voluntary. The least significant bit is “L” due to writing.
A = Acknowledge Bit (SDA “L”)
$\bar{A}$ = Not Acknowledge Bit (SDA “H”)
Select Address = Select ENABLE / LDET SETTING / HSW OCP.
Data = Data on ENABLE / LDET SETTING / HSW OCP
P = Stop Condition (Recognition of Stop Bit)

(3)I²C-bus Interface・Protocol

1)Write Mode Fundamental

S	Slave Address	A	Select Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

2)Auto Increment(The selection address does increment(+1) the number of data.)

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	・・・・	DataN	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB			MSB LSB		

(Example) ①Data 1 is set as data of the address specified in the selection address.
②Data 2 is set as data of the address specified in the selection address +1.
③Data N is set as data of the address specified in the selection address +N-1

3)Composition that cannot be transmitted(In this case, the selection address only 1 is set.)

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

(Attention) When you transmit data as selection address 2 next to data, it doesn't recognize as selection address 2, and it recognizes it as data.

4)Read Mode Protocol(Address 0x04 Read)

S	Slave Address	A	REQ Address	A	Select Address	A	P
	MSB 0xD8 LSB		MSB 0xD0 LSB		MSB 0x04 LSB		

S	Slave Address	A	※READ DATA	$\bar{A}$	P
	MSB 0xD9 LSB		MSB LSB		

Because read data outputs with synchronizing with falling edge of SCL, it latches with synchronizing with rising edge of SCL.

(4)Slave Address

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	1	0	0	1/0