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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Operational Amplifiers

Input/Output Full Swing Low Input Offset Voltage Operational Amplifier

BD5291xxx

General Description

The BD5291xxx is ideally suited for sensor signal conditioning. This features input/output full-swing operation with a supply voltage as low as 1.7V. In addition, high common-mode rejection ratio, ultra low input bias current (1pA typical) and low input offset voltage increase the precision that can be achieved using these operational amplifiers.

Features

- Low Operating Supply Voltage
- Input Output Full Swing
- Low Input Offset Voltage
- High Common Mode Rejection Ratio
- High Slew Rate

Applications

- Buffer
- Active Filter
- Sensor Amplifier
- Mobile Equipment

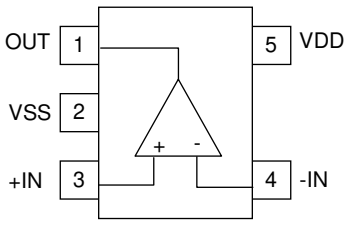
Key Specifications

- Operating Supply Voltage (Single Supply): +1.7V to +5.5V
- Slew Rate: 2.5V/µs(Typ.)
- Operating Temperature Range: -40°C to +85°C
- Input Voltage Range: VSS to VDD
- Input Offset Voltage: ±2.5mV (Max)
- Common Mode Rejection Ratio: 70dB (Min)

Package

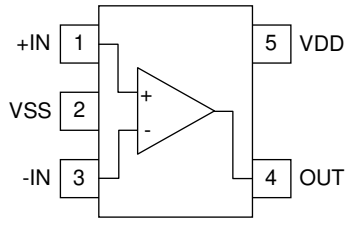
	W(Typ) x D(Typ) x H(Max)
SSOP5	2.90mm x 2.80mm x 1.25mm
VSOF5	1.60mm x 1.60mm x 0.60mm

Pin Configuration



Pin No.	Pin Name
1	OUT
2	VSS
3	+IN
4	-IN
5	VDD

BD5291FVE : VSOF5



Pin No.	Pin Name
1	+IN
2	VSS
3	-IN
4	OUT
5	VDD

Figure 1. Pin Configuration

Package	
SSOP5	VSOF5
BD5291G	BD5291FVE

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

Ordering Information

B D 5 2 9 1 x x x - T x

Part Number
BD5291G
BD5291FVE

Package
G :SSOP5
FVE :VSOF5

Packaging and forming specification
TL: Embossed tape and reel (SSOP5)
TR: Embossed tape and reel (VSOF5)

Line-up

Topr	Package		Operable Part Number
-40°C to +85°C	SSOP5	Reel of 3000	BD5291G-TL
	VSOF5	Reel of 3000	BD5291FVE-TR

Absolute Maximum Ratings(T_A=25°C)

Parameter	Symbol		Ratings	Unit
Supply voltage	VDD-VSS		+7	V
Power dissipation	P_D	SSOP5	0.67(Note 1,3)	W
		VSOF5	0.25(Note 2,3)	
Differential input voltage(Note 4)	V_{ID}		VDD - VSS	V
Input common-mode voltage range	V_{ICM}		(VSS – 0.3) to (VDD + 0.3)	V
Input current(Note 5)	I_I		±10	mA
Operating supply voltage	V_{opr}		+1.7 to +5.5	V
Operating temperature	T_{opr}		- 40 to +85	°C
Storage temperature	T_{stg}		- 55 to +150	°C
Maximum junction temperature	T_{Jmax}		+150	°C

(Note 1) To use at temperature above T_A=25°C reduce 5.4mW/°C.
(Note 2) To use at temperature above T_A=25°C reduce 2.0mW/°C.
(Note 3) Mounted on a FR4 glass epoxy PCB 70mm×70mm×1.6mm (Copper foil area less than 3%).
(Note 4) The voltage difference between inverting input and non-inverting input is the differential input voltage. Then input pin voltage is set to more than VSS.
(Note 5) An excessive input current will flow when input voltages of more than VDD+0.6V or less than VSS-0.6V are applied. The input current can be set to less than the rated current by adding a limiting resistor.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Electrical Characteristics

○BD5291G (Unless otherwise specified VDD=+3.3V, VSS=0V, T_A=25°C)

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			Min	Typ	Max		
Input offset voltage(Note 6,7)	V_{IO}	25°C	-	0.1	2.5	mV	VDD=+1.8V ,+3.3V
		Full range	-	-	3.8		
Input offset voltage drift(Note 6,7)	$\Delta V_{IO}/\Delta T$	Full range	-	0.8	-	μV/°C	-
Input offset current(Note 6,7)	I_{IO}	25°C	-	1	220	pA	-
		Full range	-	-	1700		
Input bias current(Note 6,7)	I_B	25°C	-	1	220	pA	-
		Full range	-	-	1700		
Supply current(Note 7)	I_{DD}	25°C	-	650	900	μA	RL=∞, Av=0dB, +IN=VDD/2
		Full range	-	-	970		
Maximum output voltage(High) (Note 7)	V_{OH}	25°C	VDD-0.1	-	-	V	RL=10kΩ
		Full range	VDD-0.1	-	-		
Maximum output voltage(Low) (Note 7)	V_{OL}	25°C	-	-	VSS+0.1	V	RL=10kΩ
		Full range	-	-	VSS+0.1		
Large signal voltage gain(Note 7)	A_V	25°C	80	105	-	dB	VDD=+1.8V
		Full range	80	-	-		
		25°C	80	110	-		VDD=+3.3V
		Full range	80	-	-		
Input common mode voltage	V_{ICM}	25°C	0	-	1.8	V	VDD=+1.8V, VSS to VDD
			0	-	3.3		VDD=+3.3V, VSS to VDD
Common mode rejection ratio(Note 7)	CMRR	25°C	70	90	-	dB	-
		Full range	68	-	-		
Power supply rejection ratio(Note 7)	PSRR	25°C	70	90	-	dB	-
		Full range	68	-	-		
Output source current(Note 8)	I_{source}	25°C	4	6	-	mA	OUT=VDD-0.4V
			-	17	-		output current
Output sink current (Note 8)	I_{sink}	25°C	9	15	-	mA	OUT=VSS+0.4V
			-	35	-		output current
Slew rate	SR	25°C	-	2.5	-	V/μs	CL=25pF
Gain bandwidth	GBW	25°C	-	3.0	-	MHz	VDD=+1.8V, f=100kHz, Open loop
			-	3.2	-	MHz	VDD=+3.3V, f=100kHz, Open loop
Phase margin	θ	25°C	-	40	-	deg	Open loop
Input referred noise voltage	Vn	25°C	-	18	-	nV/√Hz	Av=40dB, f=1kHz
Total harmonics distortion	THD+N	25°C	-	0.005	-	%	OUT=0.4V_{P-P}, f=1kHz

(Note 6) Absolute value
(Note 7) Full range: T_A=-40°C to +85°C
(Note 8) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

Electrical Characteristics - continued

○BD5291FVE (Unless otherwise specified VDD=+3.3V, VSS=0V, T_A=25°C)

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			Min	Typ	Max		
Input offset voltage(Note 9,10)	V_{IO}	25°C	-	0.1	2.5	mV	VDD=+1.8V ,+3.3V
		Full range	-	-	3.8		
Input offset voltage drift(Note 9,10)	$\Delta V_{IO}/\Delta T$	Full range	-	0.8	-	μV/°C	-
Input offset current(Note 9,10)	I_{IO}	25°C	-	1	220	pA	-
		Full range	-	-	1700		
Input bias current(Note 9,10)	I_B	25°C	-	1	220	pA	-
		Full range	-	-	2800		
Supply current(Note 10)	I_{DD}	25°C	-	650	900	μA	RL=∞, Av=0dB, +IN=VDD/2
		Full range	-	-	970		
Maximum output voltage(High) (Note 10)	V_{OH}	25°C	VDD-0.1	-	-	V	RL=10kΩ
		Full range	VDD-0.1	-	-		
Maximum output voltage(Low) (Note 10)	V_{OL}	25°C	-	-	VSS+0.1	V	RL=10kΩ
		Full range	-	-	VSS+0.1		
Large signal voltage gain (Note 10)	A_V	25°C	80	105	-	dB	VDD=+1.8V
		Full range	80	-	-		
		25°C	80	110	-		VDD=+3.3V
		Full range	80	-	-		
Input common mode voltage	V_{ICM}	25°C	0	-	1.8	V	VDD=+1.8V, VSS to VDD
			0	-	3.3		VDD=+3.3V, VSS to VDD
Common mode rejection ratio(Note 10)	CMRR	25°C	70	90	-	dB	-
		Full range	68	-	-		
Power supply rejection ratio(Note 10)	PSRR	25°C	70	90	-	dB	-
		Full range	68	-	-		
Output source current(Note 11)	I_{source}	25°C	4	6	-	mA	OUT=VDD-0.4V
			-	17	-		output current
Output sink current (Note 11)	I_{sink}	25°C	9	15	-	mA	OUT=VSS+0.4V
			-	35	-		output current
Slew rate	SR	25°C	-	2.5	-	V/μs	CL=25pF
Gain bandwidth	GBW	25°C	-	3.0	-	MHz	VDD=+1.8V, f=100kHz, Open loop
			-	3.2	-	MHz	VDD=+3.3V, f=100kHz, Open loop
Phase margin	θ	25°C	-	40	-	deg	Open loop
Input referred noise voltage	Vn	25°C	-	18	-	nV/√Hz	Av=40dB, f=1kHz
Total harmonics distortion	THD+N	25°C	-	0.005	-	%	OUT=0.4V_{P-P}, f=1kHz

(Note 9) Absolute value

(Note 10) Full range: T_A=-40°C to +85°C

(Note 11) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

Description of electrical characteristics

Described here are the terms of electric characteristics used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacture's document or general document.

1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

(1) Power supply voltage (VDD/VSS)
Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal without deterioration or destruction of characteristics of internal circuit.

(2) Differential input voltage (V_{ID})
Indicates the maximum voltage that can be applied between non-inverting terminal and inverting terminal without deterioration and destruction of characteristics of IC.

(3) Input common-mode voltage range (V_{ICM})
Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of characteristics. Input common-mode voltage range of the maximum ratings not assures normal operation of IC. When normal Operation of IC is desired, the input common-mode voltage of characteristics item must be followed.

(4) Power dissipation (P_D)
Indicates the power that can be consumed by specified mounted board at the ambient temperature 25°C(normal temperature). As for package product, Pd is determined by the temperature that can be permitted by IC chip in the package (maximum junction temperature) and thermal resistance of the package.

2.Electrical characteristics item

(1) Input offset voltage (V_{IO})
Indicates the voltage difference between non-inverting terminal and inverting terminal. It can be translated into the input voltage difference required for setting the output voltage at 0 V.

(2) Input offset voltage drift ($\triangle V_{IO}/\triangle T$)
Denotes the ratio of the input offset voltage fluctuation to the ambient temperature fluctuation.

(3) Input offset current (I_{IO})
Indicates the difference of input bias current between non-inverting terminal and inverting terminal.

(4) Input bias current (I_B)
Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.

(5) Supply current (IDD)
Indicates the IC current that flows under specified conditions and no-load steady status.

(6) Maximum Output Voltage(High) / Maximum Output Voltage(Low) (V_{OH}/V_{OL})
Indicates the voltage range that can be output by the IC under specified load condition. It is typically divided into maximum output voltage High and low. Maximum output voltage high indicates the upper limit of output voltage. Maximum output voltage low indicates the lower limit.

(7) Large signal voltage gain (Av)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
Av = (Output voltage) / (Differential Input voltage)

(8) Input common-mode voltage range (V_{ICM})
Indicates the input voltage range where IC operates normally.

(9) Common-mode rejection ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.
CMRR = (Change of Input common-mode voltage)/(Input offset voltage fluctuation)

(10) Power supply rejection ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC. PSRR= (Change of power supply voltage)/(Input offset voltage fluctuation)

(11) Output source current/ output sink current (I_{source} / I_{sink})
The maximum current that can be output under specific output conditions, it is divided into output source current and output sink current. The output source current indicates the current flowing out of the IC, and the output sink current the current flowing into the IC.

(12) Slew Rate (SR)
SR is a parameter that shows movement speed of operational amplifier. It indicates rate of variable output voltage as unit time.

(13) Gain Bandwidth (GBW)
Indicates to multiply by the frequency and the gain where the voltage gain decreases 6dB/octave.

Description of electrical characteristics – continued

(14) Phase Margin (θ)
Indicates the margin of phase from 180 degree phase lag at unity gain frequency.
(15) Input referred noise voltage (Vn)
Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.
(16) Total harmonic distortion + Noise (THD+N)
Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

Typical Performance Curves

OBD5291xxx

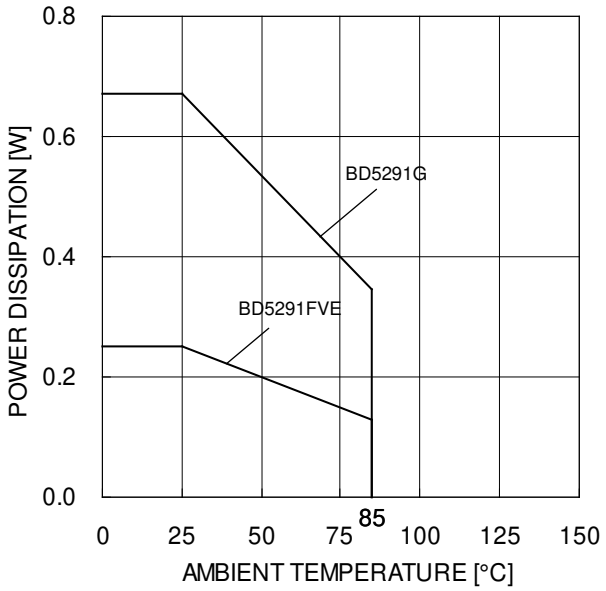


Figure 2.
Derating curve

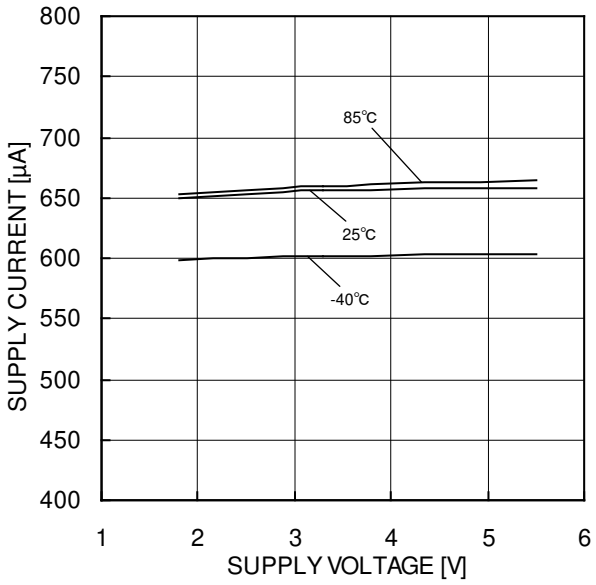


Figure 3.
Supply Current – Supply Voltage

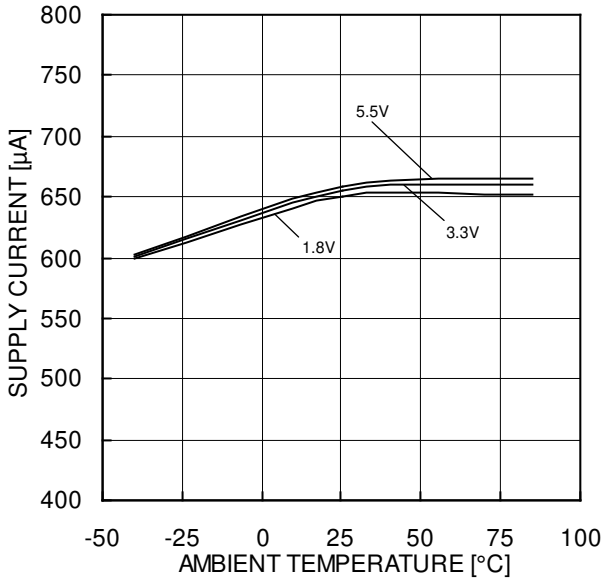


Figure 4.
Supply Current – Ambient Temperature

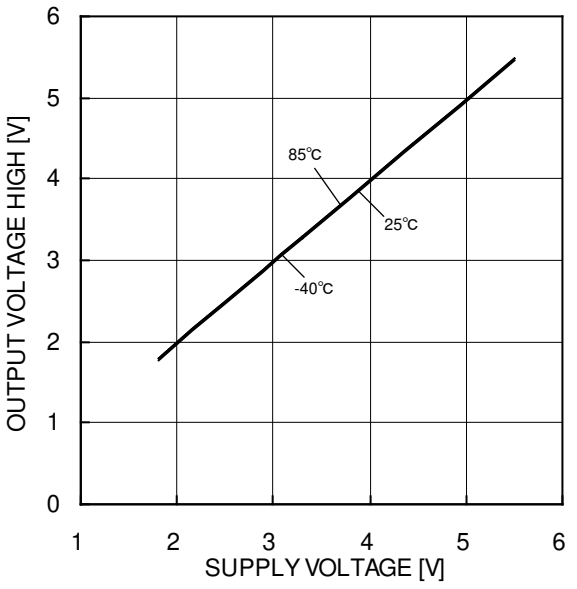


Figure 5.
Maximum Output Voltage (High) – Supply Voltage
(RL=10kΩ)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

○BD5291xxx

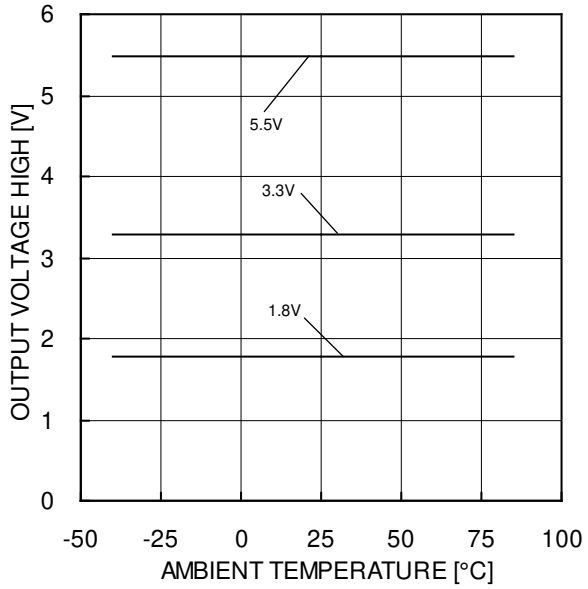


Figure 6.
Maximum Output Voltage (High) – Ambient Temperature
(RL=10kΩ)

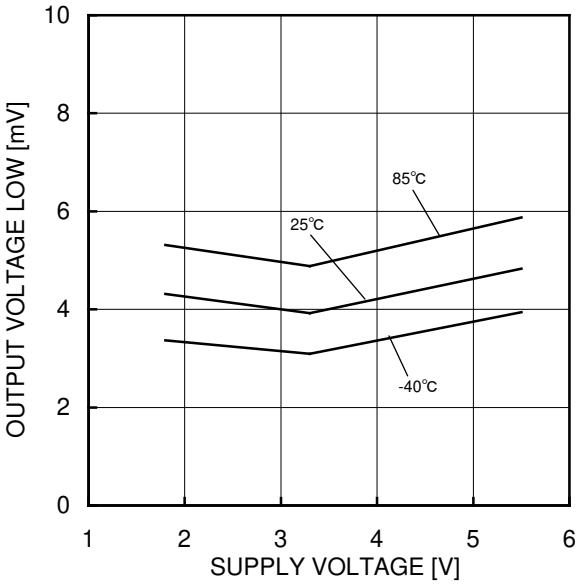


Figure 7.
Maximum Output Voltage (Low) – Supply Voltage
(RL=10kΩ)

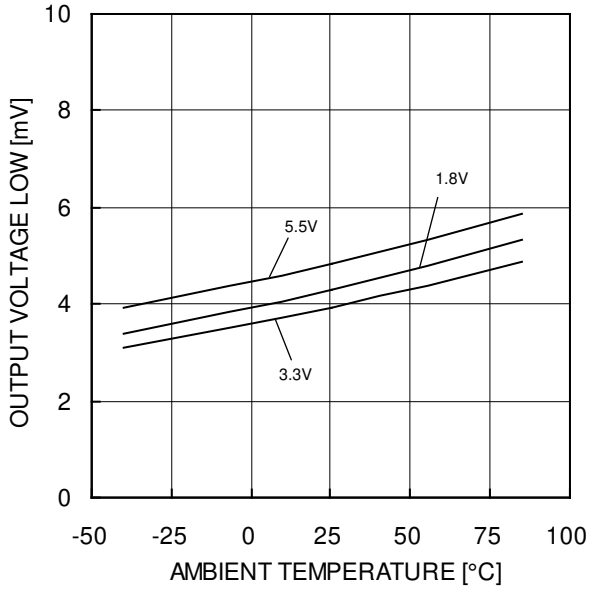


Figure 8.
Maximum Output Voltage (Low) – Ambient Temperature
(RL=10kΩ)

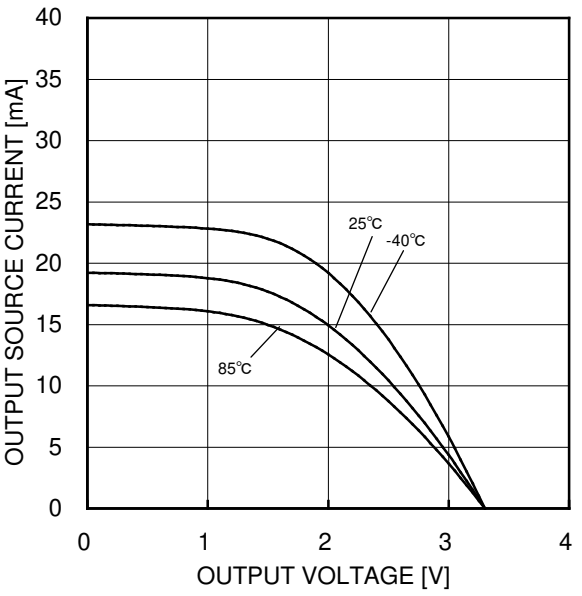


Figure 9.
Output Source Current – Output Voltage
(VDD=3.3V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

OBD5291xxx

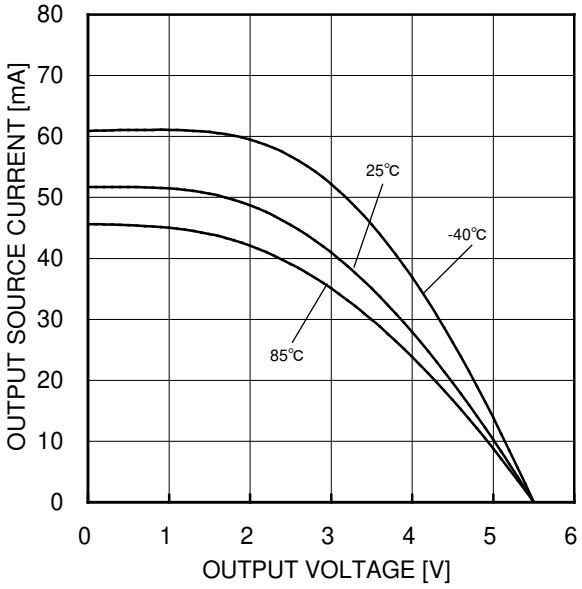


Figure 10.
Output Source Current – Output Voltage
(VDD=5.5V)

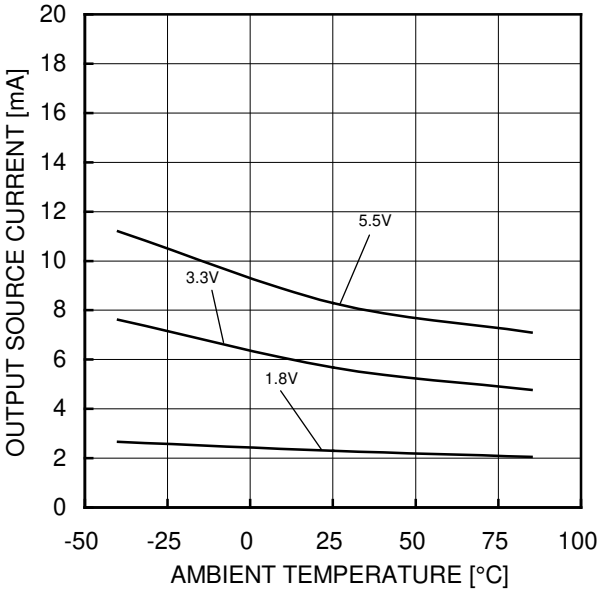


Figure 11.
Output Source Current –Ambient Temperature
(OUT=VDD-0.4V)

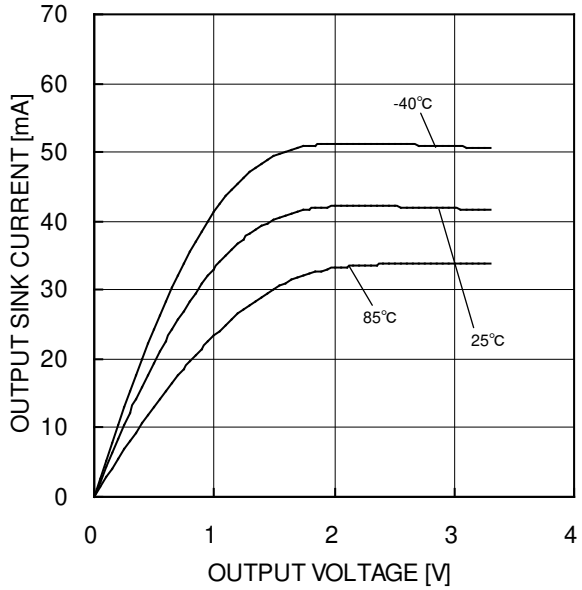


Figure 12.
Output Sink Current – Output Voltage
(VDD=3.3V)

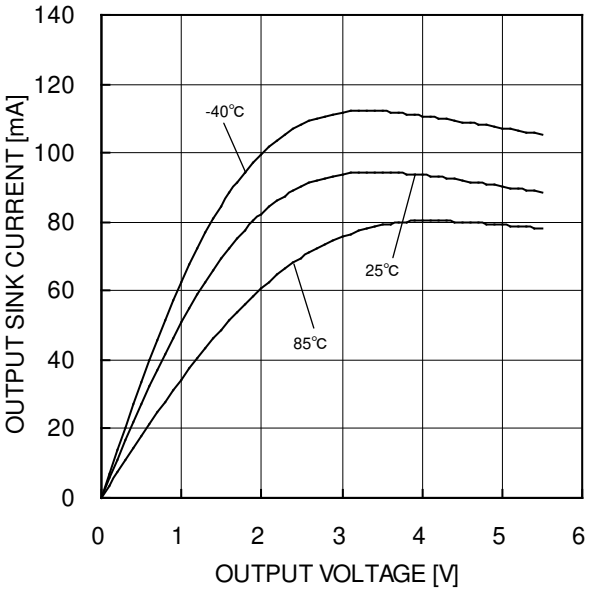


Figure 13.
Output Sink Current – Output Voltage
(VDD=5.5V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

OBD5291xxx

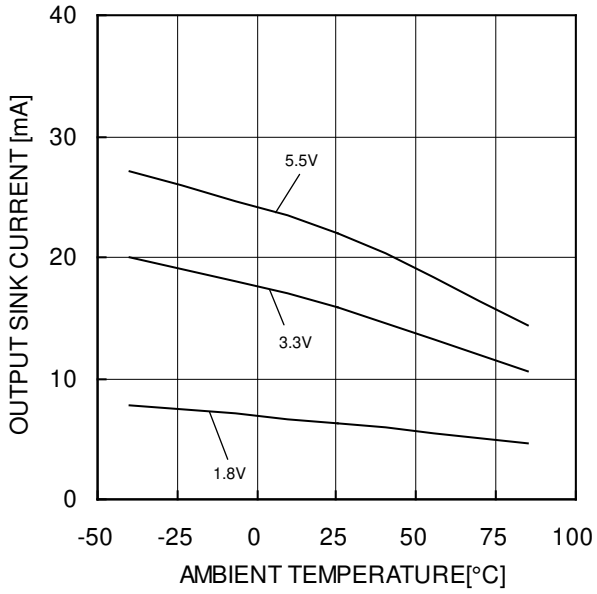


Figure 14.
Output Sink Current – Ambient Temperature
(OUT=VSS+0.4V)

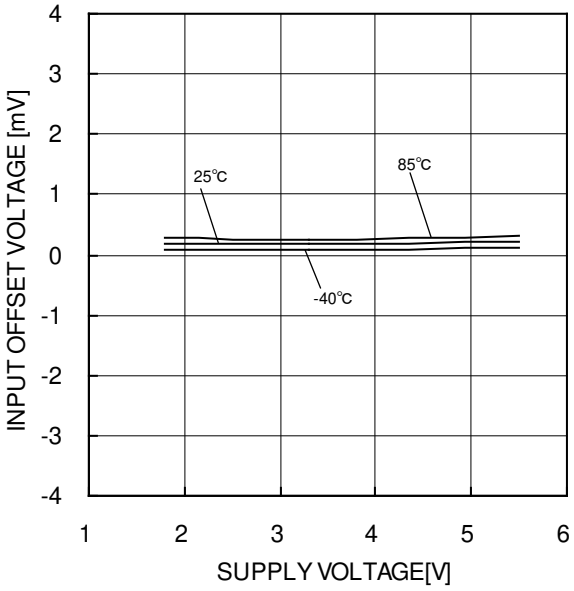


Figure 15.
Input Offset Voltage – Supply Voltage

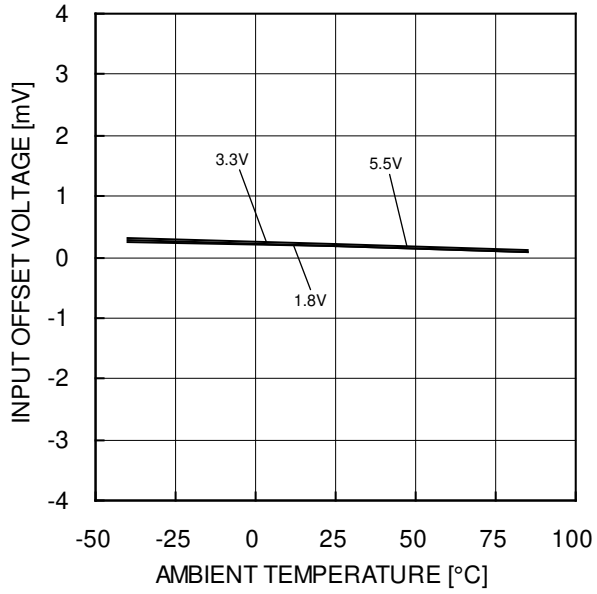


Figure 16.
Input Offset Voltage – Ambient Temperature

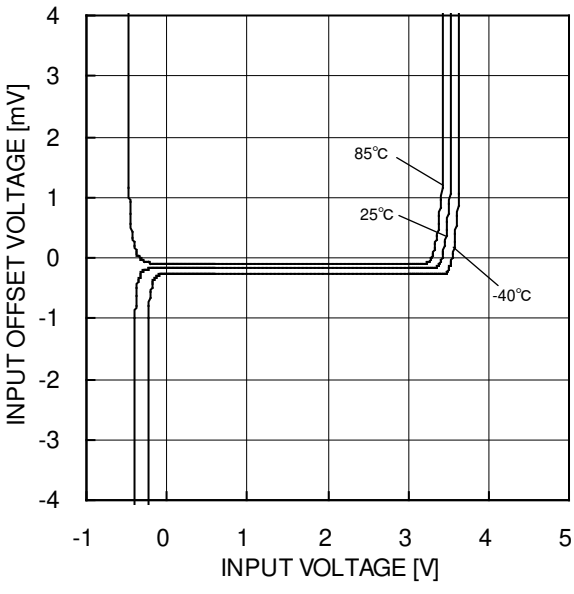


Figure 17.
Input Offset Voltage – Input Voltage
(VDD=3.3V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

○BD5291xxx

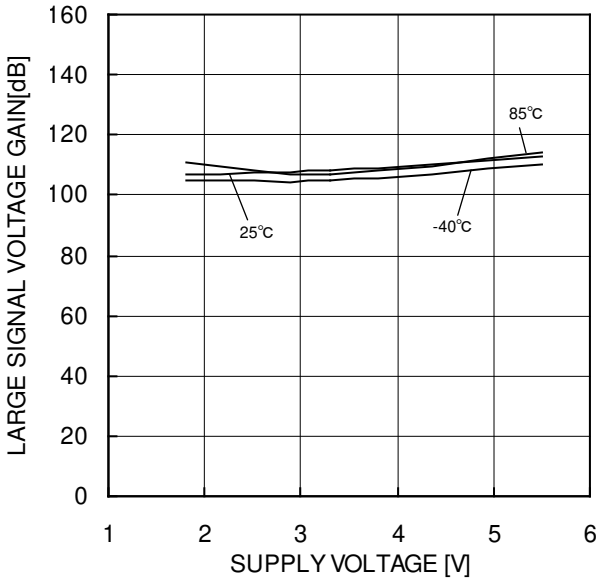


Figure 18.
Large Signal Voltage Gain – Supply Voltage

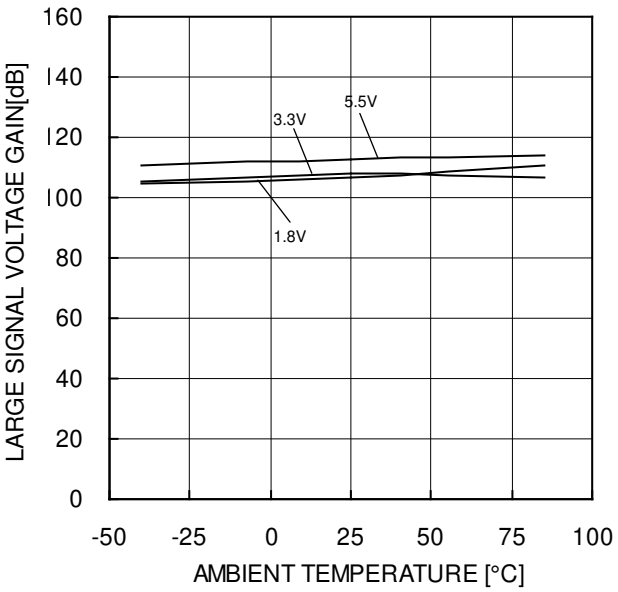


Figure 19.
Large Signal Voltage Gain – Ambient Temperature

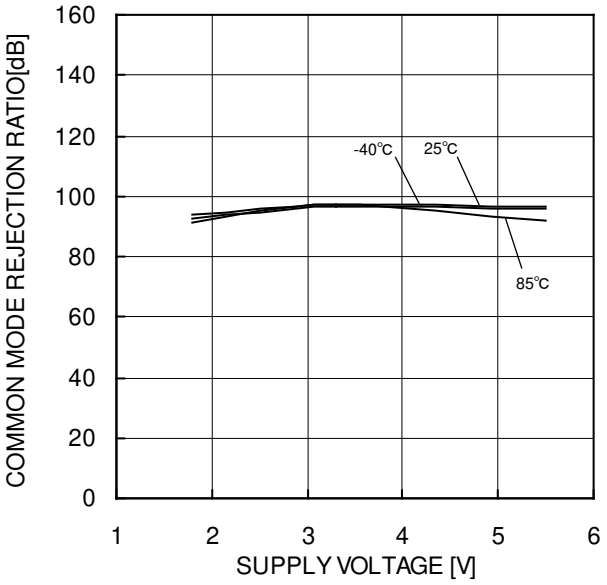


Figure 20.
Common Mode Rejection Ratio – Supply Voltage

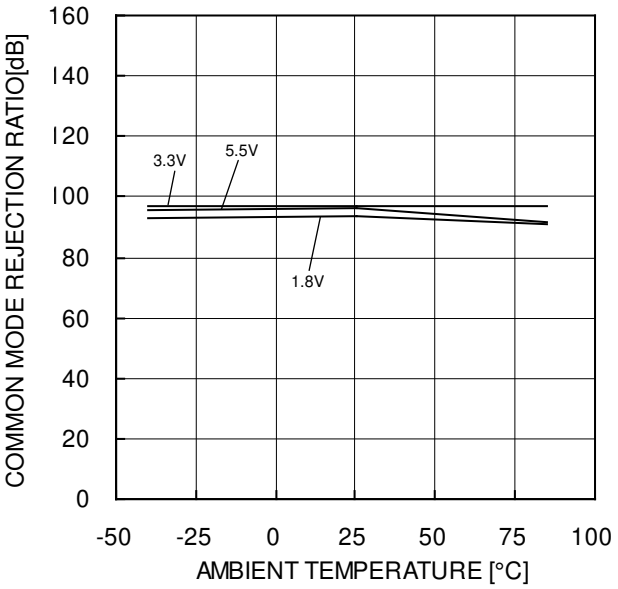


Figure 21.
Common Mode Rejection Ratio – Ambient Temperature

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

○BD5291xxx

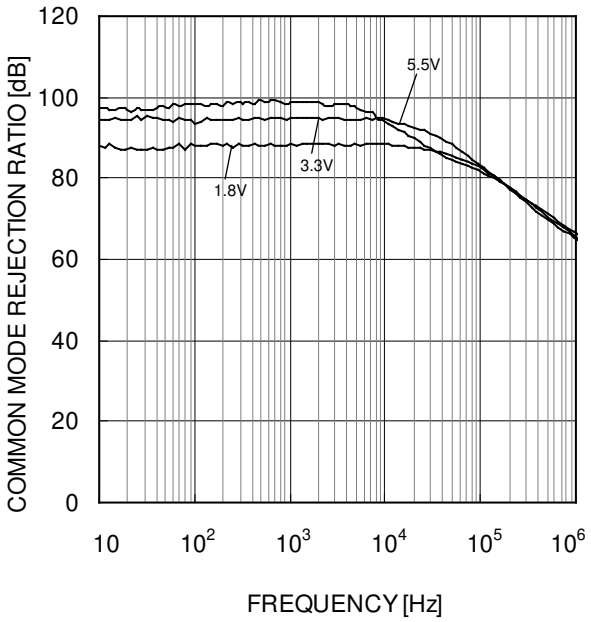


Figure 22.
Common Mode Rejection Ratio – Frequency

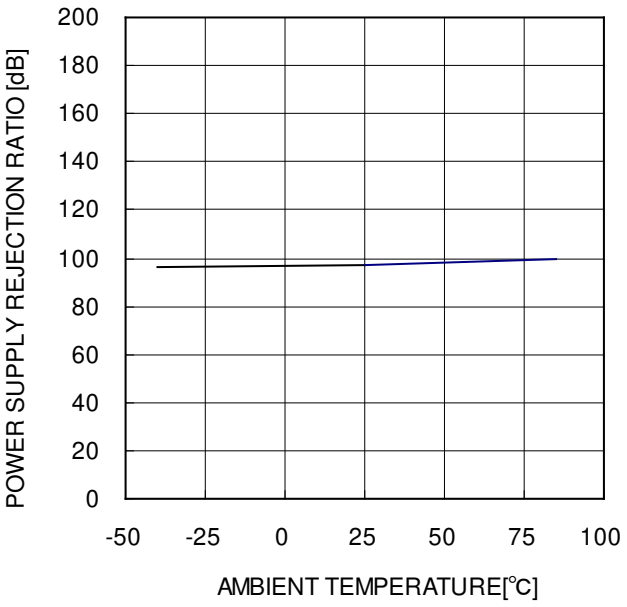


Figure 23.
Power Supply Rejection Ratio – Ambient Temperature
(VDD=1.7V to 5.5V)

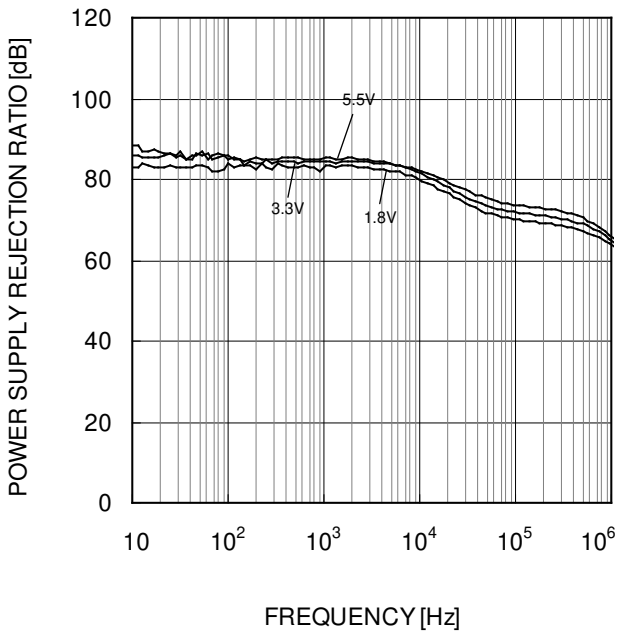


Figure 24.
Power Supply Rejection Ratio – Frequency

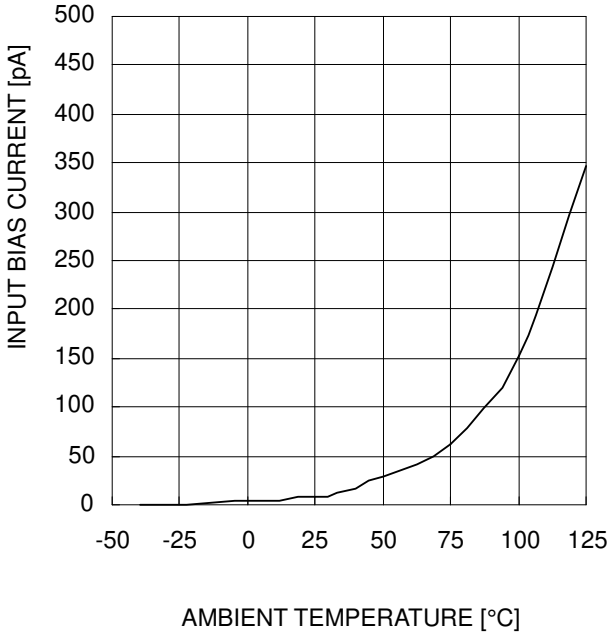


Figure 25.
Input Bias Current – Ambient Temperature
(VDD=3.3V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves – continued

○BD5291xxx

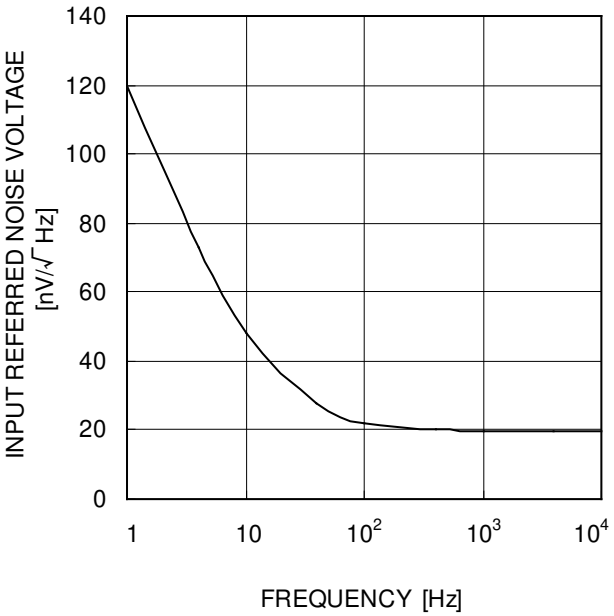


Figure 26.
Input Referred Noise Voltage－Frequency
(VDD=3.3V)

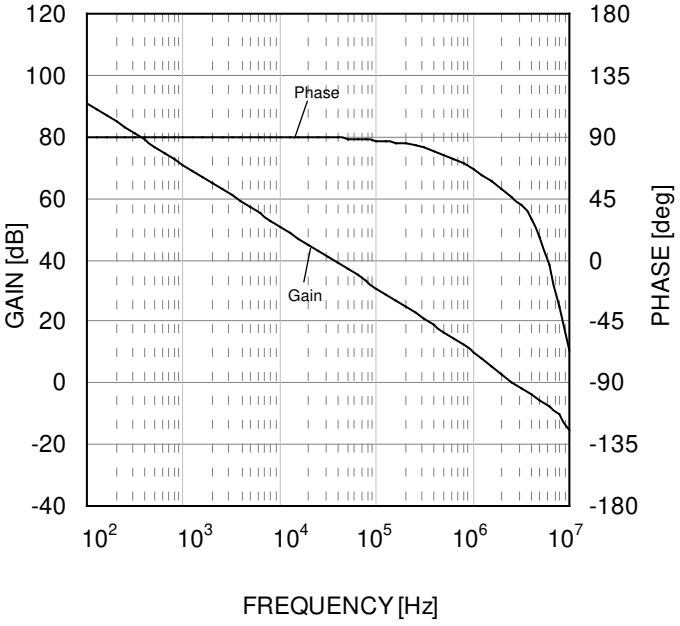


Figure 27.
Voltage Gain, Phase – Frequency
(VDD=3.3V , Open loop)

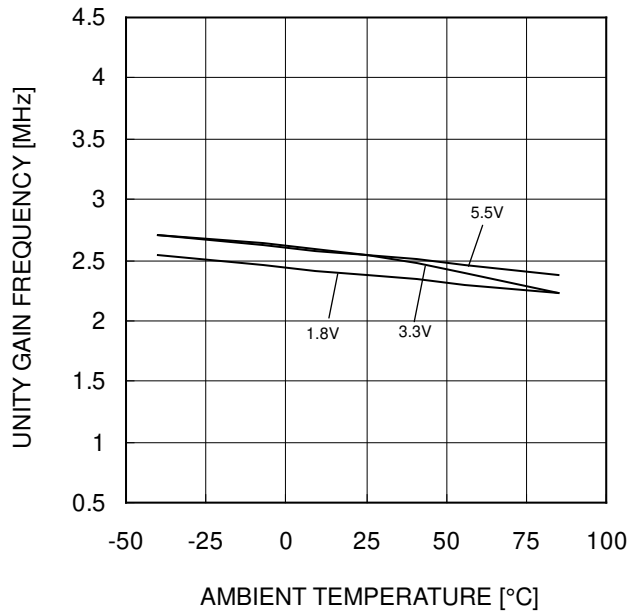


Figure 28.
Unity Gain Frequency – Ambient Temperature

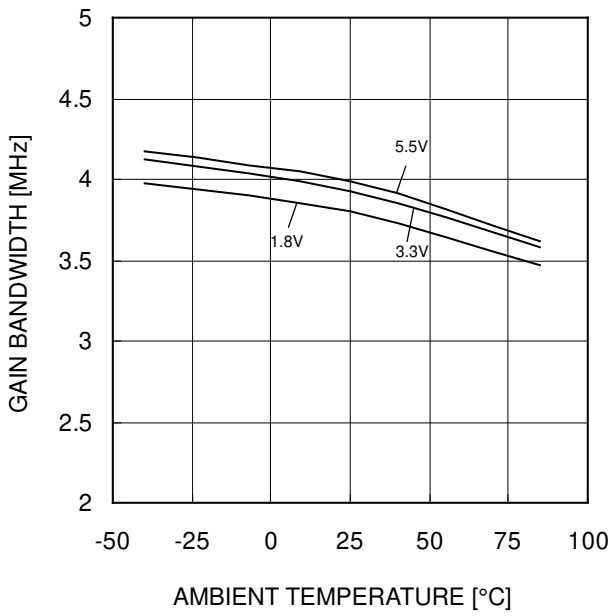


Figure 29.
Gain Bandwidth – Ambient Temperature

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves – continued

○BD5291xxx

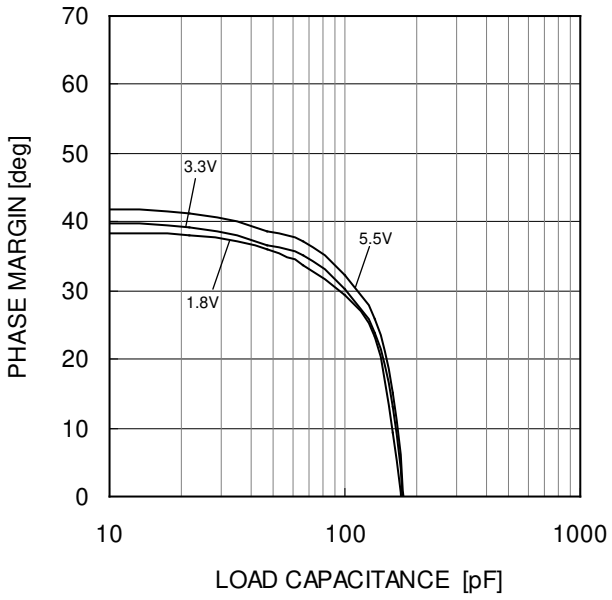


Figure 30.
Phase Margin－Load Capacitance

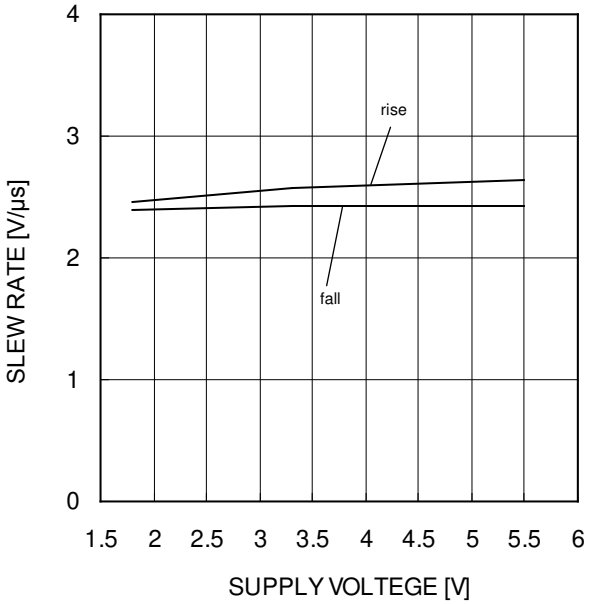


Figure 31.
Slew Rate－Supply Voltage

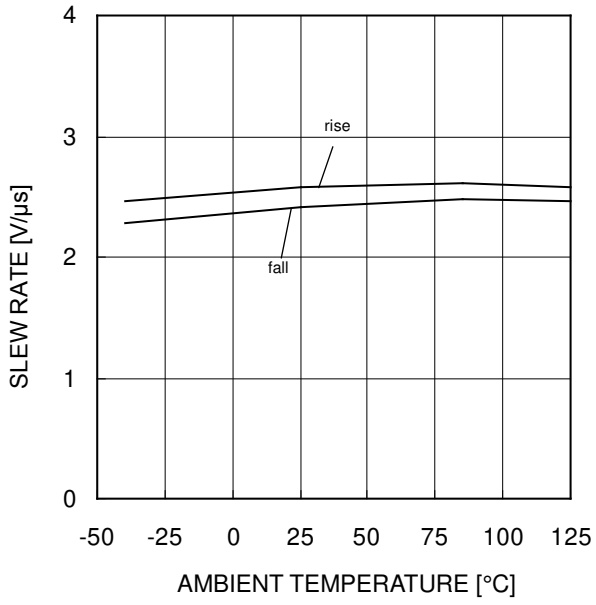


Figure 32.
Slew Rate – Ambient Temperature
(VDD=3.3V)

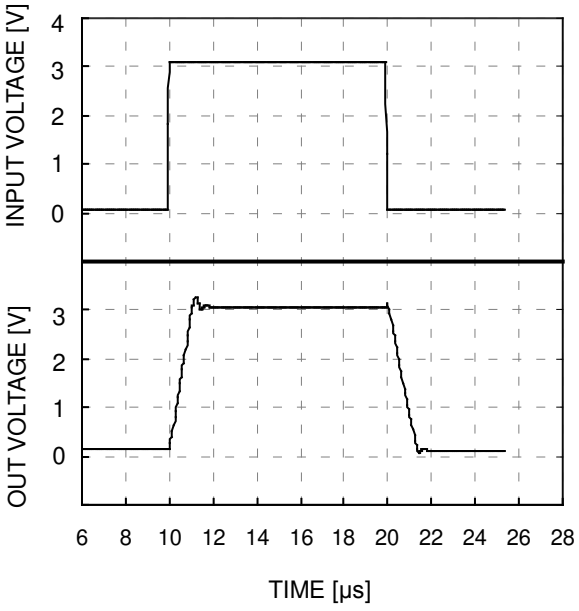


Figure 33.
Input and Output Wave Form
(VDD=5V, A_V=1, R_L=2kΩ, C_L=10pF
IN=3V_{P-P}, T_A=25℃)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

○BD5291xxx

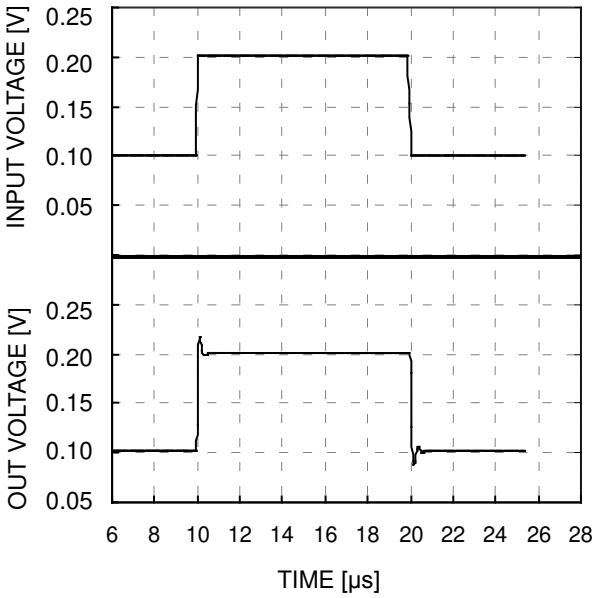


Figure 34.
Input and Output Wave Form
(VDD=5V, A_V=1, R_L=2kΩ, C_L=10pF
IN=100mV_{P-P}, T_A=25°C)

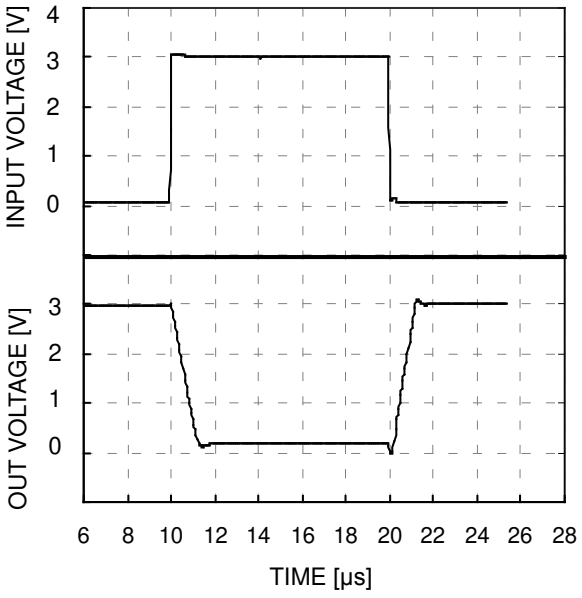


Figure 35.
Input and Output Wave Form
(VDD=5V, A_V=-1, R_L=2kΩ, C_L=10pF
IN=3V_{P-P}, T_A=25°C)

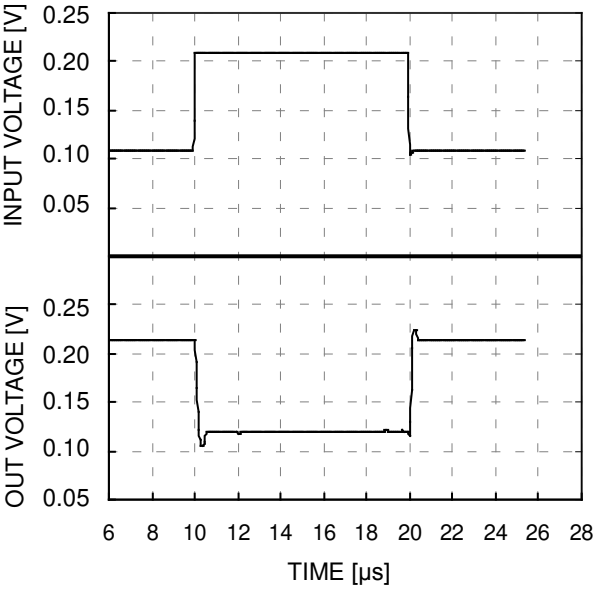


Figure 36.
Input and Output Wave Form
(VDD=5V, A_V=-1, R_L=2kΩ, C_L=10pF
IN=100mV_{P-P}, T_A=25°C)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Application Information

NULL method condition for Test Circuit 1

VDD, VSS, E_K, V_{ICM} Unit:V

Parameter	V_F	SW1	SW2	SW3	VDD	VSS	E_K	V_{ICM}	V_{RL}	Calculation
Input Offset Voltage	V_{F1}	ON	ON	OFF	3.3	0	-1.65	1.65	-	1
Large Signal Voltage Gain	V_{F2}	ON	ON	ON	3.3	0	-0.5	0.9	1.65	2
	V_{F3}						-2.5		1.65	
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	V_{F4}	ON	ON	OFF	3.3	0	-1.5	0	-	3
	V_{F5}							3.3	-	
Power Supply Rejection Ratio	V_{F6}	ON	ON	OFF	1.7	0	-0.9	0	-	4
	V_{F7}				5.5				-	

－ Calculation－

1. Input Offset Voltage (V_{IO})

$$V_{IO} = \frac{|V_{F1}|}{1+R_F/R_S} \text{ [V]}$$

2. Large Signal Voltage Gain (Av)

$$Av = 20\text{Log}\frac{\Delta V_{EK} \times (1+R_F/R_S)}{|V_{F2}-V_{F3}|} \text{ [dB]}$$

3. Common-mode Rejection Ratio (CMRR)

$$CMRR = 20\text{Log}\frac{\Delta V_{ICM} \times (1+R_F/R_S)}{|V_{F4} - V_{F5}|} \text{ [dB]}$$

4. Power Supply Rejection Ratio (PSRR)

$$PSRR = 20\text{Log}\frac{\Delta VDD \times (1+ R_F/R_S)}{|V_{F6} - V_{F7}|} \text{ [dB]}$$

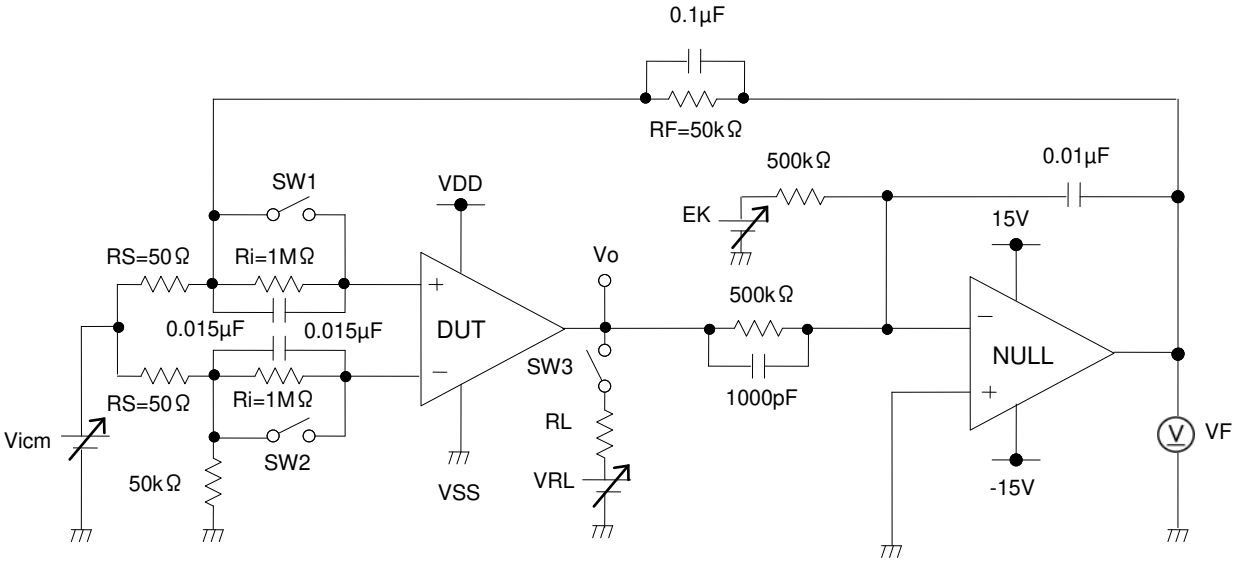


Figure 37. Test circuit 1

Application Information - continued

Switch Condition for Test Circuit 2

Parameter	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage RL=10kΩ	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Unit gain frequency	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

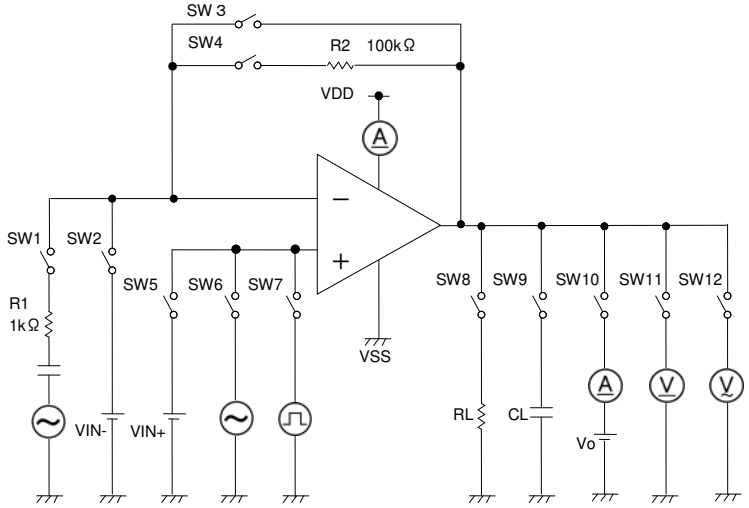


Figure 38. Test circuit 2

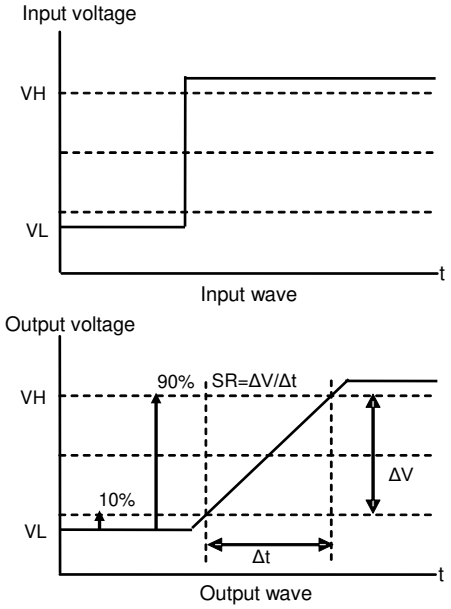


Figure 39. Slew rate input output wave

Application example

○Voltage follower

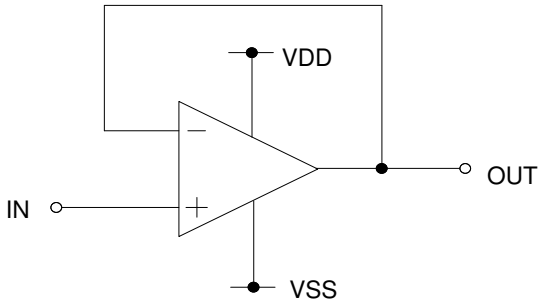


Figure 40. Voltage follower

Voltage gain is 0dB.
Using this circuit, the output voltage (OUT) is configured to be equal to the input voltage (IN). This circuit also stabilizes the output voltage (OUT) due to high input impedance and low output impedance. Expression for output voltage (OUT) is shown below.
OUT=IN

○Inverting amplifier

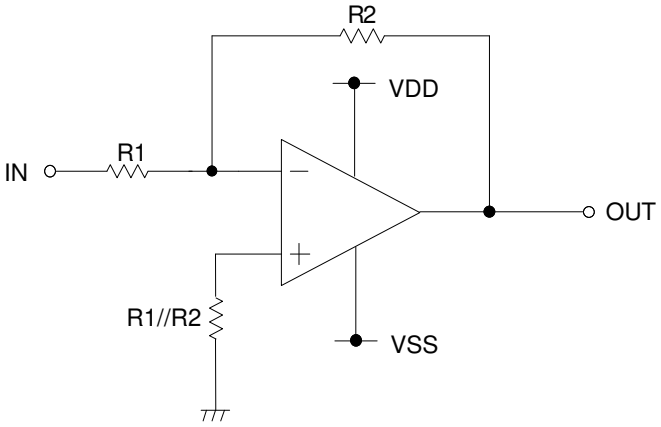


Figure 41. Inverting amplifier circuit

For inverting amplifier, input voltage (IN) is amplified by a voltage gain and depends on the ratio of R1 and R2. The out-of-phase output voltage is shown in the next expression
OUT=-(R2/R1) ・IN
This circuit has input impedance equal to R1.

○Non-inverting amplifier

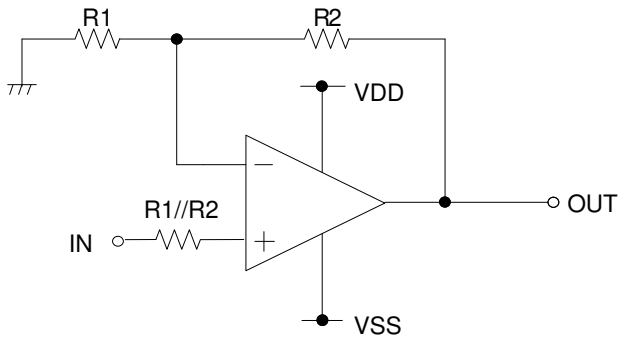


Figure 42. Non-inverting amplifier circuit

For non-inverting amplifier, input voltage (IN) is amplified by a voltage gain, which depends on the ratio of R1 and R2. The output voltage (OUT) is in-phase with the input voltage (IN) and is shown in the next expression.
OUT=(1 + R2/R1) ・IN
Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

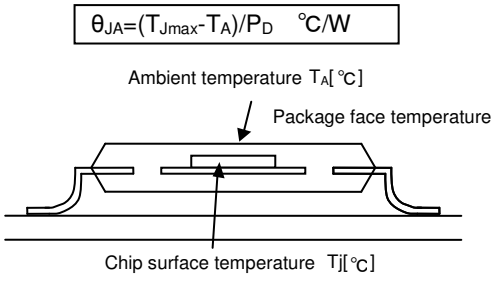
Power Dissipation

Power dissipation (total loss) indicates the power that can be consumed by IC at T_A=25°C(normal temperature).IC is heated when it consumed power, and the temperature of IC ship becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol θ_{JA}°C/W. The temperature of IC inside the package can be estimated by this thermal resistance.

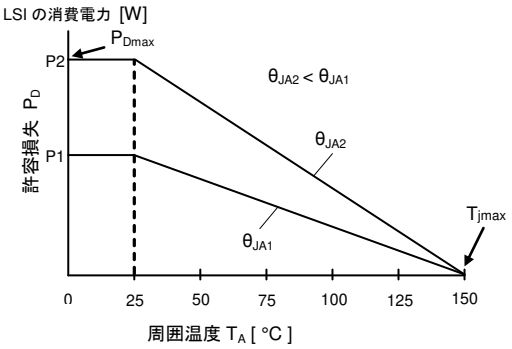
Figure 43.(a) shows the model of thermal resistance of the package. Thermal resistance θ_{JA}, ambient temperature T_A, maximum junction temperature Tjmax, and power dissipation Pd can be calculated by the equation below:

$$\theta_{JA} = (T_{Jmax} - T_A) / P_D \quad °C/W$$

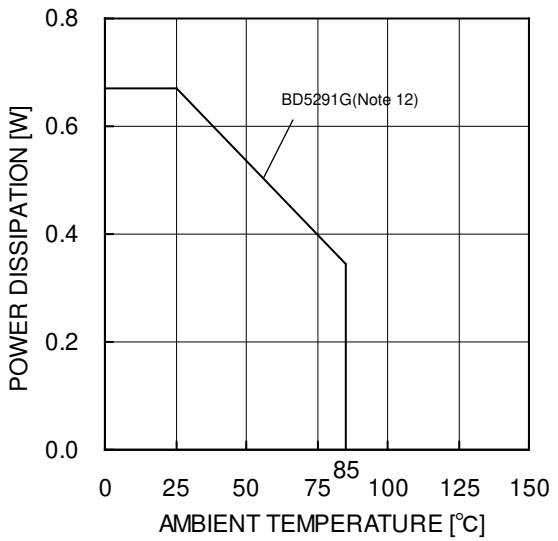
Derating curve in Figure 43.(b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{JA}. Thermal resistance θ_{JA} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 43.(c),(d) show a derating curve for an example of BD5291xxx.



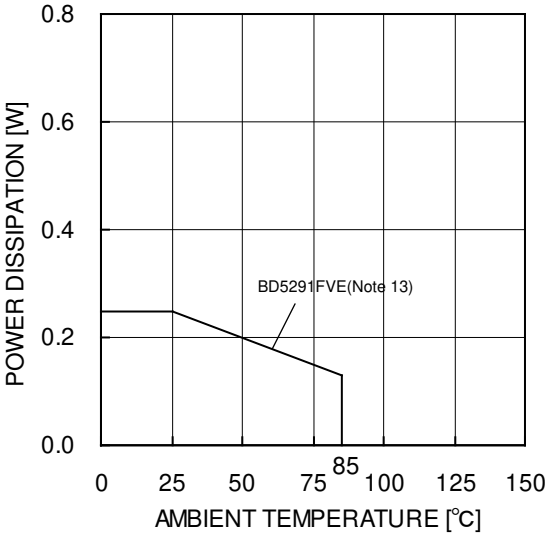
(a) Thermal resistance



(b) Derating curve



(c) BD5291G



(d) BD5291FVE

Note 12	Note 13	Unit
5.4	2.0	mW/℃

When using the unit above T_A=25°C, subtract the value above per °C. Permissible dissipation is the value when FR4 glass epoxy board 70mm × 70mm × 1.6mm (copper foil area below 3%) is mounted

Figure 43. Derating Curve

Operational Notes

1. Reverse Connection of Power Supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

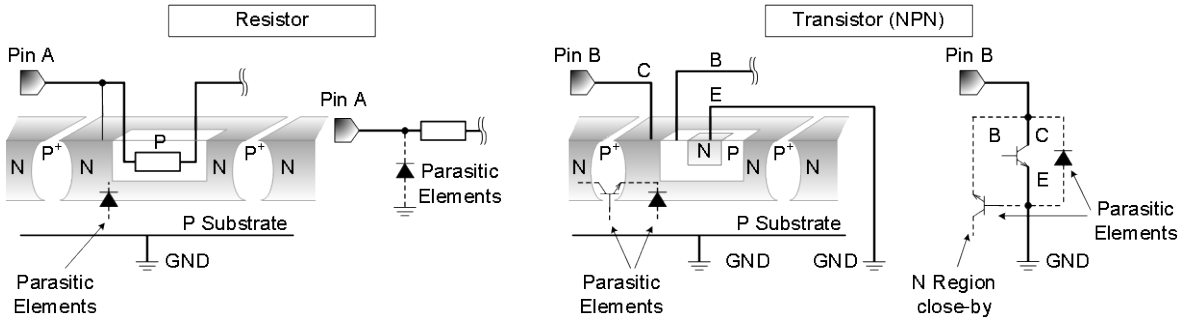


Figure 44. Example of monolithic IC structure

13. Oscillation for feed back circuit

Be careful when using the IC in feed back circuit. Phase margin of this IC is 40°.Oscillation is caused by large size capacitive load connecting to output terminal. If the circuits has large size capacitor that is connected to output terminal. Please insert of isolation resistor between output terminal and capacitive load.

14. Input Voltage

Applying VDD+0.3V to the input terminal is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

15. Power supply(single/dual)

The operational amplifiers operate when the voltage supplied is between VDD and VSS. Therefore, the single supply operational amplifiers can be used as dual supply operational amplifiers as well.

16. Output capacitor

Discharge of the external output capacitor to VDD is possible via internal parasitic elements when VDD is shorted to VSS, causing damage to the internal circuitry due to thermal stress. Therefore, when using this IC in circuits where oscillation due to output capacitive load does not occur, such as in voltage comparators, use an output capacitor with a capacitance less than 0.1µF.
Designed negative feedback circuit using this IC, verify output oscillation caused by capacitive load.

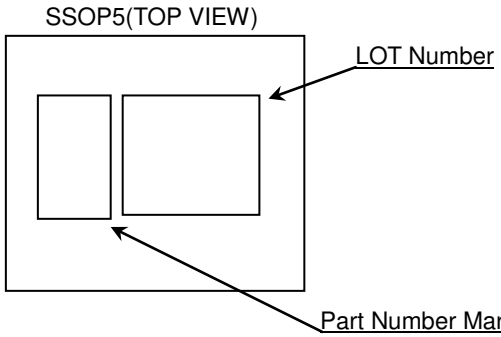
17. Latch up

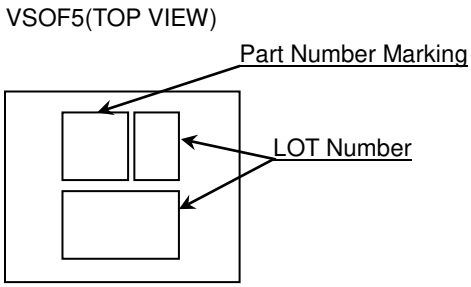
Be careful of input voltage that exceed the VDD and VSS. When CMOS device have sometimes occur latch up operation. And protect the IC from abnormaly noise.

18. Decupling Capacitor

Insert the decupling capacitance between VDD and VSS, for stable operation of operational amplifier.

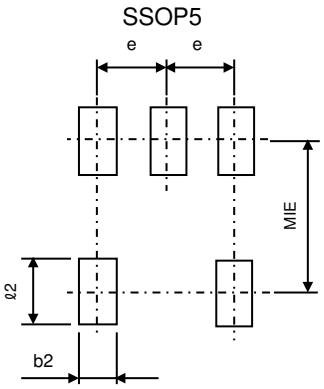
Marking Diagram





Product Name		Package Type	Marking
BD5291	G	SSOP5	L7
	FVE	VSOF5	N6

Land Pattern data

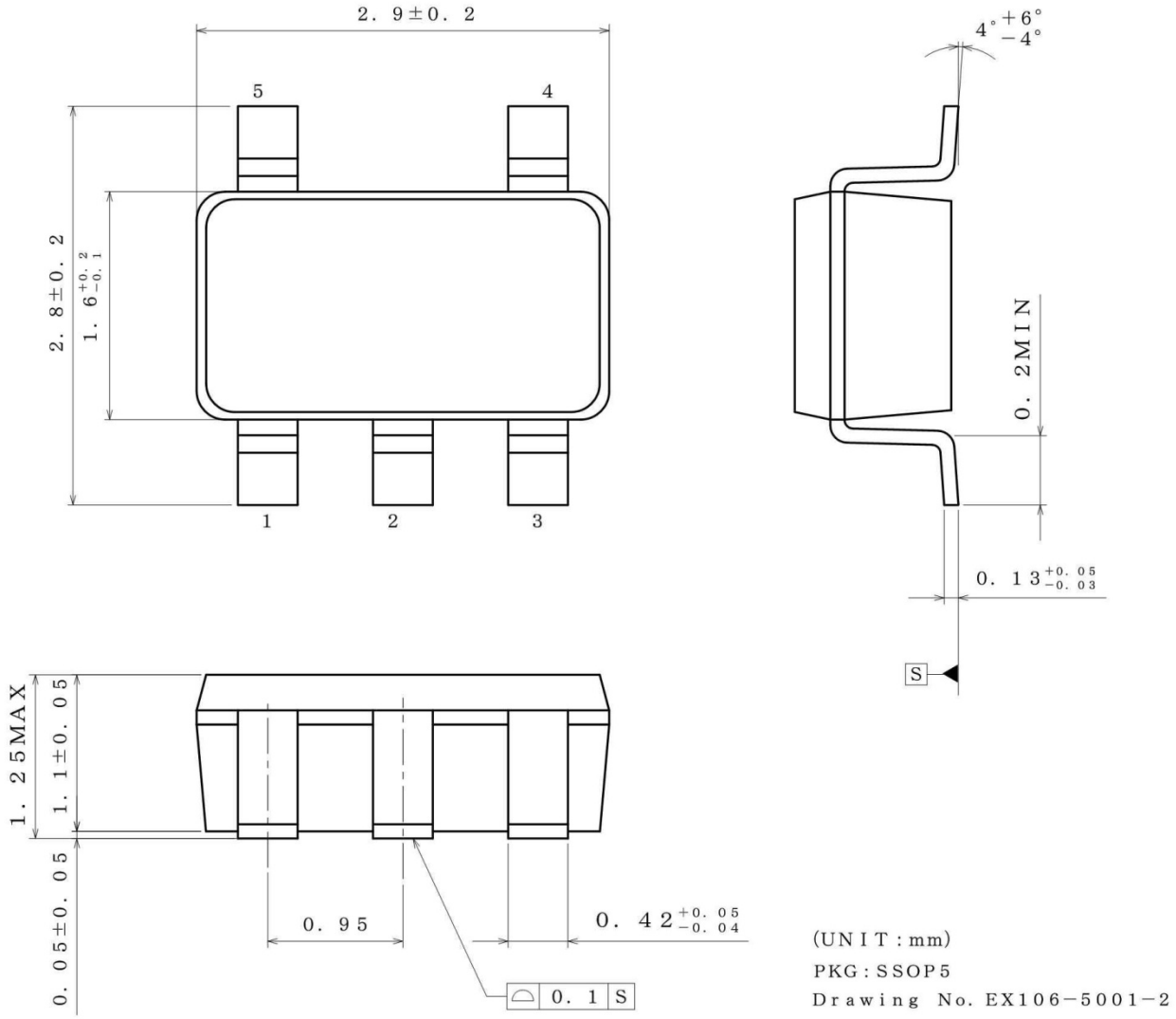


Unit : mm

PKG	Land Pitch e	Land Space MIE	Land Length ≧ℓ 2	Land Width b2
SSOP5	0.95	2.4	1.0	0.6
VSOF5	0.5	1.35	0.35	0.25

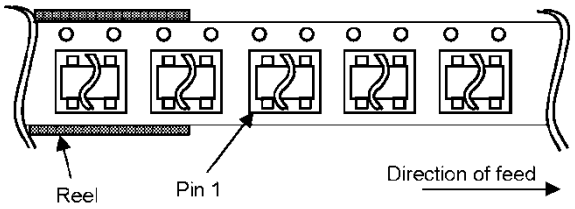
Physical Dimensions Tape and Reel Information

Package Name	SSOP5



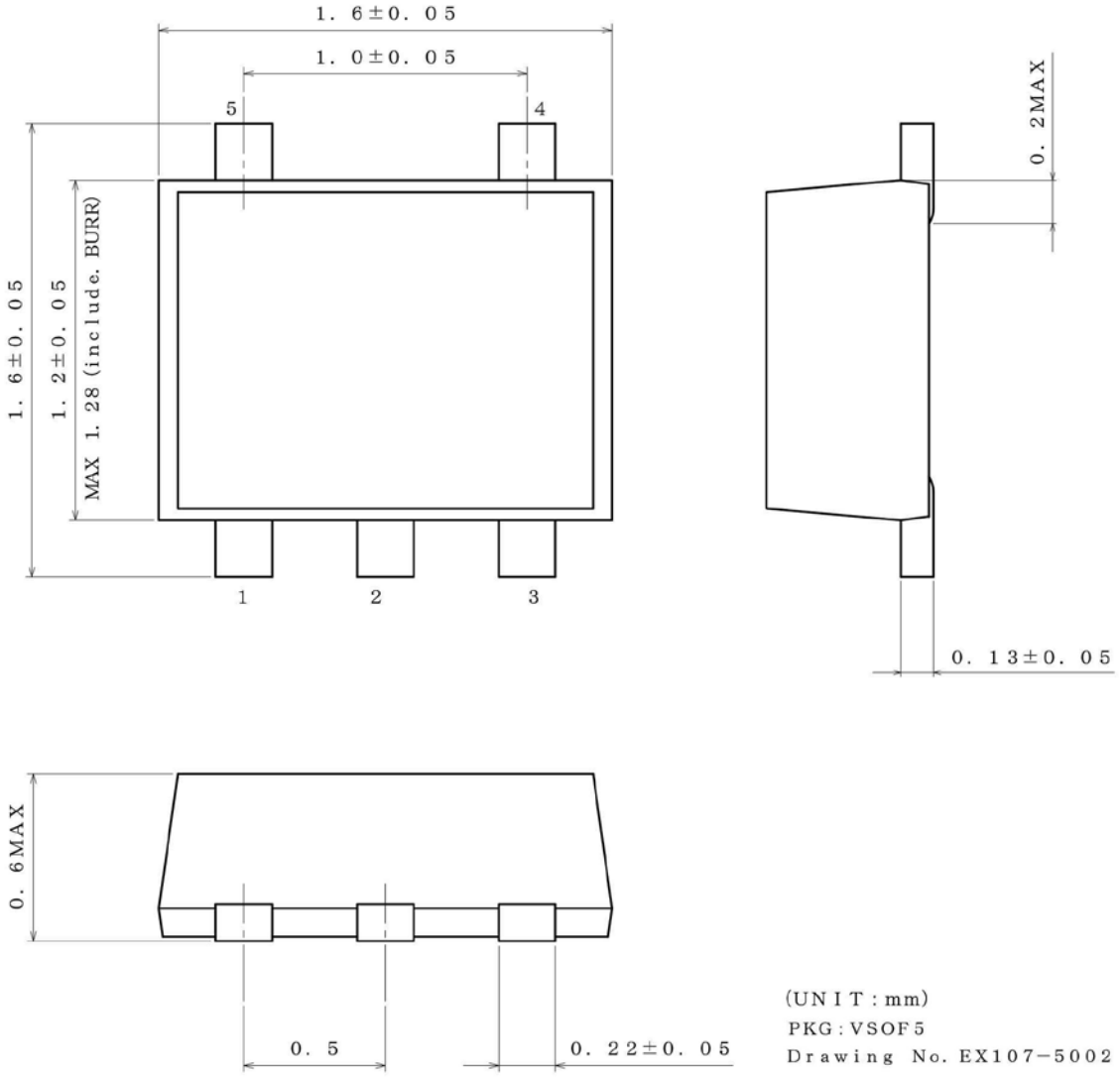
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TL (The direction is the 1pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand)



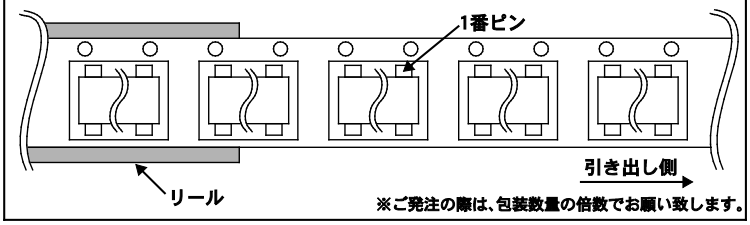
Physical Dimensions Tape and Reel Information – continued

Package Name	VSOF5



＜包装仕様＞

包装形態	エンボステーピング
包装数量	3000pcs
包装方向	TR （リールを左手に持ち、右手でテープを引き出したときに製品の1番ピンが右上にくる方向）



※ご発注の際は、包装数量の倍数でお願い致します。

Revision History

Date	Revision	Changes
10.JUN.2013	001	New Release
26.NOV.2013	002	Add BD5291FVE, Delete Simplified Schematic
13.FEB.2014	003	General Description is modified
22.APR.2014	004	Delete BD5291FVE
06.Jun.2016	005	Added BD5291FVE