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Middle Power Class-D Speaker Amplifiers

Class-D Speaker Amplifier for Digital Input

BD5446EFV

No.11075ECT14

●Description

BD5446EFV is a Class D Speaker Amplifier designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of 20W+20W. This IC employs state-of-the-art Bipolar, CMOS, and DMOS (BCD) process technology that eliminates turn-on resistance in the output power stage and internal loss due to line resistances up to an ultimate level. With this technology, the IC can achieve high efficiency of 87% (10W+10W output with 8Ω load). In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 40W. This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

●Features

1) BD5446EFV has two system of digital audio interface.
   (I^2S/LJ format, SDATA: 16 / 20 / 24bit, LRCLK: 32kHz / 44.1kHz / 48kHz, BCLK: 64fs (fixed), SYS_CLK: 256fs (fixed))
2) Within the wide range of the power supply voltage, it is possible to operate in a single power supply. (10~26V)
3) It contributes to miniaturizing, making to the thin type, and the power saving of the system by high efficiency and low heat.
4) S/N of the system can be optimized by adjusting the gain setting among 8 steps. (20~34dB / 2dB step)
5) It has the output power limitation function that can be adjusted to an arbitrary output power.
6) The decrease in sound quality because of the change of the power supply voltage is prevented with the feedback circuitry of the output. In addition, a low noise and low distortion are achieved.
7) It provides with the best stereo DAC output for the headphone usage. As a result, the output of the selection of the digital input in two systems is possible.
8) Eliminates pop noise generated when the power supply goes on/off, or when the power supply is suddenly shut off. High quality muting performance is realized by using the soft-muting technology.
9) BD5446EFV is a highly reliable design to which it has various protection functions.
   (High temperature protection, Under voltage protection, Output short protection, Output DC voltage protection and Clock stop protection)

●Applications

Flat Panel TVs (LCD, Plasma), Home Audio, Desktop PC, Amusement equipments, Electronic Music equipments, etc.,

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	30	V	Pin 25, 28, 29, 53, 54 *1 *2
Power dissipation	P_d	2.0	W	*3
		4.5	W	*4
		6.2	W	*5
Input voltage	V_{IN}	-0.3 ~ 4.5	V	Pin 7 ~ 18, 21 *1
Open-drain terminal voltage	V_{ERR}	-0.3 ~ 30	V	Pin24 *1
Operating temperature range	T_{opr}	-25 ~ +85	℃	
Storage temperature range	T_{stg}	-55 ~ +150	℃	
Maximum junction temperature	T_{jmax}	+150	℃	

∗1 The voltage that can be applied reference to GND (Pin 6, 36, 37, 45, 46).
∗2 Do not, however exceed Pd and Tjmax=150℃.
∗3 70mm×70mm×1.6mm, FR4, 1-layer glass epoxy board (Copper on bottom layer 0%)
Derating in done at 16mW/℃ for operating above Ta=25℃.
∗4 70mm×70mm×1.6mm, FR4, 2-layer glass epoxy board (Copper on bottom layer 100%)
Derating in done at 36mW/℃ for operating above Ta=25℃. There are thermal via on the board.
∗5 70mm×70mm×1.6mm, FR4, 4-layer glass epoxy board (Copper on bottom layer 100%)
Derating in done at 49.6mW/℃ for operating above Ta=25℃. There are thermal via on the board.

●Operating conditions (Ta=25℃)

Parameter	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	10 ~ 26	V	Pin 25, 28, 29, 53, 54 *1 *2
Minimum load impedance (Speaker Output)	R_{L_SP}	5.4	Ω	*6
Minimum load impedance (DAC Output)	R_{L_DA}	20	kΩ	Pin 22, 23

*6 Do not, however exceed Pd.
* No radiation-proof design.

●Electrical characteristics

(Unless otherwise specified Ta=25℃,Vcc=13V,f=1kHz,R_{L_SP}=8Ω,R_{L_DA}=20kΩ,RESETX=3.3V,MUTEX=3.3V,PDX=3.3V, Gain=20dB,fs=48kHz)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Total circuit						
Circuit current	I_{CC1}	-	45	90	mA	Pin 25, 28, 29, 53, 54 No load
Circuit current (Power down mode)	I_{CC2}	-	1.5	3	mA	Pin 25, 28, 29, 53, 54,No load RESETX=0V,MUTEX=0V,PDX=0V
Open-drain terminal Low level voltage	V_{ERR}	-	-	0.8	V	Pin 24,I_O=0.5mA
Regulator output voltage 1	V_{REG_G}	5.0	5.5	6.0	V	Pin 1, 27
Regulator output voltage 2	V_{REG_3}	3.0	3.3	3.6	V	Pin 5
High level input voltage	V_{IH}	2.5	-	3.3	V	Pin 7 ~ 18, 21
Low level input voltage	V_{IL}	0	-	0.8	V	Pin 7 ~ 18, 21
Input current (Input pull-down terminal)	I_{IH}	33	66	132	μA	Pin 7 ~ 18, 21,VIN = 3.3V
Speaker Output						
Maximum momentary output power 1	P_{O1}	-	10	-	W	THD+n=10% GAIN=26dB *7
Maximum momentary output power 2	P_{O2}	-	20	-	W	VCC=18V, THD+n=10% GAIN =26dB *7
Total harmonic distortion	THD_{SP}	-	0.07	-	%	P_O=1W, BW=20~20kHz *7
Crosstalk	CT_{SP}	65	80	-	dB	P_O=1W, BW=IHF-A *7
Output noise voltage (Sampling mode)	V_{NO_SP}	-	140	280	μVrms	-∞dBFS, BW=IHF-A *7
Residual noise voltage (Mute mode)	V_{NOR_SP}	-	5	10	μVrms	MUTEX=0V,-∞dBFS, BW=IHF-A *7
PWM sampling frequency	f_{PWM1}	-	512	-	KHz	fs=32kHz *7
	f_{PWM2}	-	705.6	-	KHz	fs=44.1kHz *7
	f_{PWM3}	-	768	-	KHz	fs=48kHz *7
DAC Output						
Maximum output voltage	V_{OMAX}	0.85	1.0	-	Vrms	0dBFS,THD+n=1%
Channel Balance	CB	-1	0	1	dB	0dBFS
Total harmonic distortion	THD_{DA}	-	0.05	0.5	%	-20dBFS,BW=20~20kHz
Crosstalk	CT_{DA}	65	80	-	dB	0dBFS,BW=IHF-A
Output noise voltage	V_{NO_DA}	-	10	20	μVrms	-∞dBFS, BW=IHF-A
Residual noise voltage	V_{NOR_DA}	-	3	10	μVrms	MUTEX=0V,PDX=0V, -∞dBFS, BW=IHF-A

*7 These items show the typical performance of device and depend on board layout, parts, and power supply.
The standard value is in mounting device and parts on surface of ROHM's board directly.

●**Electrical characteristic curves**(V_{CC}=13V,Ta=25℃,R_{L_SP}=8Ω,R_{L_DA}=20kΩ,Gain=20dB,fin=1kHz,fs=48kHz)
Measured by ROHM designed 4 layer board.

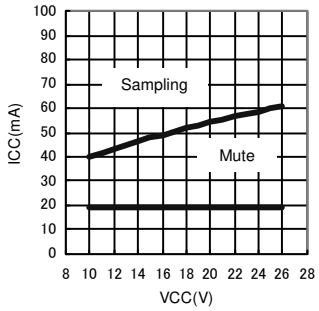


Fig.1
Current consumption
- Power supply voltage

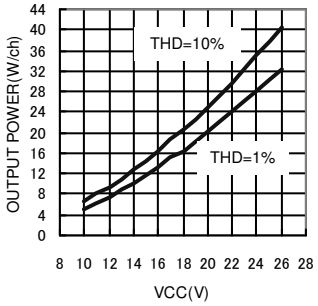


Fig.2
Output power
- Power supply voltage

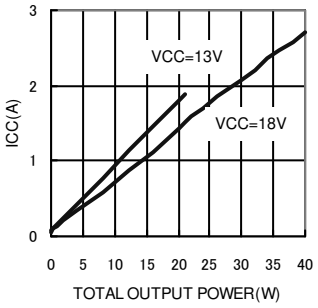


Fig.3
Current consumption
- Output power

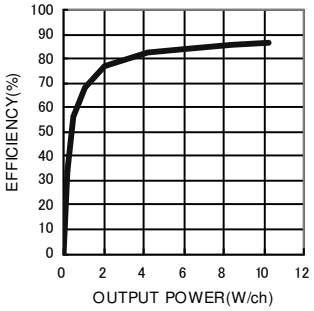


Fig.4
Efficiency - Output power

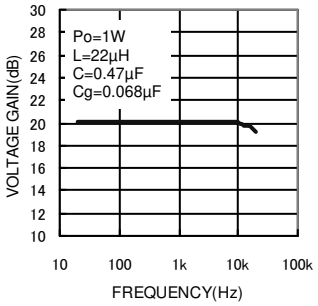


Fig.5
Voltage gain - Frequency

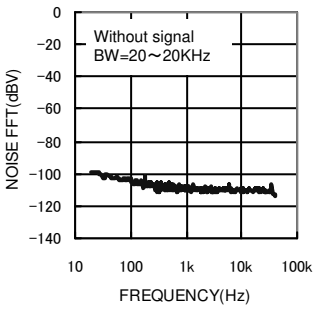


Fig.6
FFT of Output noise voltage

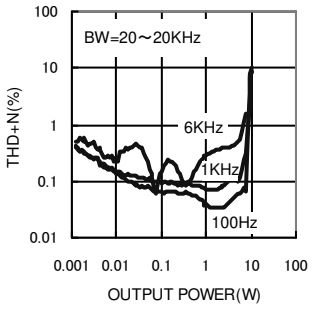


Fig.7
THD+N - Output power

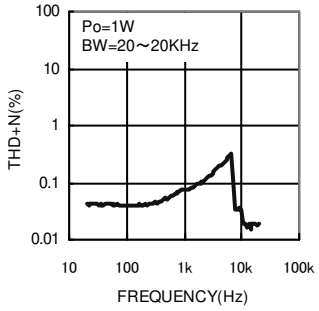


Fig.8
THD+N - Frequency

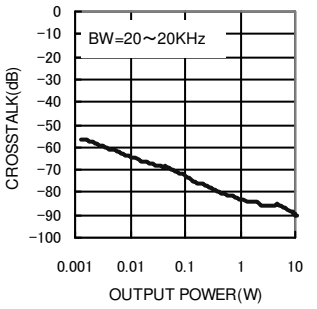


Fig.9
Crosstalk - Output power

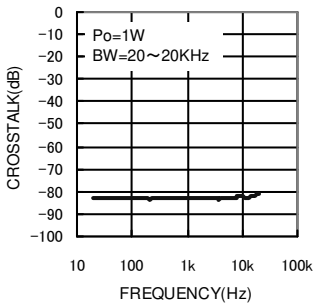


Fig.10
Crosstalk –Frequency

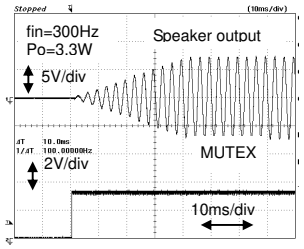


Fig.11
Wave form when
Releasing Soft-mute

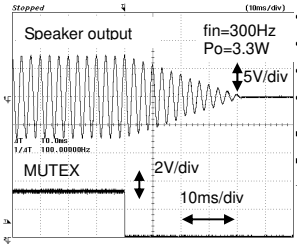


Fig.12
Wave form when
Activating Soft-mute

●**Electrical characteristic curves**(V_{CC}=18V,Ta=25℃,R_{L_SP}=8Ω,R_{L_DA}=20kΩ,Gain=20dB,fin=1kHz,fs=48kHz)
Measured by ROHM designed 4layer board.

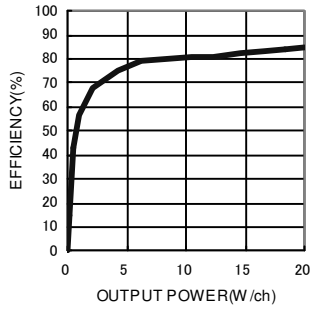


Fig.13
Efficiency – Output power

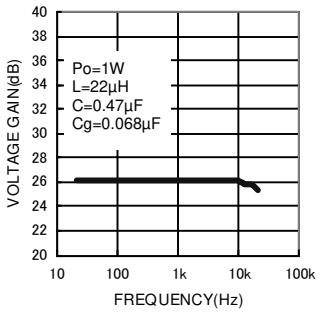


Fig.14
Voltage gain - Frequency

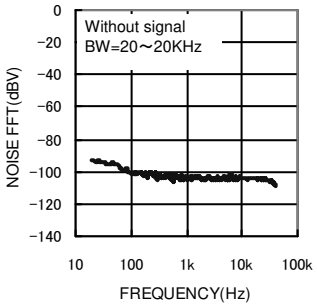


Fig.15
FFT of output noise voltage

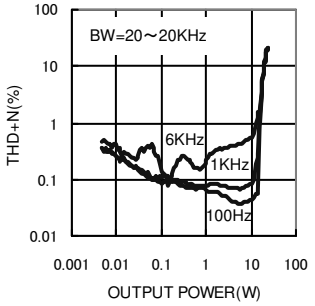


Fig.16
THD+N - Output power

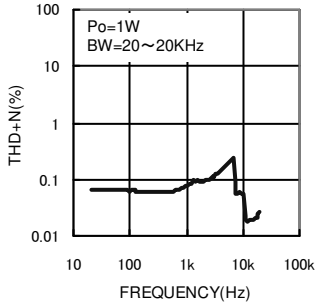


Fig.17
THD+N - Frequency

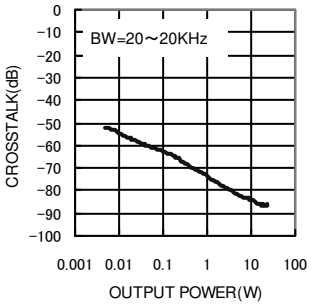


Fig.18
Crosstalk - Output power

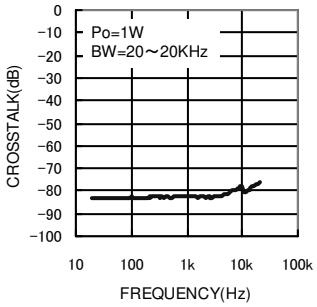
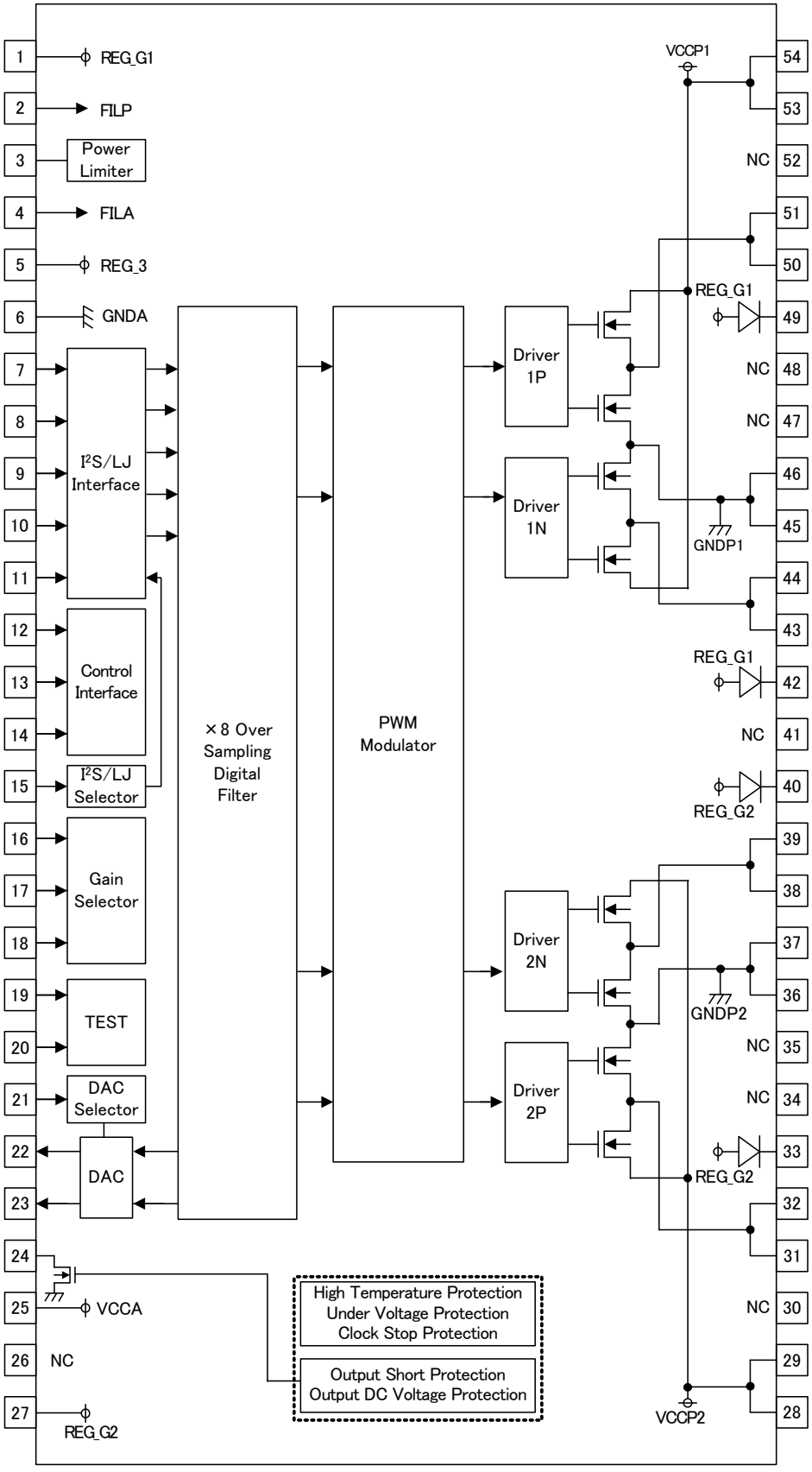
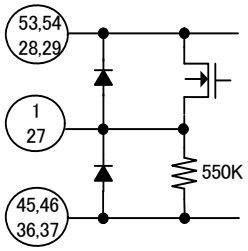
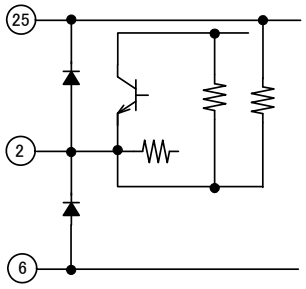
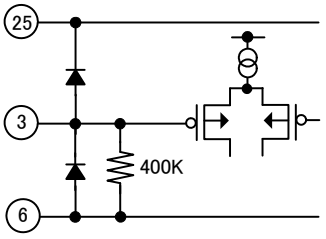
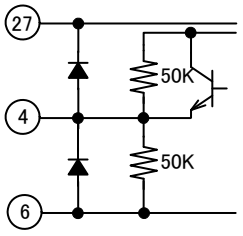
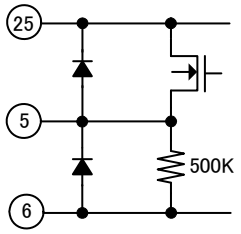


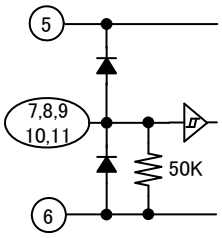
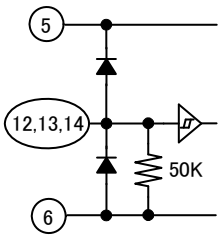
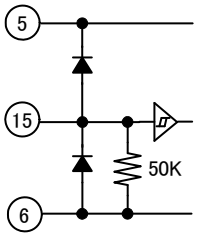
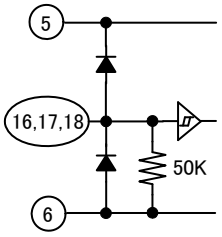
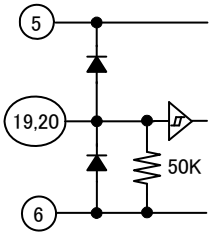
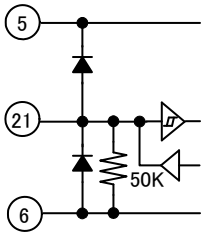
Fig.19
Crosstalk - Frequency

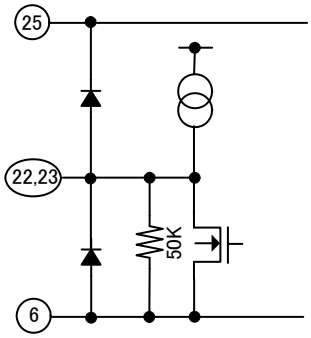
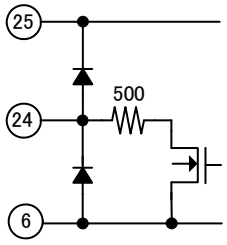
●Pin configuration and Block diagram

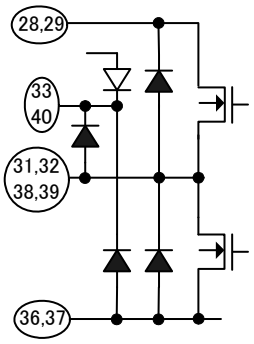
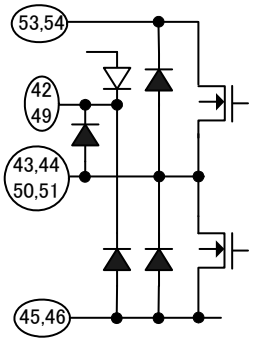


●Pin function explanation (Provided pin voltages are typ. Values)

No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
1 27	REG_G1 REG_G2	5.5V	Internal power supply pin for ch1 Gate driver Internal power supply pin for ch2 Gate driver Please connect the capacitor.	
2	FILP	1.75V~2.55V	Bias pin for PWM signal Please connect the capacitor.	
3	PLMT	0V	Power limiter setting terminal	
4	FILA	2.5V	Bias pin for Analog signal Please connect the capacitor.	
5	REG3	3.3V	Internal power supply pin for Digital circuit Please connect the capacitor.	
6	GNDA	0V	GND pin for Analog signal	—

No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
7 8 9 10 11	SYS_CLK BCLK LRCLK SDATA1 SDATA2	0V	Digital audio signal input pin	
12	RESETX	0V	Reset pin for Digital circuit H: Reset OFF L: Reset ON	
13	MUTEX		Speaker output mute control pin H: Mute OFF L: Mute ON	
14	PDX		Power down control pin H: Power down OFF L: Power down ON	
15	IIS_LJ	0V	Digital audio signal data format setting terminal H: Left Justified format L: I^2S format	
16 17 18	GAIN1 GAIN2 GAIN3	0V	Gain setting terminal Gain=20dB~34dB, 2dB step	
19 20	TEST1 TEST2	0V	Test pin Please connect to GND.	
21	SEL_DAC	0V	DAC output selection terminal H: SDATA2 is output from the DAC L: SDATA1 is output from the DAC	

No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
22 23	OUT_DAC2 OUT_DAC1	2.5V	ch2 DAC output pin ch1 DAC output pin Please connect it with the latter part circuit through the capacitor.	
24	ERROR	3.3V	Error flag pin Please connect pull-up resistor. H: While Normal L: While Error	
25	VCCA	VCC	Power supply pin for Analog signal	—
26,30 34,35 41,47 48,52	N.C.	—	Non connection pin	—

No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
28,29	VCCP2	Vcc	Power supply pin for ch2 PWM signal	
31,32	OUT2P	Vcc~0V	Output pin of ch2 positive PWM Please connect to Output LPF.	
33	BSP2P	—	Boot-strap pin of ch2 positive Please connect the capacitor.	
36,37	GNDP2	0V	GND pin for ch2 PWM signal	
38,39	OUT2N	Vcc~0V	Output pin of ch2 negative PWM Please connect to Output LPF.	
40	BSP2N	—	Boot-strap pin of ch2 negative Please connect the capacitor.	
42	BSP1N	—	Boot-strap pin of ch1 negative Please connect the capacitor.	
43,44	OUT1N	Vcc~0V	Output pin of ch1 negative PWM Please connect to Output LPF.	
45,46	GNDP1	0V	GND pin for ch1 PWM signal	
49	BSP1P	—	Boot-strap pin of ch1 positive Please connect the capacitor.	
50,51	OUT1P	Vcc~0V	Output pin of ch1 positive PWM Please connect to Output LPF.	
53,54	VCCP1	—	Power supply pin for ch1 PWM signal	

●GAIN1 pin, GAIN2 pin, GAIN3 pin function

GAIN3 (18pin)	GAIN2 (17pin)	GAIN1 (16pin)	Speaker output gain
L	L	L	20dB
L	L	H	22dB
L	H	L	24dB
L	H	H	26dB
H	L	L	28dB
H	L	H	30dB
H	H	L	32dB
H	H	H	34dB

●SEL_DAC pin function

SEL_DAC (21pin)	OUT_DAC1 (23pin)	OUT_DAC2 (24pin)
L	The Lch signal of SDATA1 is output	The Rch signal of SDATA1 is output
H	The Lch signal of SDATA2 is output	The Rch signal of SDATA2 is output

●RESETX pin function

RESETX (10pin)	State of Digital block
L	Reset ON
H	Reset OFF

●RESETX pin

RESETX (12pin)	State of Digital block
L	Reset ON
H	Reset OFF

●PDX pin,MUTEX pin function

PDX (12pin)	MUTEX (11pin)	Power Down	DAC output (24,25pin)	PWM output (33,34,38,39,43,44,48pin)
L	L or H	ON	HiZ_Low	HiZ_Low
H	L	OFF	Normal operation	
H	H			Normal operation

●IIS_LJ pin function

IIS_LJ (15pin)	Digital data format
L	I2S
H	Left Justified

●Input digital audio signal sampling frequency (fs) explanation

PWM sampling frequency, Soft-start, Soft-mute time, and the detection time of the DC voltage protection in the speaker depends on sampling frequency (fs) of the digital audio input.

Sampling frequency of the digital audio input (fs)	PWM sampling frequency (fpwm)	Soft-start / Soft-mute time	DC voltage protection in the speaker detection time
32kHz	512kHz	64msec.	64msec.
44.1kHz	705.6kHz	46msec.	46msec.
48kHz	768kHz	43msec.	43msec.

●For voltage gain (Gain setting)

BD5446EFV prescribe voltage gain at speaker output (BTL output) under the definition 0dBV (1Vrms) as full scale input of the digital audio input signal. For example, digital audio input signal = Full scale input, Gain setting = 20dB, Load resistance R_{L_SP} = 8Ω will give speaker output (BTL output) amplitude as Vo=10Vrms. (Output power Po = Vo^2/R_{L_SP} = 12.5W)

●Speaker output and DAC output

Digital audio input signal SDATA1 will be output to the speaker. (SDATA2 will not be output to the speaker. DAC output can be selected either from digital audio input signal SDATA1 or SDATA2.)

●Format of digital audio input

・SYS_CLK: It is System Clock input signal.
It will input LRCLK, BCLK, SDATA1 (SDATA2) that synchronizes with this clock that are 256 times of sampling frequency (256fs).

・LRCLK: It is L/R clock input signal.
It corresponds to 32kHz/44.1kHz/48kHz with those clock (fs) that are same to the sampling frequency (fs) .
The data of a left channel and a right channel for one sample is input to this section.

・BCLK: It is Bit Clock input signal.
It is used for the latch of data in every one bit by sampling frequency's 64 times sampling frequency (64fs).

・SDATA1 & SDATA2: It is Data input signal.
It is amplitude data. The data length is different according to the resolution of the input digital audio data.
It corresponds to 16/ 20/ 24 bit.

●I²S data format

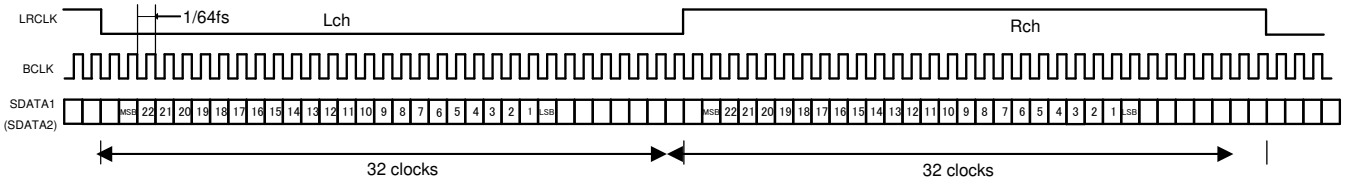


Fig.20 I²S Data Format 64fs, 24 bit Data

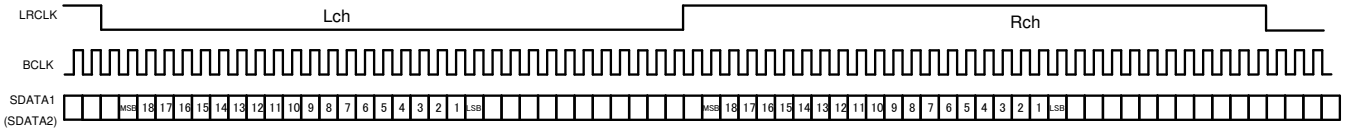


Fig.21 I²S Data Format 64fs, 20 bit Data

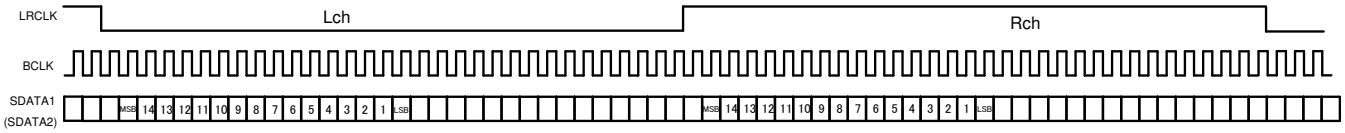


Fig.22 I²S Data Format 64fs, 16 bit Data

The Low section of LRCLK becomes Lch, the High section of LRCLK becomes Rch.
After changing LRCLK, second bit becomes MSB.

●Left-justified format

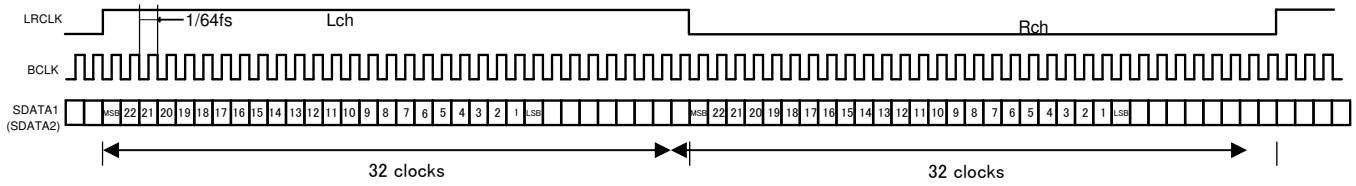


Fig.23 Left-Justified Data Format 64fs, 24 bit Data

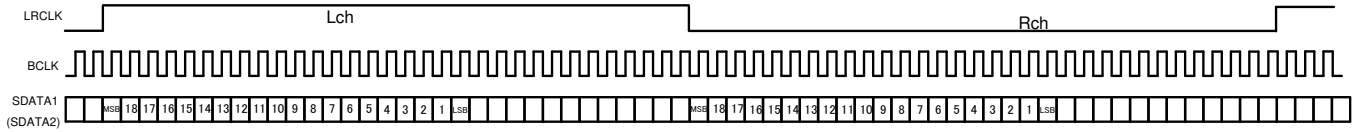


Fig.24 Left-Justified Data Format 64fs, 20 bit Data

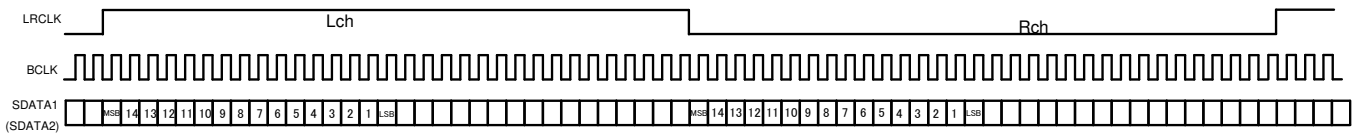


Fig.25 Left-Justified Data Format 64fs, 16 bit Data

The High section of LRCLK becomes Lch, the Low section of LRCLK becomes Rch.
After changing LRCLK, first bit becomes MSB.

●Audio Interface format and timing

Recommended timing and operating conditions (MCLK, BCLK, LRCLK, SDATA)

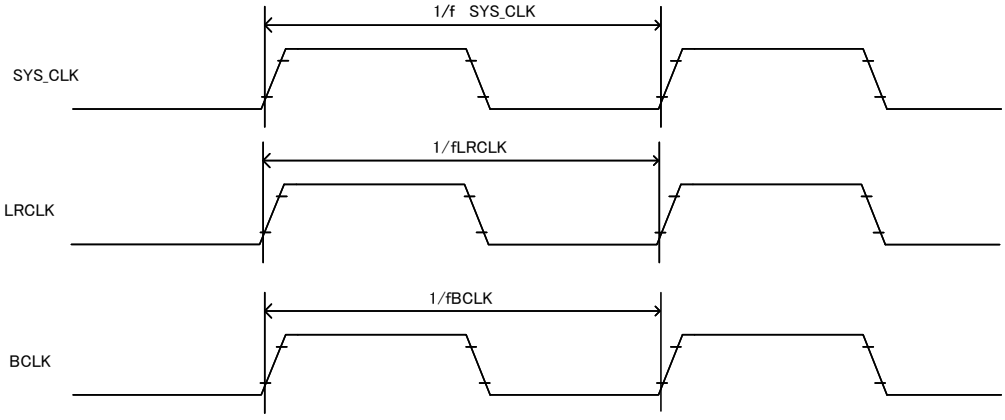


Fig-26 Clock timing

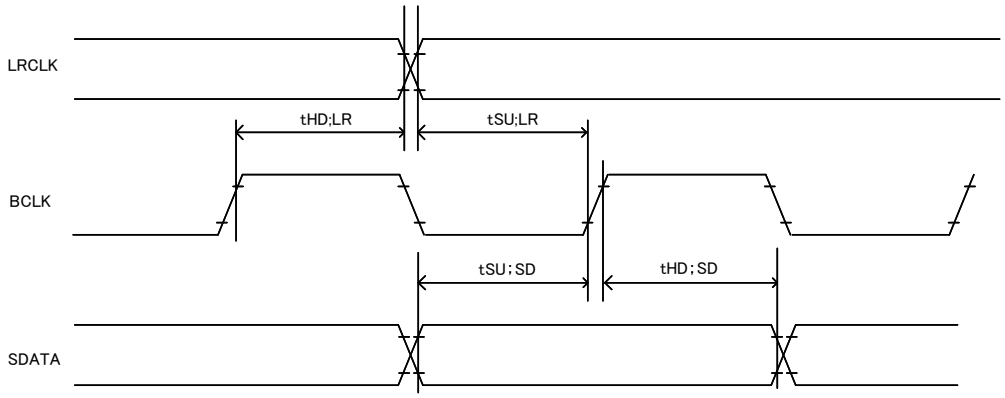


Fig-27 Audio Interface timing (1)

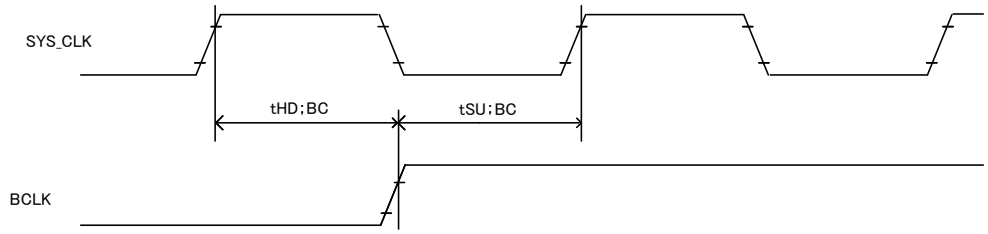


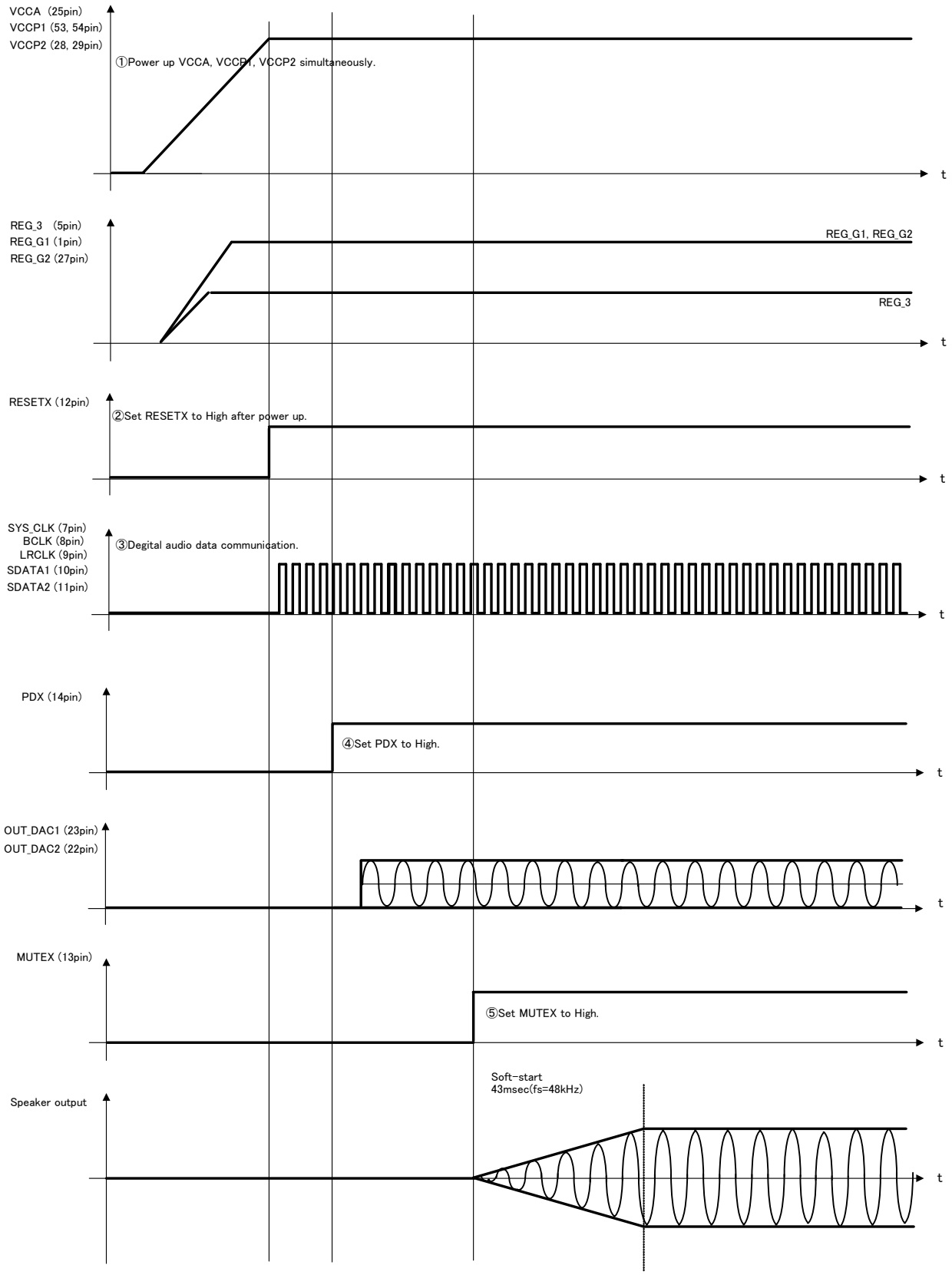
Fig-28 Audio Interface timing (2)

Parameter		Symbol	Limit		Unit
			Min.	Max.	
1	SYS_CLK frequency	fSYS_CLK	8.192	12.288	MHz
2	LRCLK frequency	fLRCLK	32	48	kHz
3	BCLK frequency	fBCLK	2.048	3.072	MHz
4	Setup time, LRCLK※1	tSU;LR	20	−	ns
5	Hold time, LRCLK※1	tHD;LR	20	−	ns
6	Setup time, SDATA	tSU;SD	20	−	ns
7	Hold time, SDATA	tHD;SD	20	−	ns
8	Setup time, BCLK※2	tSU;BC	2.5	−	ns
9	Hold time, BCLK※2	tHD;BC	3.5	−	ns

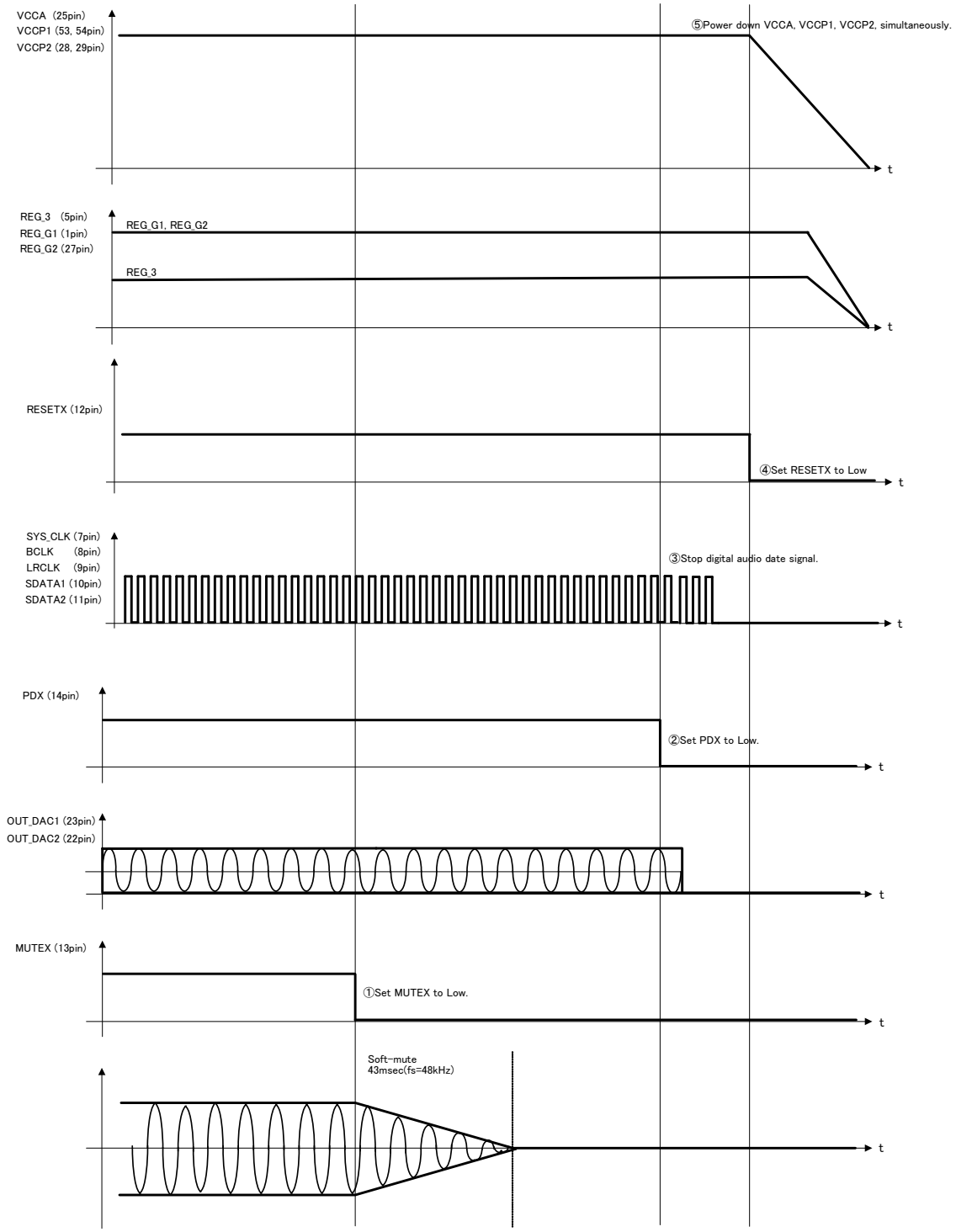
※1 This regulation is to keep rising edge of LRCK and rising edge of BCLK from overlapping.

※2 This regulation is to keep rising edge of SYS_CLK and rising edge of BCLK from overlapping.

●Power supply start-up sequence



●Power supply shut-down sequence



●About the protection function

Protection function	Detecting & Releasing condition		DAC Output	PWM Output	ERROR Output
Output short protection	Detecting condition	Detecting current = 10A (TYP.)	Normal operation	HiZ_Low (Latch)	L (Latch)
DC voltage protection in the speaker	Detecting condition	PWM output Duty=0% or 100% 43msec(fs=48kHz) above fixed		HiZ_Low (Latch)	L (Latch)
High temperature protection	Detecting condition	Chip temperature to be above 150℃ (TYP.)	Normal operation	HiZ_Low	H
	Releasing condition	Chip temperature to be below 120℃ (TYP.)		Normal operation	
Under voltage protection	Detecting condition	Power supply voltage to be below 8V (TYP.)	Normal operation	HiZ_Low	H
	Releasing condition	Power supply voltage to be above 9V (TYP.)		Normal operation	
Clock stop protection	Detecting condition	No change to SYS_CLK more than 1usec (TYP.)	Irregular output	HiZ_Low	H
	Releasing condition	Normal input to SYS_CLK	Normal operation	Normal operation	

∗ The ERROR pin is Nch open-drain output.

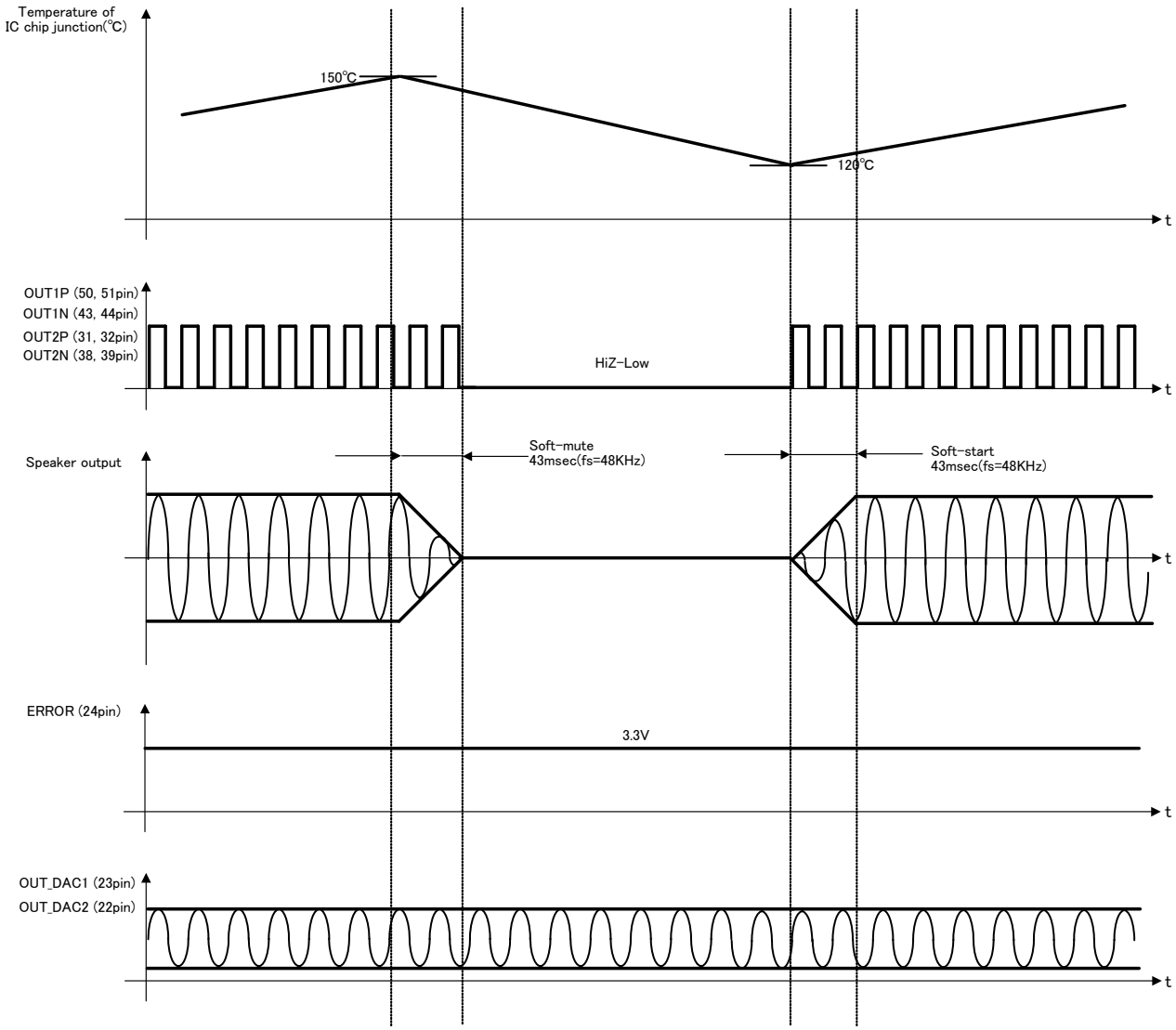
∗ Once an IC is latched, the circuit is not released automatically even after an abnormal status is removed.
The following procedures ① or ② is available for recovery.
①After the MUTEX pin is made Low once, the MUTEX pin is returned to High again.
②Turning on the power supply again.

1) High temperature protection

This IC has the high temperature protection circuit that prevents thermal reckless driving under an abnormal state for the temperature of the chip to exceed Tjmax=150℃.

Detecting condition - It will detect when MUTE pin is set High and the temperature of the chip becomes 150℃(TYP.) or more. The speaker output is muted through a soft-mute when detected.

Releasing condition - It will release when MUTE pin is set High and the temperature of the chip becomes 120℃(TYP.) or less. The speaker output is outputted through a soft-start when released.

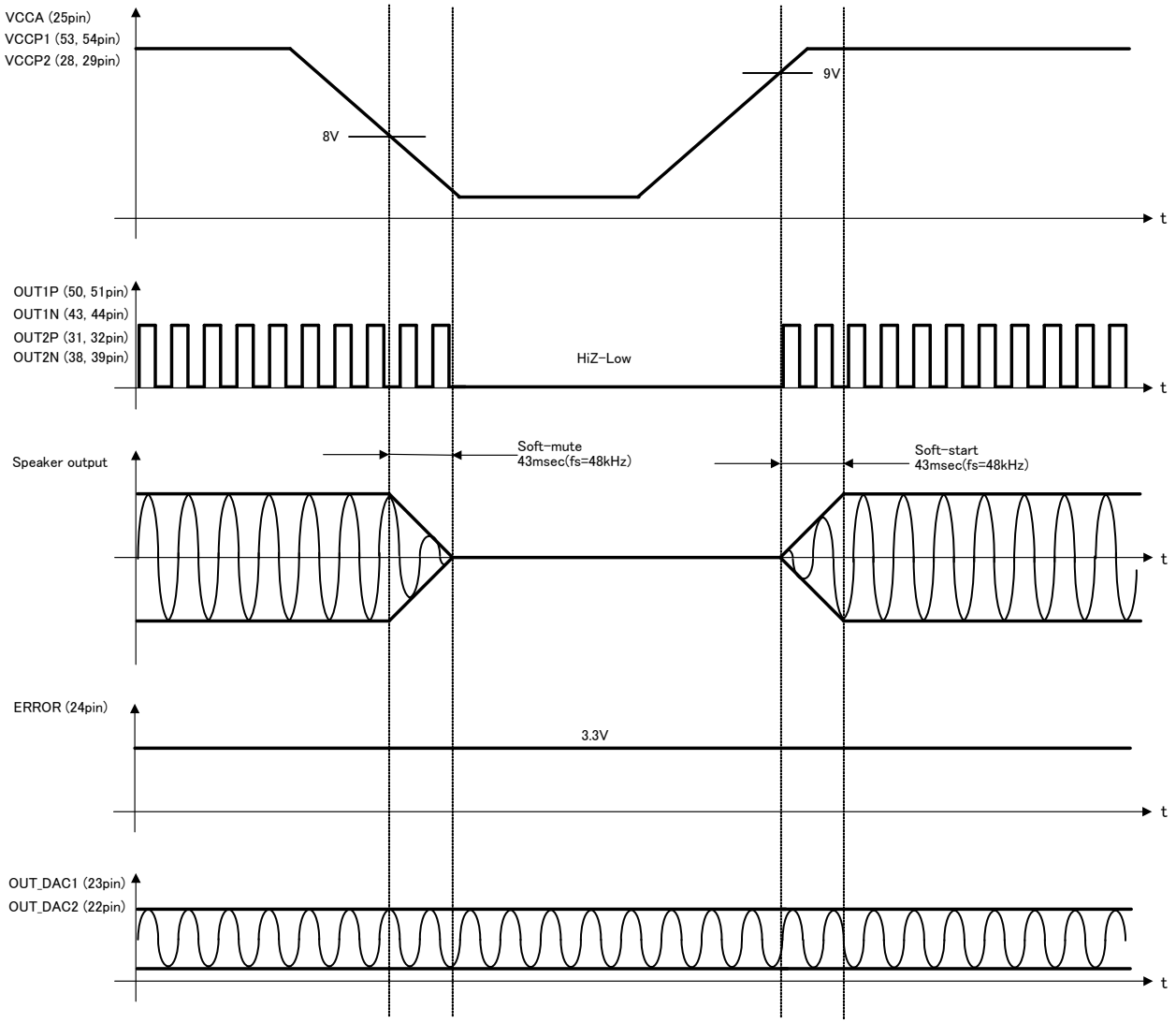


2) Under voltage protection

This IC has the under voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition – It will detect when MUTE pin is set High and the power supply voltage becomes lower than 8V. The speaker output is muted through a soft-mute when detected.

Releasing condition – It will release when MUTE pin is set High and the power supply voltage becomes more than 9V. The speaker output is outputted through a soft-start when released.

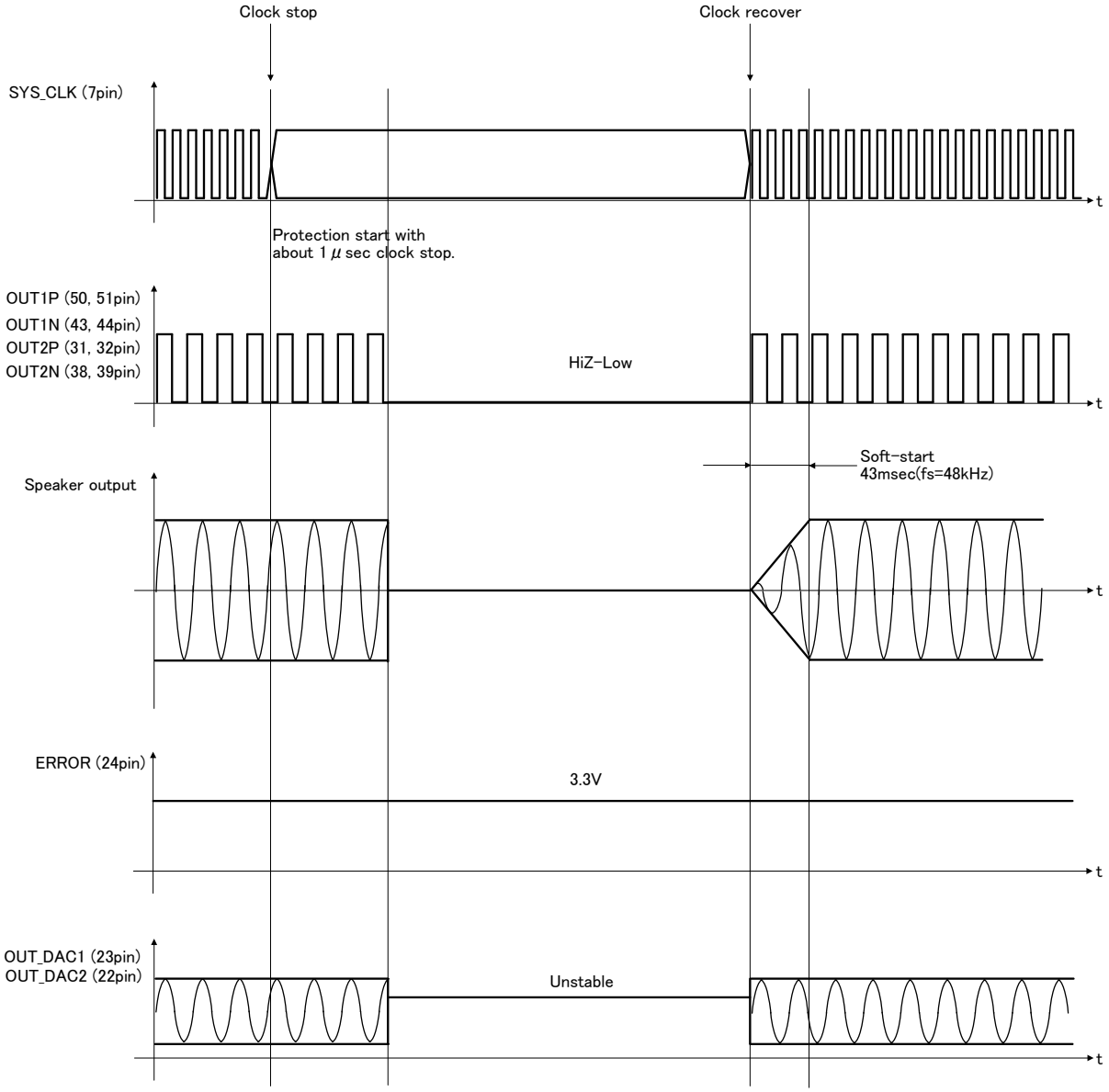


3) Clock stop protection

This IC has the clock stop protection circuit that make the speaker output mute when the SYS_CLK signal of the digital audio input stops.

Detecting condition - It will detect when MUTE pin is set High and the SYS_CLK signal stops for about 1usec or more. The speaker output is muted through a soft-mute when detected.

Releasing condition - It will release when MUTE pin is set High and the SYS_CLK signal returns to the normal clock operation. The speaker output is outputted through a soft-start when released.

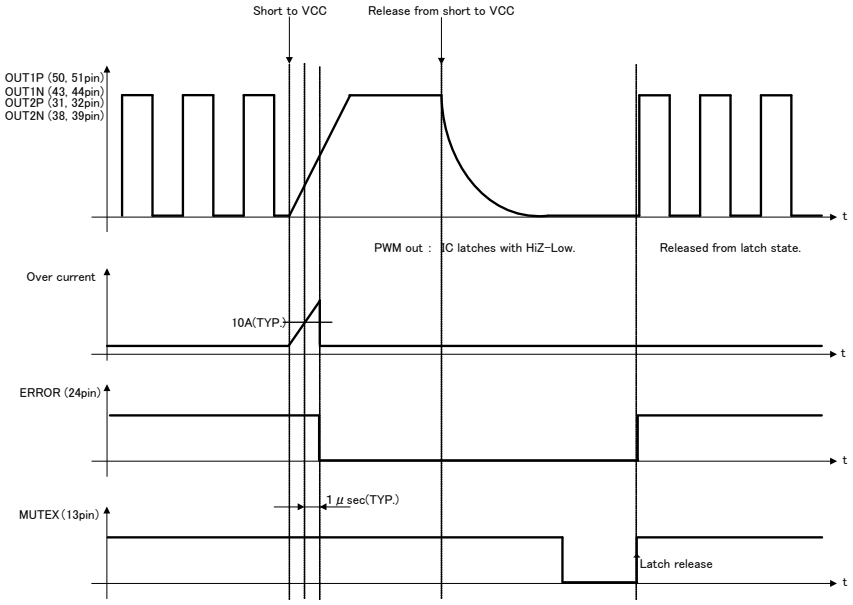


4)Output short protection(Short to the power supply)

This IC has the PWM output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTE pin is set High and the current that flows in the PWM output pin becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After the MUTEX pin is set Low once, the MUTEX pin is set High again.
②Turning on the power supply again.

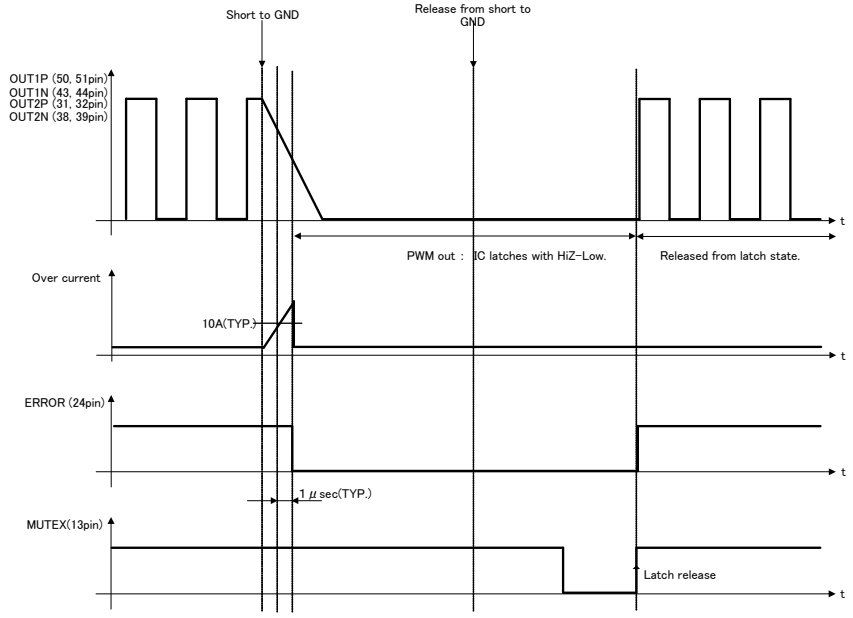


5) Output short protection(Short to GND)

This IC has the PWM output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTE pin is set High and the current that flows in the PWM output terminal becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method – ①After the MUTEX pin is set Low once, the MUTEX pin is set High again.
②Turning on the power supply again.

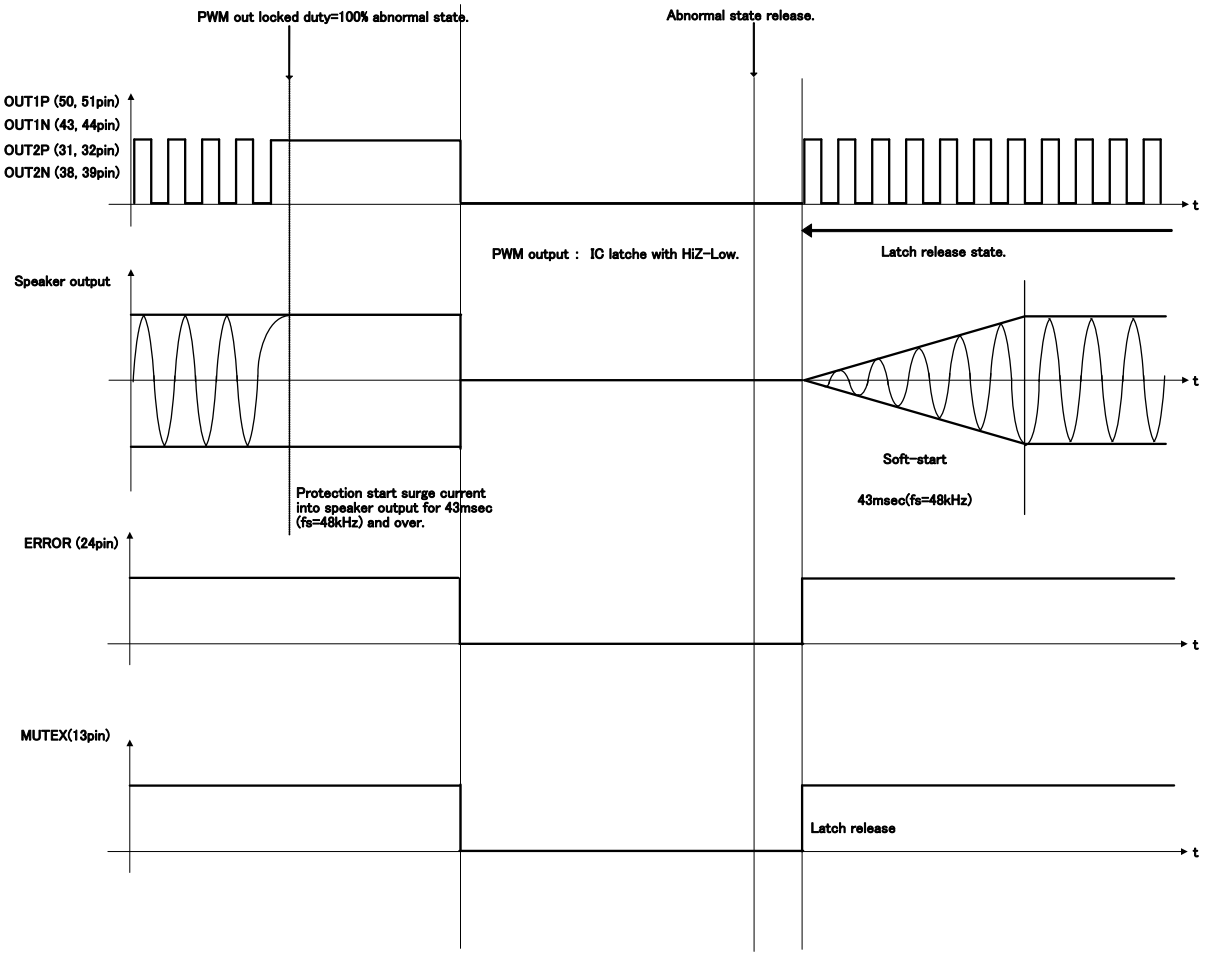


6) DC voltage protection in the speaker

When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.

Detecting condition - It will detect when MUTE pin is set High or Low and PWM output Duty=0% or 100% , 43msec(fs=48kHz) or above. Once detected, The PWM output instantaneously enters the state of HiZ-Low, and IC does the latch.

Releasing method – ①After the MUTEX pin is set Low once, the MUTEX pin is set High again.
②Turning on the power supply again



●Output power limiter function

This IC is provided with an output power limiter function to protect speakers from destruction by an excessive output. Limiter values are freely specified by changing external resistors R1/R2 as shown in Fig-26. Fig-27 shows a speaker output waveform that is generated with use of the output limiter function. Because the waveform is soft-clipped, unusual noises on audible signals are significantly reduced under operation of limiter.

Use resistors with a high degree of accuracy for R1 and R2 (±1% or higher accuracy is recommended). The capacitor C is for the noise removal of output power limitation terminal (3pin). Provide grounding with a 1µF capacitor. Specify a resistor of 10kΩ or higher resistor R1 and R2. If the output power limiter function is not used, R1, R2 and C is unnecessary. However, connect 3pin with GNDA.

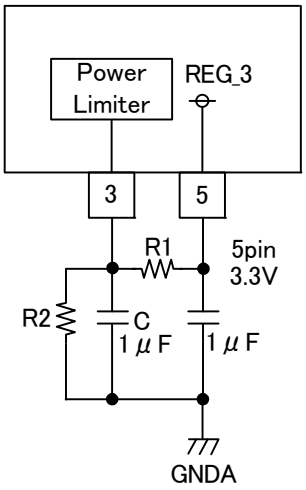


Fig-29

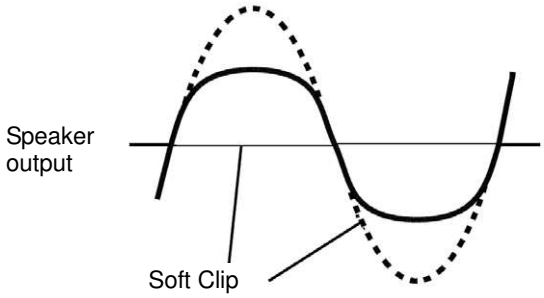


Fig-30

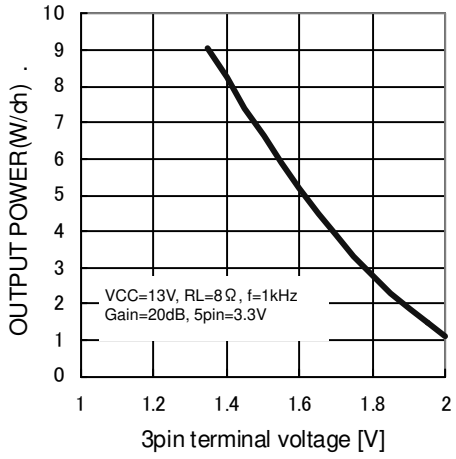
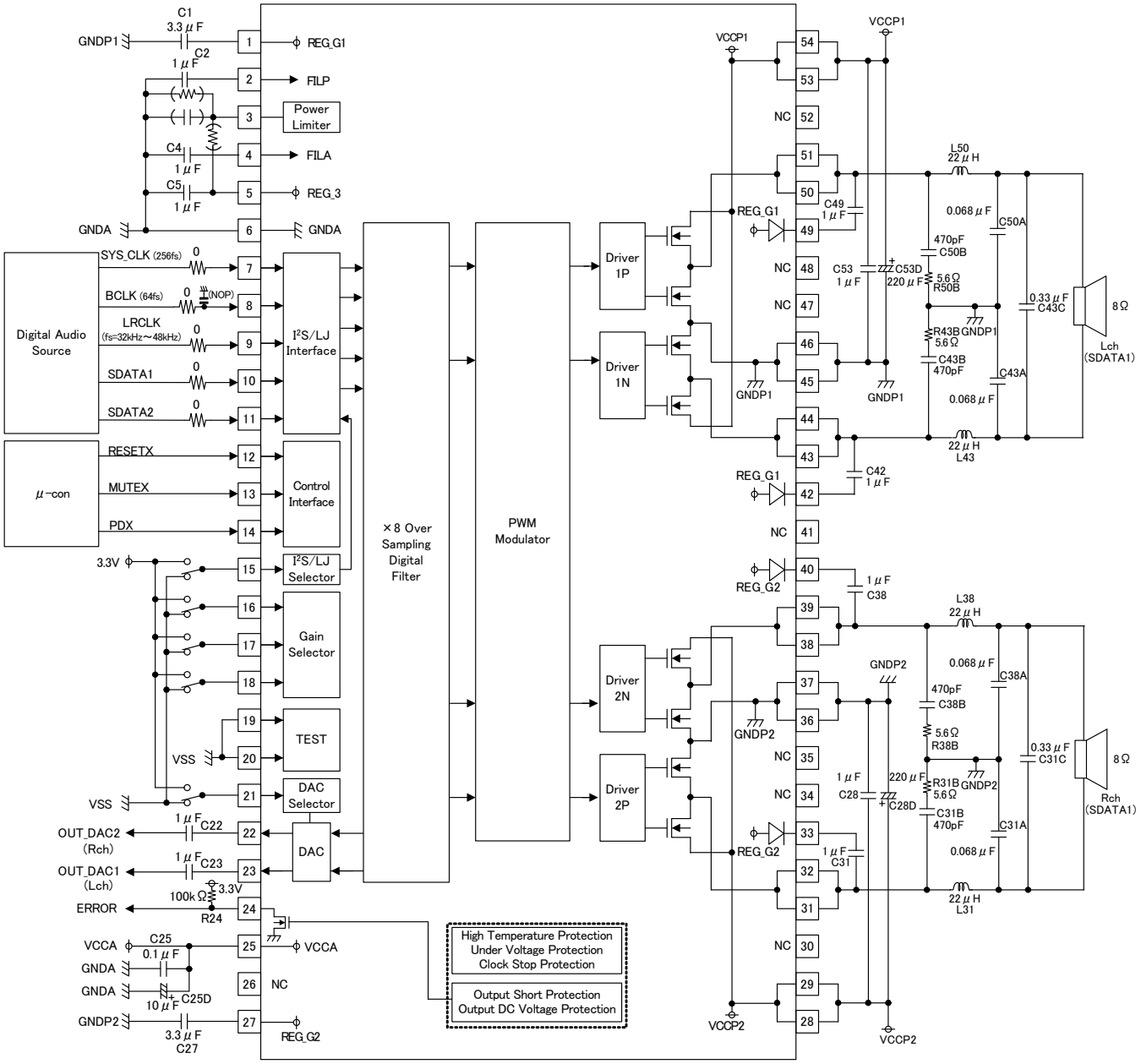


Fig.31

Output power
– 3pin terminal voltage

●Application Circuit Example(R_{L_SP}=8Ω)



●BOM list(R_{L_SP}=8Ω)

Parts	Parts No.	Value	Company	Product No.	Rated Voltage	Tolerance	Size
IC	U1	—	ROHM	BD5446EFV	—	—	18.5mm×9.5mm
Inductor	L31, L38, L43, L50	22μH	TOKO	1168ER-0001	-	(±20%)	10.3mm×7.6mm
			SAGAMI	DBE7210H-220M	-	(±20%)	10.5mm×6.4mm
Resistor	R31B, R38B R43B, R50B	5.6Ω	ROHM	MCR18PZHZFL5R60	1/4W	F(±1%)	3.2mm×1.6mm
Capacitor	C31, C38, C42, C49	1μF	MURATA	GRM185B31C105KE43	16V	B(±10%)	1.6mm×0.8mm
	C25, C28, C53	0.1μF		GRM188B31H104KA92	50V	B(±10%)	1.6mm×0.8mm
	C31A, C38A C43A, C50A	0.068μF		GRM21BB11H683KA01	50V	B(±10%)	2.0mm×1.25mm
	C31C, C43C	0.33μF		GRM219B31H334KA87	50V	B(±10%)	2.0mm×1.25mm
	C1, C27	3.3μF		GRM188B31A335KE15	10V	B(±10%)	1.6mm×0.8mm
	C2, C4, C5 C22, C23	1μF		GRM185B30J105KE25	6.3V	B(±10%)	1.6mm×0.8mm
	C31B, C38B C43B, C50B	470pF		GRM188B11H471KA	50V	B(±10%)	2.0mm×1.2mm
Electrolytic Capacitor	C28D, C53D	220μF	Panasonic	ECA1VMH221	35V	±20%	φ8mm×11.5mm
	C25D	10μF		EEUFC1H100L	50V	±20%	φ5mm×11mm