Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Middle Power Class-D Speaker Amplifier series

15W+15W
Class D Speaker Amplifier for Digital Input

BD5452AMUV

●General Description

BD5452AMUV is a Class D Speaker Amplifier designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of 15W+15W. This IC employs state-of-the-art Bipolar, CMOS, and DMOS (BCD) process technology. With this technology, the IC can achieve high efficiency. In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 30W. This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

●Features

- This IC has one system of digital audio interface.(I2S format, SDATA: 16 / 20 / 24bit, LRCLK: 32kHz / 44.1kHz / 48kHz, BCLK: 64fs(fixed), MCLK: 256fs / 512fs)
- Low supply current at RESET mode.
- The decrease in sound quality because of the change of the power supply voltage is prevented with the feedback circuitry of the output. In addition, a low noise and low distortion are achieved.
- Eliminate large electrolytic-capacitors for high performance of Power Supply Rejection.
- Power Limit Function. (at RL =8Ω, 10W /5W /OFF)
- Available for Monaural mode.
- Within the wide range of the power supply voltage, it is possible to operate in a single power supply. (10 to 18V)
- It contributes to miniaturizing, making to the thin type, and the power saving of the system by high efficiency and low heat.
- Eliminates pop noise generated when the power supply goes on/off, or when the power supply is suddenly shut off. High quality muting performance is realized by using the soft-muting technology.
- This IC is a highly reliable design to which it has various protection functions. (High temperature protection, under voltage protection, Output short protection, Output DC voltage protection and Clock stop protection, (MCLK, BCLK, LRCLK)
- Small package (VQFN032V5050 package) contributes to reduction of PCB area.

●Applications

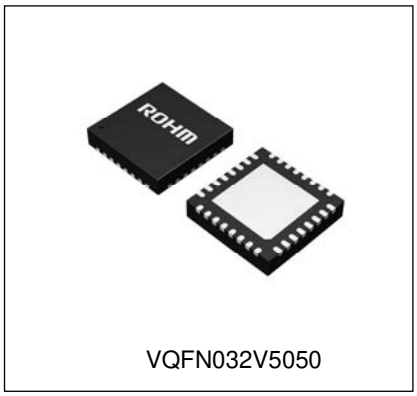
- Flat Panel TVs (LCD, Plasma), Home Audio, Desktop PC, Amusement equipments, Electronic Music equipments, etc.

●Key Specifications

- Supply voltage: 10V to 18V
- Speaker output power: 15W+15W (VCC=16V, RL=8Ω, Power Limit=Off)
- Total harmonic distortion: 0.08%(Po=4.5W)
- Crosstalk: 80dB(Typ.)
- PSRR: 65dB(Typ.)
- Output noise voltage: 100μVrms(Typ.)
- Standby current: 100μA (Typ.)
- Operating temperature range: -25℃ to +85℃

●Package(s)

	W(Typ.) x D(Typ.) x H(Max.)
VQFN032V5050	5.00mm x 5.00mm x 1.00mm



VQFN032V5050

●Typical Application Circuit

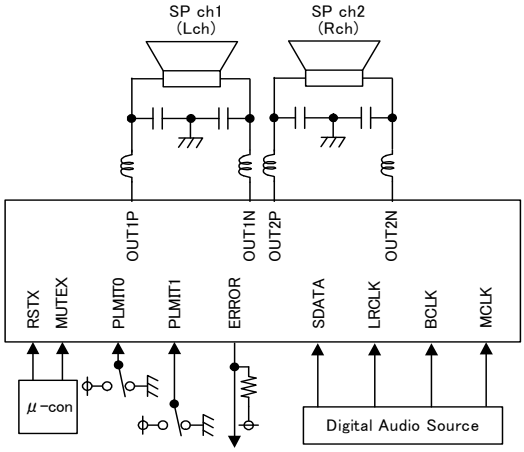


Figure 1. Typical Application Circuit

●Pin Configuration

(TOP VIEW)

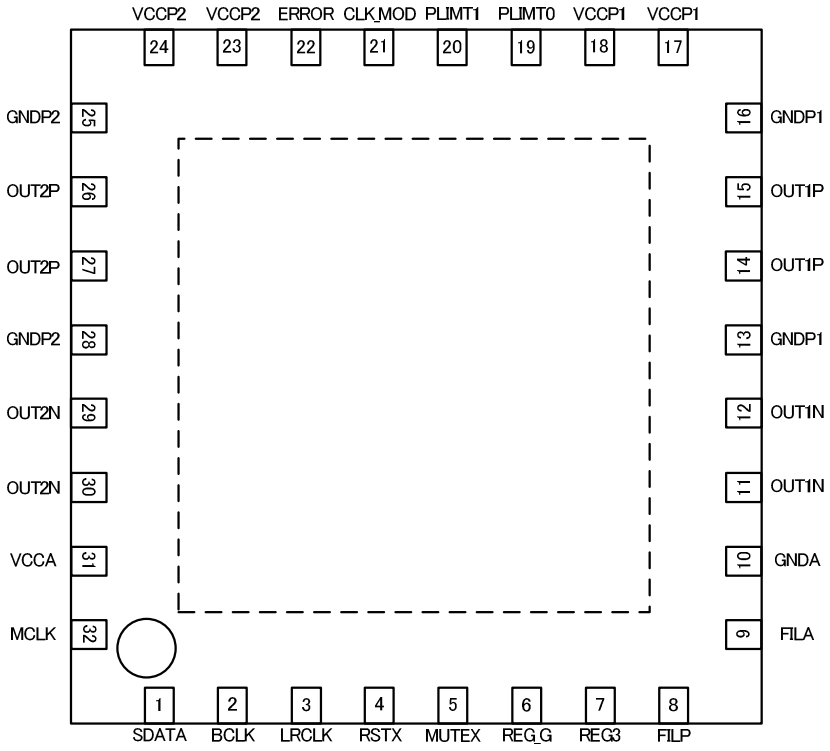


Figure 2. Pin Configuration

●Pin Description

Pin No.	Symbol	I/O	Pin No.	Symbol	I/O	Pin No.	Symbol	I/O	Pin No.	Symbol	I/O
1	SDATA	I	9	FILA	O	17	VCCP1	I	25	GNDP2	-
2	BCLK	I	10	GNDA	-	18		I	26	OUT2P	O
3	LRCLK	I	11	OUT1N	O	19	PLIMT0	I	27		O
4	RSTX	I	12		O	20	PLIMT1	I	28	GNDP2	-
5	MUTEX	I	13	GNDP1	-	21	CLK_MOD	I	29	OUT2N	O
6	REG_G	O	14	OUT1P	O	22	ERROR	O	30		O
7	REG3	O	15		O	23	VCCP2	I	31	VCCA	I
8	FILP	O	16	GNDP1	-	24		I	32	MCLK	I

●**Block Diagram**

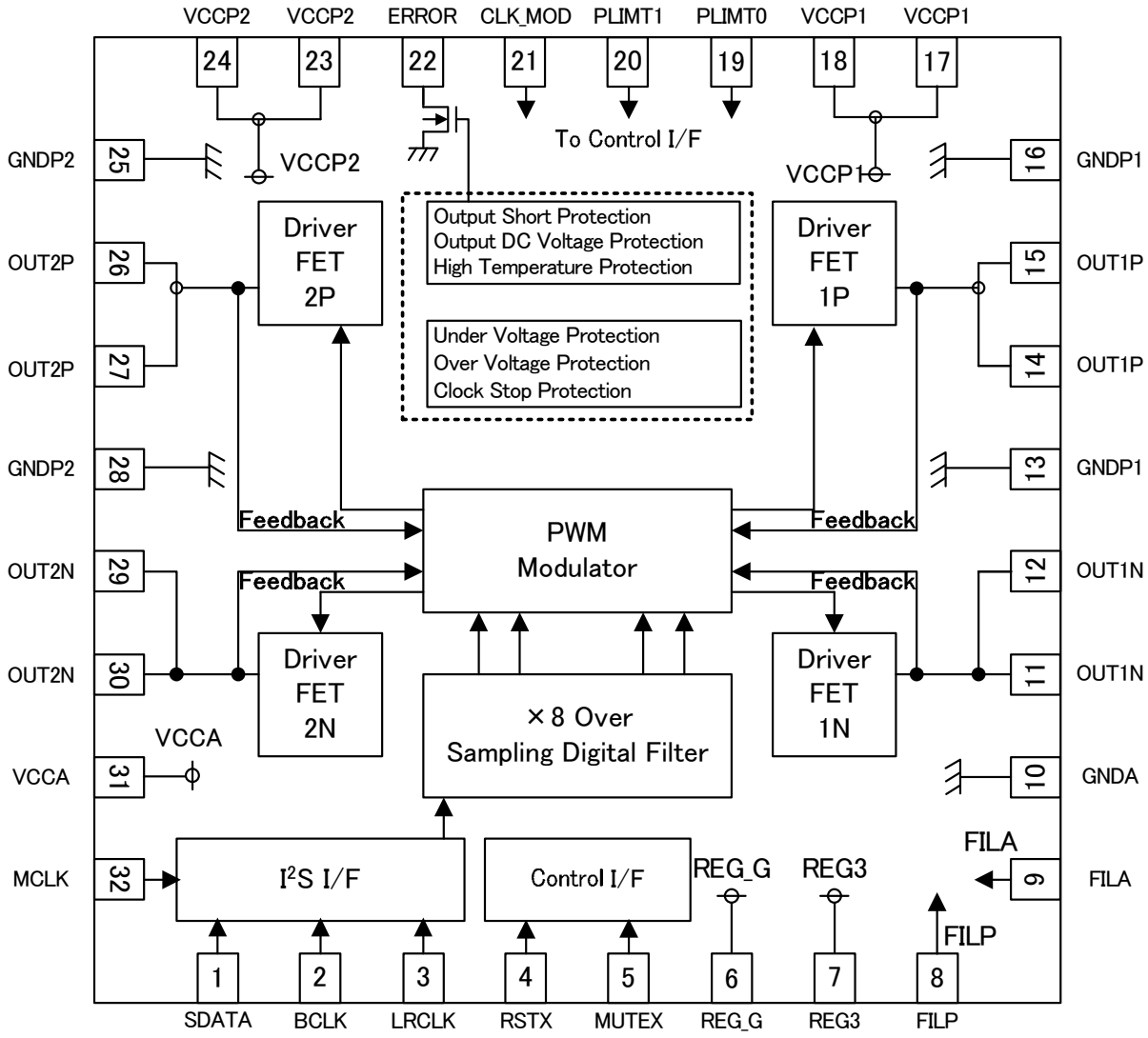


Figure 3. Block Diagram

●Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Conditions
Supply voltage	VCCmax	-0.3 to 22	V	Pin 17,18,23,24,31 ※1 ※2
Power dissipation	Pd	3.26	W	※3
		4.56	W	※4
Input voltage	VIN	-0.3 to 4.5	V	Pin 1 to 5, 19 to 21, 32
Terminal voltage 1	VPIN1	-0.3 to 7.0	V	Pin 6,8,9
Terminal voltage 2	VPIN2	-0.3 to 4.5	V	Pin 7
Terminal voltage 3 ※5	VPIN3	-0.3 to 22	V	Pin 11,12,14,15,26,27,29,30
Open-drain terminal voltage	VERR	-0.3 to 22	V	Pin 22
Operating temperature range	Topr	-25 to +85	℃	
Storage temperature range	Tstg	-55 to +150	℃	
Maximum junction temperature	Tjmax	+150	℃	

※1 The voltage that can be applied reference to GND (Pin 10, 13, 16, 25, 28).
※2 Do not, however exceed Pd and Tjmax=150℃.
※3 74.2mm×74.2mm×1.6mm, FR4, 4-layer glass epoxy board
(Top and bottom layer back copper foil size: 20.2mm^2, 2nd and 3rd layer back copper foil size: 5505mm^2)
Derating in done at 26.1mW/℃ for operating above Ta=25℃. There are thermal via on the board.
※5 (Reference info.) It is confirmed to this terminal to be able to tolerate undershoot within the range of the following Figure 4 with ROHM evaluation board.

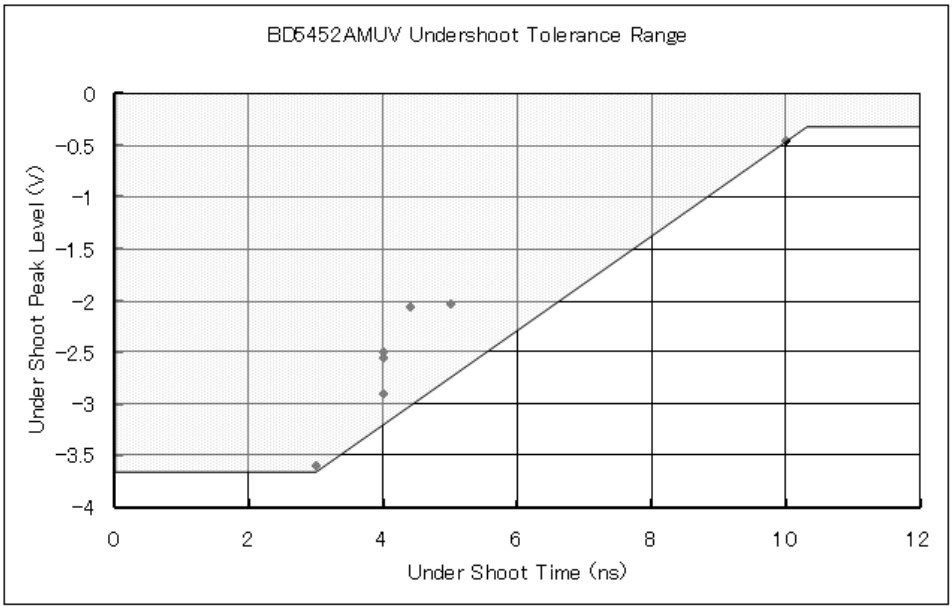


Figure 4. Undershoot Tolerance Range

●Recommended Operating Rating

Item	Symbol	Limit	Unit	Conditions
Supply voltage	Vcc	10 to 18	V	
Minimum load impedance	RL	3.6	Ω	Vcc≦18V
		3.2	Ω	Vcc≦16V

●Electrical Characteristics

（Unless otherwise specified Ta=25℃, Vcc=12V, f=1kHz, RL=8Ω, RSTX=3.3V, MUTEX=3.3V, PLIMT0=L, PLIMT1=L, fs=48kHz, MCLK=256fs, Output LC filter：L=10uH, C=0.1uF）

Item	Symbol	Limit			Unit	Pin Condition
		Min	Typ	Max		
Total circuit						
Circuit current (Reset mode)	ICC1	-	0.1	0.2	mA	No load, RSTX=0V, MUTEX=0V
Circuit current (Mute mode)	ICC2	-	15	25	mA	No load, RSTX=3.3V, MUTEX=0V
Circuit current (Sampling mode)	ICC3	-	50	80	mA	No load, RSTX=3.3V, MUTEX=3.3V
Open-drain terminal Low level voltage	VERR	-	-	0.8	V	Pin22, I_O=0.5mA
Regulator output voltage 1	VREGG	4.7	5.0	5.3	V	Pin6
Regulator output voltage 2	VREG3	3	3.3	3.6	V	Pin7
High level input voltage	VIH	2	-	3.3	V	Pin 1 to 5, 1921, 32
Low level input voltage	VIL	0	-	0.9	V	Pin 1 to 5, 19 to 21, 32
Input current (Input pull-down terminal)	IIH	50	66	95	μA	Pin 1 to 5, 19 to 21, 32, VIN = 3.3V
Speaker Output						
Maximum output power 1	PO1	-	15	-	W	Vcc=16V, THD+n=10%, PLIMT0=L, PLIMT1=L ※6
Maximum output power 2	PO2	10	-	-	W	Vcc=16V, THD+n=10%, PLIMT0=H, PLIMT1=L ※6
Maximum output power 3	PO3	5	-	-	W	Vcc=16V, THD+n=10%, PLIMT0=H, PLIMT1=H ※6
Voltage gain1	GV26	25	26	27	dB	Po=1W, PLIMT0=L, PLIMT1=L ※6
Voltage gain2	GV20	19	20	21	dB	Po=1W, PLIMT0=H, PLIMT1=L ※6
Voltage gain3	GV17	16	17	18	dB	Po=1W, PLIMT0=H, PLIMT1=H ※6
Total harmonic distortion1	THD1	-	0.16	-	%	P_O=1W, BW=20 to 20kHz (AES17) PLIMT0=H, PLIMT1=L ※6
Total harmonic distortion2	THD2	-	0.08	-	%	P_O=4.5W, BW=20 to 20kHz (AES17) PLIMT0=H, PLIMT1=L ※6
Total harmonic distortion3	THD3	-	0.24	0.3	%	P_O=1W, BW=20 to 20kHz (AES17) VCC=15.7V, PLIMT0=H, PLIMT1=L ※6
Crosstalk	CT	60	80	-	dB	P_O=1W, BW=IHF-A PLIMT0=H, PLIMT1=L ※6
PSRR (Sampling mode)	PSRR	-	65	-	dB	Vripple=1Vrms, f=1kHz ※6 PLIMT0=H, PLIMT1=L ※6
Output noise voltage (Sampling mode)	VNO	-	100	200	μVrms	-∞dBFS, BW=IHF-A ※6 PLIMT0=H, PLIMT1=L
PWM sampling frequency	fPWM1	-	256	-	kHz	fs=32kHz ※6
	fPWM2	-	352.8	-	kHz	fs=44.1kHz ※6
	fPWM3	-	384	-	kHz	fs=48kHz ※6

※6 These items show the typical performance of device and depend on board layout, parts, and power supply.
The standard value is in mounting device and parts on surface of ROHM's board directly.

●Typical Performance Curves (Reference) (1/8)

（Unless otherwise specified Ta=25℃, Vcc=12V, f=1kHz, RL=8Ω, RSTX=3.3V, MUTEX=3.3V, PLIMT0=L, PLIMT1=L, fs=48kHz, MCLK=256fs, Output LC filter：L=10uH, C=0.1uF）

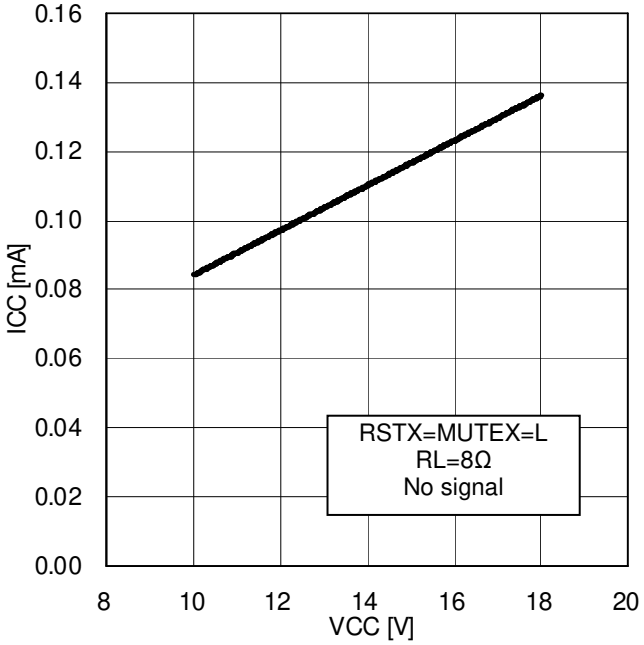


Figure 5. VCC vs. ICC

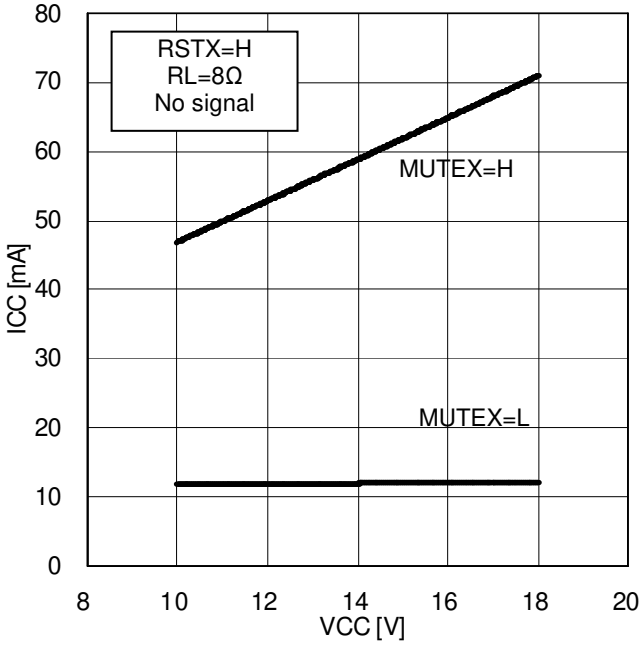


Figure 6. VCC vs. ICC

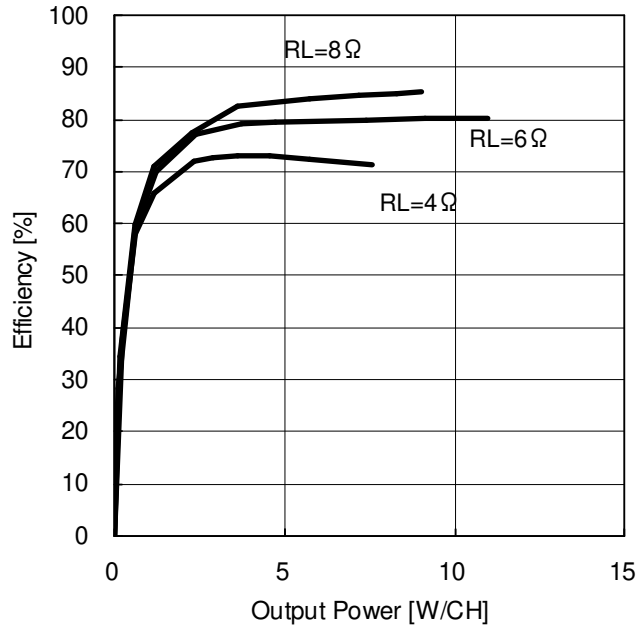


Figure 7. Output Power vs. Efficiency
PLIMT0=L, PLIMT1=L

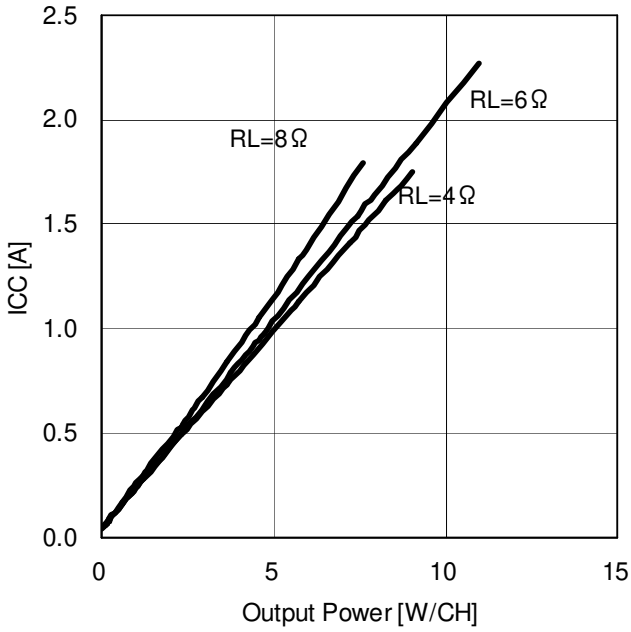


Figure 8. Output Power vs. ICC
PLIMT0=L, PLIMT1=L

●Typical Performance Curves (Reference) (2/8)

（Unless otherwise specified Ta=25℃, Vcc=12V, f=1kHz, RL=8Ω, RSTX=3.3V, MUTEX=3.3V, PLIMT0=L, PLIMT1=L, fs=48kHz, MCLK=256fs, Output LC filter：L=10uH, C=0.1uF）

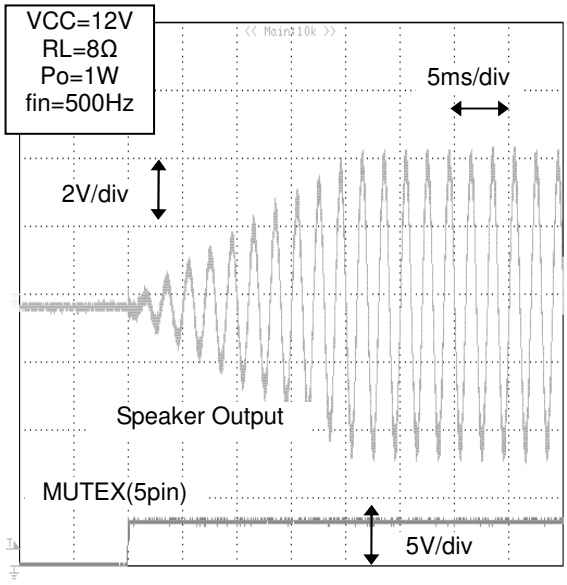


Figure 9. Waveform of Soft Start

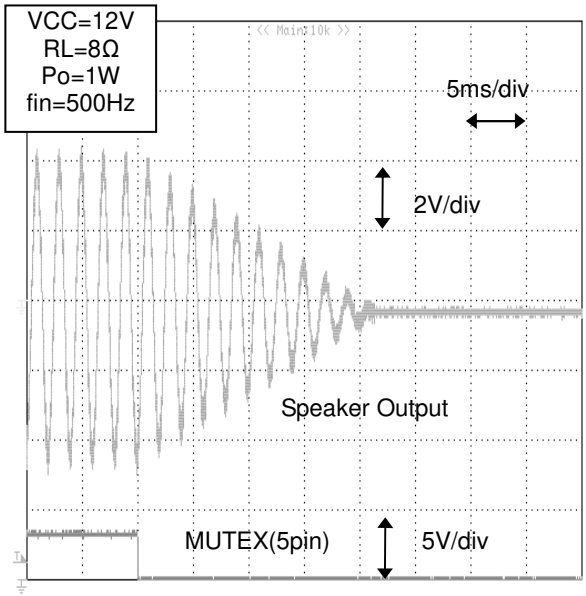


Figure 10. Waveform of Soft Mute

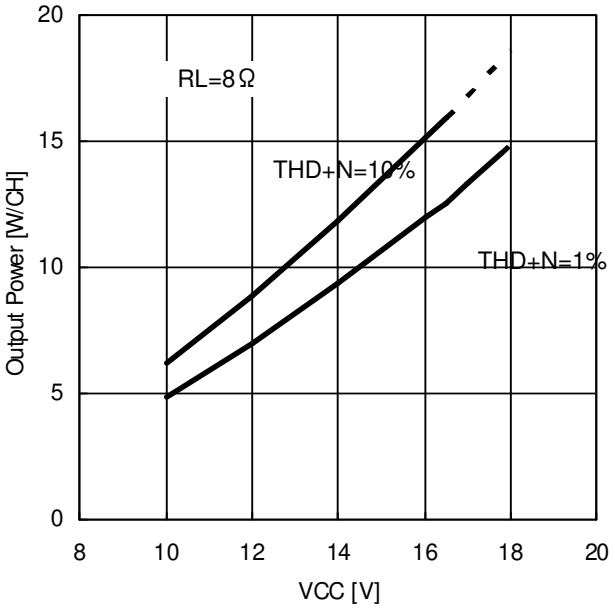


Figure 11. VCC vs. Output Power ※
PLIMT0=L, PLIMT1=L

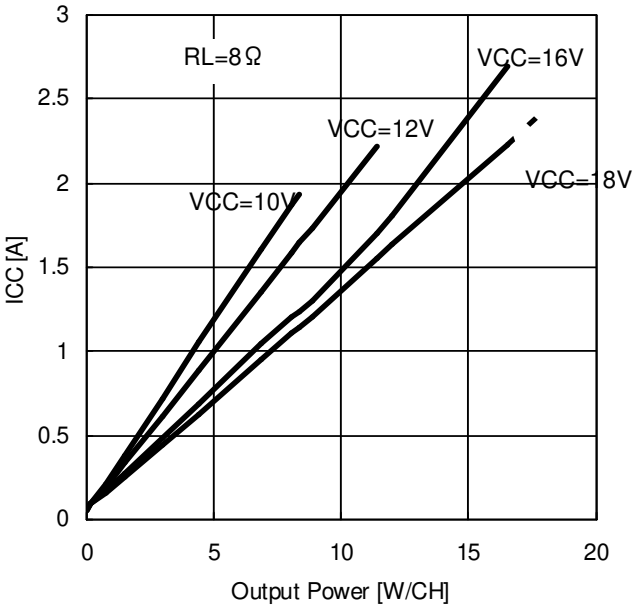


Figure 12. Output Power vs. ICC ※
PLIMT0=L, PLIMT1=L

※ Dotted line means internal dissipation is over package power.

●Typical Performance Curves (Reference) (3/8)

（Unless otherwise specified Ta=25℃, Vcc=12V, f=1kHz, RL=8Ω, RSTX=3.3V, MUTEX=3.3V, PLIMT0=L, PLIMT1=L, fs=48kHz, MCLK=256fs, Output LC filter：L=10uH, C=0.1uF）

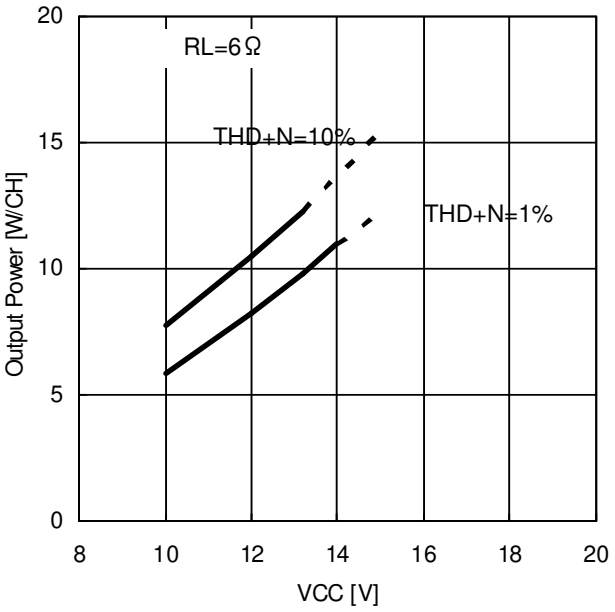


Figure 13. VCC vs. Output Power ※
PLIMT0=L, PLIMT1=L

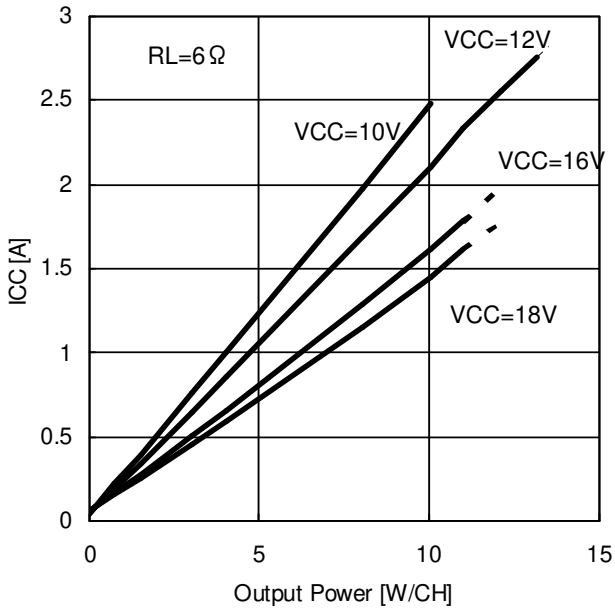


Figure 14. Output Power vs. ICC ※
PLIMT0=L, PLIMT1=L

※ Dotted line means internal dissipation is over package power.

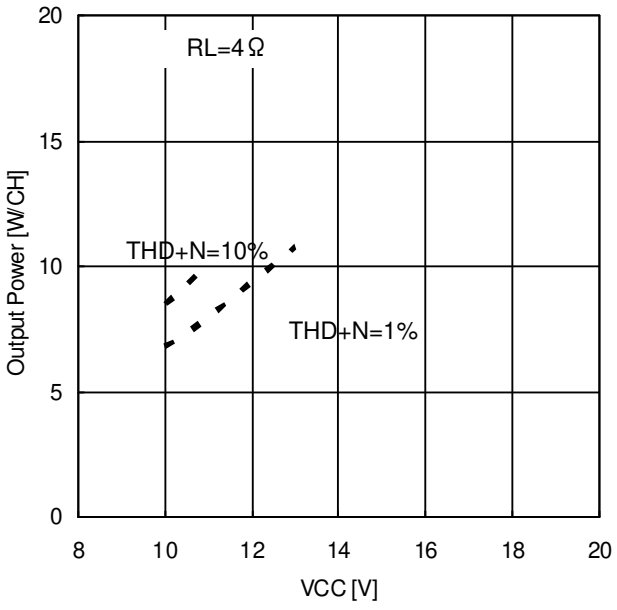


Figure 15. VCC vs. Output Power ※
PLIMT0=L, PLIMT1=L

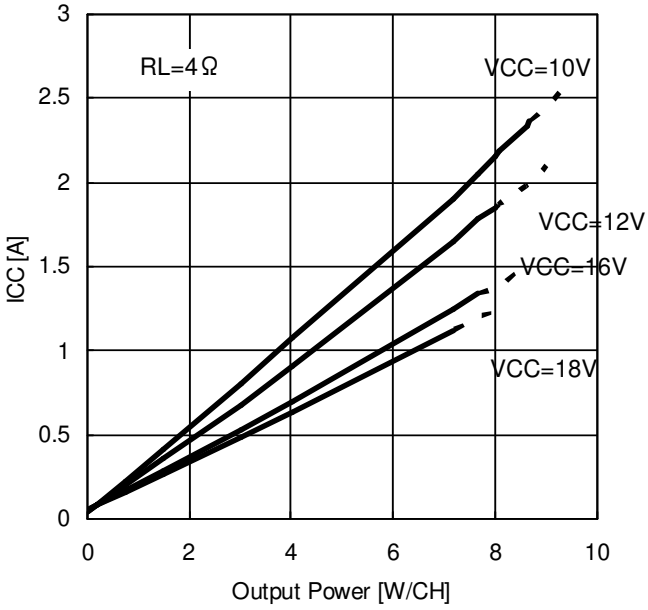


Figure 16. Output Power vs. ICC ※
PLIMT0=L, PLIMT1=L

※ Dotted line means internal dissipation is over package power.

●Typical Performance Curves (Reference) (4/8)

（Unless otherwise specified Ta=25℃, Vcc=12V, f=1kHz, RL=8Ω, RSTX=3.3V, MUTEX=3.3V, PLIMT0=L, PLIMT1=L, fs=48kHz, MCLK=256fs, Output LC filter：L=10uH, C=0.1uF）

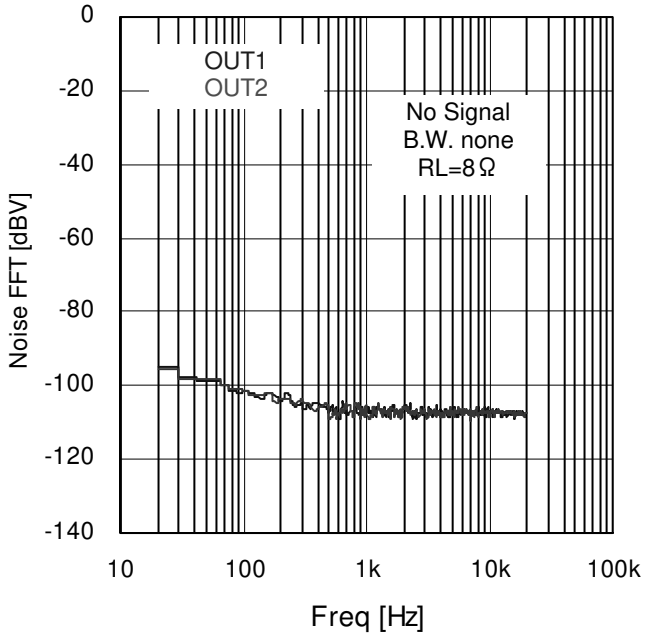


Figure 17. FFT of output noise voltage

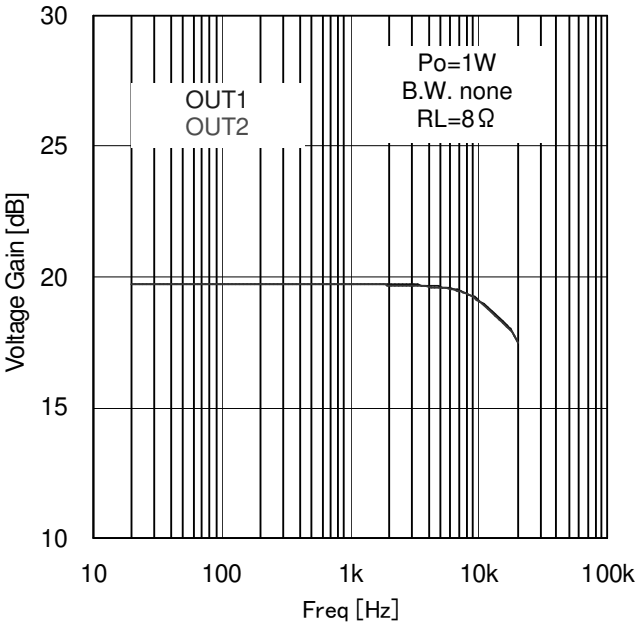


Figure 18. Freq vs. Voltage Gain

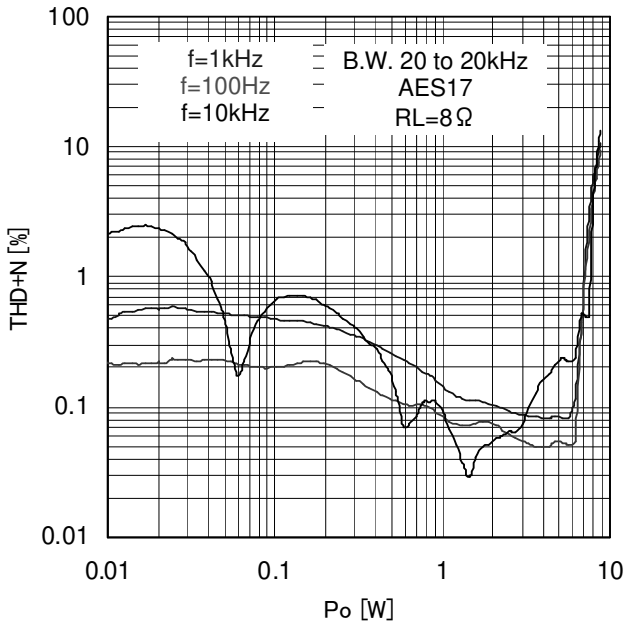


Figure 19. Po vs. THD+N

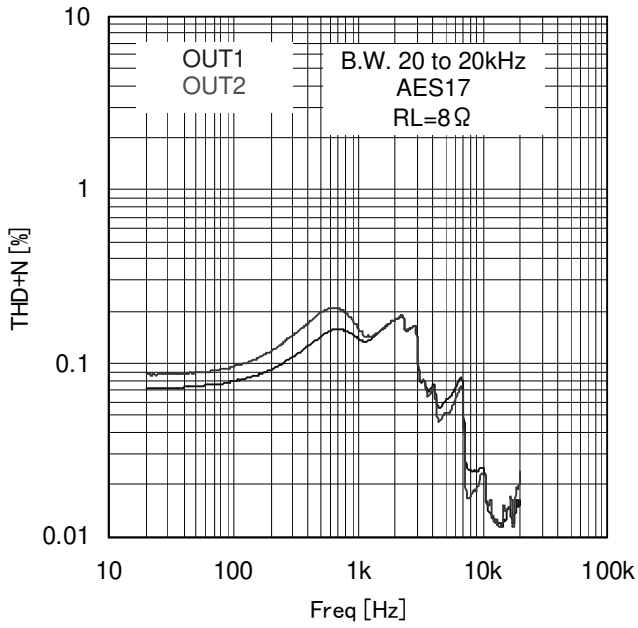


Figure 20. Freq vs. THD+N

●Typical Performance Curves (Reference) (5/8)

（Unless otherwise specified Ta=25℃, Vcc=12V, f=1kHz, RL=8Ω, RSTX=3.3V, MUTEX=3.3V, PLIMT0=L, PLIMT1=L, fs=48kHz, MCLK=256fs, Output LC filter：L=10uH, C=0.1uF）

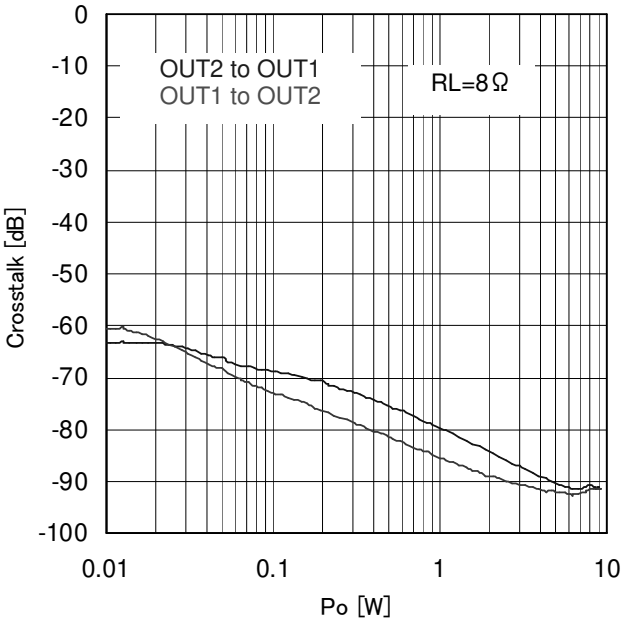


Figure 21. Po vs. Crosstalk

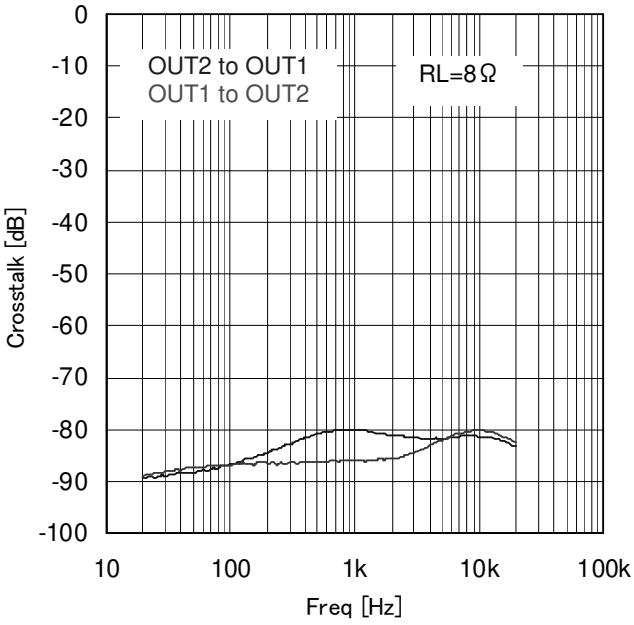


Figure 22. Freq vs. Crosstalk

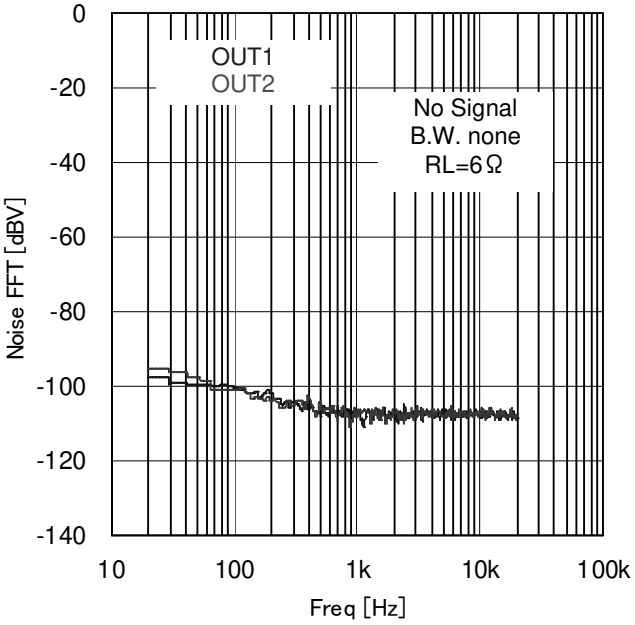


Figure 23. FFT of output noise voltage

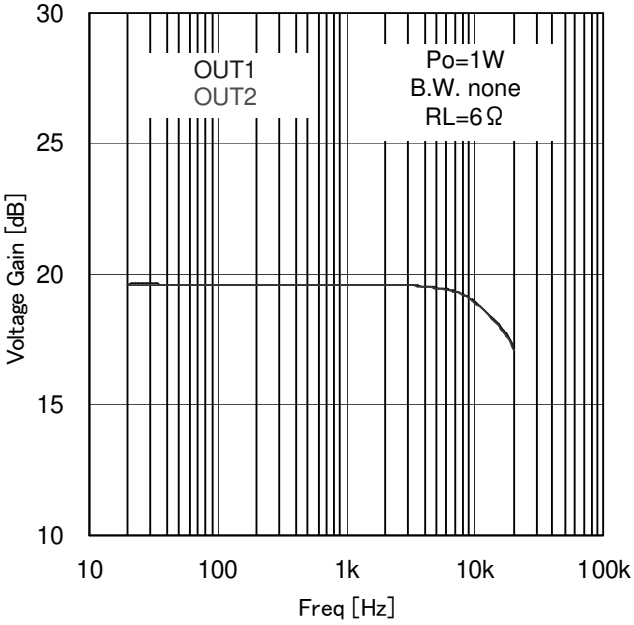


Figure 24. Freq vs. Voltage Gain

●Typical Performance Curves (Reference) (6/8)

（Unless otherwise specified Ta=25℃, Vcc=12V, f=1kHz, RL=8Ω, RSTX=3.3V, MUTEX=3.3V, PLIMT0=L, PLIMT1=L, fs=48kHz, MCLK=256fs,
Output LC filter：L=10uH, C=0.1uF）

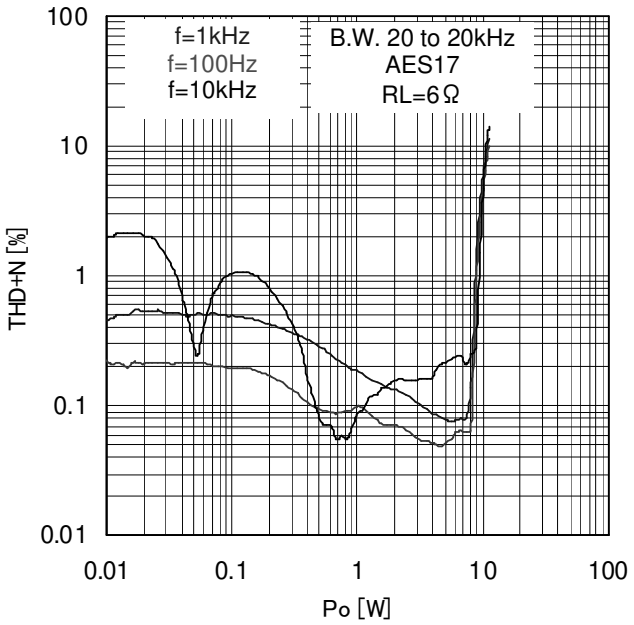


Figure 25. Po vs. THD+N

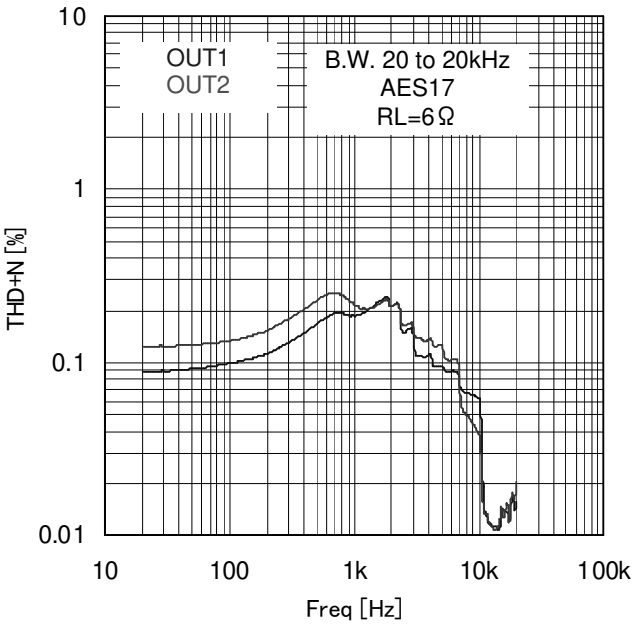


Figure 26. Freq vs. THD+N

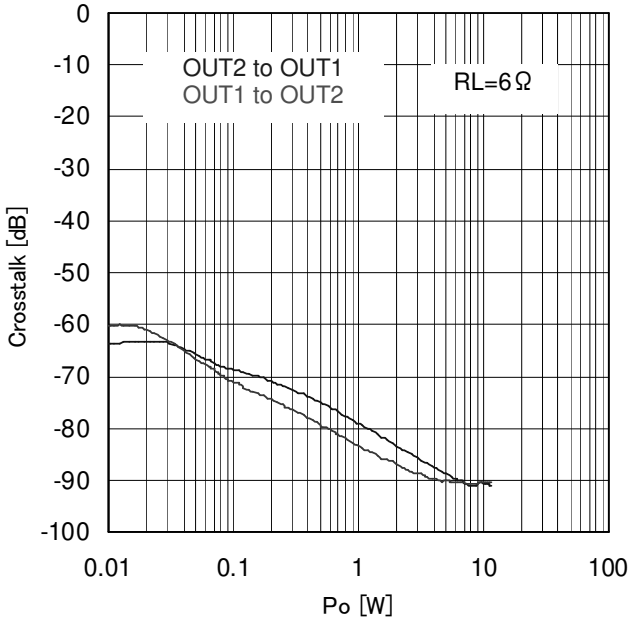


Figure 27. Po vs. Crosstalk

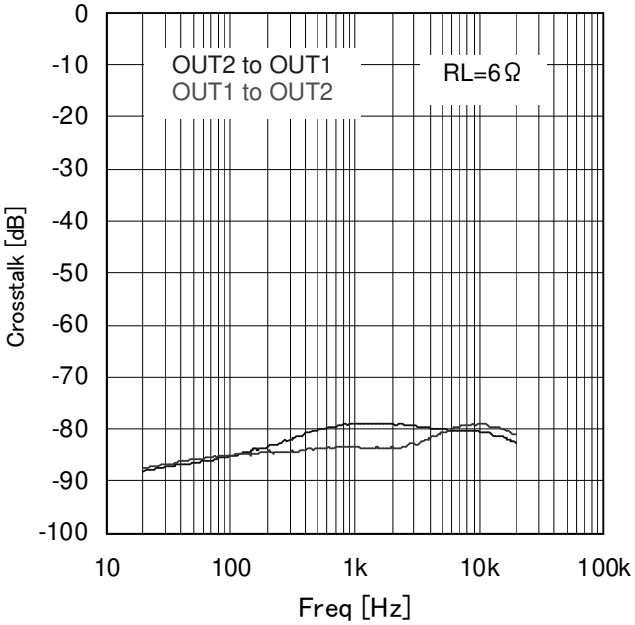


Figure 28. Freq vs. Crosstalk

●Typical Performance Curves (Reference) (7/8)

（Unless otherwise specified Ta=25℃, Vcc=12V, f=1kHz, RL=8Ω, RSTX=3.3V, MUTEX=3.3V, PLIMT0=L, PLIMT1=L, fs=48kHz, MCLK=256fs, Output LC filter：L=10uH, C=0.1uF）

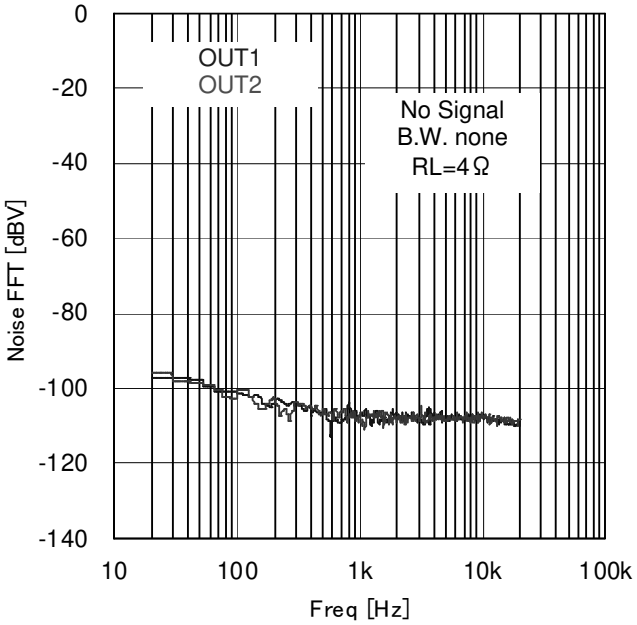


Figure 29. FFT of output noise voltage

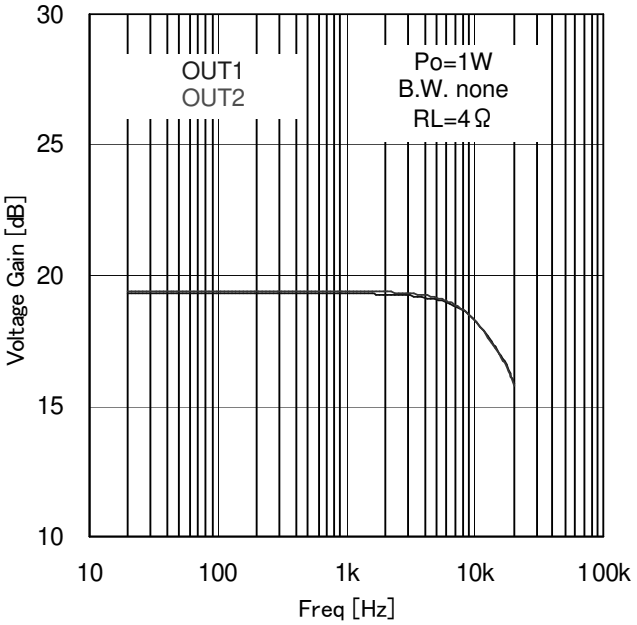


Figure 30. Freq vs. Voltage Gain

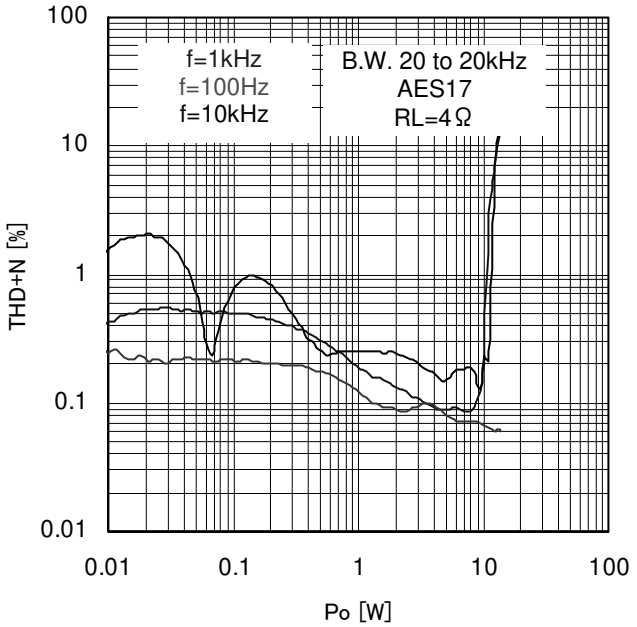


Figure 31. Po vs. THD+N

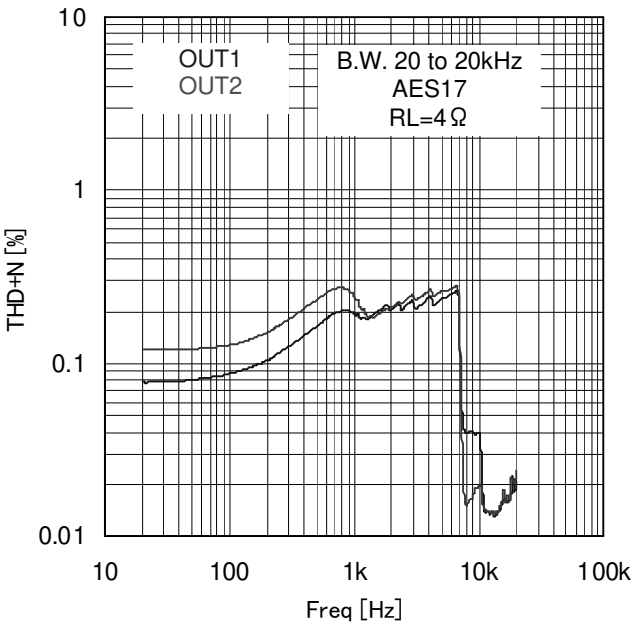


Figure 32. Freq vs. THD+N

●Typical Performance Curves (Reference) (8/8)

（Unless otherwise specified Ta=25℃, Vcc=12V, f=1kHz, RL=8Ω, RSTX=3.3V, MUTEX=3.3V, PLIMT0=L, PLIMT1=L, fs=48kHz, MCLK=256fs, Output LC filter：L=10uH, C=0.1uF）

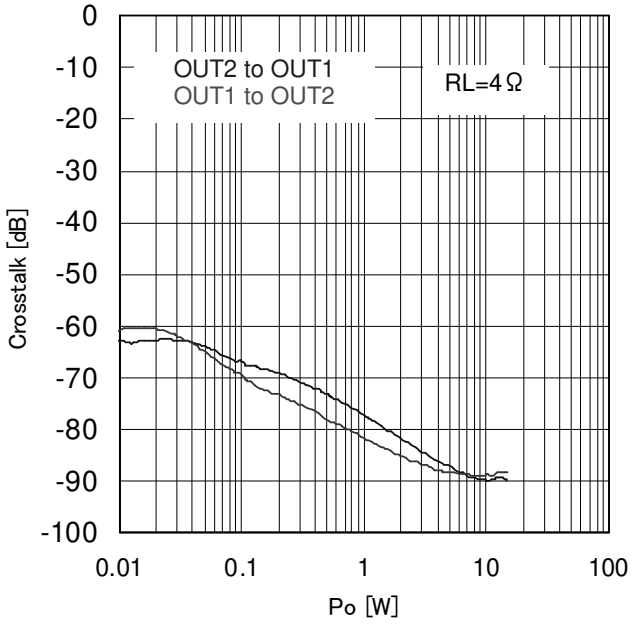


Figure 33. Po vs. Crosstalk

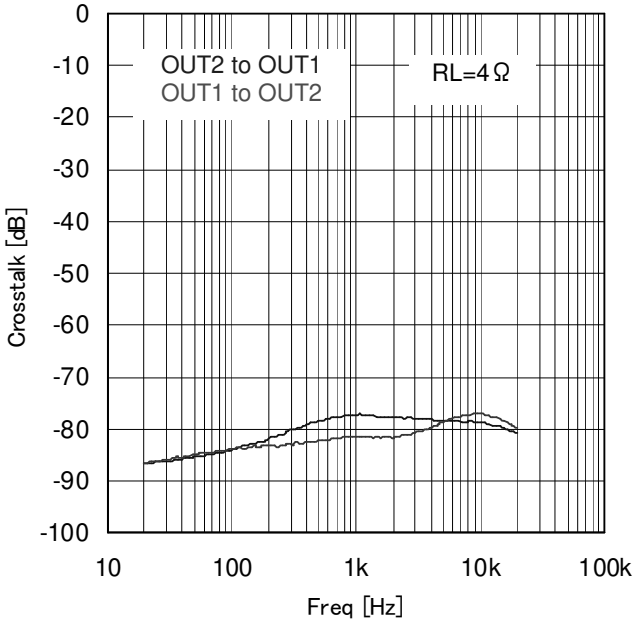


Figure 34. Freq vs. Crosstalk

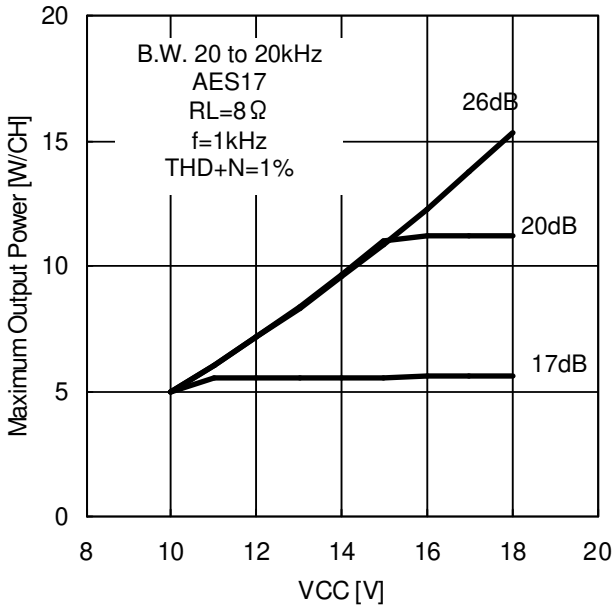


Figure 35. VCC vs. Maximum Output Power

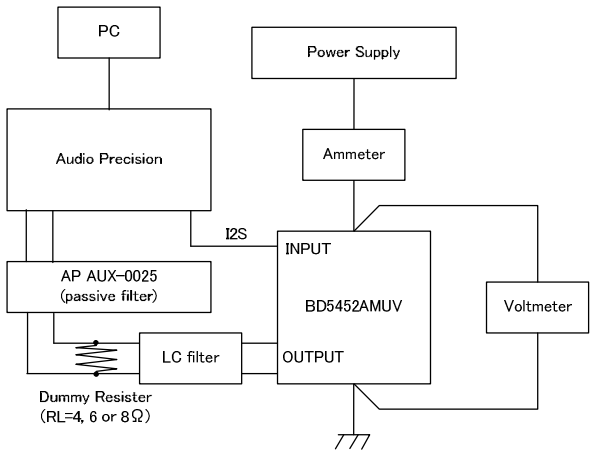


Figure 36. Audio Characteristics Measurement Environment

●About digital audio input

1) Input digital audio signal sampling frequency (fs) explanation

PWM sampling frequency, Soft-start, Soft-mute time, and the detection time of the DC voltage protection in the speaker depends on sampling frequency (fs) of the digital audio input.

Sampling frequency of the digital audio input (fs)	PWM sampling frequency (fpwm)	Soft-start / Soft-mute time	DC voltage protection in the speaker detection time
32kHz	256kHz	32msec.	1.02sec
44.1kHz	352.8kHz	23msec.	0.74sec
48kHz	384kHz	21.5msec.	0.68sec

2) Format of digital audio input

MCLK: It is System Clock input signal.

It will input LRCLK, BCLK, SDATA that synchronizes with this clock that are 256 times of sampling frequency (256fs) or 512 times of sampling frequency (512fs).

LRCLK: It is L/R clock input signal.

It corresponds to 32kHz/44.1kHz/48kHz with that clock(fs) which are same to the sampling frequency (fs). The data of a left channel and a right channel for one sample is input to this section

BCLK: It is Bit Clock input signal.

It is used for the latch of data in every one bit by sampling frequency's 64 times sampling frequency (64fs).

SDATA: It is Data input signal.

It is amplitude data. The data length is different according to the resolution of the input digital audio data. It corresponds to 16/ 20/ 24 bit.

3) I2S data format

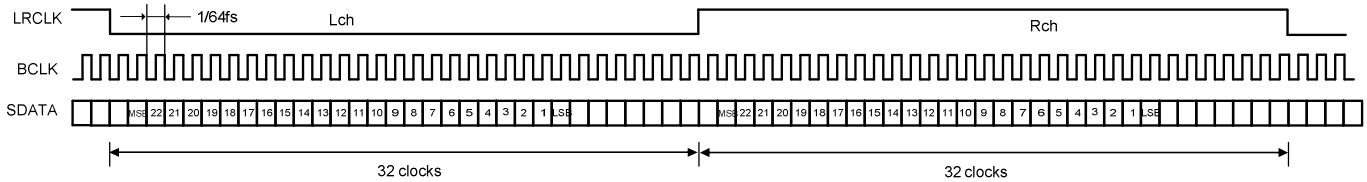


Figure 37. I2S Data Format 64fs, 24bit Data

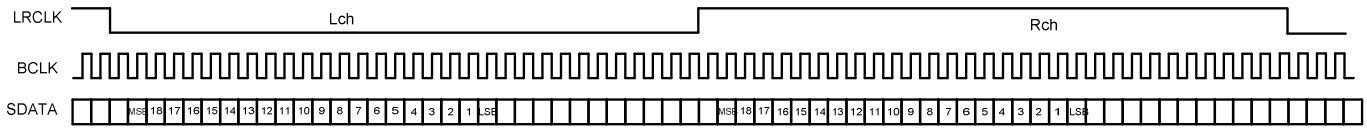


Figure 38. I2S Data Format 64fs, 20bit Data

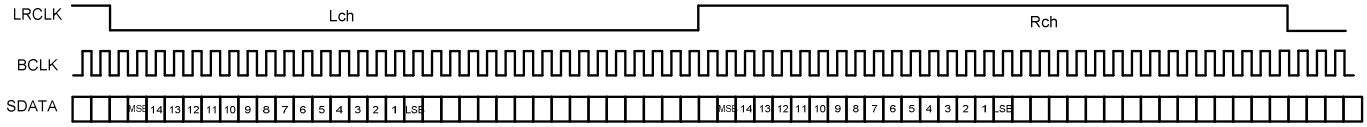


Figure 39. I2S Data Format 64fs, 16bit Data

The Low section of LRCLK becomes Lch, the High section of LRCLK becomes Rch.

After changing LRCLK, second bit becomes MSB.

4) Audio Interface format and timing

Recommended timing and operating conditions(MCLK, BCLK, LRCLK and SDATA)

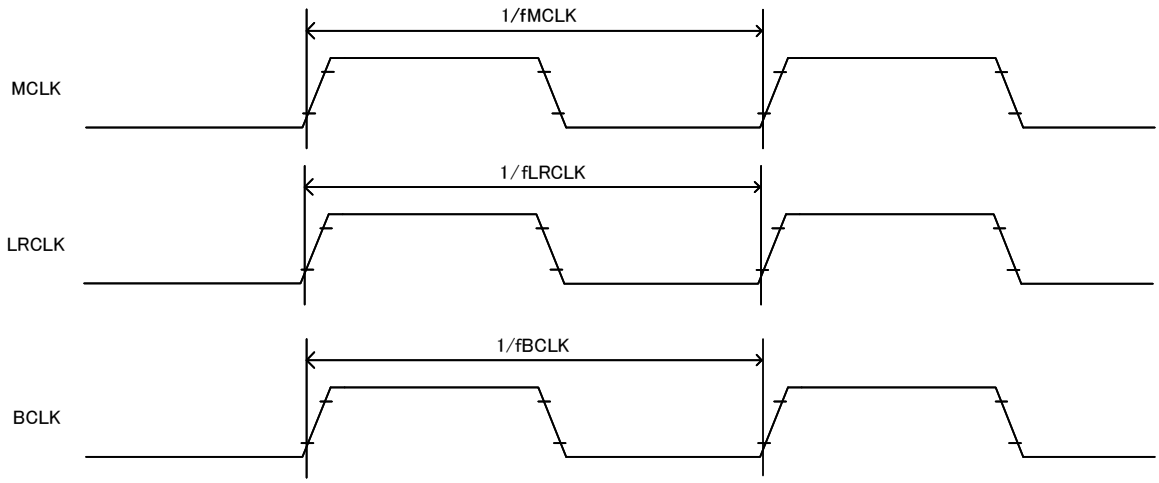


Figure 40. Clock timing

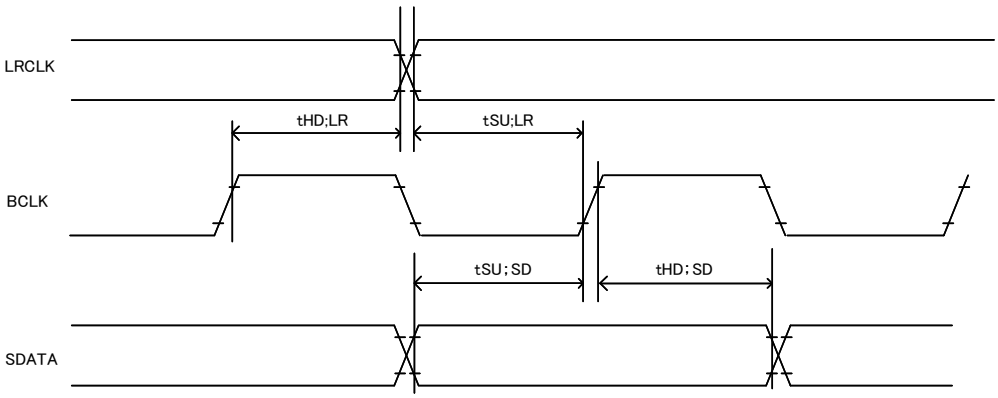


Figure 41. Audio Interface timing

No.	Parameter	Symbol	Limit				Unit
			MCLK=256fs		MCLK=512fs		
			Min.	Max.	Min.	Max.	
1	MCLK frequency	fMCLK	8.192	12.288	16.384	24.576	MHz
2	LRCLK frequency	fLRCLK	32	48	32	48	kHz
3	BCLK frequency	fBCLK	2.048	3.072	2.048	3.072	MHz
4	Setup time, LRCLK※7	tSU;LR	20	—	20	—	ns
5	Hold time, LRCLK※7	tHD;LR	20	—	20	—	ns
6	Setup time, SDATA	tSU;SD	20	—	20	—	ns
7	Hold time, SDATA	tHD;SD	20	—	20	—	ns
8	MCLK, DYTY	dMCLK	40	60	40	60	%
9	LRCLK, DYTY	dLRCLK	40	60	40	60	%
10	BCLK, DUTY	dBCLK	40	60	40	60	%

※7 This regulation is to keep rising edge of LRCK and rising edge of BCLK from overlapping.

●Timing Chart

1) Power supply start-up sequence

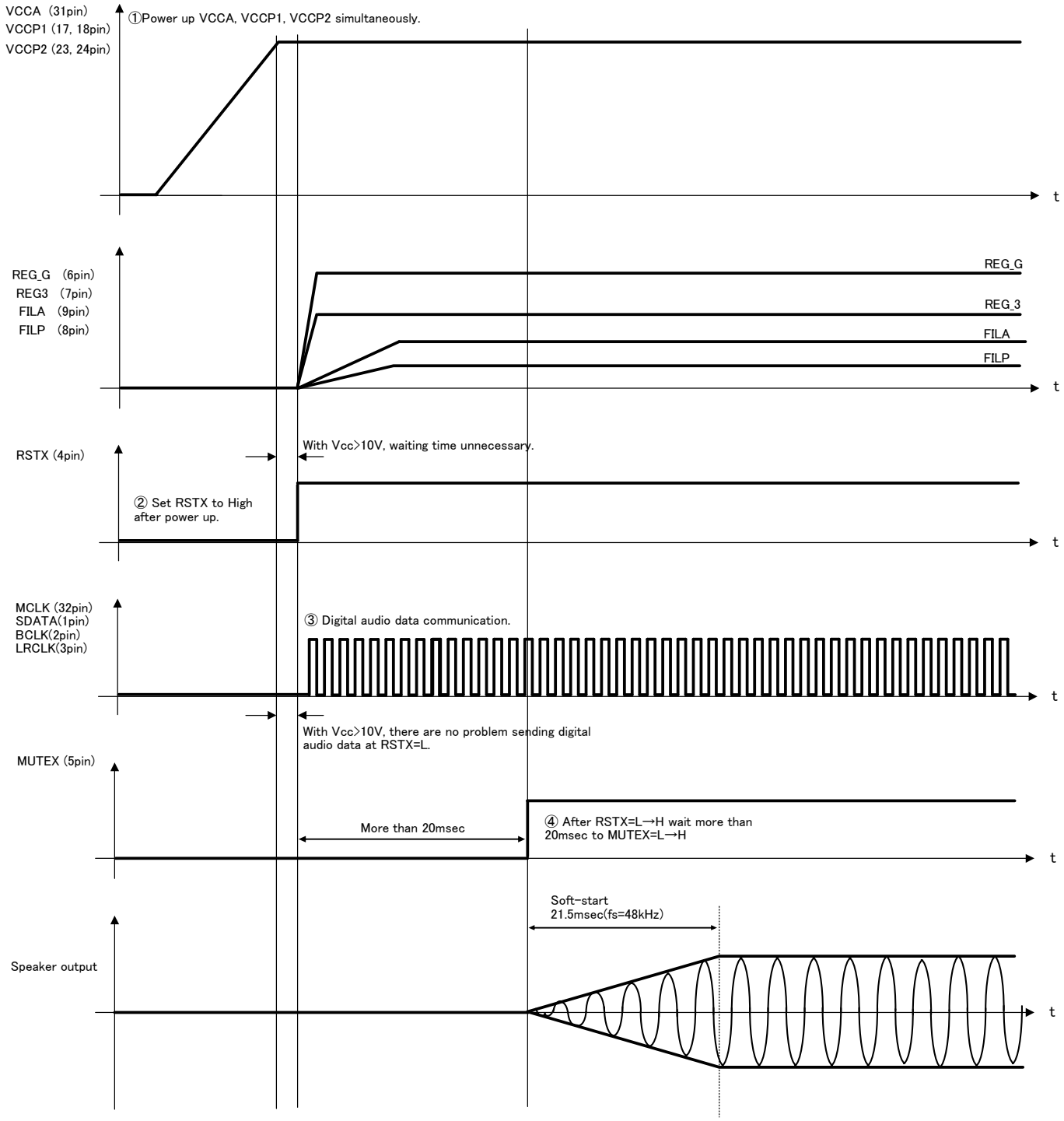


Figure 42. Power supply start-up sequence

2) Power supply shut-down sequence

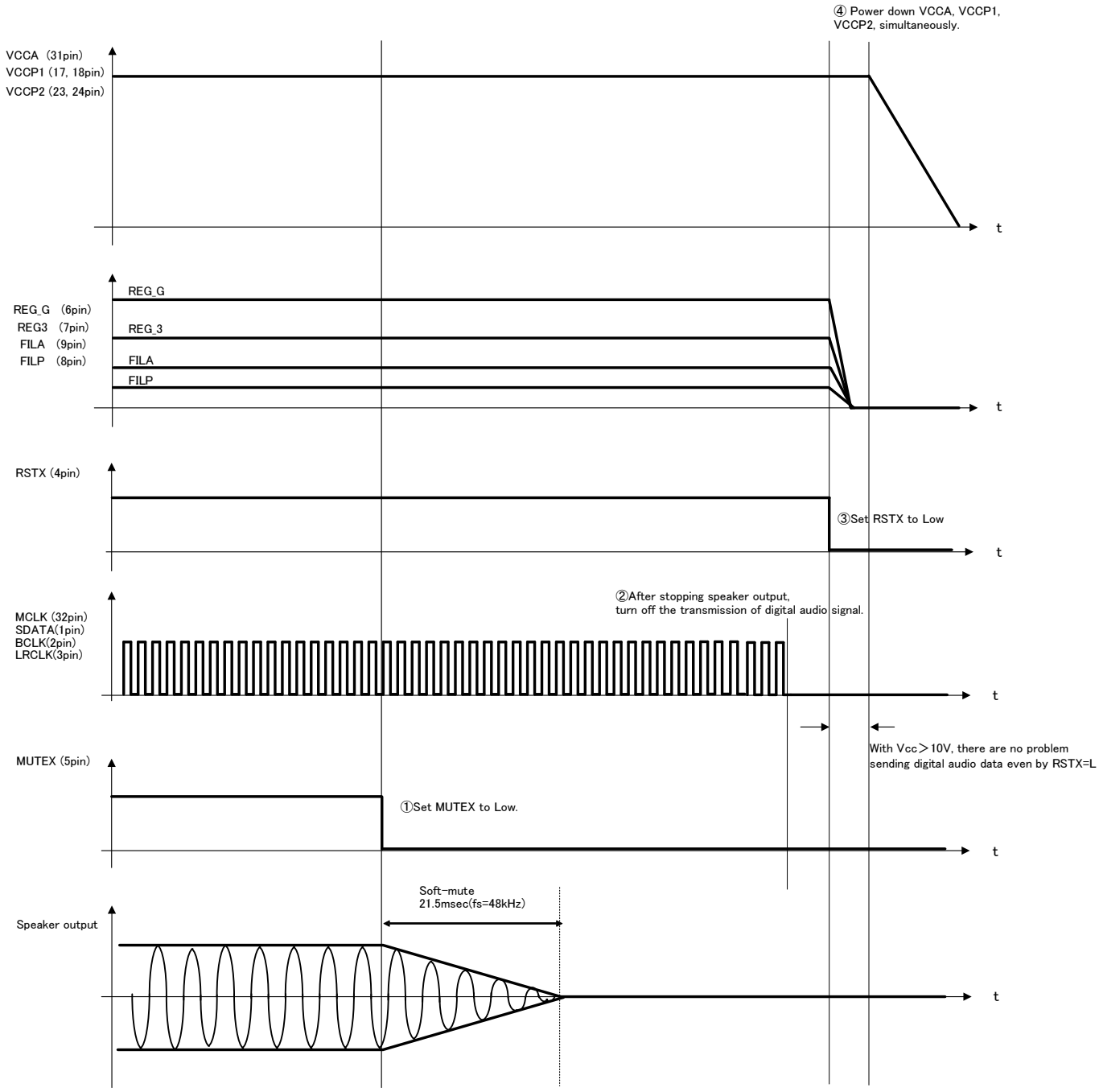


Figure 43. Power supply shut-down sequence

3) About changing audio signal

The output PWM frequency of BD5452AMUV becomes the frequency of eight times of the sampling frequency fs. Therefore output PWM frequency becomes unstable when MCLK seems to become unstable at the time of channel switching at input switching and so on, too. It is possible that the LC resonance is occurred and a short protections function worked.

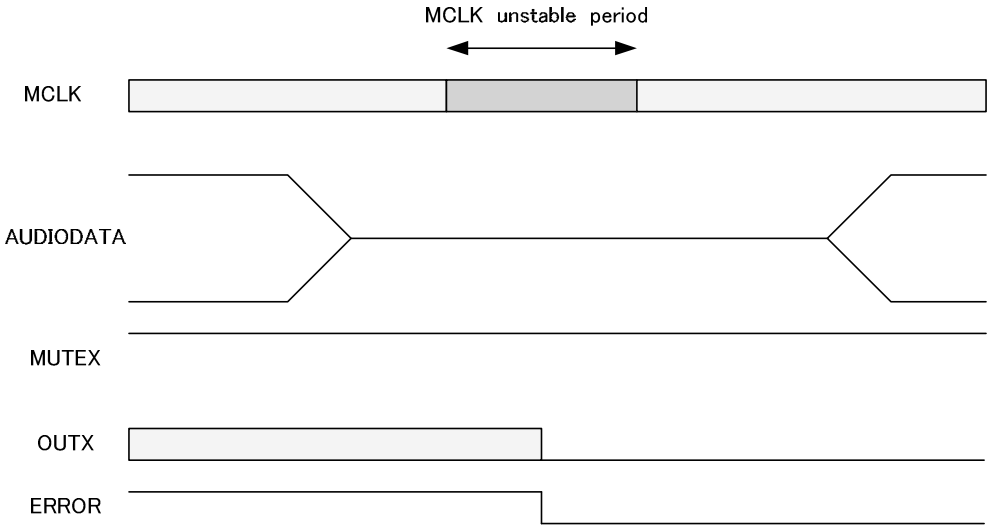


Figure 44. Action at MCLK unstable1

If you can expect MCLK unstable period, we suggest following process.
1. Mute AUDIODATA from scalar IC.(A)
2. After muting AUDIODATA from scalar IC (B), set MUTEX=L(C).
3. After MCLK go to stable state, set MUTEX=H(D).
4. Release mute AUDIODARA from scalar IC(E).

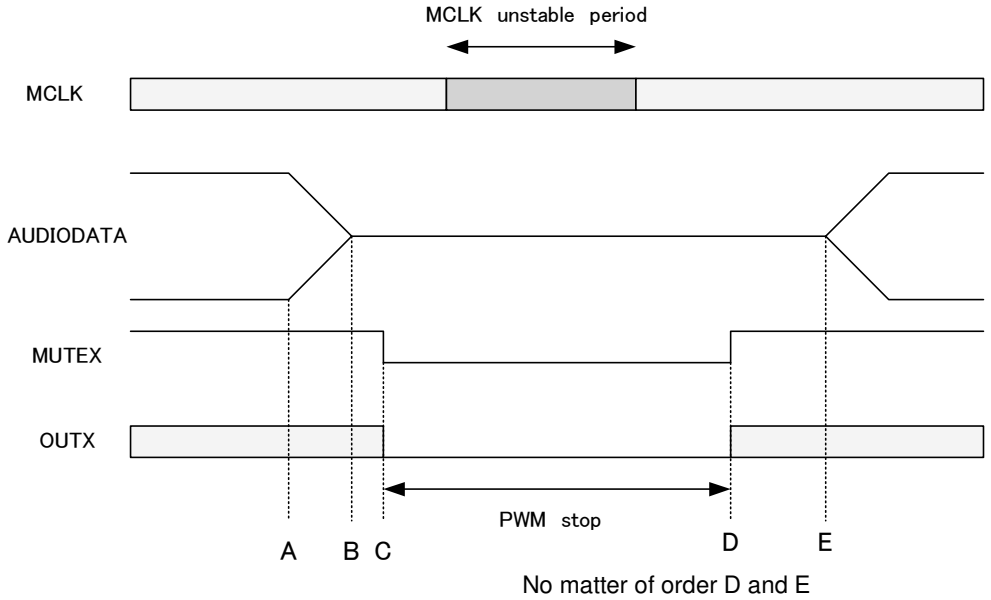


Figure 45. Action at MCLK unstable2

●About the protection function

Protection function	Detecting & Releasing condition		PWM Output	ERROR Output
Output short protection	Detecting condition	Detecting current = 10A (TYP.)	HiZ_Low (Latch)	L (Latch)
DC voltage protection in the speaker	Detecting condition	At speaker output, impressed DC voltage over 0.68sec (fs=48kHz) over 3.5Vbetween (power limit off), 1.75V(power limit 10W) or 1.225V(power limit 5W)	HiZ_Low (Latch)	L (Latch)
High temperature protection	Detecting condition	Chip temperature to be above 150℃ (TYP.)	HiZ_Low	L
	Releasing condition	Chip temperature to be below 120℃ (TYP.)	Normal operation	
Under voltage protection	Detecting condition	Power supply voltage to be below 8V (TYP.)	HiZ_Low	H
	Releasing condition	Power supply voltage to be above 9V (TYP.)	Normal operation	
Over voltage Protection	Detecting condition	Power supply voltage to be above 20V(TYP.)	HiZ_Low	H
	Releasing condition	Power supply voltage to be below 19.5V(TYP.)	Normal operation	
Clock stop protection	Detecting condition	No change to MCLK more than 1usec (TYP.) or no change to BCLK more than 1usec (TYP.) or no change to LRCLK more than 21usec (at fs=48kHz.).	HiZ_Low	H
	Releasing condition	Normal input to MCLK, BCLK and LRCLK.	Normal operation	

* The ERROR pin is Nch open-drain output.
* Once an IC is latched, the circuit is not released automatically even after an abnormal status is removed. The following procedures ① or ② is available for recovery.
  ①After turning MUTEX terminal to Low(holding time to Low = 10msec(Min.)) turn back to High again.
  ②Restore power supply after dropping to power supply voltage Vcc＜3V(10msec (Min.) holding) which internal power on reset circuit activates.

1) Output short protection（Short to the power supply）

This IC has the PWM output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output pin becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After turning MUTEX terminal to Low(holding time to Low = 10msec(Min.)) turn back to High again.
②Restore power supply after dropping to power supply voltage Vcc＜3V(10msec (Min.) holding) which internal power on reset circuit activates.

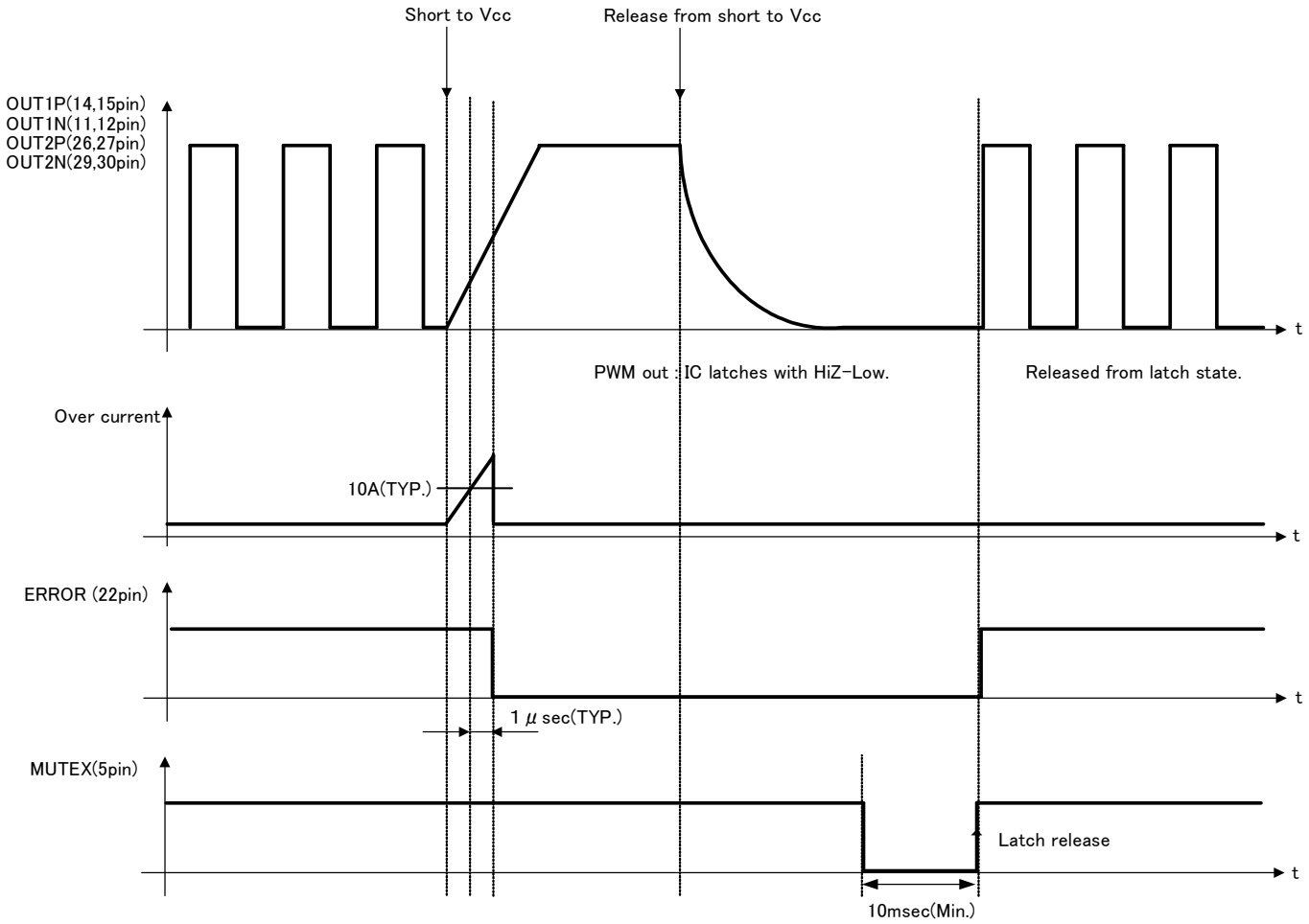


Figure 46. Sequence of the Output short protection

2) Output short protection（Short to GND）

This IC has the PWM output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output terminal becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After turning MUTEX terminal to Low(holding time to Low = 10msec(Min.)) turn back to High again.
②Restore power supply after dropping to power supply voltage Vcc＜3V (10msec (Min.) holding) which internal power on reset circuit activates.

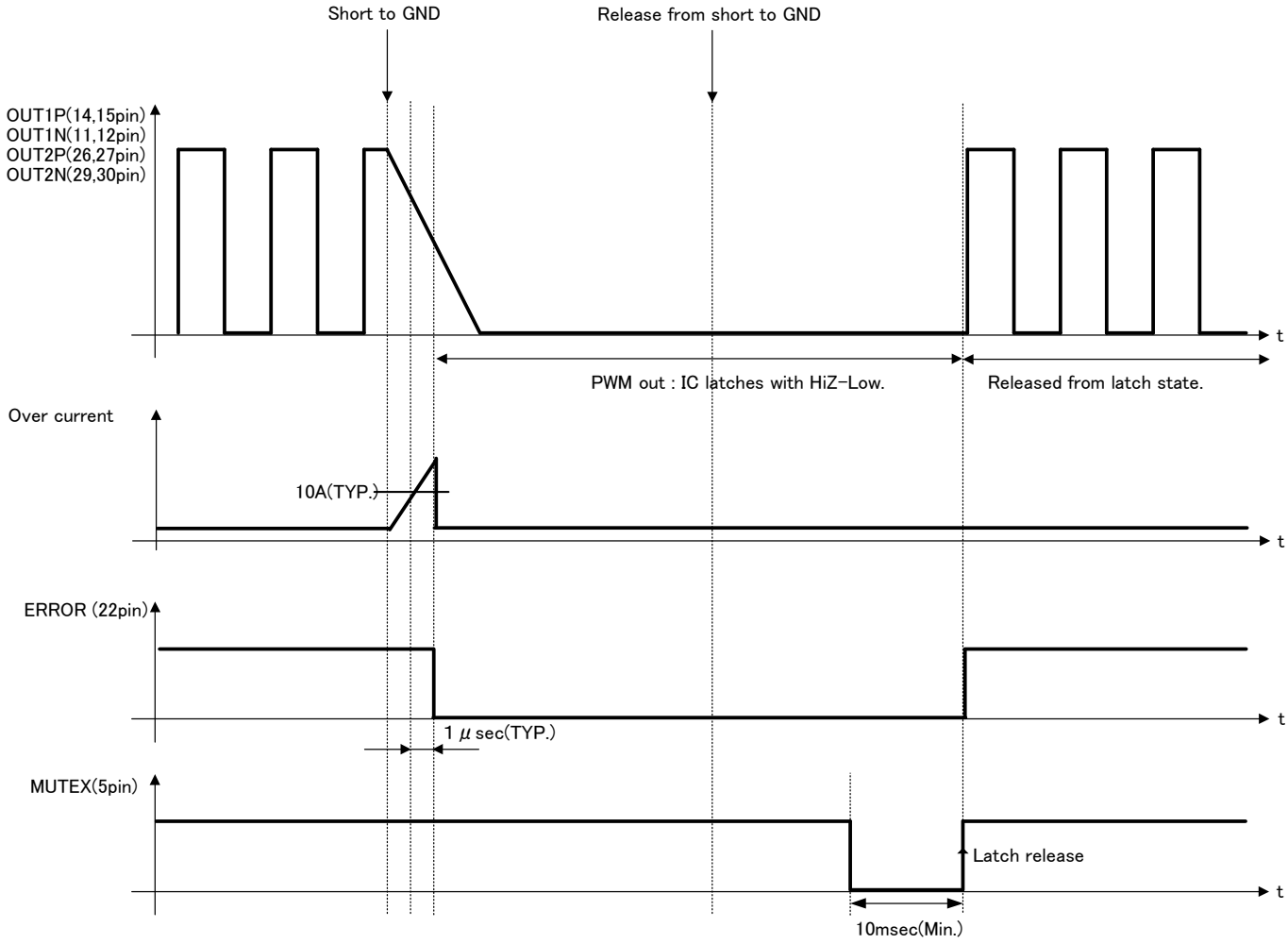


Figure 47. Sequence of the Output short protection

3) DC voltage protection in the speaker1

When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.

Detecting condition - It will detect when MUTEX pin is set High and speaker output is more than 3.5V(TYP, Power Limit OFF setting), 1.75V(TYP, Power Limit 10W setting), 1.225V(TYP, Power Limit 5W setting), 0.68sec(fs=48kHz) or above.
Once detected, The PWM output instantaneously enters the state of HiZ-Low, and IC does the latch.

Releasing method - ①After turning MUTEX terminal to Low(holding time to Low = 10msec(Min.)) turn back to High again.
②Restore power supply after dropping to power supply voltage Vcc＜3V
(10msec (Min.) holding) which internal power on reset circuit activates.

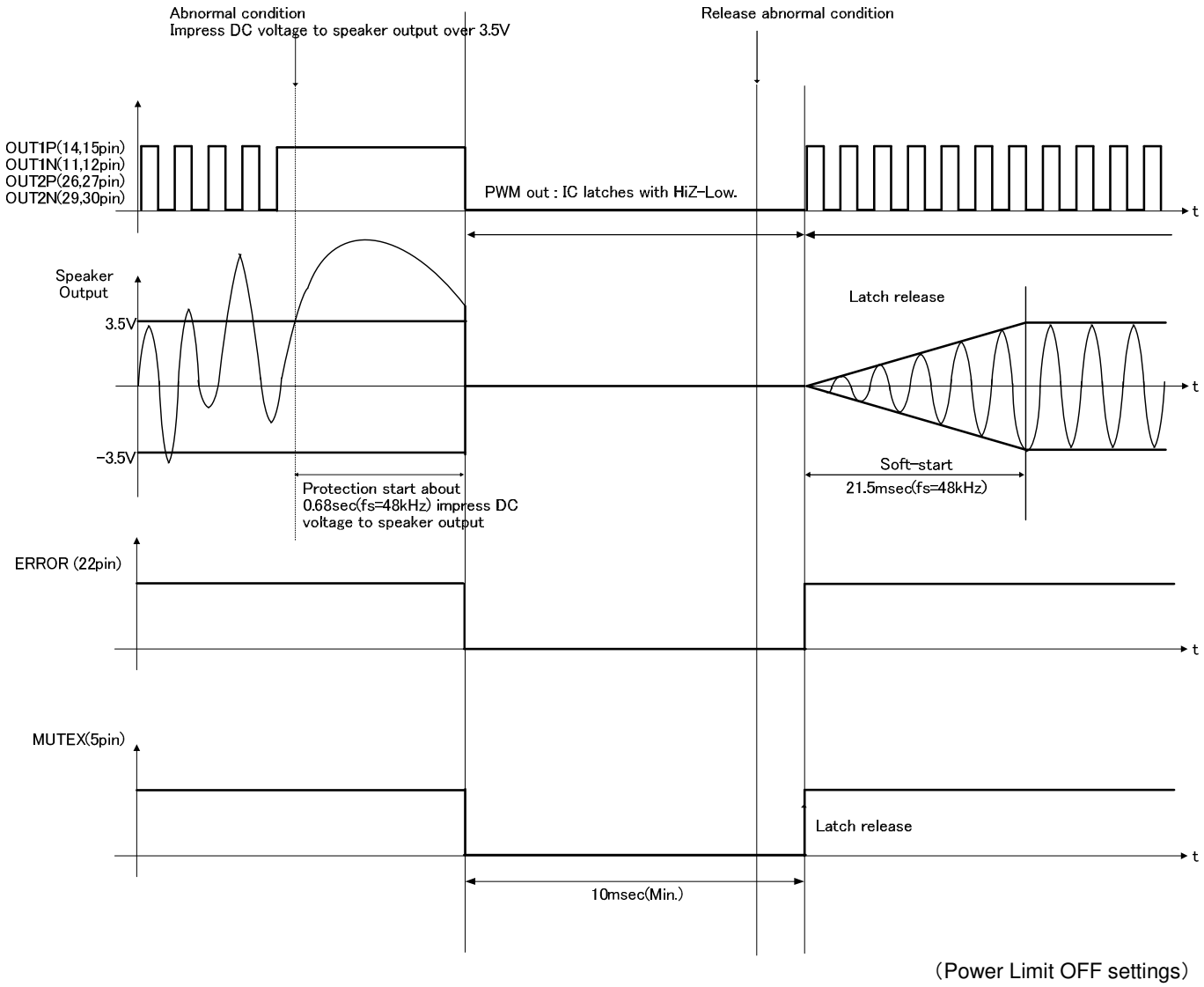


Figure 48. Sequence of DC voltage protection in the speaker1

4) DC voltage protection in the speaker2

About DC voltage protection at PWM output Duty=0% or 100%
When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.

Detecting condition - It will detect when MUTEX pin is set High or Low and PWM output Duty=0% or 100% , 43msec(fs=48kHz) or above. Once detected, The PWM output instantaneously enters the state of HiZ-Low, and IC does the latch.

Releasing method - ①After turning MUTEX terminal to Low(holding time to Low = 10msec(Min.)) turn back to High again.
②Restore power supply after dropping to power supply voltage Vcc＜3V (10msec (Min.) holding) which internal power on reset circuit activates.

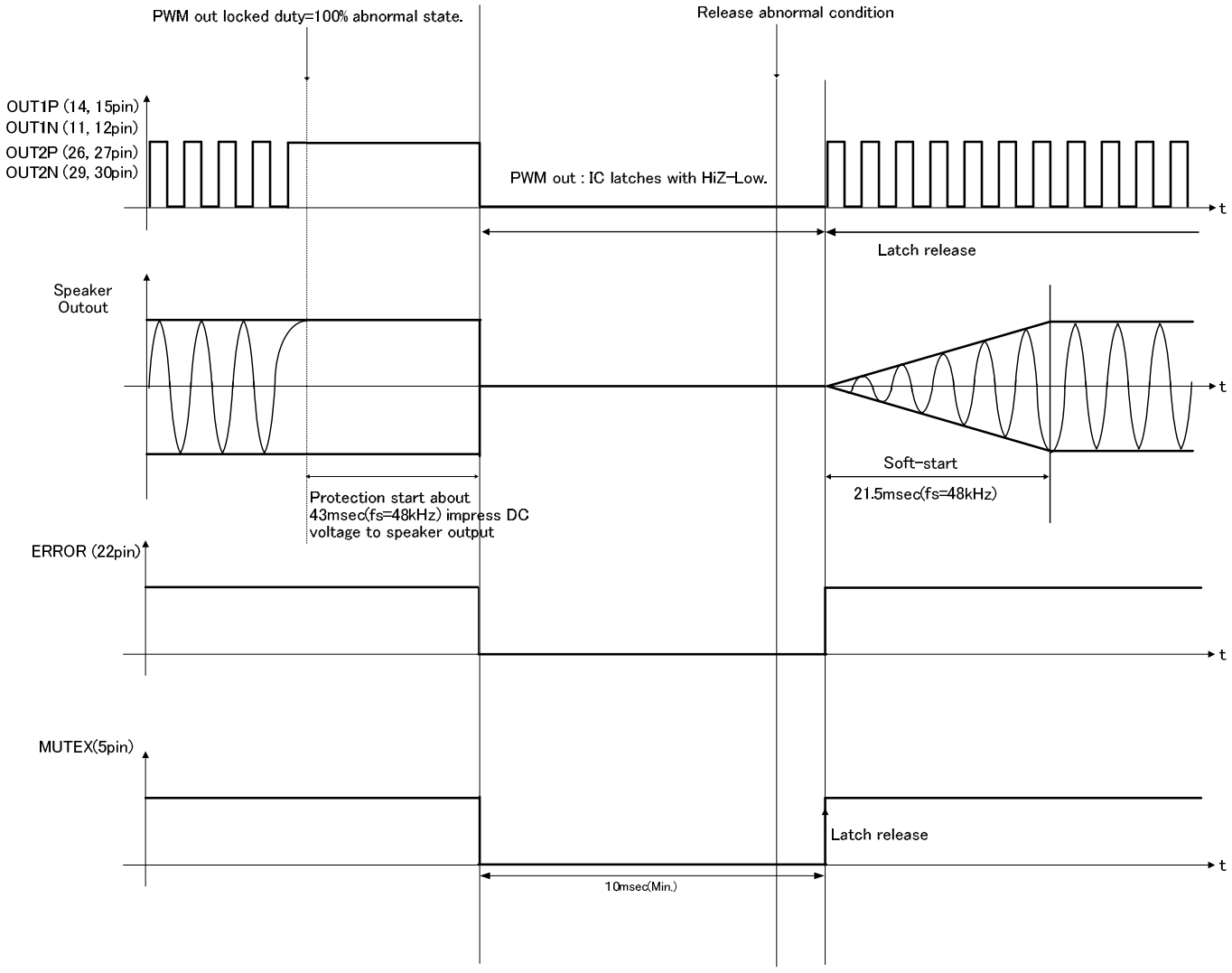


Figure 49. Sequence of DC voltage protection in the speaker2

5) High temperature protection

This IC has the high temperature protection circuit that prevents thermal reckless driving under an abnormal state for the temperature of the chip to exceed Tjmax=150℃.

Detecting condition - It will detect when MUTEX pin is set High and the temperature of the chip becomes 150℃(TYP.) or more. Speaker output turns MUTE immediately, when High temperature protection is detected.

Releasing condition - It will release when MUTEX pin is set High and the temperature of the chip becomes 120℃(TYP.) or less. The speaker output is outputted through a soft-start when released. (Auto recovery)

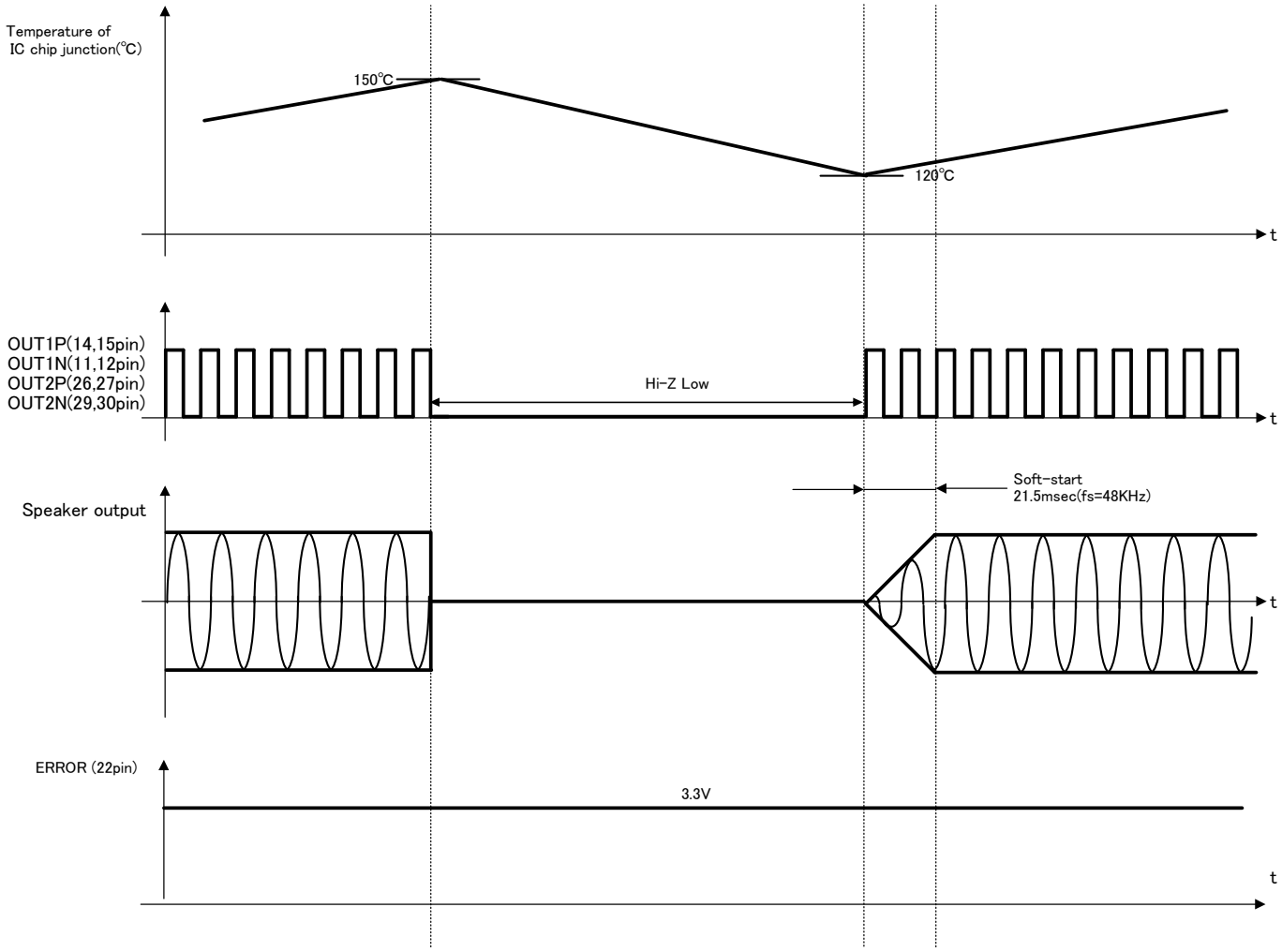


Figure 50. Sequence of High temperature protection

6) Under voltage protection

This IC has the under voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition - It will detect when MUTEX pin is set High and the power supply voltage becomes lower than 8V(TYP.).Speaker output turn MUTE immediately, when Under voltage protection is detected.

Releasing condition - It will release when MUTEX pin is set High and the power supply voltage becomes more than 9V(TYP.). The speaker output is outputted through a soft-start when released. (Auto recovery)

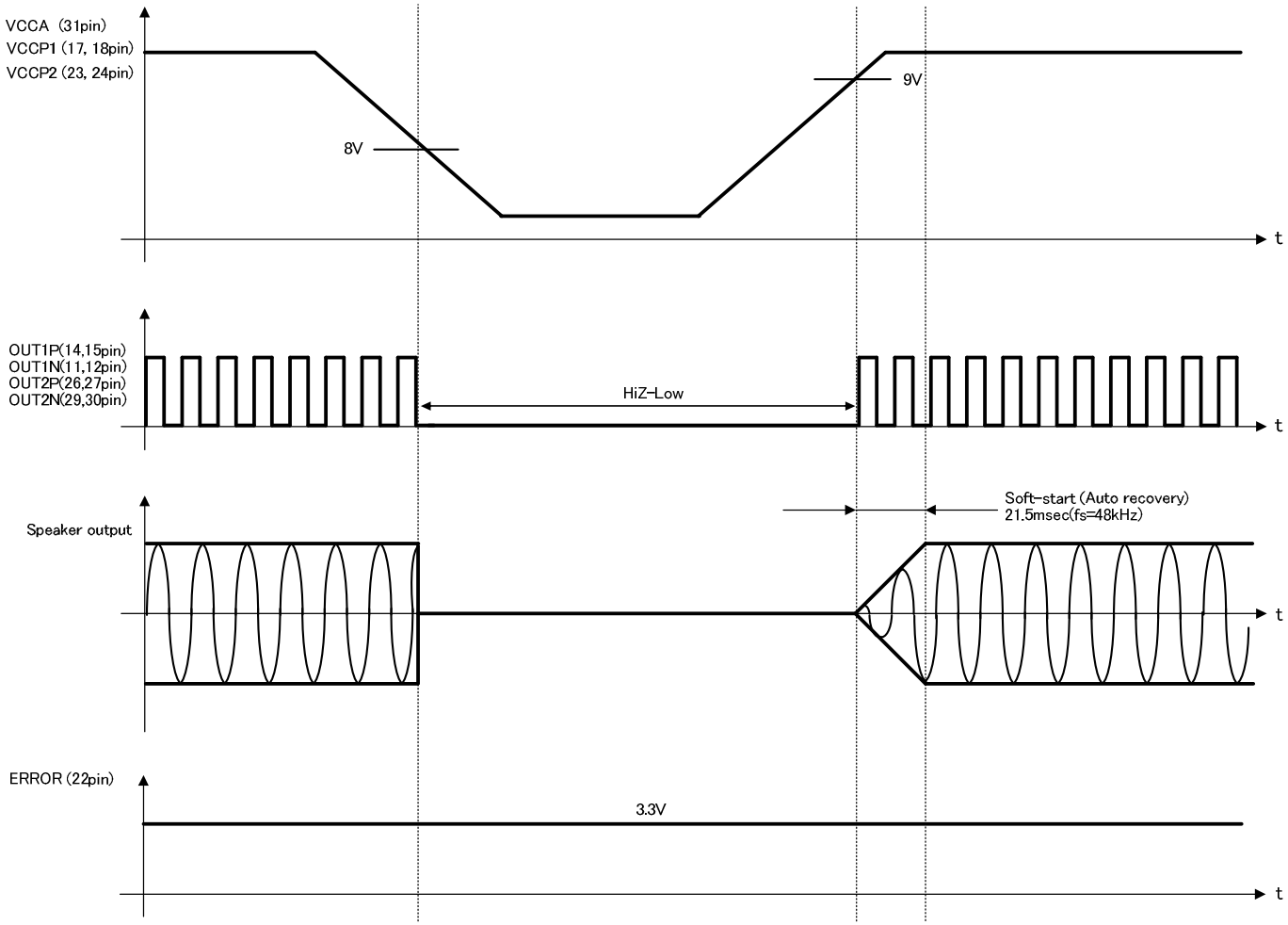


Figure 51. Sequence of Under voltage protection