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Wireless Power Consortium Qi Compliant
AirFuel Alliance PMA Compliant

Wireless Power Receiver IC

BD57015GWL

General Description

BD57015GWL is a stand-alone wireless power receiver IC. The device integrates a fully synchronous rectifier circuit with low-impedance FETs, Qi compliant and PMA compliant packet controller, adjustable regulated voltage output, and an open-drain output terminal to communicate with the power transmitter using amplitude modulation.
BD57015GWL is targeted at mobile applications implementing wireless charging compliant to Qi Extended Power Profile (EPP) standard and the PMA standard.

Key Specification

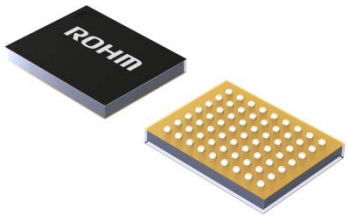
- 7 Programmable Output Voltages 5.0 to 12.0 V
- Maximum Input Voltage 20 V (Max)
- Maximum Input/ Output Current 1.5 A (Max)
- AC Input Frequency Range 100 to 480 kHz

Package

UCSP50L4C W(Typ) D(Typ) H(Max)
4.1mm × 3.2mm × 0.57mm
(0.4mm pitch)

Features

- Low Impedance FET rectifier
- High efficiency fully synchronous rectifier
- Maximum Input Voltage of 20V
- Supports Qi standard ver1.2, PMA standard SR1
- Automatic Detection of Qi / PMA, or selection by external pin
- Open-Drain output terminal for modulation
- TX-RX coil Position Gap alarm



Applications

Qi and/or PMA Compliant Devices
- Smart Phones
- Cell Phones
- Hand-held Mobile Devices

Typical Application Circuit

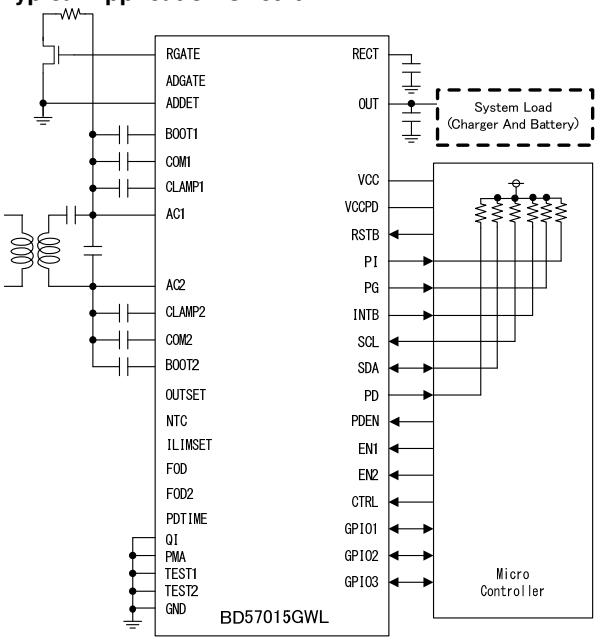


Figure 1. Typical Application Circuit

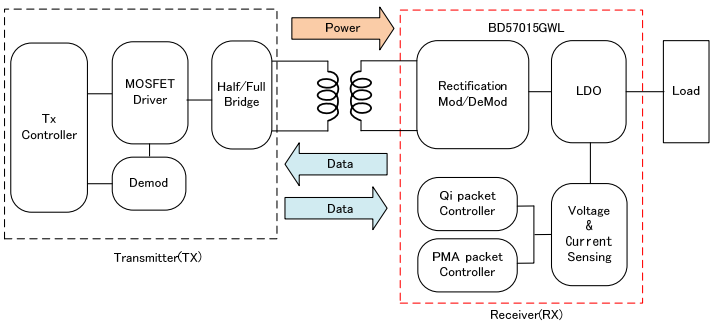


Figure 2. Wireless Power Transfer System

Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
RECT,OUT, AC1,AC2,COM1, COM2,CLAMP1,CLAMP2 Voltage	VINOUT_H1	-0.3 to +20	V
BOOT1,BOOT2 Voltage	VINOUT_H2	-0.3 to +26	V
BOOT1-AC1, BOOT2-AC2 Voltage	VBOOT_AC	-0.3 to +7.0	V
PG, PI, INTB, SDA,SCL,TEST1,TEST2,EN1,EN2, PMA,QI,CTRL,RGATE,PD, PDEN Voltage	VINOUT_L1	-0.3 to +7.0	V
VCC,REG25,GPIO1-3,FOD,FOD2 OUTSET,NTC,ILIMSET,RSTB, PDTIME,VCCPD Voltage	VINOUT_L2	-0.3 to +4.5	V
ADDET, ADGATE Voltage	VAD_H1	-0.3 to +28	V
Input/ Output Rating Current	IMAX	1.5(Note 1)	A
PG, PI, INTB pin rated Current	IMAX_PG	15	mA
Power Dissipation	Pd	1.64(Note 2)	W
Operation Temperature Range	Ta	-30 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(Note 1) Applies to AC1, AC2, RECT, GND terminals when all of them are connected to a common pattern on the PCB.
(Note 2) If mounted on a standard ROHM PCB (PCB size: 54mm x 62mm x 1.6mm), reduce by 13.12mW/°C (Ta ≥25°C).
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum rating

Recommended Operating Range

Parameter	Symbol	Range	Unit
Rectified Voltage Range	VRECT	0 to 17.4	V
AC1,AC2 Input Peak Voltage Range	VAC1,VAC2	17.4	V
ADDET Input Voltage	VADDET	15.0	V
OUT Terminal Voltage	VOUT	5.0 to 12.0(Note 3)	V
VCC Voltage Range	VCC	2.5 to 3.0	V
VCCPD Voltage Range	VCCPD	2.5 to 3.0	V
Capacitance between RECT-GND	CRECT	Min 20	μF

(Note 3) Supported VOUT is up to 10V.

Electrical Characteristics (Unless otherwise specified, Ta = 25 °C, VRECT = 5.0V, VCC = 2.65V)

Parameter	Symbol	Compliant Value			Unit	Conditions
		Min	Typ	Max		
General						
Operating Circuit Current 1	I_{RECT1}	-	44	50	mA	VRECT=5.0V, OUT off.
Operating Circuit Current 2	I_{RECT2}	-	27	35	mA	VRECT=5.0V, OUT on
OUT Terminal Quiescent Current (wireless charging is disabled)	I_{OUT}	-	50	100	μA	VOUT=5.0V, RECT=0V ADDET=OPEN
Protection circuit						
RECT Under Voltage Lockout	V_{RECTUV}	2.5	2.6	2.7	V	VRECT:0V → 5V
RECT Under Voltage Lockout Hysteresis	$V_{RECTUVHYS}$	150	300	450	mV	VRECT:5V → 0V
RECT Over Voltage Protection Detection Voltage	V_{RECTOV}	15.6	16.5	17.4	V	VRECT:10V → 20V
RECT Over Voltage Protection Hysteresis	$V_{RECTOVHYS}$	75	150	300	mV	VRECT:20V → 10V
LDO Block						
OUT Terminal Output Voltage 1	$V_{OUTLDO1}$	6.86	7.00	7.14	V	I load=100mA,VOUT=7.0V setting, VRECT=7.5V
OUT Terminal Output Voltage Accuracy	$RATE_{OUT}$	-3	0	+3	%	VOUT=5V,5.3V,8V,9V,10V, 12V
OUT Terminal Load Regulation	dV_{OUT}	-	-	200	mV	Iload=0-500mA VRECT=7.2V VOUT=7V
Maximum Output Current	$I_{LOADmax}$	-	-	1.5	A	
PADDET Block						
PDTIME Input Off Leak Current	$I_{LEAKPDTIME}$	-	-	2.0	μA	VCCPD=2.65V, AC2=Open, PDTIME=2.65V
PDTIME Detection Voltage	V_{PDDET}	0.4	0.7	1.0	V	
PD Output L Level	V_{PDVOL}	-	0.1	0.2	V	Isink=1mA
PD Pin Leak Current	I_{LEAKPD}	-	-	2.0	μA	VPD=2.65V, AC2=Open, PDTIME=0V, PD=7V
COM Block						
COM1, COM2 ON Resistance	RON_{COM}	-	1.5	3.0	Ω	
COM1, COM2 Pin Leak Current	$ILEAK_{COM}$	-	-	2	μA	VCOM1,2=20V
RGATE Block						
RGATE Pin Output H Level	VH_{RGATE}	4.3	4.8	5.3	V	I_{SOURCE}=-1mA, VRECT=7V
RGATE Pin Output L Level	VL_{RGATE}	-	0.1	0.5	V	I_{SINK}=1mA
CLAMP Block						
CLAMP1, CLAMP2 ON Resistance	RON_{CLAMP}	-	2.5	5.0	Ω	
CLAMP1,CLAMP 2 Pin Leak Current	$ILEAK_{CLAMP}$	-	-	2	μA	VCLAMP1,2=20V

Electrical Characteristics (Unless otherwise specified, Ta = 25 °C, VRECT = 5.0V, VCC = 2.65V)

Parameter	Symbol	Compliant Value			Unit	Conditions
		Min	Typ	Max		
Adapter Detection Block						
Adapter Input Detection Threshold Voltage	VADDET	3.4	3.6	3.8	V	Vaddet:0 → 5V
Adapter Input Detection Hysteresis Voltage	VHYS_AD	200	400	600	mV	Vaddet:5 → 0V
Adapter Input Overvoltage Detection Voltage	VADDET_OV	14.0	14.5	15.0	V	Vaddet:13 → 16V
Adapter Input Overvoltage Detection Hysteresis Voltage	VHYS_AD_OV	500	720	940	mV	Vaddet:16 → 13V
ADDET Pin Input Current	IADGATE	-	150	300	μA	VADDET=5V, OUT=OPEN
ADGATE Pin Output L Level	VL_{ADGATE}	-	0.12	0.25	V	Isink=1mA
PMA, QI, EN1, EN2, CTRL, PDEN Pin						
PMA,QI,EN1,EN2,CTRL Pin L Level Input Voltage	VIL_{mode}	-	-	0.4	V	
PMA,QI,EN1,EN2,CTRL Pin H Level Input Voltage	VIH_{mode}	1.3	-	-	V	
PMA,QI,EN1,EN2,CTRL Pin Pull Down	RI_{mode}	-	200	-	kΩ	
PDEN Pin L Level Input Voltage	VIL_{PDEN}	-	-	0.4	V	
PDEN Pin H Level Input Voltage	VIH_{PDEN}	1.3	-	-	V	
RSTB Pin						
RSTB Pin L Level Input Voltage	VIL_{RSTB}	-	-	0.6	V	VCC=2.65V
RSTB Pin Pull Up Resistance	RI_{RSTB}	-	100	-	kΩ	
RSTB Pin L Level Output Voltage	VL_{RSTB}	-	0.15	0.30	V	Isink=1 mA
PG,PI Pin						
PG,PI Pin Output L Level	VL_{PG}	-	0.25	0.5	V	Isink=5mA
PG, PI Pin Leak Current	$ILEAK_{PG}$	-	-	2	μA	VPG=7V
INTB Pin						
INTB Pin Output L Level	VL_{INT}	-	0.25	0.5	V	Isink=5mA
INTB Leak Current	$ILEAK_{INT}$	-	-	2	μA	VINTB=7V

Electrical Characteristics (Unless otherwise specified, Ta = 25 °C, VRECT = 5.0V, VCC = 2.65V)

Parameter	Symbol	Compliant Value			Unit	Conditions
		Min	Typ	Max		
GPIO Pin						
GPIO Pin L Level Input Voltage	VIL_{GPIO}	-	-	VCC×0.3	V	
GPIO Pin H Level Input Voltage	VIH_{GPIO}	VCC×0.7	-	-	V	
GPIO Pull Down Resistance	PD_{GPIO}	-	100	-	kΩ	
GPIO Pull Up Resistance	PU_{GPIO}	-	100	-	kΩ	
L Level Output Voltage	VOL_{GPIO}	-	-	VCC×0.2	V	Isink=1mA
H Level Output Voltage	VOH_{GPIO}	VCC×0.8	-	-	V	Isource=-1mA
Serial Interface						
SCL, SDA Pin L Level Input Voltage	VIL_{SCL} VIL_{SDA}	-	-	0.4	V	
SCL, SDA Pin H Level Input Voltage	VIH_{SCL} VIH_{SDA}	1.3	-	-	V	
SCL, SDA Pin L Level Input Current	IIL_{SCL} IIL_{SDA}	-1	-	-	μA	VSCL=VSDA=0V
SCL, SDA Pin H Level Input Current	IIH_{SCL} IIH_{SDA}	-	-	1	μA	VSCL=VSDA=2.65 V
SDA Pin L Level Output Voltage	VOL_{SDA}	-	-	0.4	V	Isink=2.5 mA

Pin Configuration (Bottom View)

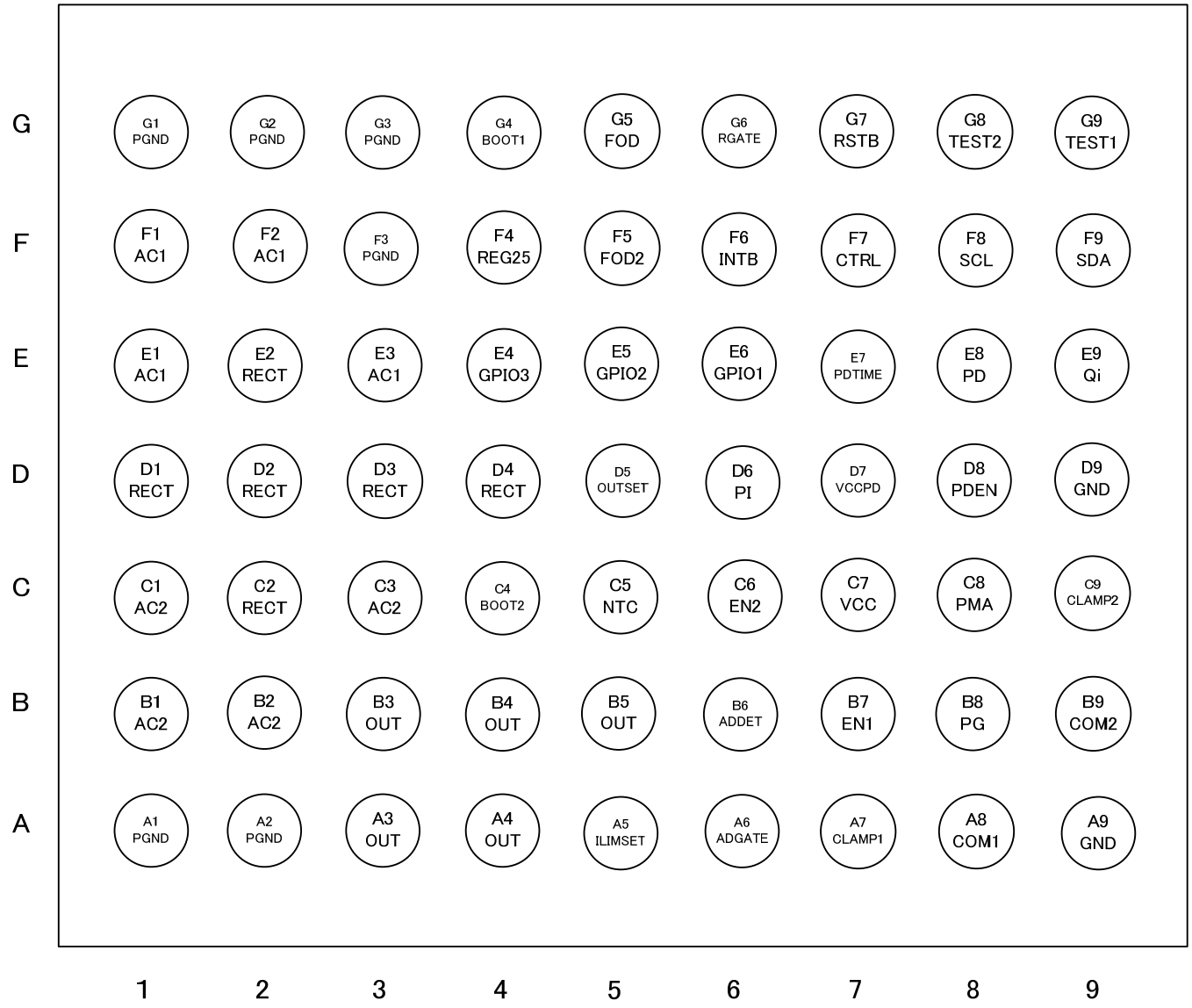


Figure 3. Pin Configuration

Pin Description

Pin No.	Pin Name	I/O	Function
E1,F1,F2,E3(NOTE1)	AC1	Out	AC input pin 1
B1,B2,C1,C3(NOTE1)	AC2	Out	AC input pin 2
G4	BOOT1	Out	Bootstrap capacitor connection pin 1 for the internal FET driver
C4	BOOT2	Out	Bootstrap capacitor connection pin 2 for the internal FET driver
A3,A4,B3,B4, B5(NOTE1)	OUT	Out	LDO Output pin
C2,D1,D2,D3,E2, D4(NOTE1)	RECT	Out	Rectifier Output pin
D5	OUTSET	Input	Resistance Connection pin for the Output Voltage setting
G6	RGATE	Output	Output Control pin for PMA setting If only Qi mode is used, leave the pin OPEN.
A7	CLAMP1	Input	AC1 Clamp protection pin
A8	COM1	Output	Output Control pin 1
B9	COM2	Output	Output Control pin 2
C9	CLAMP2	Input	AC2 Clamp protection pin
C5	NTC	Input	Resistance Connection pin for the thermal Detection setting(NOTE3)
F5	FOD2	Input	Resistance Connection pin 2 for the Foreign Object Detection Adjustment setting If only PMA mode is used, leave the pin OPEN.
G5	FOD	Input	Resistance Connection pin 1 for the Foreign Object Detection Adjustment setting If only PMA mode is used, leave the pin OPEN.
A5	ILIMSET	Input	Resistance Connection pin for the Current Limit setting
D6	PI	Output	Qi BPP(Baseline Power Profile) / EPP(Extended Power Profile) identification pin
D8	PDEN	Input	PAD Detection Enable pin(NOTE2)
E7	PDTIME	Input	PAD Detection Time setting pin(NOTE2)
E8	PD	Output	PAD Detection Output pin
A6	ADGATE	Output	External Adaptor Path Gate Driver pin
B6	ADDET	Input	External Adaptor Voltage Detection pin(NOTE2)
B7	EN1	Input	Enable pin 1 for Wired or Wireless Charging
C6	EN2	Input	Enable pin 2 for Wired or Wireless Charging
B8	PG	Output	Open Drain Output pin to notify if LDO Output is ON
G7	RSTB	Input/Output	System Reset Input and Output pin(NOTE3)
F6	INTB	Output	Interrupt Output pin
F7	CTRL	Input	Control pin for Wireless Charging
G9	TEST1	Input	Test pin 1 (Usually these pins are connected to GND.)
G8	TEST2	Input	Test pin 2 (Usually these pins are connected to GND.)
F8	SCL	Input	Serial Interface Clock Input pin(NOTE2)
F9	SDA	Input/Output	Serial Interface Data Input/Output pin(NOTE2)
E6	GPIO1	Input/Output	GPIO 1 pin(NOTE4)
E5	GPIO2	Input/Output	GPIO 2 pin(NOTE4)
E4	GPIO3	Input/Output	GPIO 3 pin(NOTE4)
C8	PMA	Input	PMA setting pin
E9	Qi	Input	Qi setting pin
D7	VCCPD	Power	Power Supply for Pad Detection pin(NOTE2)
C7	VCC	Power	External Power Supply Application pin for LOGIC Block(NOTE4)
F4	REG25	Output	2.5V Internal Voltage pin
A9,D9(NOTE1)	GND	Ground	Ground pin
A1,A2,F3,G1,G2, G3(NOTE1)	PGND	Ground	Power Ground pin

(NOTE1) If one function pin have several pin numbers, please connect same function pins to a common board node.
(NOTE2) When the pin is unused, please connect the pin to GND.
(NOTE3) When the pin is unused, please leave the pin OPEN.
(NOTE4) When the pin is unused, please connect the pin to GND or leave the pin OPEN.

Block Diagram

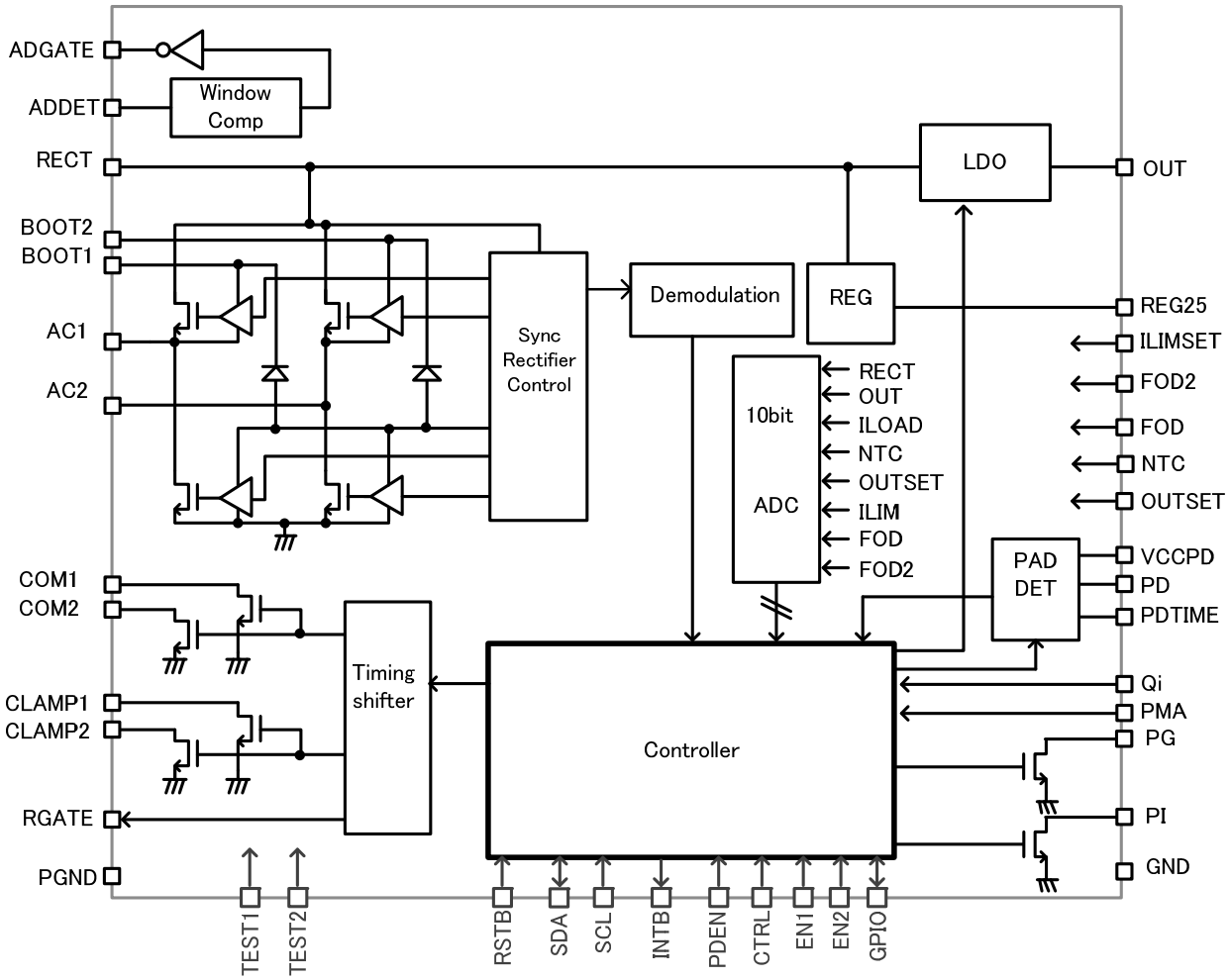


Figure 4. Block Diagram

Description of operation

1. Qi/PMA operation mode selection

The BD57015GWL is compliant with both Qi and PMA standards. Qi/PMA operation mode can be detected automatically by the internal circuit or set by external terminal. The automatic detection depends on the carrier frequency from TX during Digital Ping. The operation mode is shown as follow:

PMA pin	QI pin	Operation Mode
L	L	Automatic detection based on the internal circuit
L	H	Qi mode only (It won't operate in other modes)
H	L	PMA mode only (It won't operate in other modes)
H	H	Reserved (Do not use this setting)

If H is needed connect these pins to the REG25 pin using a pullup resistance.
When the Automatic detection of operation mode is selected, the active operation mode can be reported using the Mode Status Register (0x8D).

Mode Status register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
MODE STATUS	0x8D	[7] Reserved [6] PMA_MODE PMA mode detection 0x0: Undetected 0x1: Operating in PMA mode [5] QI_MODE Qi mode detection 0x0: Undetected 0x1: Operating in Qi mode [4:0] Reserved	0x00	R

Reserved bits read an undefined value.

The charge start detection interrupt can be used as an indicator for when to check this register. Refer to section "*16.Interrupt Control Block"* for the details on the charge start detection interrupt.

2. Qi Controller block

If Qi mode is detected as the operation mode of BD57015GWL, it will proceed to following the Qi compliant Ping phase. In this phase, it will send the Signal Strength value which indicates the degree of coupling between the RX and TX. Then BD57015GWL will proceed to the Identification & Configuration phase and send the ID information and the necessary information about RX to the TX. When BD57015GWL is in EPP mode, (set by Qi Power Mode setting register (0x0E)), it sends the information of the configuration and requests a transition to the Negotiation phase. If TX responses the ACK message, it will proceed to the Negotiation phase.
If this negotiation succeeds, it will move to the Calibration phase and the Power Transfer phase at EPP. If this negotiation fails, or the TX does not respond, or BPP mode is set by register, it will move to the Power Transfer phase at BPP.
The power transfer mode can be checked by the PI pin. If PI pin is L, it is in EPP mode, and if it is H, it means that it is charging in BPP mode. The power mode can be also confirmed by checking the Qi Monitor Mode register (0x0F).

Qi Power Mode setting register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial Value	R/W
EPP_MODE	0x0E	[7:0] EPP_MODE_SET EPP Mode setting 0x10 : BPP Mode only 0x01 : EPP Mode (During PI=L, this must be selected) 0x11 : EPP Mode (During PI=H, this must be selected) Other : Reserved	0x10	R/W

Please don't set Reserved value.

Qi Monitor Mode register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial Value	R/W
MONI_MODE	0x0F	[7:1] Reserved [0] EPP_MODE Classification of the operation mode 0x0 : Operation in BPP Mode 0x1 : Operation in EPP Mode	0x00	R

Reserved bits read “0”

In the Power Transfer Phase, the previously specified output voltage is output at the OUT pin and the device is ready to start charging. The charging will be stopped when setting the EN1 pin to “H” which then sends the End Power Transfer packet (Charging Complete, EPT) to the TX. The following are the supporting messages regarding EPT packet. The EPT value can be checked in the Qi EPT Code Register (0x1C) when EPT is sent.

End Power Transfer Packet			
Value	**Reason**	**Support**	**Condition**
0x00	Unknown	Send	Adapter Input detection
0x01	Charge Complete	Send	Charge Complete (EN1=H Detection)
0x02	Internal Fault	Send	Internal Temperature error, ILIMSET pin setting error, OUTSET pin setting error, FOD pin setting error, FOD2 pin setting error.
0x03	Over Temperature	Send	External Temperature Error (CTRL=H Detection, Detection for using the information from NTC pin)
0x04	Over Voltage	Not Sent	-
0x05	Over Current	Not Sent	-
0x06	Battery Failure	Not Sent	-
0x07	Reserved	Not Sent	-
0x08	No Response	Send	No convergence to desired point for RECT voltage
0x09	Reserved	Not Sent	-
0x0A	Negotiation Failure	Send	Negotiation can’t be done normally
0x0B	Restart Power Transfer	Not Sent	-

When sending this packet, an interrupt can be generated for the external microcontroller.

Qi EPT Code register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial Value	R/W
EPT_CODE	0x1C	[7:0] EPT_CODE EPT value (code) When the status is not EPT, this register is 0xFF.	0xFF	R

3. PMA Controller block

When the operation of BD57015GWL is set to PMA mode, BD57015GWL will proceed to the digital Ping phase of PMA. In this phase, BD57015GWL will send the ACK message to the TX and signal that a device based on PMA exists. Next, BD57015GWL proceeds to the Identification phase and sends information to the TX. TX will check the ID Information and if it is correct, it will proceed to the Power Transfer phase. However if it is incorrect, it will go back to the Digital Ping phase. In the Power Transfer phase, an output voltage is produced in the OUT pin and charging can start. The charging can be stopped when setting the EN1 pin to “H” which then sends an EOC signal to the TX. When the charging stops, it can also generate an interrupt signal. The reason for charging stop is stored in the PMA EOC Code register (0x1D. Other conditions that produce an End of Charge (EOC) signal are described below.

PMA EOC Code register (Only for PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
EOC_WR	0x1D	[7:0] EOC_CODE Cause of the output EOC. (”1” indicates “Detection”) [7] : During NTC detection [6] : No Load Detection (continuous for more than 42 seconds)NOTE 1 [5] : Full Charge Detection (Low Current Detection for long hours)NOTE 1 [4] : UVLO Detection of Output [3] : External Temperature Error (CTRL=H Detection) 150 degrees [2] : Internal Temperature Error or ILIMSET pin setting Error or OUTSET pin setting Error [1] : Charge Complete (EN1=H Detection) [0] : Adapter Input Detection	0x00	R

(NOTE1) These functions are cleared when the device is reset. This setting shall remain in effect with the following registers (EOC MASK:0x86)

PMA EOC Mask register (Only for PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
EOC_MASK	0x86	[7:4] Reserved [3] MASK _NO LOAD EOC output for the No Load Detection Disable (0x0 : Enable 0x1 : Disable) [2] MASK _FULL EOC output for the Full Charge Detection Disable (0x0 : Enable 0x1 : Disable) [1:0] Reserved	0x0C	R/W

Please set an initial value into Reserved bits.

Description of Operation for Common Blocks

4. Rectifier block

By inputting AC signal into both ends of a primary side (TX) coil, a voltage is generated by electromagnetic induction in the secondary side coil. Full-wave rectification is performed after detection of output current from the secondary coil as mentioned above, and using the built-in FET connected to AC1 and AC2 pins. The current detection is done by comparing the AC pin voltage (FET Ron × Icoil) with GND level. The on/off signal of built-in FET will be generating based on this detection signal. The on/off timing of L side FET and H side FET are monitored to prevent a shoot through current. The bootstrap drive system for the Nch FET on H side and L side is used for high efficiency. Therefore, a capacitor is needed between BOOT1 (BOOT2) pin and AC1 (AC2) pin.

5. Low Drop Out (LDO) Block

The OUT pin output voltage can be set through the OUTSET pin or through a register, please refer to section "*13. OUTSET setting*" for details. The current limit value of the OUT pin can be set through the ILIMSET pin or through a register as explained in section "*9. ILIM setting*".

6. A/D Converter Block

When making a packet, every analog signal that is needed for calculation will be converted to digital value. The A/D converter uses the 10bit sequential comparison (SAR) architecture. This conversion cannot be controlled from outside.

7. External control input (CTRL, EN1 and EN2).

When CTRL = H, during an external temperature error, the wireless power transfer will stop after an EPT or EOC output. Charging from wireless supply or wired (adapter) supply can be enabled or disabled using EN1 and EN2.
In the default condition (EN1=L and EN2=L), both wireless power supply and adapter control are active. When both sources are available, priority is given to the adapter (wired power), wireless power is stopped according to the sequence explained in adapter detection block, and the electrical connection of the path from an adapter is active.
When EN1 becomes H, the Qi mode will produce an End Power Transfer (0x01: Charge Complete) packet and the PMA mode will produce an End of Charge (EOC) packet and wireless power supply will be stopped.

CTRL	Operation
L	Will maintain the normal feed condition.
H	During external temperature error, the wireless power transfer will stop because of an EPT or EOC output.

EN1	EN2	Operation
L	L	Both the wireless power charging and external adapter control are enabled. Priority is given to the external adapter. That is, if a sufficient adapter input is detected during wireless power charging, wireless power will immediately stop and only an adapter charging will continue.
L	H	Both the wireless power charging and external adapter control are enabled. Priority is given to the external adapter. That is, if a sufficient adapter input is detected during wireless power charging, wireless power will immediately stop and only an adapter charging will continue.
H	L	Wireless power charging is disabled. Wired power charging is enable.
H	H	Both an adapter and wireless power charging are disabled. That is, in this mode, power cannot be supplied from OUT.

8. Adapter detection block

If the ADDET pin detects more than 3.6V (Typ), ADGATE will output LOW and turn ON the PMOS switch of the adapter line. Since priority is given to adapter (cable), wireless power supply will be stopped (EPT / EOC output), and then the OUT output will be stopped. After that, the voltage at OUT will be checked and if it is less than 0.7V and the adapter line of PMOS switch will be turned ON (ADGATE: H to L).
The sequence of operation during adapter detection is as follows.

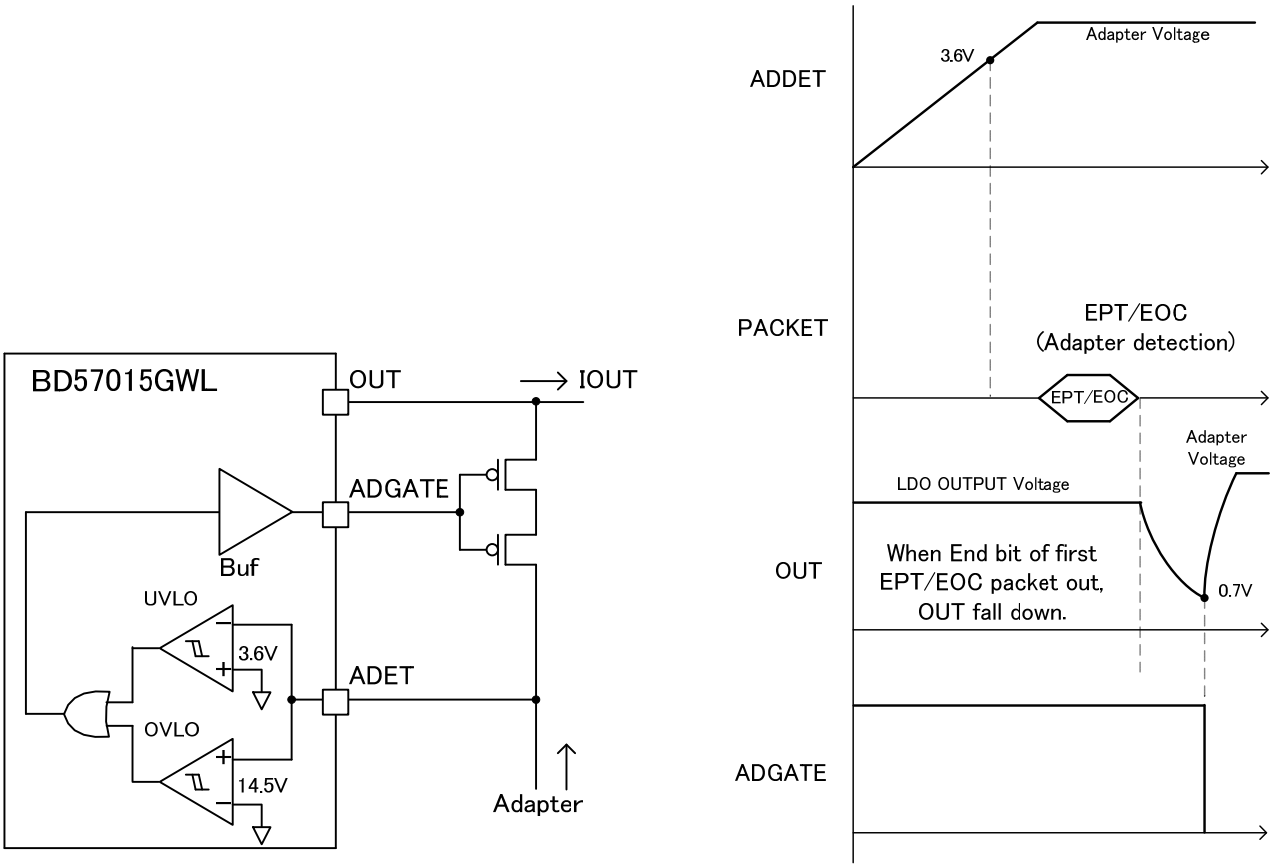


Figure 5. Adapter Detection

If the ADDET voltage is more than the threshold of OVP, the PMOS will be switched off regardless of the wireless power supply.

9. ILIM setting

The current limit of the OUT pin can be set by the resistance connected to the ILIMSET pin or the register shown below. The following formula shows the relation between setting resistance and limit current (ILIM).

Current Limit ILIM [mA]	RILIMSET [kΩ]
ILIMSET register setting	OPEN
500	120
700	75
900	56
1000	43
1100	36
1200	30
1300	24
1500	20
EPT or NoCh	SHORT

The resistance should have accuracy of ±1%.

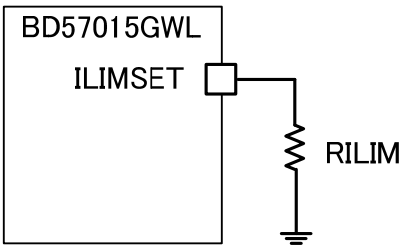


Figure 6. ILIMSET setting

If ILIMSET pin is shorted to GND, there will be a setting error and BD57015GWL will send EPT (internal fault) in Qi mode..And BD57015GWL will send NoCh signal repeatedly, then the charging will not be started in PMA mode.
When the ILIMSET pin is OPEN or the bit [7] of the following register is set to “1”, the Output Current Limit value (of ILIM) can be set depending on the following register (0x0A). If the bit [7] of this register is set to “1”, the register setting has priority regardless of the resistance connected to the ILIMSET pin. Furthermore, the state related to the ILIMSET pin can be confirmed by the ILIM_STATE register (0x0B).

ILIMSET setting register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
ILIM_SET	0x0A	[7] ILIM_REG_EN 0x0 : If ILIMSET pin is not OPEN, the setting of this register (bit[5:0]) is invalid. 0x1 : The setting of this register (bit[5:0]) is valid forcibly. [6] Reserved [5:0] ILIM_SET_VAL OUT Pin Current Limit Level setting 0x5 : 0.5A / 0x6 : 0.55A / 0x7 : 0.6A / 0x8 : 0.65A / 0x9 : 0.7A / 0xA : 0.75A / 0xB : 0.8A / 0xC : 0.85A / 0xD : 0.9A / 0xE : 0.95A / 0xF : 1.0A 0x10 : 1.05A / 0x11 : 1.1A / 0x12 : 1.15A / 0x13 : 1.2A / 0x14 : 1.25A / 0x15 : 1.3A / 0x16 : 1.35A / 0x17 : 1.4A / 0x18 : 1.45A / 0x19 : 1.5A / Other : Reserved	0x0F	R/W
ILIM_STATE	0x0B	[7] ILIM_SHORT_DET Short detection of ILIMSET pin. 0x0 : not short 0x1 : short [6:4] ILIM_ADC_VAL Current limit value set based on the read value in A/D. If the read value in A/D is outside the setting range, it is 0x0. 0x0 : 500mA / 0x1 : 700mA / 0x2 : 900mA / 0x3 : 1000mA / 0x4 : 1100mA / 0x5 : 1200mA / 0x6 : 1300mA / 0x7 : 1500mA [3] ILIM_OPEN_DET Enable/Disable of the register setting. 0x0 : Disable 0x1 : Enable (make ILIMSET pin OPEN to enable this) [2:0] : Reserved	0x00	R

Please set an initial value into Reserved bits.

10. FOD setting (Qi mode only)

To implement FOD (Foreign Object Detection) function in Qi mode, it is required to compute the received power and to compare it with the transmitted power from the TX side. Fine power adjustment to adjust for other power losses (e.g. LC loss) outside the IC is performed by using the resistance connected to the FOD and FOD2 pin or the register shown below. The relation of the received power (PRP) supply and each parameter is shown on the formula below.

$$P_{PR} = \alpha \times f(RECT, IOUT) + \beta[W]$$
$$\alpha = FOD2$$
$$\beta = FOD[W]$$

FOD Value [mW]	RFOD[kΩ]
FOD1_SET register setting	OPEN or 820
-64	300
-32	180
32	130
64	100
96	82
128	68
160	56
192	47
224	39
256	33
288	27
320	24
352	22
384	20
EPT or NoCh	SHORT

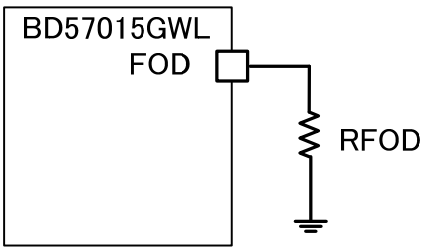


Figure 7. FOD setting

The resistance should have accuracy of ±1%.

If FOD pin is shorted to GND, there will be a setting error and BD57015GWL will send EPT (Internal Fault) in Qi mode. And BD57015GWL will send NoCh signal repeatedly, then the charging will not be started in PMA mode.

FOD2 Value [-]	RFOD2[kΩ]
FOD2_SET register setting	OPEN or 820
1.054	300
1.062	180
1.070	130
1.078	100
1.086	82
1.094	68
1.102	56
1.110	47
1.118	39
1.126	33
1.134	27
1.142	24
1.150	22
1.158	20
EPT or NoCh	SHORT

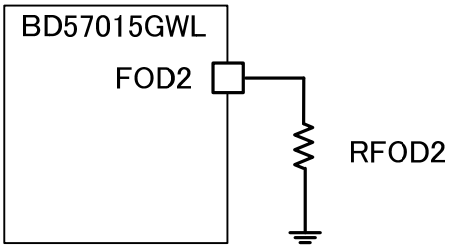


Figure 8. FOD2 setting

The resistance should have accuracy of ±1%.

If FOD2 pin is shorted to GND, there will be a setting error and BD57015GWL will send EPT (Internal Fault) in Qi mode. And BD57015GWL will send NoCh signal repeatedly, then the charging will not be started in PMA mode.

In the formula shown above, α is the inclination adjustment. β is the offset adjustment. Function f(RECT, IOUT) is proportional to the received power and calculated in the internal IC.

When these parameters are adjusted, external physical factors have to be considered. For example, external physical factors are a materials and shape of a coil, an environments around coil, and a distance to a coil of TX.

It is possible to set the FOD and FOD2 parameters in the registers (0x01, 0x03) by leaving FOD and FOD2 pins OPEN or setting the bit [7] of these registers (0x01, 0x03) to “1”. If bit [7] of these registers is set to “1”, the setting of the registers have priority regardless of the resistance connected to the FOD and FOD2 pin.

In addition, the related states in FOD and FOD2 can be confirmed on the next registers (0x02, 0x04).

FOD1 register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial Value	R/W
FOD1_SET	0x01	[7] FOD1_REG_EN 0x0 : If FOD pin is not OPEN, the resistance has priority. 0x1 : The setting of this register (bit[4:0]) has priority. [6] FOD1_POLARITY Set the polarity 0x0 : Plus mode (Add the setting value) 0x1 : Minus mode (Subtract the setting value) [5] Reserved [4:0] FOD1 Setting of the FOD value. 0x00 : 0 mW 0x01 : 32 mW 0x02 : 64 mW 0x03 : 96 mW 0x04 : 128 mW 0x05 : 160 mW 0x06 : 192 mW 0x07 : 224 mW 0x08 : 256 mW 0x09 : 288 mW 0x0A : 320 mW 0x0B : 352 mW 0x0C : 384 mW 0x0D : 416 mW 0x0E : 448 mW Other : Reserved	0x00	R/W
FOD1_STATE	0x02	[7] FOD1_SHORT_DET Short detection of FOD pin. 0x0 : not short 0x1 : short [6:3] FOD1_ADC_VAL The set value based on the read value in A/D. 0xF when the read value in A/D was detected short. 0x0 when the read value in A/D was detected open. 0x1 : -64 mW 0x2 : -32 mW 0x3 : +32 mW 0x4 : +64 mW 0x5 : +96 mW 0x6 : +128 mW 0x7 : +160 mW 0x8 : +192 mW 0x9 : +224 mW 0xA : +256 mW 0xB : +288 mW 0xC : +320 mW 0xD : +352 mW 0xE : +384 mW [2] FOD1_OPEN_DET Enable/ Disable of the register setting. 0x0 : Disable 0x1 : Enable (make FOD pin OPEN to enable this) [1:0] Reserved	0x00	R

Please set an initial value into Reserved bits.

FOD2 register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial Value	R/W
FOD2_SET	0x03	[7] FOD2_REG_EN 0x0 : If FOD2 pin is not OPEN, the setting of this register (bit[5:0]) is invalid. 0x1 : The setting of this register (bit[5:0]) is valid forcibly. [6] Reserved [5:0] FOD2 Setting of the FOD2 value. 0x01 : 1.054 times 0x08 : 1.110 times 0x02 : 1.062 times 0x09 : 1.118 times 0x03 : 1.070 times 0x0A : 1.126 times 0x04 : 1.078 times 0x0B : 1.134 times 0x05 : 1.086 times 0x0C : 1.142 times 0x06 : 1.094 times 0x0D : 1.150 times 0x07 : 1.102 times 0x0E : 1.158 times Other : Reserved	0x07	R/W
FOD2_STATE	0x04	[7] FOD2_SHORT_DET Short detection of FOD2 pin. 0x0 : not short 0x1 : short [6:3] FOD2_ADC_VAL The set value based on the read value in A/D. 0xF when the read value in A/D was detected short. 0x0 when the read value in A/D was detected open. 0x01 : 1.054 times 0x08 : 1.110 times 0x02 : 1.062 times 0x09 : 1.118 times 0x03 : 1.070 times 0x0A : 1.126 times 0x04 : 1.078 times 0x0B : 1.134 times 0x05 : 1.086 times 0x0C : 1.142 times 0x06 : 1.094 times 0x0D : 1.150 times 0x07 : 1.102 times 0x0E : 1.158 times [2] FOD2_OPEN_DET Enable/ Disable of the register setting. 0x0 : Disable 0x1 : Enable (make FOD2 pin OPEN to enable this) [1:0] Reserved	0x00	R

Please set an initial value into Reserved bits.

Depending on the situation, fine tuning of the FOD function and additional EPP setting can be done using the following register.

Register Name	Address	Bit[7:0]	Initial Value	R/W
FOD3_H	0x05	For the fine tuning of Received Power packet value.	0x25	R/W
FOD3_L	0x06	For the fine tuning of Received Power packet value.	0x55	R/W
RCOIL_SET	0x07	For the setting of resistance of coil.	0x05	R/W
IDET_DUMP_I	0x41	For the fine tuning of dump current used for calculating Received Power packet value.	0xC0	R/W
IDET_STATE	0x4C	For the monitor of load current.	0x01	R
DUMP_T	0x4E	For the fine tuning of dump current used for calculating Received Power packet value.	0x00	R/W
T_DP_OFFSET_QI_1	0x51	For the fine tuning of target RECT voltage value.	0x00	R/W
T_DP_OFFSET_QI_2	0x52	For the fine tuning of target RECT voltage value.	0x00	R/W
T_DP_I_THRD_QI	0x55	For the fine tuning of setting with regard to target RECT voltage.	0x00	R/W
CALIB_LL_DP_SET	0x5D	For the fine tuning of target RECT voltage value in EPP mode.	0x00	R/W
ADC_RECT_H	0xC5	For the monitor of RECT voltage.	0x00	R
ADC_RECT_L	0xC6	For the monitor of RECT voltage.	0x00	R

Regarding the detail of these register, Rohm support individually. Because the necessity and the setting value of register are different by the configuration of device such as smart phones.

11. Q value setting

In the Qi standard for EPP it is a requirement for the RX to send FOD Status packet with the information of the Q value to the TX. Then the TX can perform foreign object detection (Foreign Object Detection) . The Q value shown here is a Q value of the coil of the TX when RX is put on Test TX#MP1 as defined in the Qi standard. It is necessary to set it to the following Q value setting register (0x37, 0x3A).

Q value setting register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial Value	R/W
FOD_S_PCKT_EN	0x37	[7] Reserved [6] SEL_FOD_DATA_FUSE 0 : Use the Set Q value in register 0x3A. 1 : Restricted (in EPP mode) [5:1] Reserved [0] FOD_PCKT_EN 0 : Restricted 1 : Enable the sending of the Q value packet (FOD Status packet)	0x41	R/W
FOD_S_PCKT1_1	0x3A	[7:0] FOD_PCKT_B1 Q value sent as FOD Status packet. A Q level does not have a unit. For example, in the case of Q=1, set 0x01.	0x00	R/W

Please set an initial value into Reserved bits.

12. Position Gap detection function during start-up

The RECT voltage at start-up is monitored, and it can detect the position gap of the RX coil in reference to the XY position on the TX coil. The threshold value (Vthpos) used for position gap detection can also be set through the POSSET setting register (0x24).
When the RECT voltage is lower than Vthpos, the interrupt signal can be generated at the INTB pin. By default, this function is disabled. The Position Gap Detection setting register need to be changed to enable this function in the situation that impressed the external power supply on the VCC pin. Detection of the position gap occurs about 30ms after the RX was put on the TX, RECT waked up, and VRECTUV was released. At that time, the interrupt signal would be generated at the INTB pin.

The initial value of Vthpos is the LDO Output Voltage setting value × 40%.

Vthpos is determined using the formula below.
Vthpos = LDO output voltage setting value × set ratio in the register
(Refer to section "*13.OUTSET setting"* for LDO Output Voltage setting.)

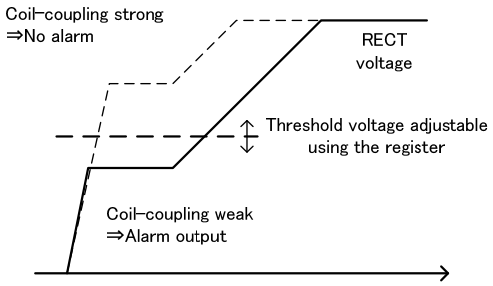


Figure 9. Detection of Position Gap

Position Setting (POSSET) register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
POS_GAP_LV_SET	0x24	[7:4] Reserved [3:0] POS_GAP_LV_SET Set the Vthpos voltage. 0x0 : LDO Output Voltage setting ×40% 0x1 : LDO Output Voltage setting ×45% 0x2 : LDO Output Voltage setting ×50% 0x3 : LDO Output Voltage setting ×55% 0x4 : LDO Output Voltage setting ×60% 0x5 : LDO Output Voltage setting ×65% 0x6 : LDO Output Voltage setting ×70% 0x7 : LDO Output Voltage setting ×75% 0x8 : LDO Output Voltage setting ×80% 0x9 : LDO Output Voltage setting ×85% 0xA : LDO Output Voltage setting ×90% 0xB : LDO Output Voltage setting ×95% 0xC : LDO Output Voltage setting ×100% 0xD : LDO Output Voltage setting ×105% 0xE : LDO Output Voltage setting ×110% 0xF : LDO Output Voltage setting ×115%	0x00	R/W

Please set an initial value into Reserved bits.

Position Gap Detection setting register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
ALIGN_DET_EN	0x21	[7:1] Reserved [0] ALIGN_DET_EN_WAKEUP Position Gap Detection Function Enable (during start up) 0x0 : disable 0x1 : enable	0x00	R/W

Please set an initial value into Reserved bits.

13. OUTPUT Voltage (OUTSET) setting

The Output voltage of the OUT pin could be set by the resistance connected to the OUTSET pin or the register setting, as shown below.

OUT Pin Output Voltage[V]	ROUTSET[kΩ]
OUTSET_SET register setting	OPEN or 470
5.0	75
5.3	56
7.0	43
8.0	36
9.0	30
10.0	24
EPT or NoCh	SHORT

The used resistance should have accuracy of ±1%.

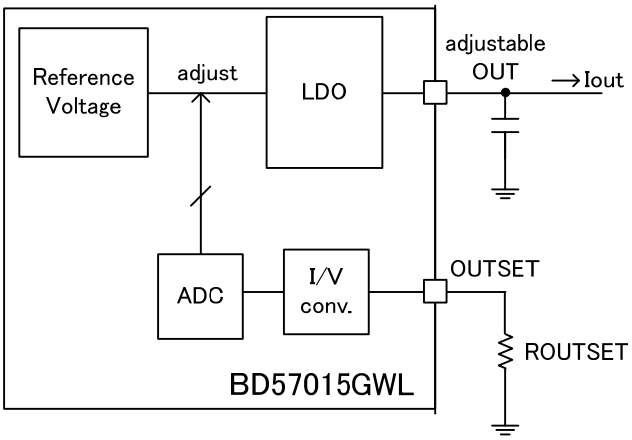


Figure 10. OUTSET setting

If OUTSET pin is shorted to GND, there will be a setting error and BD57015GWL will send EPT (internal fault) in Qi mode. And BD57015GWL will send NoCh signal repeatedly, then the charging will not be started in PMA mode.
If the bit [7] of this register is set to "1", or OUTSET pin is OPEN, the setting of register has priority regardless of the resistance connected to the OUTSET pin. The related states on OUTSET pin can be confirmed depending on the next register (0x09).

OUTSET setting register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
OUTSET_SET	0x08	[7] OUTSET_REG_EN 0x0 : The setting of the resistance has priority. 0x1 : The setting of this register (bit[2:0]) has priority. [6:3] Reserved [2:0] OUTSET Set the LDO output voltage. 0x0 : Restricted setting 0x4 : 8.0V 0x1 : 5.0V 0x5 : 9.0V 0x2 : 5.3V 0x6 : 10.0V 0x3 : 7.0V 0x7 : 12.0V	0x01	R/W
OUTSET_STATE	0x09	OUTSET status [7] OUTSET_SHORT_DET Short detection of the OUTSET pin. 0x0 : not short 0x1 : short [6:4] OUTSET_ADC_VAL Set LDO output voltage on the read value of A/D 0x0 when the read value in A/D is outside the setting range. 0x0 : 4.5V 0x4 : 8.0V 0x1 : 5.0V 0x5 : 9.0V 0x2 : 5.3V 0x6 : 10.0V 0x3 : 7.0V 0x7 : 12.0V [3] OUTSET_OPEN_DET Enable / Disable of the register setting 0x0 : disable 0x1 : enable (make the OUTSET pin OPEN to enable this) [2:0] OUTSET_OUTPUT Actual LDO output voltage to be used 0x0 : 4.5V 0x4 : 8.0V 0x1 : 5.0V 0x5 : 9.0V 0x2 : 5.3V 0x6 : 10.0V 0x3 : 7.0V 0x7 : 12.0V	0x00	R

Please set an initial value into Reserved bits.

14. NTC setting

Please connect the recommended NTC thermistor to the NTC pin when detecting abnormal temperature as described by the PMA standard. An EOC signal will be sent to the Transmitter in the PMA mode when the voltage on the NTC pin is higher than the threshold Vntc0 set in the NTC setting register (0x0C). The abnormal temperature detection in NTC is not available in Qi mode.

In addition to using the NTC thermistor, the EOC signal can also be sent by using the CTRL pin when temperature is monitored. Refer to section "*7.External Control Input (EN1, EN2, and CTRL)*" for the details. (Common to both PMA and Qi modes.)

The Vntc0 threshold can be defined in the following expressions.

$$Vntc0 = \frac{\mathrm{Vref_{ntc}}}{\mathrm{Rntc}} \times \mathrm{Rntc0}$$
$$= \frac{25000^{(\mathrm{NOTE1})}[\Omega \times \mathrm{V}]}{\mathrm{Rntc}[\Omega]}$$

(NOTE1) precision includes variation of 21250 to 28750.

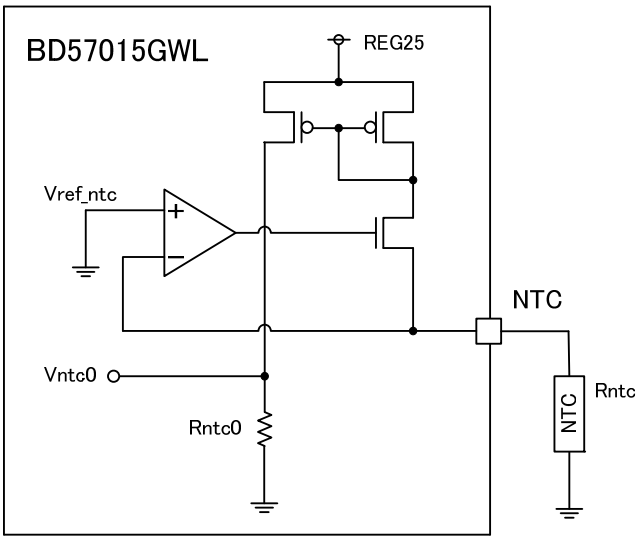


Figure 11. NTC setting

NTC setting register (Only for PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
NTC_SET	0x0C	[7] Reserved [6] NTC_EN (PMA mode) NTC temperature detection function 0x0 : NTC temperature detection function disabled 0x1 : NTC temperature detection function enabled [5:4] Reserved [3:0] NTC_TH Vntc0 threshold setting for the abnormal temperature detection 0x0 : more than 0.5 V 0x1 : more than 0.6 V 0x2 : more than 0.7 V 0x3 : more than 0.8 V 0x4 : more than 0.9 V 0x5 : more than 1.0 V 0x6 : more than 1.1 V 0x7 : more than 1.2 V 0x8 : more than 1.3 V 0x9 : more than 1.4 V 0xA : more than 1.5 V 0xB : more than 1.6 V 0xC : more than 1.7 V 0xD : more than 1.8 V 0xE : more than 1.9 V 0xF : more than 2.0 V	0x44	R/W
NTC_STATE	0X0D	[7:1] Reserved [0] NTC_DET Abnormal temperature detection for NTC. 0x0 : Abnormal temperature undetected 0x1 : Abnormal temperature detected	0x00	R

Please set an initial value into Reserved bits.

Rohm recommends NTC thermistor NCP15WF104F03RC (MURATA Co., Ltd.).

Resistance value (25°C)	100kΩ
Resistance value (25°C) tolerance	±1%
B constant (25/50°C)	4250K
B constant (25/50°C) tolerance	±1%
B constant (25/85°C)(Typ)	4311K

15. PAD_DETECTION

The PAD_DETECTION function can send a signal to the host when the RX is removed from the TX after charging has been completed. To use this function, connect the external power supply to the VCCPD, with a pull-up resistance to PD and connect to the VCCPD.
The host can detect when the PD signal changes from L to H to monitor if it was removed from the charger.

The flow to the detection
1. After end of charging, Rx receives Digital Ping or Analog Ping signal from Tx. (AC2 of figure below)
2. The Ping fully charges a capacitor connected to PD_TIME pin to VCCPD. PD pin goes L.
3. If Rx is removed from Tx the pulse to AC2 is not generated, so the voltage on PD_TIME pin falls. The PD pin will go H after a time dependent on the CR network.

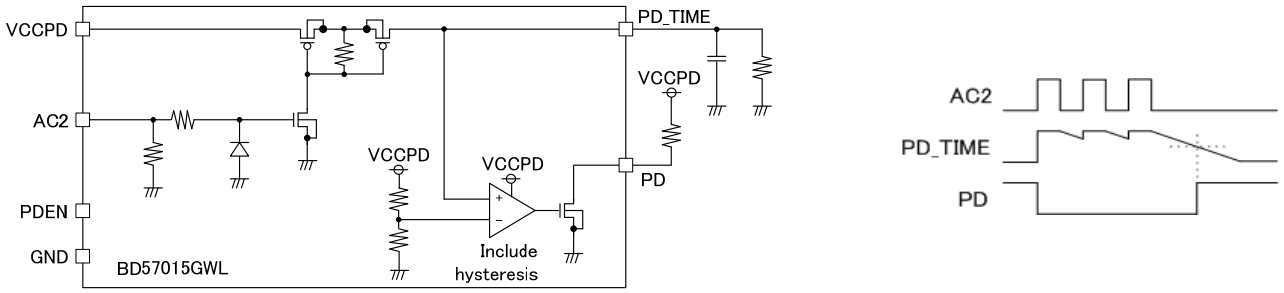


Figure 12. PAD_DETECTION

16. Interrupt Control Block

The circuit for Interruption Generation is shown below.
This circuit detects the edge of the interrupt signal. An interrupt is sent on INTB pin depending on the events triggering the interrupt as set by the Interrupt Mask register. INTB is active L.

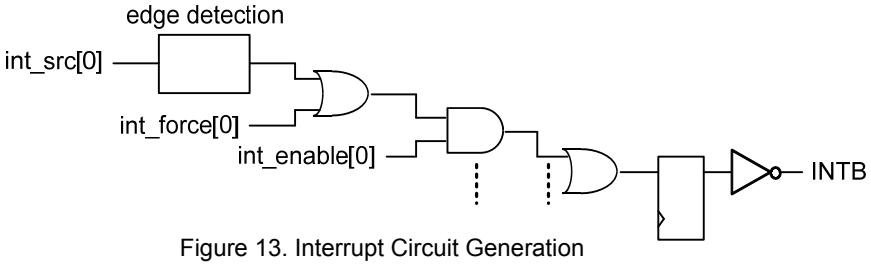


Figure 13. Interrupt Circuit Generation

16.1 Interrupt Control Register

The generation of interruption for each can be controlled by this register. If a bit is set to 1, the corresponding interrupt event will be enabled, if it is set to 0, it will be masked. The interrupt is masked by default.

Interrupt Control register 1 (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
INTEN1	0x10	[7:6] Reserved [5] INT_EN_PMA_EOC PMA EOC interrupt detection activation setting [4:2] Reserved [1] INT_EN_EPT_DET End Power Transfer interrupt detection activation setting [0] INT_EN_CHG_START_DET Charging start interrupt detection activation setting	0x00	R/W

Please set an initial value into Reserved bits.

Interrupt Control register 2 (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
INTEN2	0x11	[7:2] Reserved [1] INT_EN_ERR_POSSET_CLR Clear POSSET Error interrupt detection activation setting (During start-up) [0] INT_EN_ERR_POSSET POSSET Error interrupt detection activation setting (During start-up)	0x00	R/W

Please set an initial value into Reserved bits.