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DC Brushless Fan Motor Drivers

Multifunction Single-phase Full-wave Fan Motor Driver

BD61241FV

General Description

BD61241FV is a 1chip driver that is composed of H-bridge power DMOS FET. The pin is compatible with BD61240FV(rotation speed pulse signal output).

Features

- SSOP Small Package
- Driver Including Power DMOS FET
- Speed Controllable by DC / PWM Input
- I/O Duty Slope Adjust
- PWM Soft Switching
- Current Limit
- Start Duty Assist
- Lock Protection and Automatic Restart
- Quick Start
- Lock alarm signal (AL) output

Applications

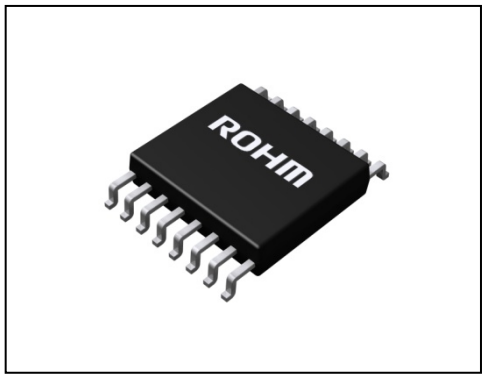
- Fan motors for general consumer equipment of desktop PC, Projector, etc.

Key Specifications

- Operating Voltage Range: 5.5V to 16V
- Operating Temperature Range: -40°C to +105°C
- Output Voltage (Total): 0.2V(Typ) at 0.2A

Package

W(Typ) x D(Typ) x H(Max)
5.00mm x 6.40mm x 1.35mm



SSOP-B16

Typical Application Circuits

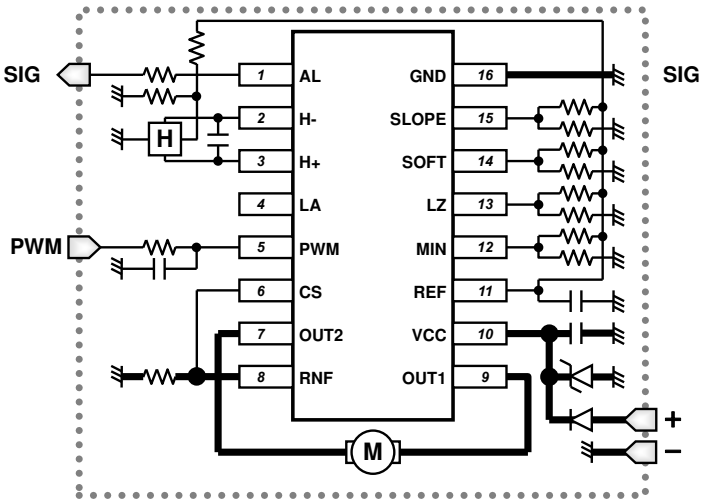


Figure 1. Application of PWM Input

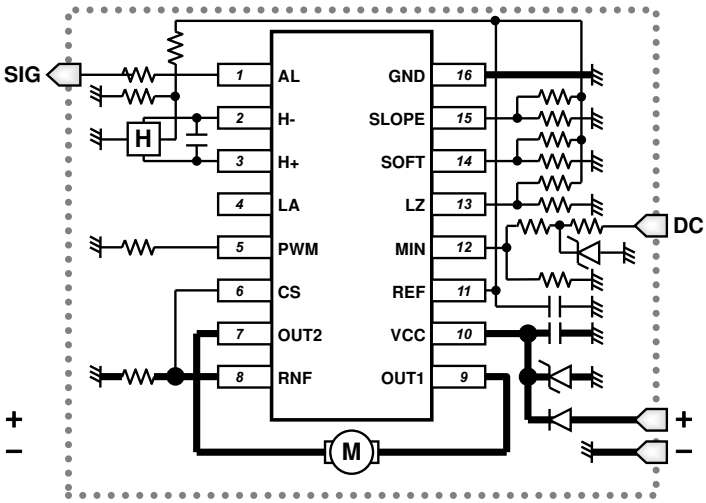
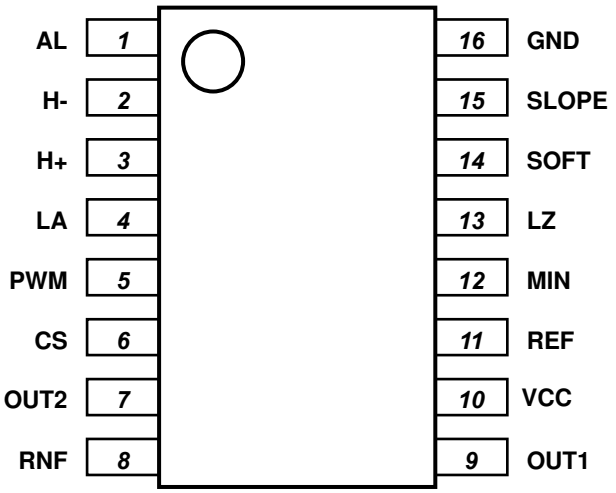


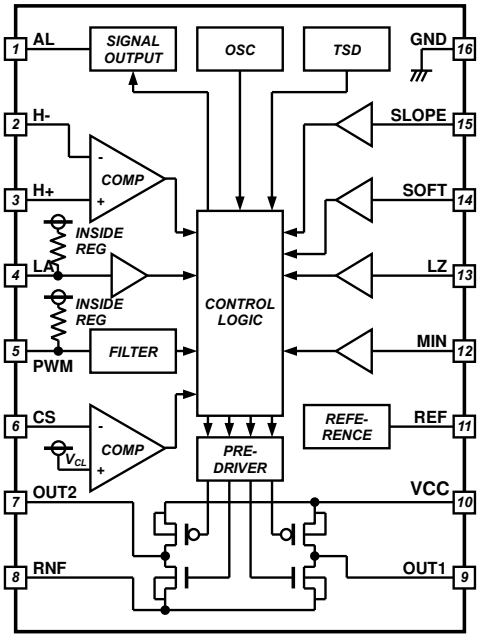
Figure 2. Application of DC Voltage Input

Pin Configuration

(TOP VIEW)



Block Diagram



Pin Description

Pin No.	Pin Name	Function
1	AL	Lock alarm signal output terminal
2	H–	Hall – input terminal
3	H+	Hall + input terminal
4	LA	Lead angle function select terminal
5	PWM	PWM input duty terminal
6	CS	Output current detecting terminal
7	OUT2	Motor output terminal 2
8	RNF	Output current detecting resistor connecting terminal (motor ground)
9	OUT1	Motor output terminal 1
10	VCC	Power supply terminal
11	REF	Reference voltage output terminal
12	MIN	Minimum output duty setting terminal
13	LZ	Recirculate period setting terminal
14	SOFT	Soft switching setting terminal
15	SLOPE	I/O duty slope setting terminal
16	GND	Ground terminal (signal ground)

I/O Truth Table

Hall Input		Driver Output	
H+	H–	OUT1	OUT2
H	L	L	H
L	H	H	L

H; High, L; Low

Motor state	AL
Rotating	L
Locking	Hi-Z

AL output is open-drain type.

Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Supply Voltage	V_{CC}	18	V
Power Dissipation	Pd	0.87 (Note 1)	W
Operating Temperature Range	Topr	-40 to +105	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Output Voltage	V_O	18	V
Output Current	I_O	1.2 (Note 2)	A
Lock Alarm Signal (AL) Output Voltage	V_{AL}	18	V
Lock Alarm Signal (AL) Output Current	I_{AL}	10	mA
Reference Voltage (REF) Output Current	I_{REF}	10	mA
Input Voltage1 (H+,H–,MIN,CS,LA,SOFT,LZ,SLOPE)	V_{IN1}	3.6	V
Input Voltage2 (PWM)	V_{IN2}	6.5	V
Junction Temperature	Tj	150	°C

(Note 1) Reduce by 7.0mW/°C when operating over Ta=25°C. (Mounted on 70.0mm×70.0mm×1.6mm glass epoxy board)
(Note 2) Do not exceed Pd.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Limit	Unit
Operating Supply Voltage Range	V_{CC}	5.5 to 16	V
Input Voltage Range1 (H+, H–, MIN, LA, SOFT, LZ, SLOPE)	V_{IN1}	0 to V_{REF}+0.3	V
Input Voltage Range2 (CS)	V_{IN2}	0 to 1/2 x V_{REF}	V
Input Voltage Range3 (PWM)	V_{IN3}	0 to 5	V
PWM Input Duty Range	D_{PWM}	0 to 100	%
PWM Input Frequency Range	f_{PWM}	15 to 50	kHz

Electrical Characteristics (Unless otherwise specified Ta=25°C, V_{CC}=12V)

Parameter	Symbol	Limit			Unit	Conditions	Reference Data
		Min	Typ	Max			
Circuit Current	I_{CC}	3.0	4.5	6.5	mA		Figure 3
Output Voltage	V_O	-	0.2	0.35	V	I_{OUT}=±200mA, high and low side total	Figure 4 to Figure 7
Lock Detection ON Time	t_{ON}	0.3	0.5	0.7	s		Figure 8 to Figure 10
Lock Detection OFF Time	t_{OFF}	3.0	5.0	7.0	s		
Hall Input Hysteresis Voltage+	V_{HYS}+	7	12	17	mV		Figure 11
Hall Input Hysteresis Voltage-	V_{HYS}-	-5	-10	-15	mV		
AL Output Low Voltage	V_{ALL}	-	-	0.30	V	I_{AL}=5mA	Figure 12 to Figure 13
AL Output Leak Current	I_{ALL}	-	-	10	µA	V_{AL}=16V	Figure 14
PWM Input High Level Voltage	V_{PWMH}	2.5	-	5.0	V		-
PWM Input Low Level Voltage	V_{PWML}	0.0	-	1.0	V		-
PWM Input Current	I_{PWMH}	-10	0	10	µA	V_{PWM}=5V	Figure 15 to Figure 16
	I_{PWML}	-50	-25	-12	µA	V_{PWM}=0V	
Reference Voltage	V_{REF}	3.0	3.3	3.6	V	I_{REF}=-1mA	Figure 17 to Figure 18
Current Limit Setting Voltage	V_{CL}	235	265	295	mV		Figure 19
LA Input High Level Voltage	V_{LAH}	2.5	-	3.3	V		-
LA Input Low Level Voltage	V_{LAL}	0.0	-	1.0	V		-
LA Input Current	I_{LAH}	-10	0	10	µA	V_{LA}=REF	Figure 20
	I_{LAL}	-0.47	-0.33	-0.25	mA	V_{LA}=0V	Figure 21
CS Input Bias Current	I_{CS}	-0.4	-	-	µA	V_{CS}=0V	Figure 22

For parameters involving current, positive notation means inflow of current to IC while negative notation means outflow of current from IC.

Typical Performance Curves (Reference Data)

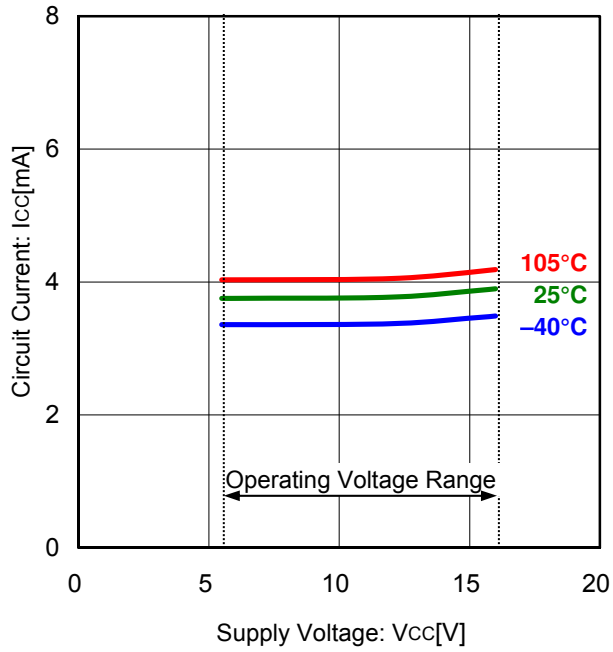


Figure 3. Circuit Current vs Supply Voltage

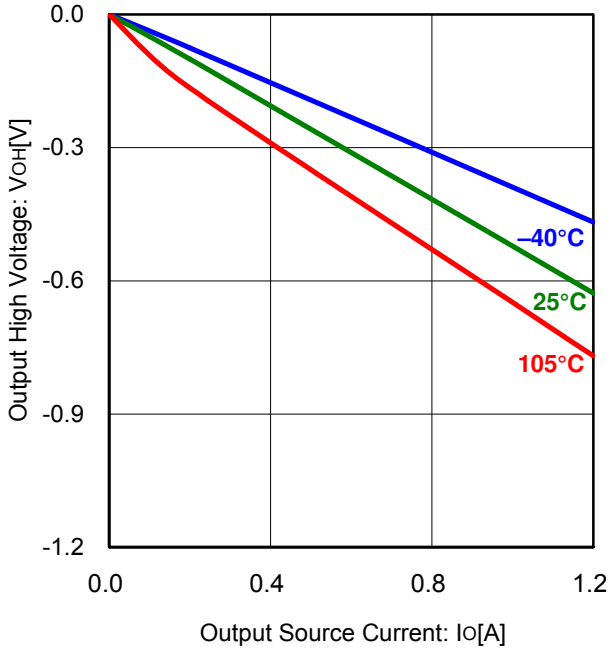


Figure 4. Output High Voltage vs Output Source Current (VCC=12V)

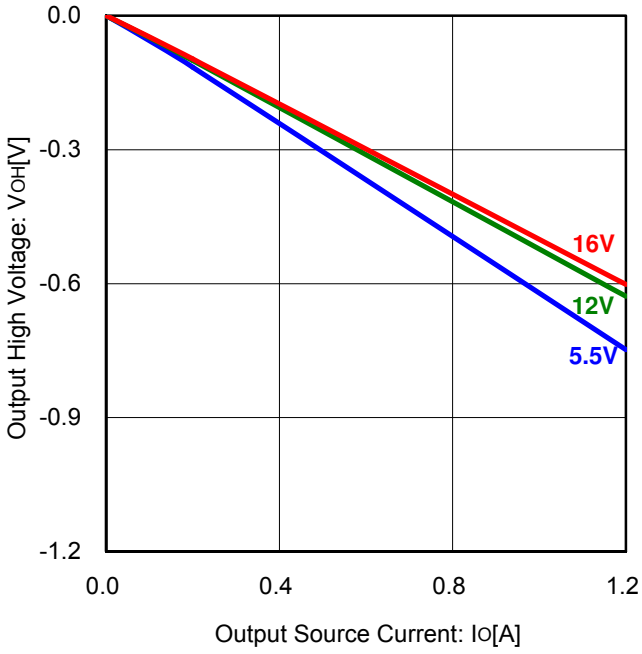


Figure 5. Output High Voltage vs Output Source Current

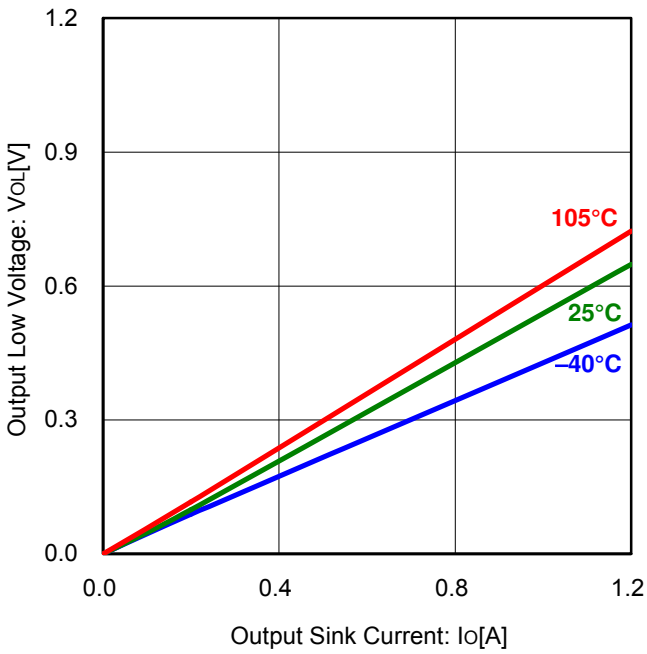


Figure 6. Output Low Voltage vs Output Sink Current (VCC=12V)

Typical Performance Curves (Reference Data) – continued

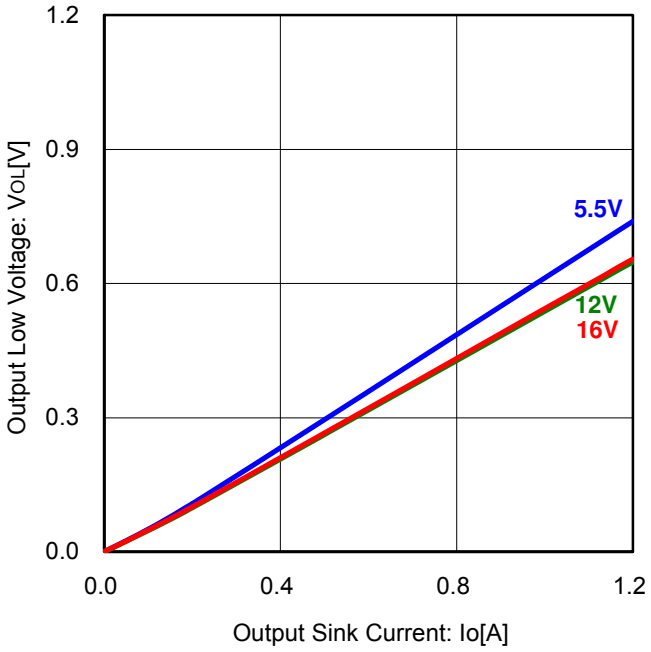


Figure 7. Output Low Voltage vs Output Sink Current (Ta=25°C)

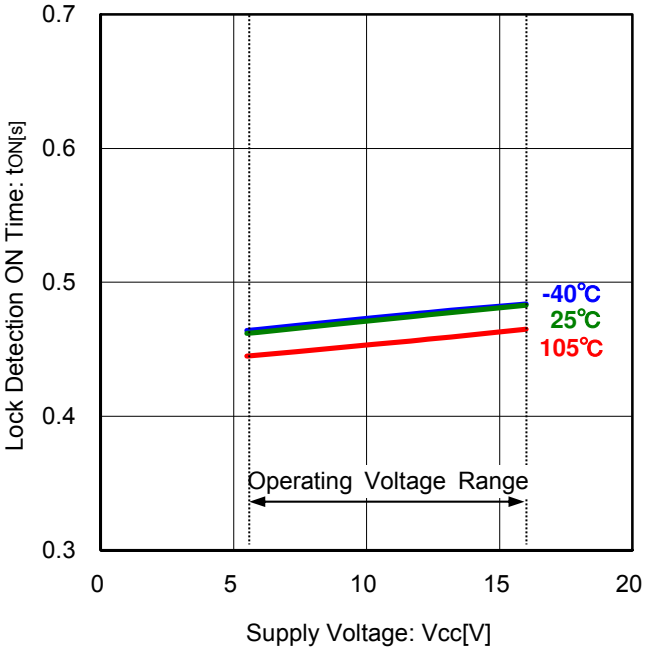


Figure 8. Lock Detection ON Time vs Supply Voltage

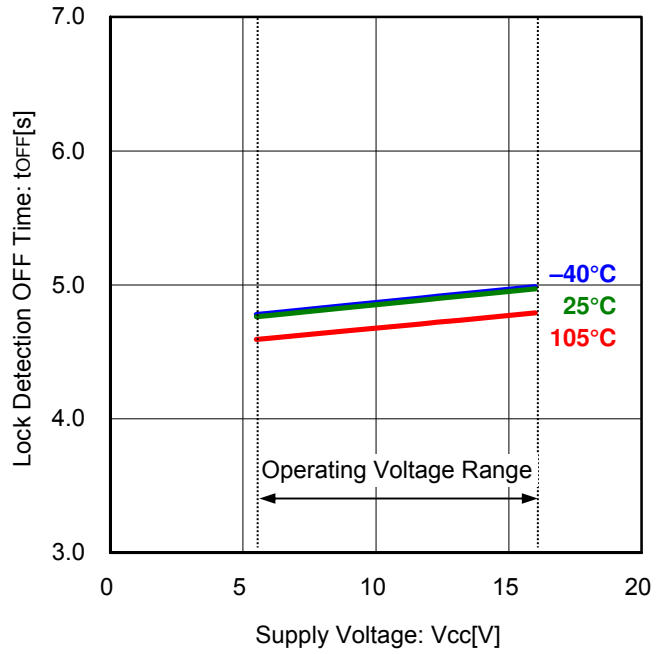


Figure 9. Lock Detection OFF Time vs Supply Voltage

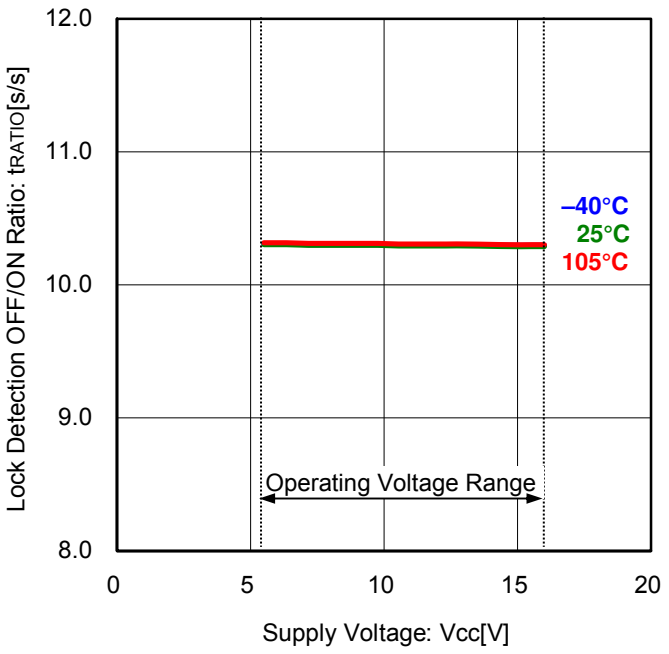


Figure 10. Lock Detection OFF/ON Ratio vs Supply Voltage

Typical Performance Curves (Reference Data) – continued

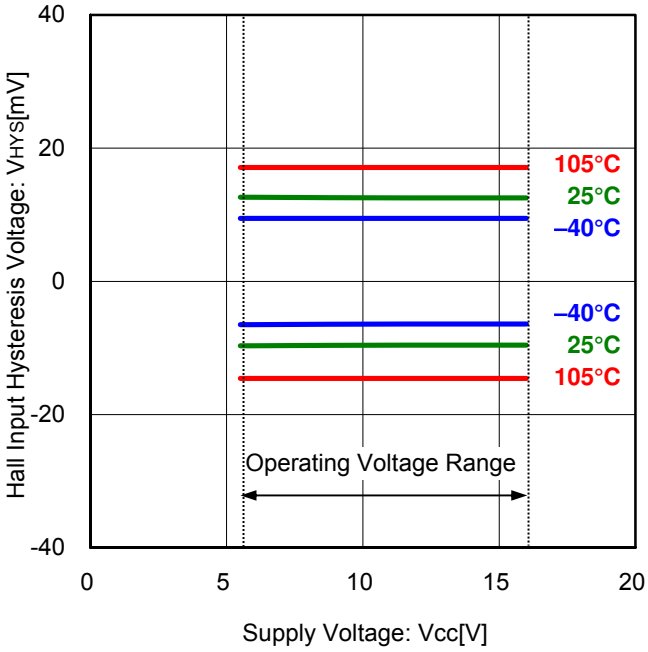


Figure 11. Hall Input Hysteresis Voltage vs Supply Voltage

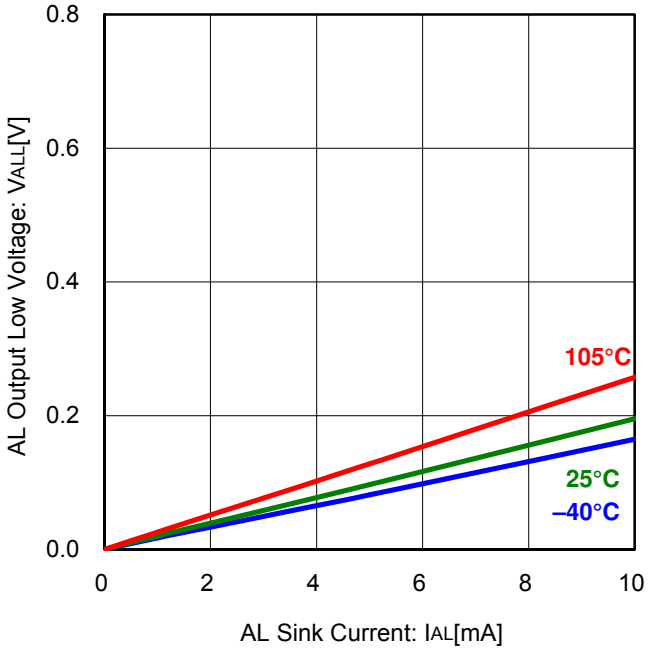


Figure 12. AL Output Low Voltage vs FG Sink Current (VCC=12V)

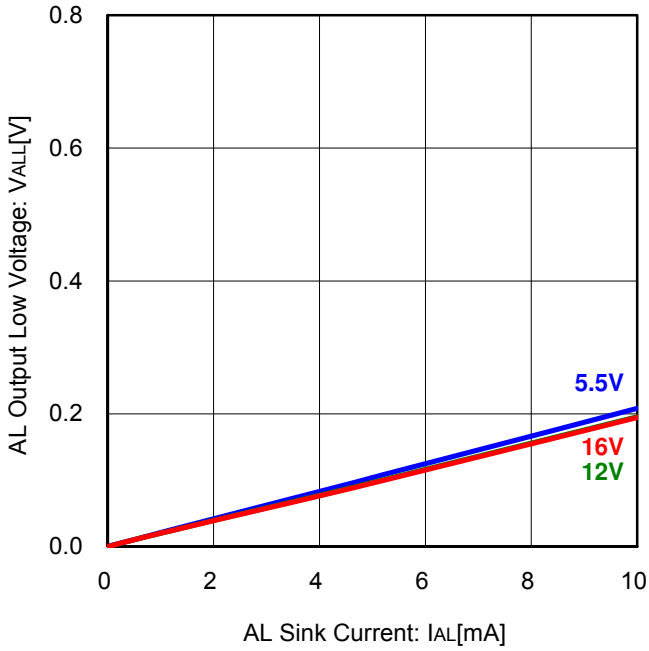


Figure 13. AL Output Voltage vs AL Sink Current (Ta=25°C)

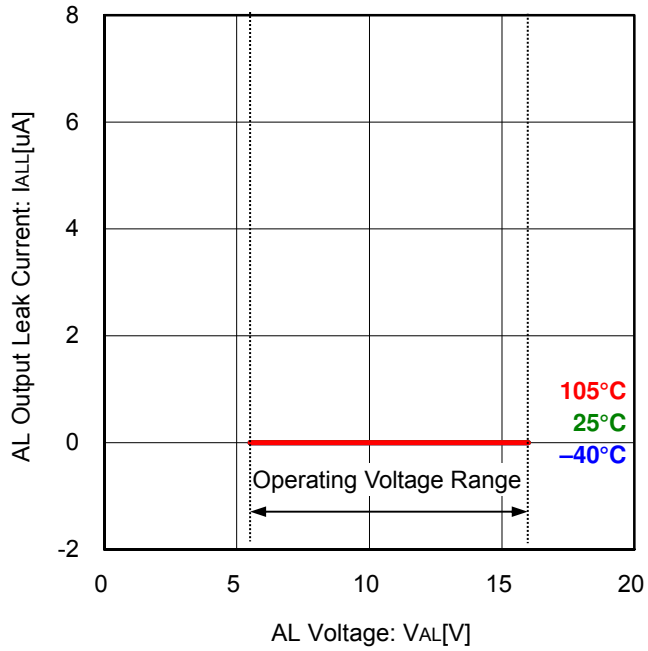


Figure 14. AL Output Leak Current vs AL Voltage

Typical Performance Curves (Reference Data) – continued

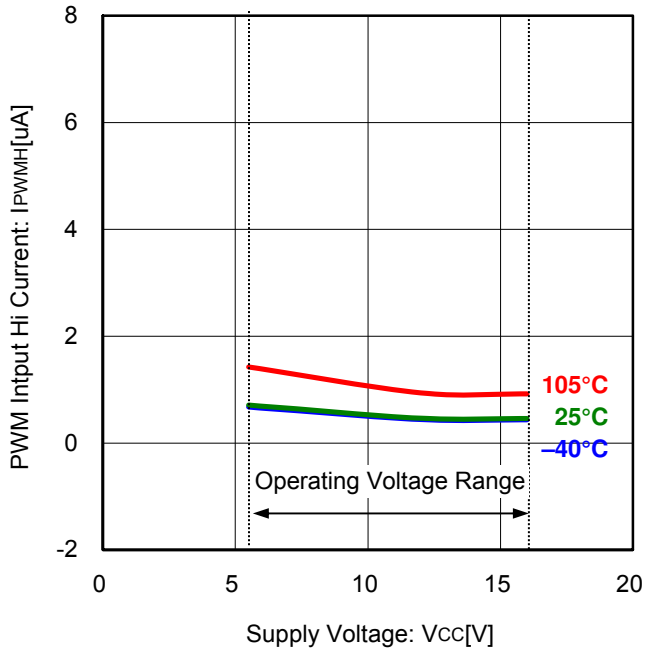


Figure 15. PWM Input Hi Current vs Supply Voltage

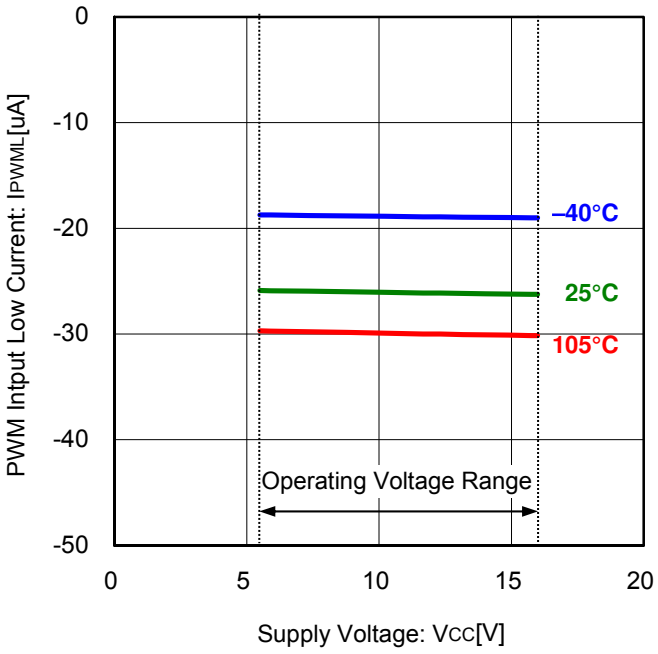


Figure 16. PWM Input Low Current vs Supply Voltage

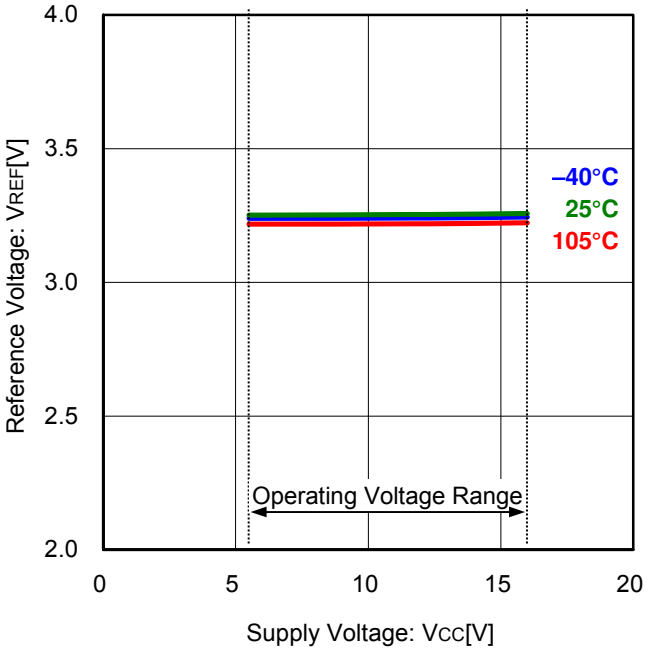


Figure 17. Reference Voltage vs Supply Voltage
(IREF=-1mA)

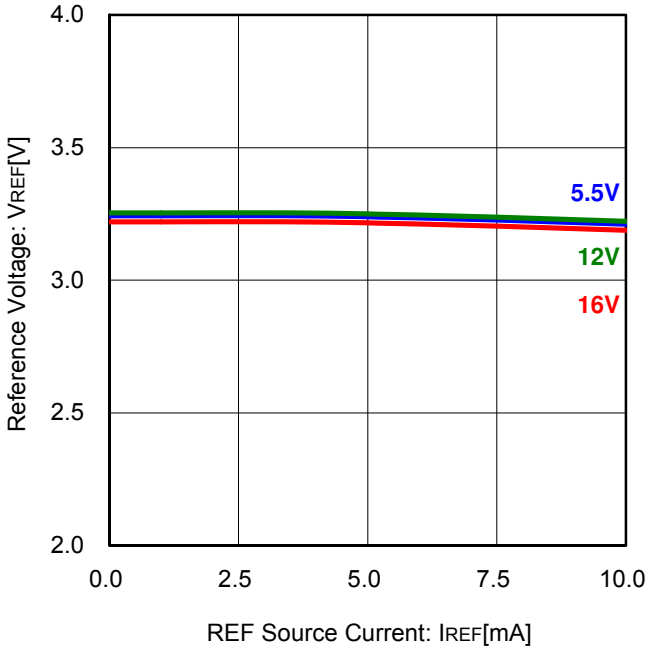


Figure 18. Reference vs REF Source Current
(VCC=12V)

Typical Performance Curves (Reference Data) – continued

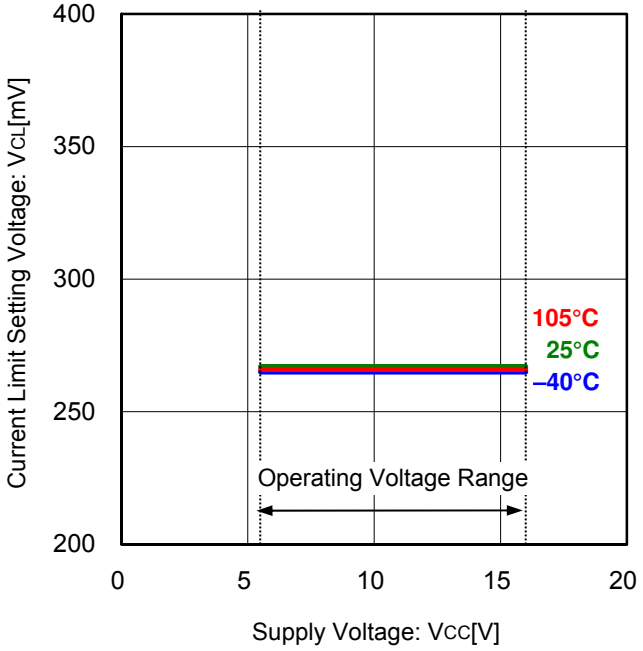


Figure 19. Current Limit Setting Voltage vs Supply Voltage

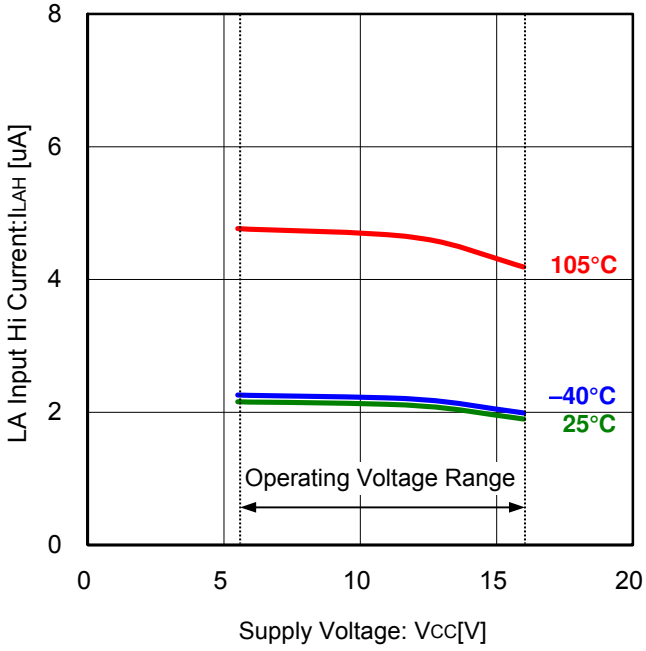


Figure 20. LA Input Hi Current vs Supply Voltage

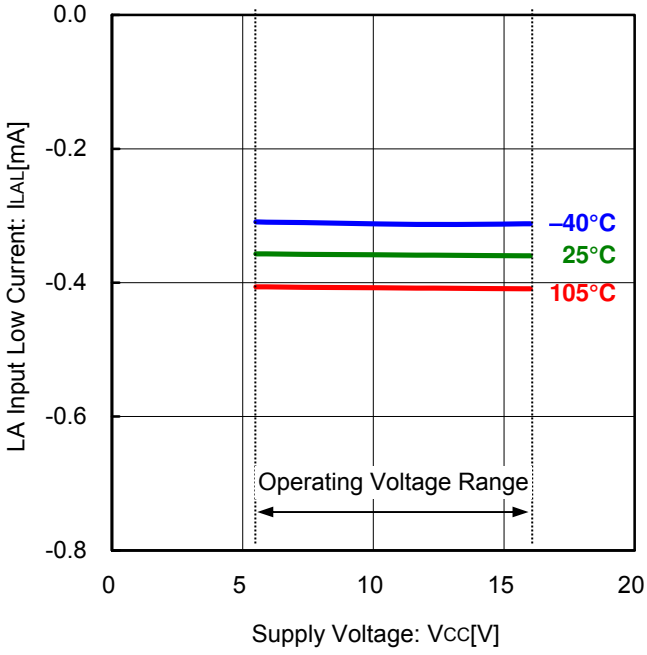


Figure 21. LA Input Low Current vs Supply Voltage

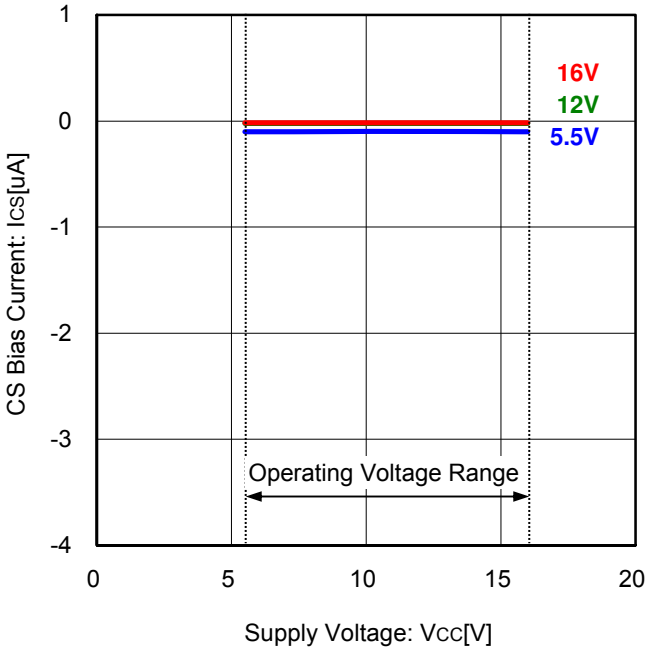


Figure 22. CS Input Bias Current vs Supply Voltage

Application Information

Application Circuit Examples (Constant Values are for Reference)

1. PWM Input Application

This is an example of the application of inverting the external PWM input, and controlling the rotational speed. In this application, minimum rotational speed can be set.

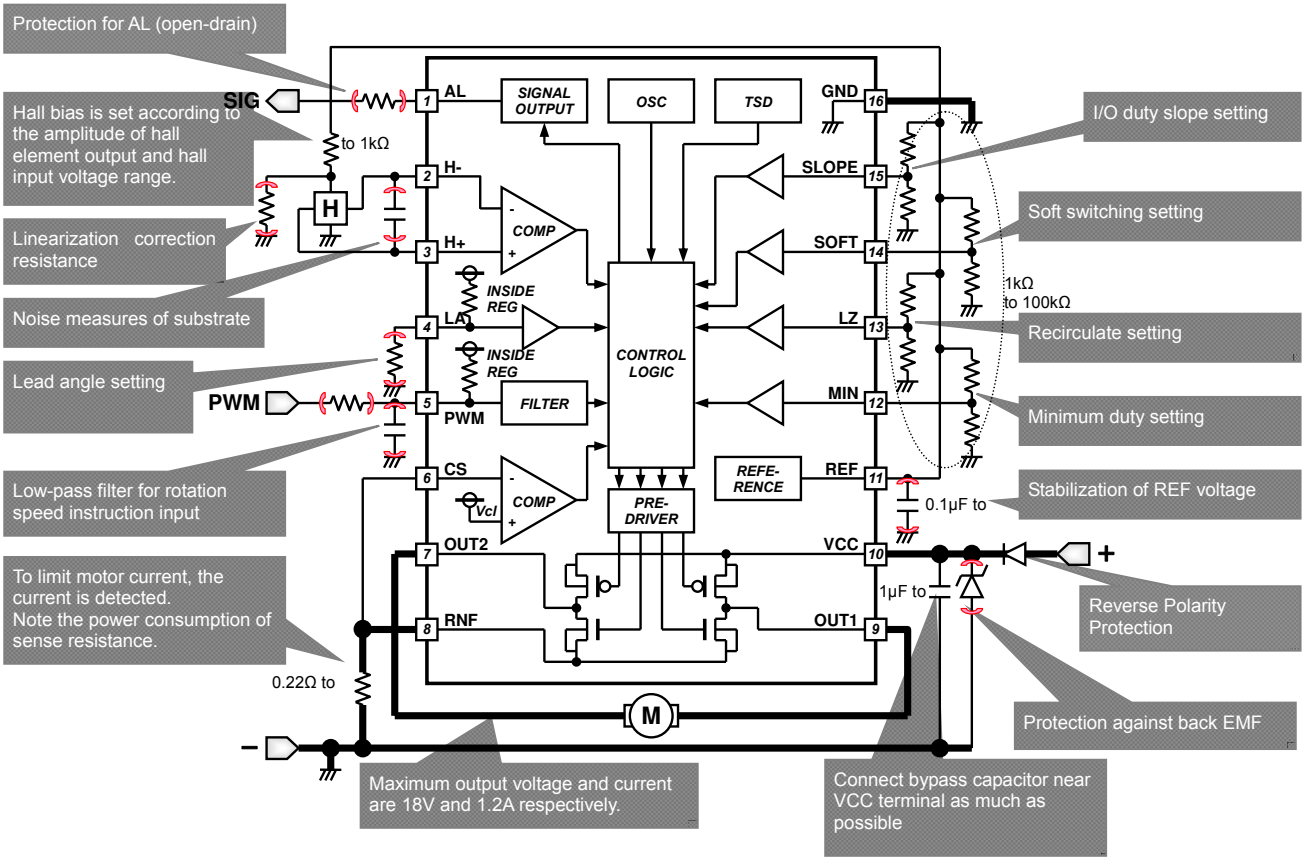


Figure 23. PWM Input Application

Application Design Note

(a) The bypass capacitor connected must be more than the recommended constant value because there is a possibility of the motor start-up failure etc. due to IC malfunction.

Substrate Design Note

(a) IC power (V_{CC}), motor outputs (OUT1, 2), and motor ground lines are made as wide as possible.
(b) IC ground (GND) line is common with the application ground except motor ground (i.e. hall ground etc.), and arranged near to (–) land.
(c) The bypass capacitor and/or Zener diode are placed near to VCC pin.
(d) H+ and H– lines are arranged side by side and made from the hall element to IC as short as possible, because it is easy for the noise to influence the hall lines.

2. DC Voltage Input Application

This is an example application circuit for fixed rotation speed control by DC voltage. In this application, minimum rotational speed cannot be set.

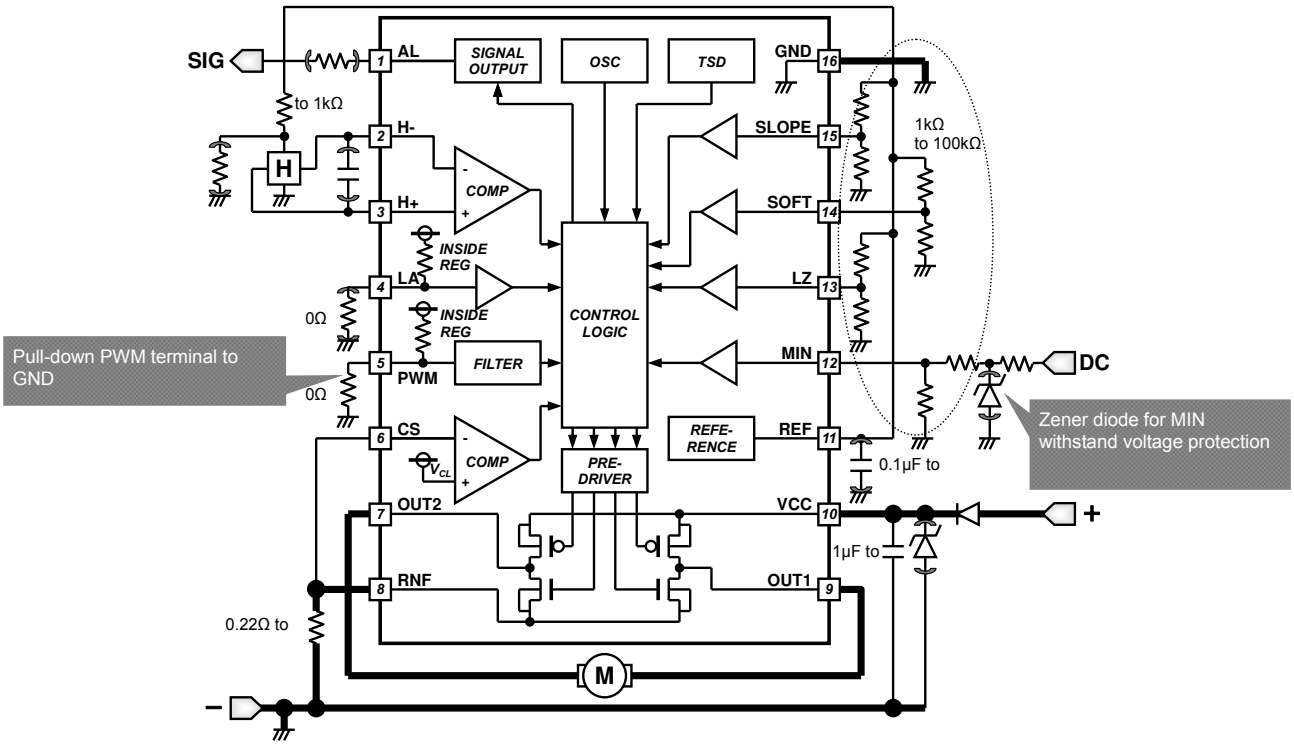


Figure 24. DC Voltage Input Application

Functional Descriptions

1. Variable Speed Operation

The rotational speed of the motor changes by the PWM duty of the motor outputs (OUT1 and OUT2 terminals). However, it provides for the motor's output not by the rotational speed but by the duty in the BD61241FV, because the rotational speed is not uniquely decided by the motor output duty.
The changeable speed operation is controlled by these two input terminals.

(1) PWM Operation by Pulse Input in PWM Terminal
(2) PWM Operation by DC Input in MIN Terminal
(Note) PWM frequency of output is 50kHz (Typ). Hence, input PWM frequency is not equal to PWM frequency of output.

(1) PWM Operation by Pulse Input in PWM Terminal

The PWM signal from the controller can be input directly to IC in Figure 25. The output duty is controlled by the input PWM duty (Figure 26). Refer to recommended operating conditions (P.3) and electrical characteristics (P.4) for the input condition.
Internal power-supply voltage (INTERNAL REG; Typ 5.0V) is impressed when the PWM terminal is open, it becomes 100% input of the duty and equivalent, and a full torque is driven. There must be a pull-down resistance outside of IC to make it to torque 0 when the PWM terminal opens (However, only at the controller of the complimentary output type.). Insert the protective resistance and capacitor for noise removal if necessary.

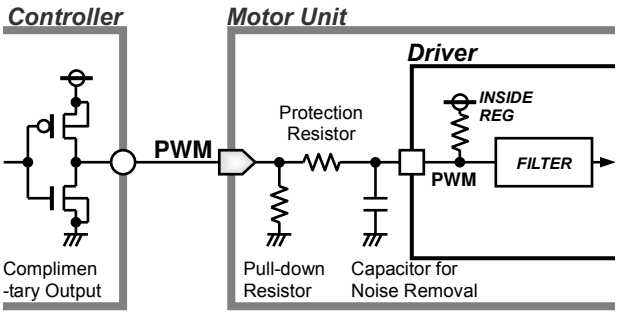


Figure 25. PWM Input Application

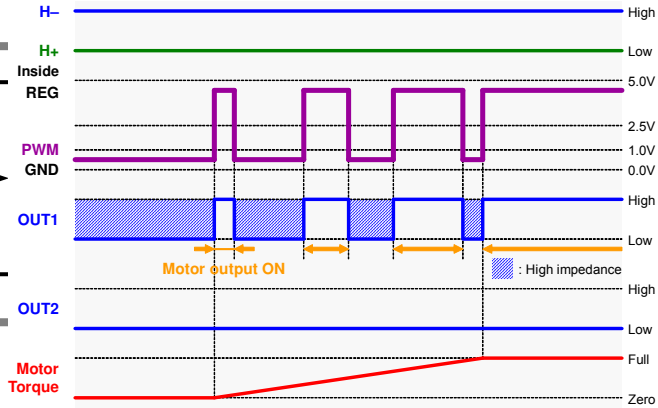


Figure 26. PWM Input Operation Timing Chart

Full torque (V_{PWM}>2.5V) and zero torque (V_{PWM}<1.0V) can recognize the DC voltage input of the PWM terminal. However, the variable speed control in the DC voltage between 0V and 5.0V should be not able to be done.

(a) Setting of Minimum Output Duty (MIN)

Minimum rotational speed can be set by MIN terminal in Figure 27. The resolution of the MIN terminal is 128 steps. MIN terminal should be shorted to GND when this function is not used.

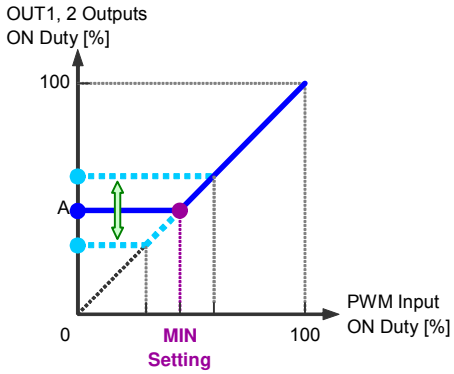


Figure 27. Setting of Minimum Output Duty

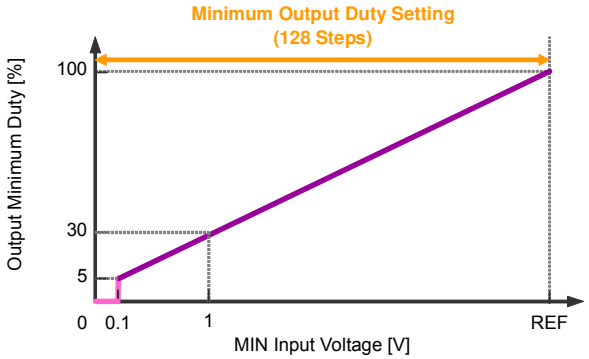


Figure 28. Relation of MIN Input Voltage and Output Duty

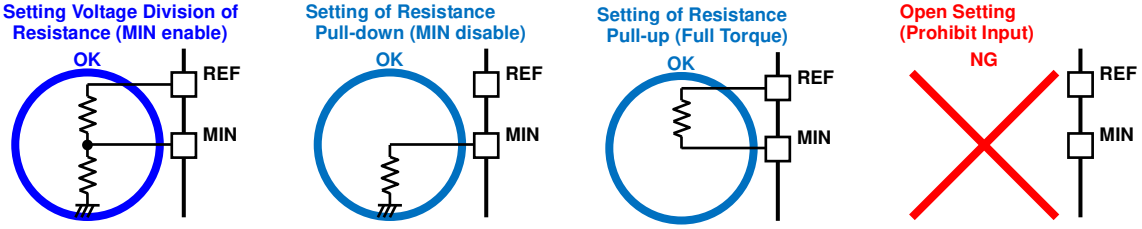


Figure 29. MIN Terminal Setting

(b) Setting of Slope of I/O Duty (SLOPE)

Slope of output duty and the input duty to PWM terminal can be established by SLOPE setting in Figure 30. The resolution of MIN is 128 steps. But if the voltage of the SLOPE terminal is 0.4V to 0.825V (Typ), then the slope of the input and output duty is fixed to 0.5, and if it is less than 0.4V (Typ) the slope is fixed to 1 (Figure 31). SLOPE terminal should be shorted to GND when this function is not used.

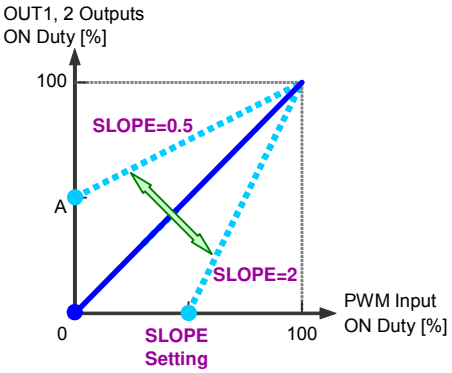


Figure 30. Adjust of Slope of I/O Duty

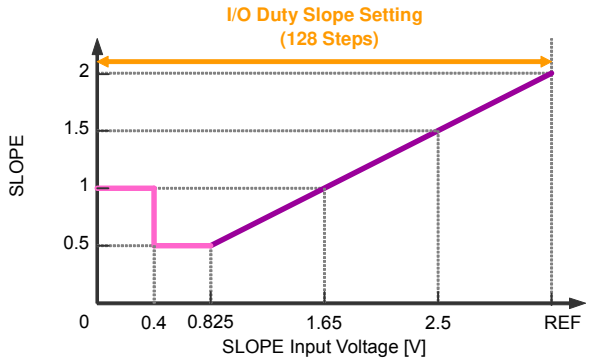


Figure 31. Relation of SLOPE Voltage and Slope of I/O Duty

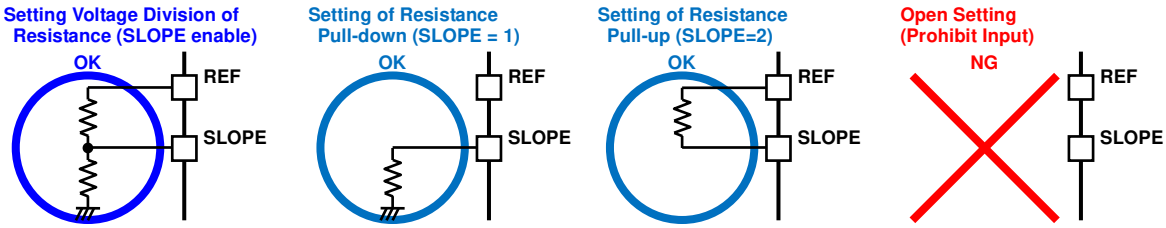


Figure 32. SLOPE Terminal Setting

(2) PWM Operation by DC Input in MIN Terminal

The output duty can be varied by inputting DC voltage into MIN terminal. PWM terminal should be shorted to GND when this function is used. Please refer to input voltage range 1(P.3) for the input condition of the MIN terminal. MIN Terminal voltage becomes unsettled when MIN terminal is in an open state. The voltage of the terminal becomes irregular if MIN terminal is open. Input voltages to MIN terminals when you turn ON IC power supply (V_{CC}) in Figure 32.

*In the case of DC voltage input, it cannot set the lowest output duty.

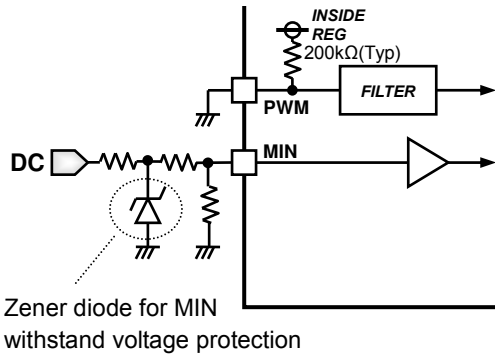


Figure 33. DC Input Application

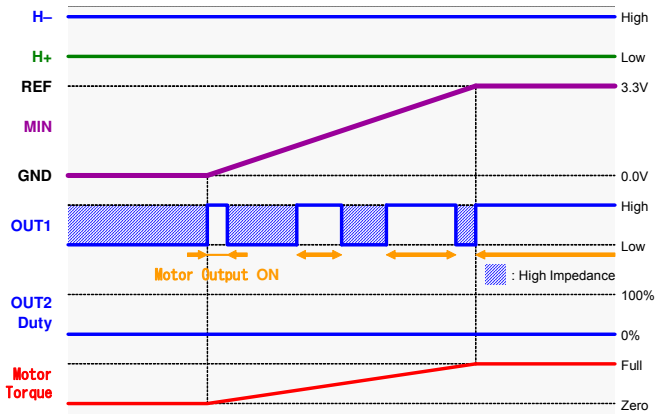


Figure 34. DC Input Operation Timing Chart

(a) Setting of Slope of I/O Duty (SLOPE)

Slope of output duty and the input voltage to MIN terminal can be established by SLOPE setting in Figure 35. The resolution of SLOPE is 128 steps. But if the voltage of the SLOPE terminal is 0.4V to 0.825V (Typ), then the slope of the input and output duty is fixed to 0.5, and if it is less than 0.4V (Typ) the slope is fixed to 1 (Figure 31). SLOPE terminal should be shorted to GND when this function is not used.

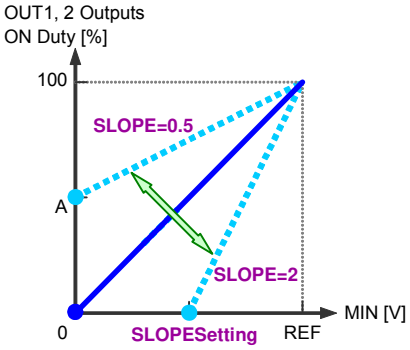


Figure 35. Relation of MIN Input Voltage and Slope of I/O Duty

2. About Setting of Phase Switching of Output

The period of Soft Switching and Recirculate can be adjusted by SOFT and LZ setting.

(1) Soft Switching Period Setting (SOFT)

The soft switching section in the output can be set by SOFT terminal. By adjusting SOFT voltage, soft switching section can be set from 22.5° to 90° as one period of hall signal 360°. The resolution of SOFT is 128 steps in Figure 37. Timing chart is shown in Figure 36.

*A soft switching period is the section where ON duty of the output changes from a target duty into 0% by 16 steps.

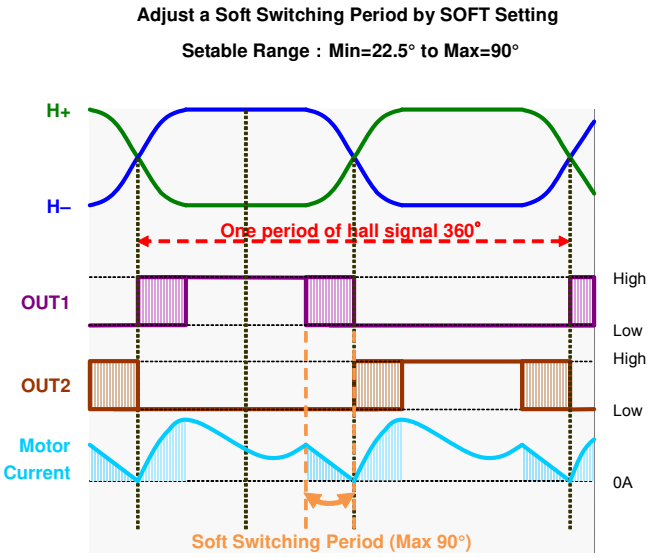


Figure 36. Soft Switching Period Setting

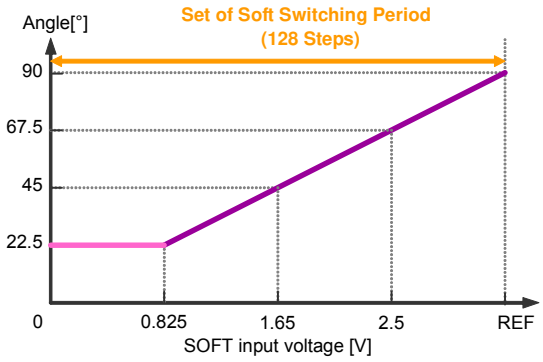


Figure 37. Relation of SOFT Input Voltage and Soft Switching Period

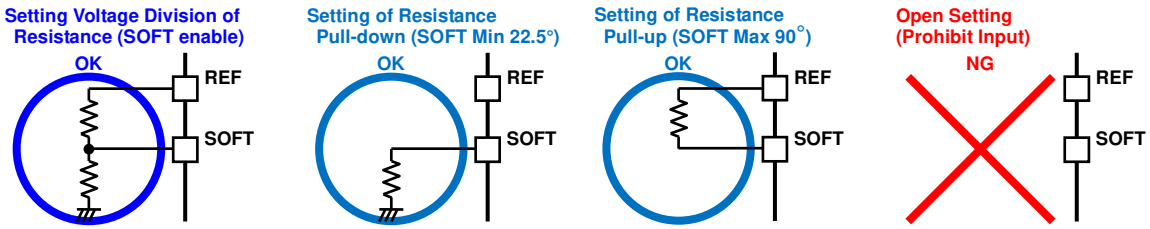


Figure 38. SOFT Terminal Setting

(2) Recirculate Period Setting (LZ)

The recirculate period in fall of the output can be set by LZ terminal. By adjusting LZ voltage, recirculate period can be set from 0° to 90° as one period of hall signal 360° in Figure 40. The resolution of LZ is 128 steps. Timing chart is shown in Figure 39.

About priority of SOFT and LZ setting, the setting priority of the period to recirculate than a soft switching period is high.

For example, V_{SOFT}=1.65V, V_{LZ} = 0.825V

Soft switching period = (1.65/3.3)*90° - (0.825/3.3)*90°=45°-22.5°=22.5°

Recirculate period = (0.825/3.3)*90°=22.5°

When you set a period to recirculate for longer than soft switching period, a soft switching section for 5.6° (Typ) enters.

* A recirculate period is a current recirculate period before phase switching of output.
In the recirculate period, the logic of the output transistor is decided by the hall input logic.
The phase of output Hi becomes the high impedance, and the phase of output Low is Low.

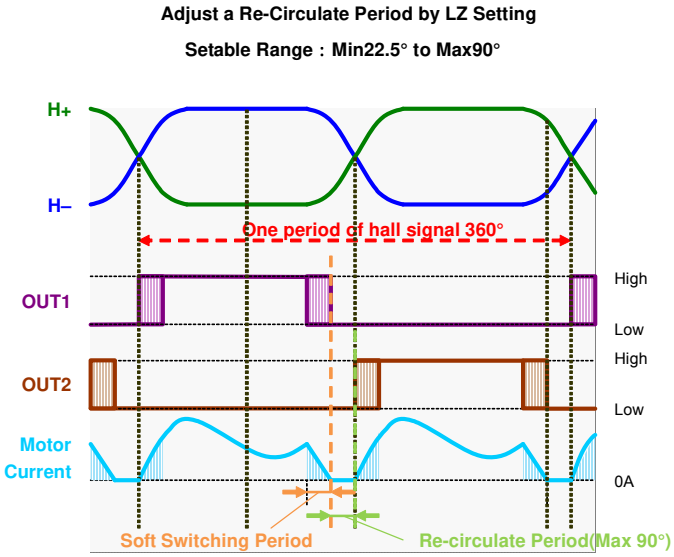


Figure 39. Recirculate Period Setting

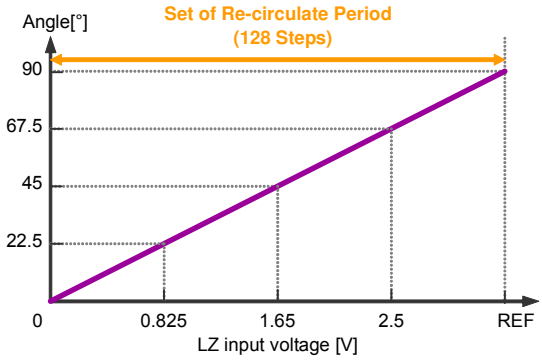


Figure 40. Relation of LZ Input Voltage and Recirculate Period

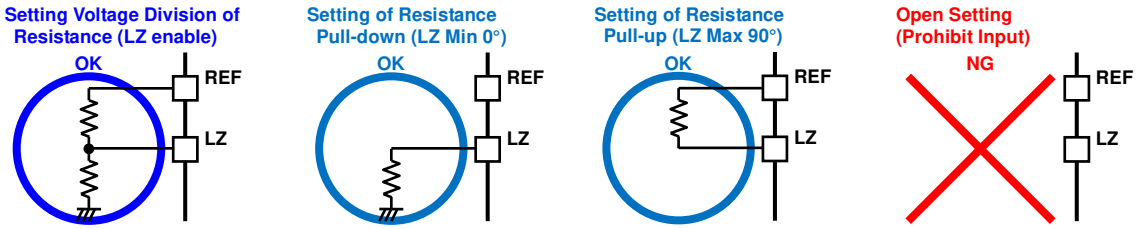


Figure 41. LZ Terminal Setting

(3) Function of Lead Angle Setting (LA)

This function automatically detects a current phase gap, and an aspect change point is revised to lead angle.
When a current phase is delayed for a hall phase, output phase can be changed up to 22.5° automatically.
When you use the Lead Angle function, Please set the LA terminal open.
When you are not using the Lead Angle function, please connect LA terminal to GND.
Timing chart is shown in Figure 42 and 43.

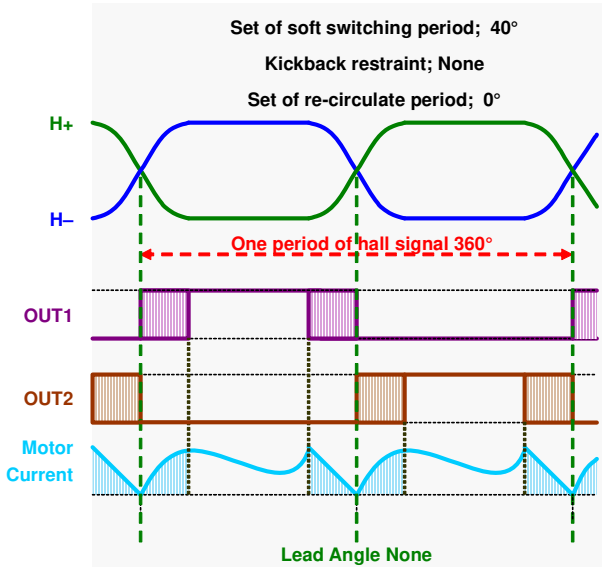


Figure 42. Lead Angle Function Disable

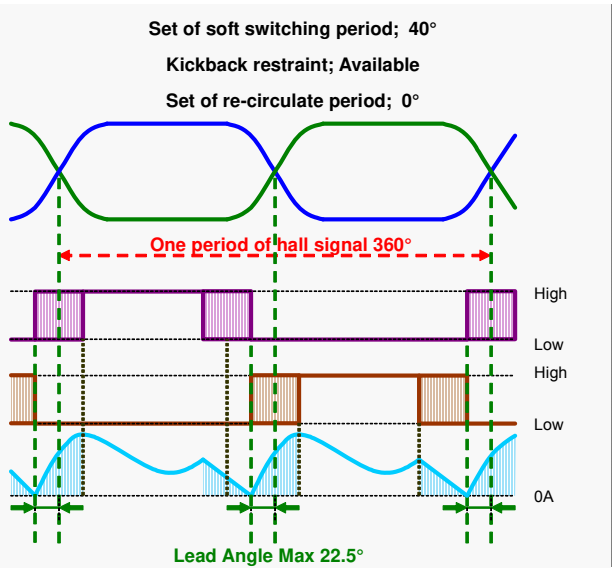


Figure 43. Lead Angle Function Enable

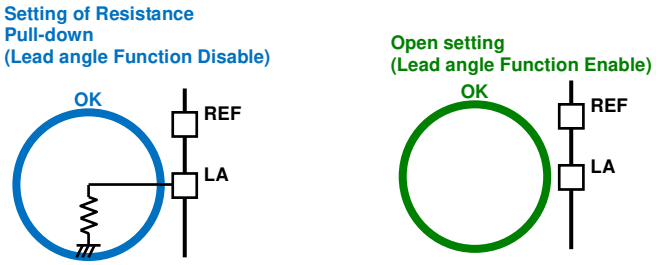


Figure 44. LA Terminal Setting

3. Current Limit

The current limit circuit turns OFF the output when the current that flows to the motor coil is detected exceeding a set value. The current value that current limit operates is determined by internal setting voltage and CS terminal. In Figure 46, I_{OUT} is the current flowed to the motor coil, R_{NF} is the resistance detecting the current, and P_{RMAX} is the power

$$Io[A] = V_{CL}[V] / R_{NF}[\Omega] = 265[mV] / 0.33[\Omega] = 0.803[A]$$

$$P_{RMAX}[W] = V_{CL}[V] \times Io[A] = 265[mV] \times 0.803[A] = 0.213[W]$$

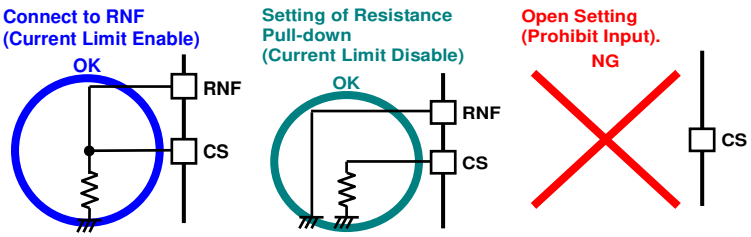


Figure 45. CS Terminal Setting

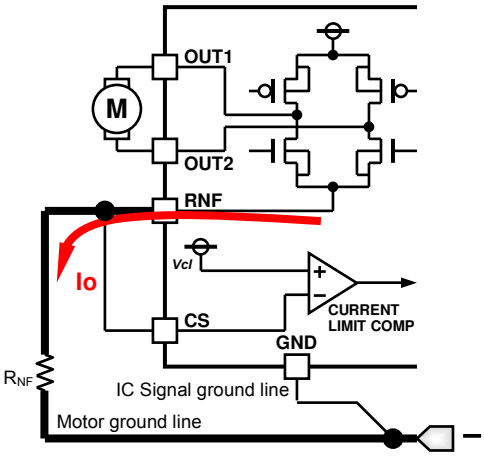


Figure 46. Setting of Current Limit and Ground Lines

When you use the current limit function, please connect the CS terminal and the RNF terminal.
When you are not using the current limit function, please connect the CS terminal to GND.

4. Lock Protection and Automatic Restart

Motor rotation is detected by hall signal, and the IC internal counter set lock detection ON time (t_{ON}) and OFF time (t_{OFF}). Timing chart is shown in Figure 47.

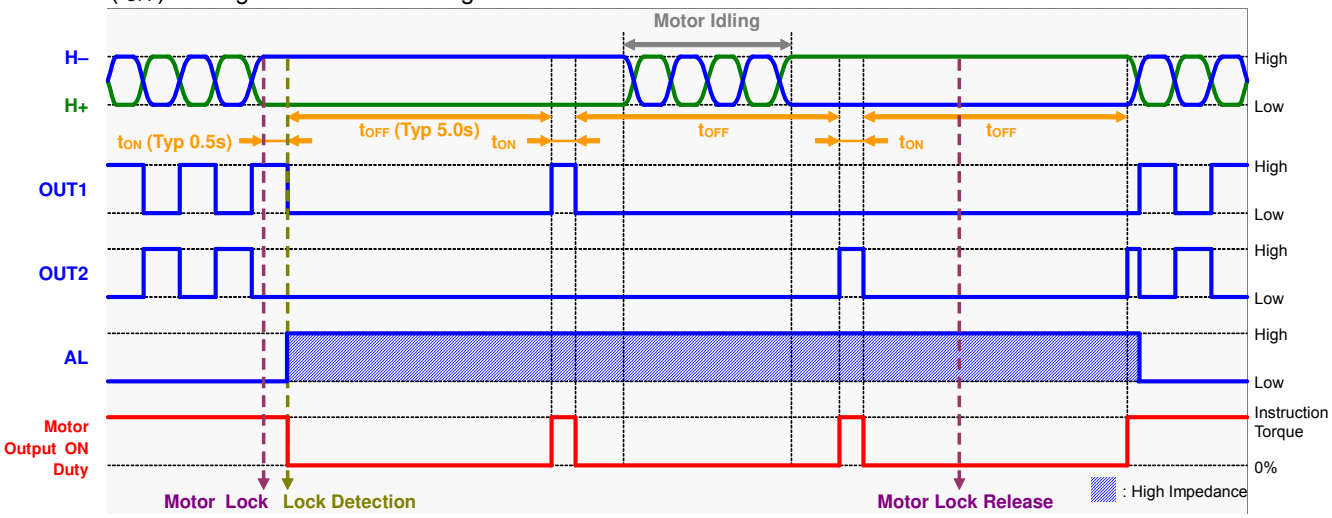


Figure 47. Lock Protection (Incorporated Counter System) Timing Chart

5. Quick Start

When torque OFF logic is input by the control signal over a fixed time, the lock protection function is disabled. The motor can restart quickly once the control signal is applied.

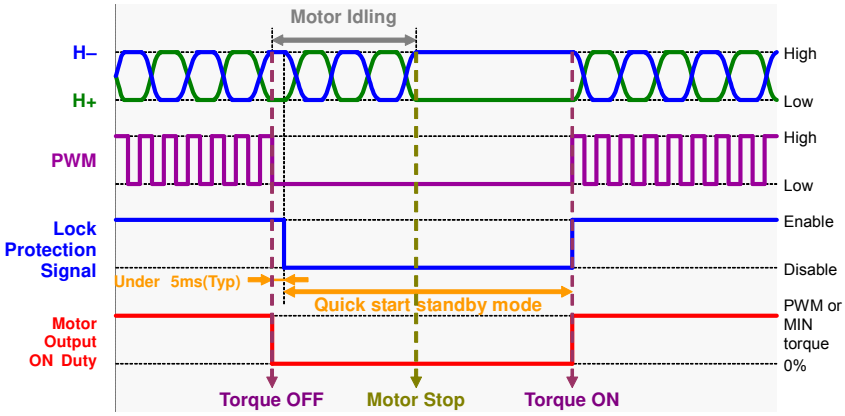


Figure 48. Quick Start Timing Chart (PWM Input Application)

6. Start Duty Assist

Start Duty Assist can secure a constant starting torque even at low duty. The IC is driven by a constant output duty (D_{OHL}; Typ 50%) within detection of motor rotation. When Output ON duty is less than 50% (Typ), Start Duty Assist function operates under the following conditions:

(1) Power ON
(2) Lock Release
(3) Quick Start
(4) Thermal Shut Down(TSD) Release

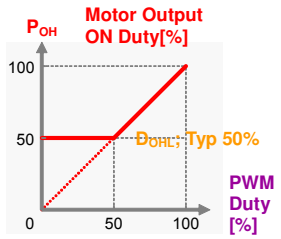


Figure 49. I/O Duty Characteristic in Start Duty Assist

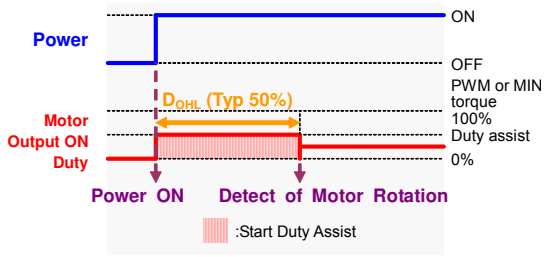


Figure 50. Timing Chart of Power ON

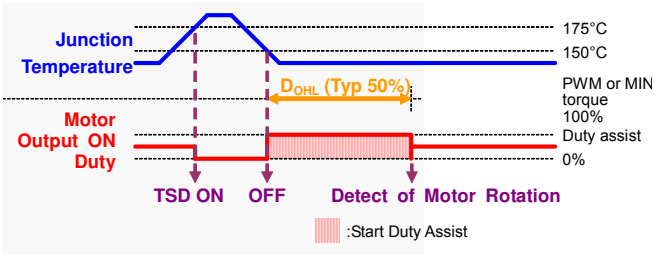


Figure 51. Timing Chart of TSD Release

7. Hall Input Setting

Hall input voltage range is shown in operating conditions (P.3). Adjust the value of hall element bias resistor R_1,R_2 in Figure 53 so that the input voltage of a hall amplifier is input in "Input Voltage Range 1"(P.3) including signal amplitude. R_2 is resistance to correct the temperature characteristic of the hall element.

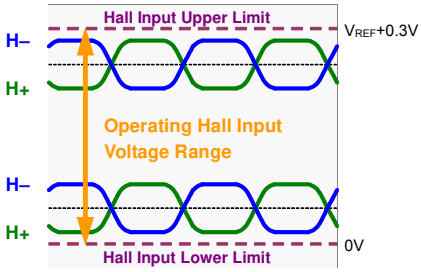


Figure 52. Hall Input Voltage Range

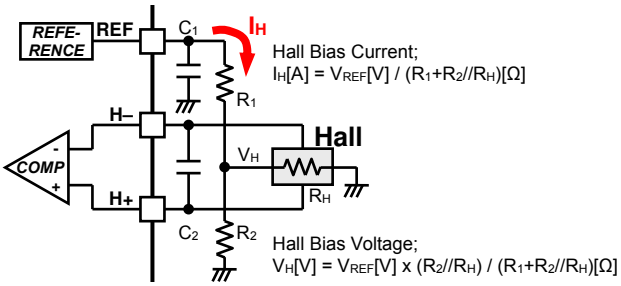


Figure 53. Hall Input Application

Reducing the Noise of Hall Signal

V_{CC} noise or the like depending on the wiring pattern of board may affect Hall element. In this case, place a capacitor like C_1 in Figure 56. In addition, when wiring from the hall element output to IC hall input is long, noise may be induced on wiring. In this case, place a capacitor like C_2.

8. High-speed Detection Protection

High-speed detection protection begins lock protection action when it detects that the hall input signal is in an abnormal state (more than Typ 2.5kHz). Noise may be induced on wiring. In this case, place a capacitor like C_2 in Figure 53.

Safety Measure

1. **Reverse Connection Protection Diode**
Reverse connection of power results in IC destruction as shown in Figure 54. When reverse connection is possible, reverse connection protection diode must be added between power supply and VCC.

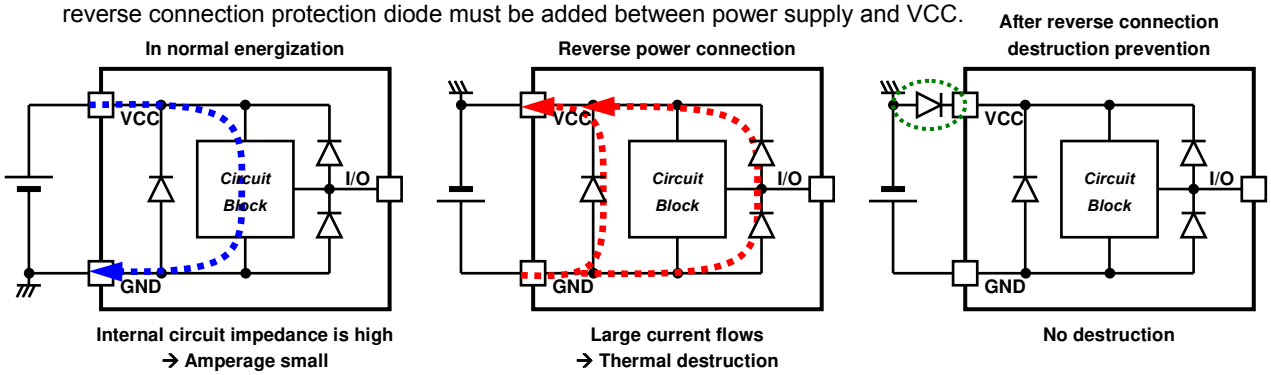


Figure 54. Flow of Current When Power is Connected Reversely

2. **Protection against V_{CC} Voltage Rise by Back Electromotive Force**
Back electromotive force (Back EMF) generates regenerative current to power supply. However, when reverse connection protection diode is connected, V_{CC} voltage rises because the diode prevents current flow to power supply.

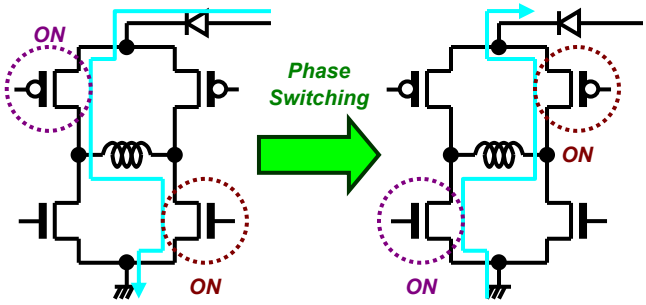


Figure 55. V_{CC} Voltage Rise by Back Electromotive Force

When the absolute maximum rated voltage may be exceeded due to voltage rise by back electromotive force, place (A) Capacitor or (B) Zener diode between VCC and GND. If necessary, add both (C).

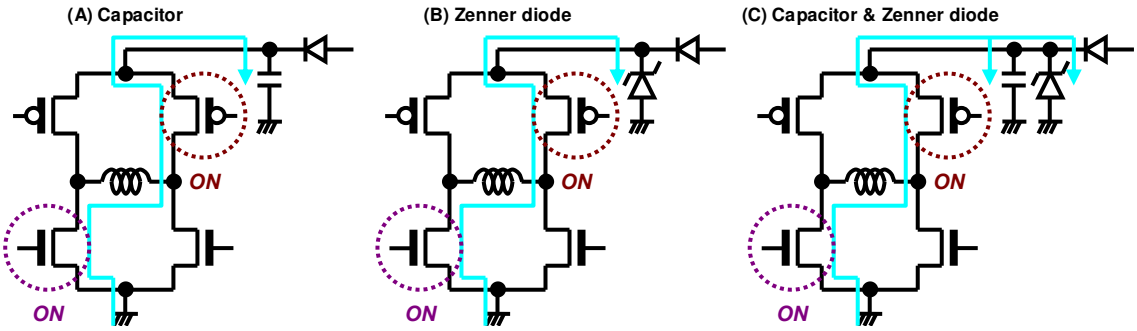


Figure 56. Measure against V_{CC} and Motor Driving Outputs Voltage

3. **Problem of GND line PWM Switching**
Do not perform PWM switching of GND line because GND terminal potential cannot be kept to a minimum.

4. **Lock Alarm Signal (AL) Open-Drain Output**
AL output is an open drain and requires pull-up resistor. Adding resistor can protect the IC. Exceeding the absolute maximum rating, when AL terminal is directly connected to power supply, could damage the IC.

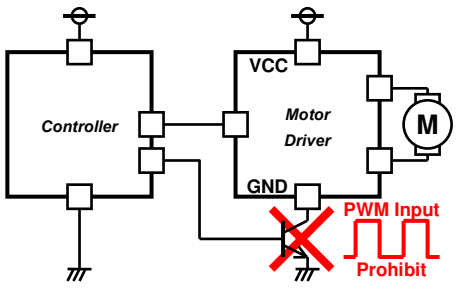


Figure 57. GND Line PWM Switching Prohibited

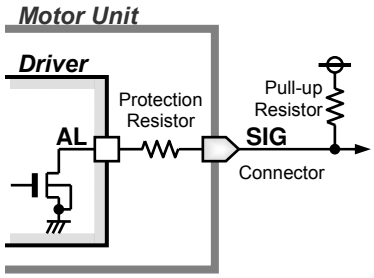


Figure 58. Protection of AL Terminal

Power Consumption

1. Current Pathway

The current pathways that relates to driver IC are the following.

(1) Circuit Current (I_{CC})
(2) Motor Current (I_M)
(3) Reference Bias Current to the Resistors (I_{REF})
(4) AL Output Sink Current (I_{AL})

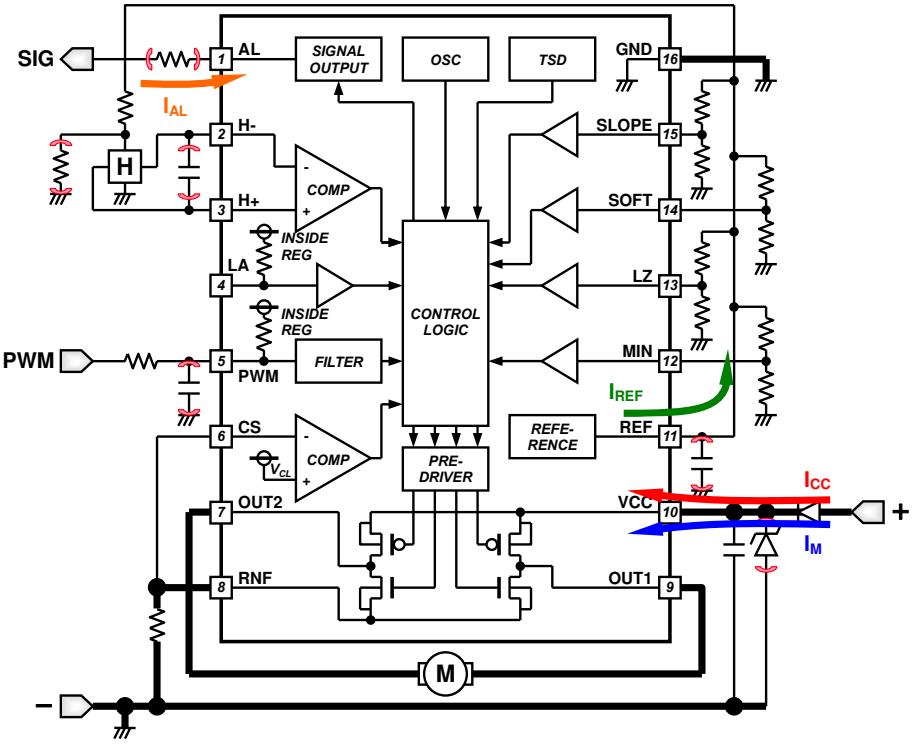


Figure 59. Current Pathway of IC

2. Calculation of Power Consumption

(1) Circuit Current (I_{CC})
$P_{Wa}[W] = V_{CC}[V] \times I_{CC}[A]$ (I_{CC} current doesn't include I_M,I_{REF})
(ex.) $V_{CC} = 11.3[V]$, $I_{CC} = 4.5[mA]$
$P_{Wa}[W] = 11.3[V] \times 4.5[mA] = 50.85\ [mW]$

(2) Motor Driving Current (I_M)
V_{OH} is the output saturation voltage of OUT1 or OUT2 high side, V_{OL} is the other low side voltage,
$P_{Wb}[W] = (V_{OH}[V] + V_{OL}[V]) \times I_M[A]$
(ex.) $V_{OH} = 0.10[V]$, $V_{OL} = 0.10[V]$, $I_M = 200[mA]$
$P_{Wb}[W] = (0.10[V] + 0.10[V]) \times 200[mA] = 40.0[mW]$

(3) Reference Bias Current to the LPF and Resistors (I_{REF})
$P_{Wc}[W] = (V_{CC}[V] - V_{REF}[V]) \times I_{REF}[A]$
(ex.) $I_{REF} = 6.0[mA]$
$P_{Wc}[W] = (11.3[V] - 3.3[V]) \times 6.0[mA] = 48.0[mW]$

(4) AL Output Sink Current (I_{AL})
$P_{Wd}[W] = V_{AL}[V] \times I_{AL}[A]$
(ex.) $V_{AL} = 0.10[V]$, $I_{AL} = 5.0[mA]$
$P_{Wd}[W] = 0.10[V] \times 5.0[mA] = 0.5[mW]$

Total power consumption of driver IC becomes the following by the above (1) to (4).
$P_{Wttl}[W] = P_{Wa}[W] + P_{Wb}[W] + P_{Wc}[W] + P_{Wd}[W]$
(ex.) $P_{Wttl}[W] = 50.85[mW] + 40.0[mW] + 48.0[mW] + 0.5[mW] = 139.35[mW]$

Refer to next page when you calculate the chip surface temperature (Tj) and the package surface temperature (Tc) by using the power consumption value.

Power Dissipation

1. Power Dissipation

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25°C (normal temperature). IC is heated when it consumes power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip into the package, that is junction temperature of the absolute maximum rating, depends on circuit configuration, manufacturing process, etc. Power dissipation is determined by this maximum joint temperature, the thermal resistance in the state of the substrate mounting, and the ambient temperature. Therefore, when a power dissipation that provides by the absolute maximum rating is exceeded, the operating temperature range is not a guarantee. The maximum junction temperature is in general equal to the maximum value in the storage temperature range.

θja = (Tj - Ta) / P [°C/W]

2. Thermal Resistance

Heat generated by consumed power of IC is radiated from the mold resin or lead frame of package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance. In the state of the substrate mounting, thermal resistances from the chip junction to the ambience and to the package surface are shown respectively with θja [°C/W] and θjc [°C/W]. Thermal resistance is classified into the package part and the substrate part, and thermal resistance in the package part depends on the composition materials such as the mold resins and the lead frames. On the other hand, thermal resistance in the substrate part depends on the substrate heat dissipation capability of the material, the size, and the copper foil area etc. Therefore, thermal resistance can be decreased by the heat radiation measures like installing a heat sink etc. in the mounting substrate.
The thermal resistance model and calculations are shown in Figure 61.

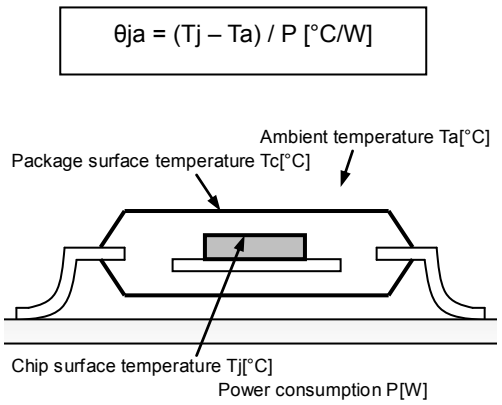
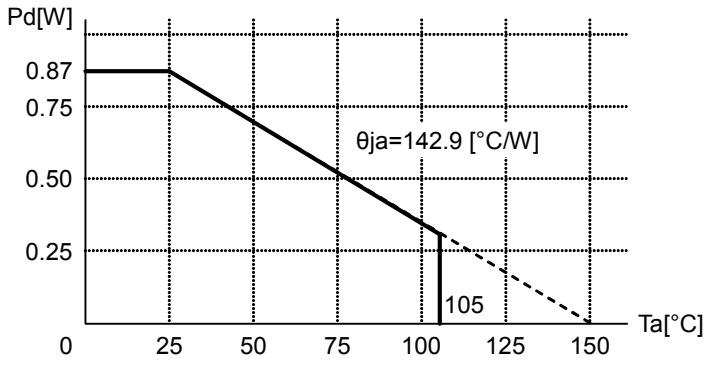


Figure 60. Thermal Resistance Model of Surface Mount

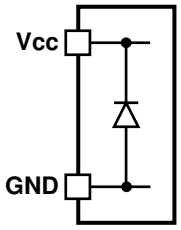


(Note) Reduce by 7.0mW/°C when operating over Ta=25°C
(Mounted on 70.0mm x 70.0mm x 1.6mm glass epoxy board)

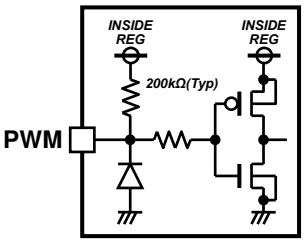
Figure 61. Power Dissipation vs Ambient Temperature

I/O Equivalent Circuit (Resistance Values are Typical)

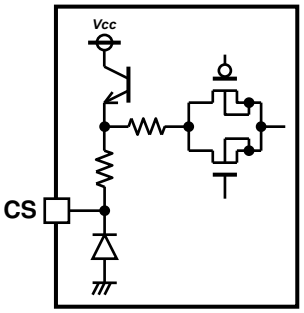
1. Power supply terminal round terminal



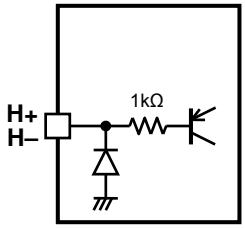
2. PWM input duty terminal



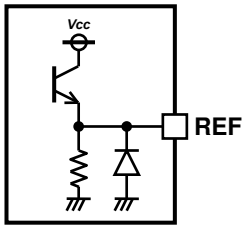
3. Output current detecting terminal



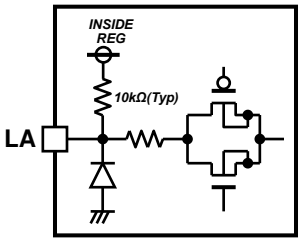
4. Hall +/- input terminal



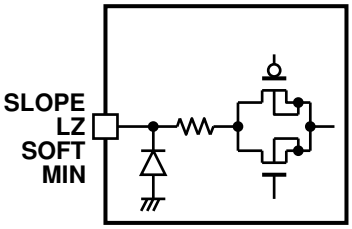
5. Reference voltage output terminal



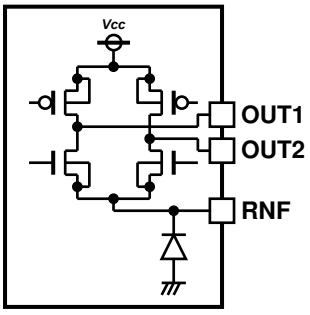
6. Lead angle function select terminal



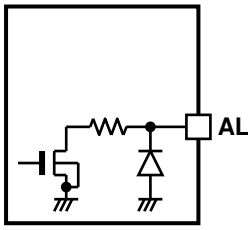
7. I/O duty slope setting terminal minimum output duty setting terminal, recirculate period setting terminal and soft switching setting terminal



8. Motor output terminal 1/2
Output current detecting resistor connecting terminal



9. Lock alarm signal output terminal



Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the power dissipation stated in this datasheet is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to raise heat dissipation capability.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, width of power and ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage. The IC's power supply should always be turned OFF completely before connecting or removing it from the test setup during the inspection process.

10. **Mounting Errors and Inter-pin Short**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. Especially, if it is not expressed on the datasheet, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

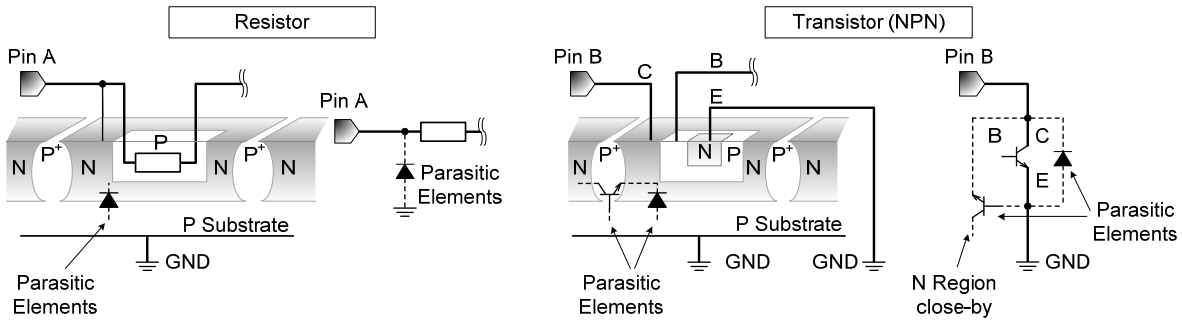


Figure 62. Example of Monolithic IC Structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown (TSD) Circuit

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature will rise which will activate the TSD circuit that will turn OFF all output pins. When the junction temperature falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.