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Load Switch ICs

BD6520F BD6522F

●General Description

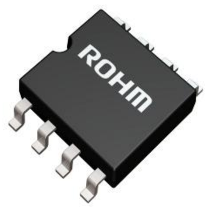
This power switch for expansion module is a power management switch having one circuit of N-channel Power MOSFET. The typical value of ON Resistance of the switch is as low as 50mΩ. The switch turns on smoothly by the built-in charge pump, therefore, it is possible to reduce inrush current at switch on; Soft start control by external capacitor is available.
Furthermore, it contains the following circuit: Under voltage lockout circuit, thermal shutdown circuit and a circuit that discharges electric charge from capacitive load at switch off.

●Key Specifications

- Input voltage range: 3.0V to 5.5V
- ON resistance :
  - $R_{ON}1$ (at V_{DD}=5V BD6520F, BD6522F) 50mΩ (Typ.)
  - $R_{ON}2$ (at V_{DD}=3V BD6520F) 60mΩ (Typ.)
  - $R_{ON}2$ (at V_{DD}=3.3V BD6522F) 60mΩ (Typ.)
- Continuous current: 2.0 A
- Operating temperature range: -25℃ to +85℃

●Package

	W(Typ.) x D(Typ.) x H (Max.)
SOP8	5.00mm x 6.20mm x 1.71mm



SOP8

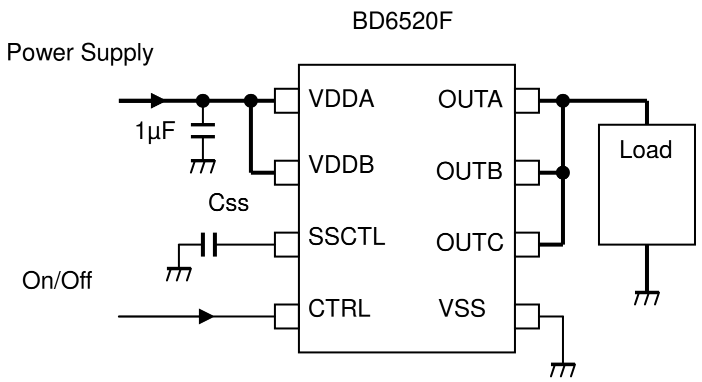
●Features

- Low on resistance (50mΩ, Typ.) N-MOS switch built in
- Maximum output current: 2A
- Built-in Discharge Circuit
- Built-in Soft Start Control
- Built-in Under voltage lockout (UVLO) circuit
- Thermal shutdown (Output off latching)
- Reverse current flow blocking at switch off (Only at BD6522F)

●Applications

Notebook PC, PC peripheral device, etc.

●Typical Application Circuit



●Lineup

OUT Rise Time	OUT Fall Time	Reverse current flow blocking at switch off	Package		Orderable Part Number
1000µs	3µs	-	SOP8	Reel of 2500	BD6520F - E2
1000µs	4µs	○	SOP8	Reel of 2500	BD6522F - E2

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

●Block Diagrams

(BD6520F)

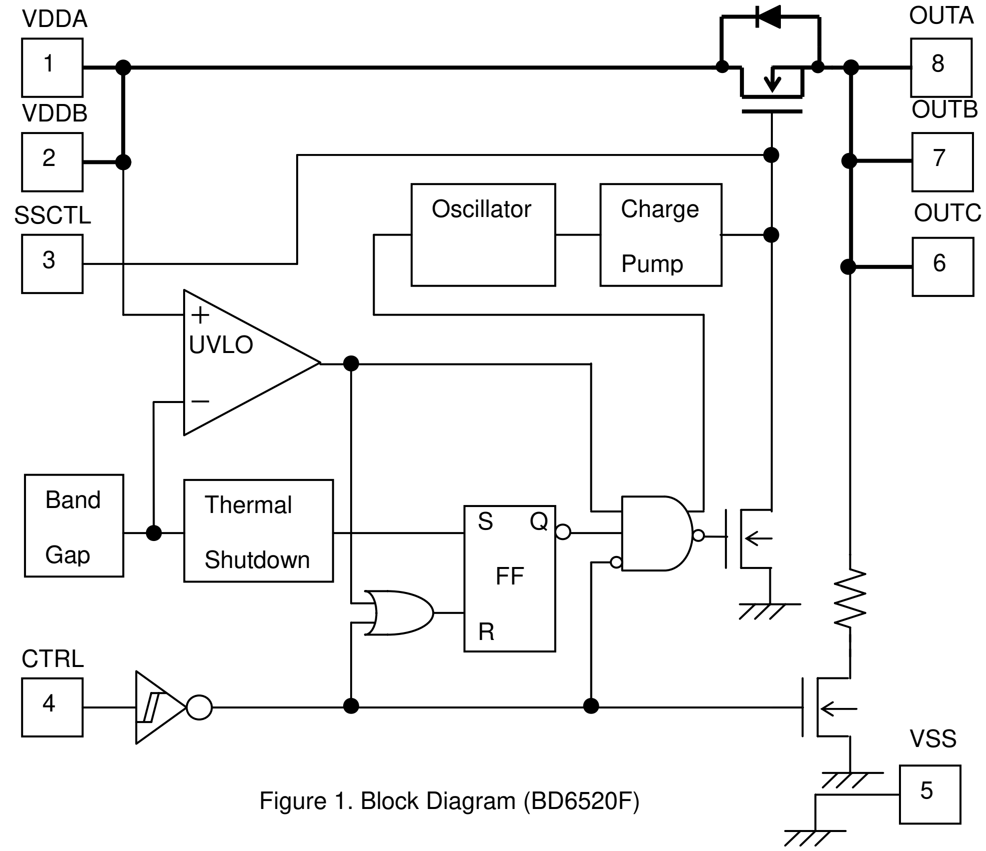


Figure 1. Block Diagram (BD6520F)

(BD6522F)

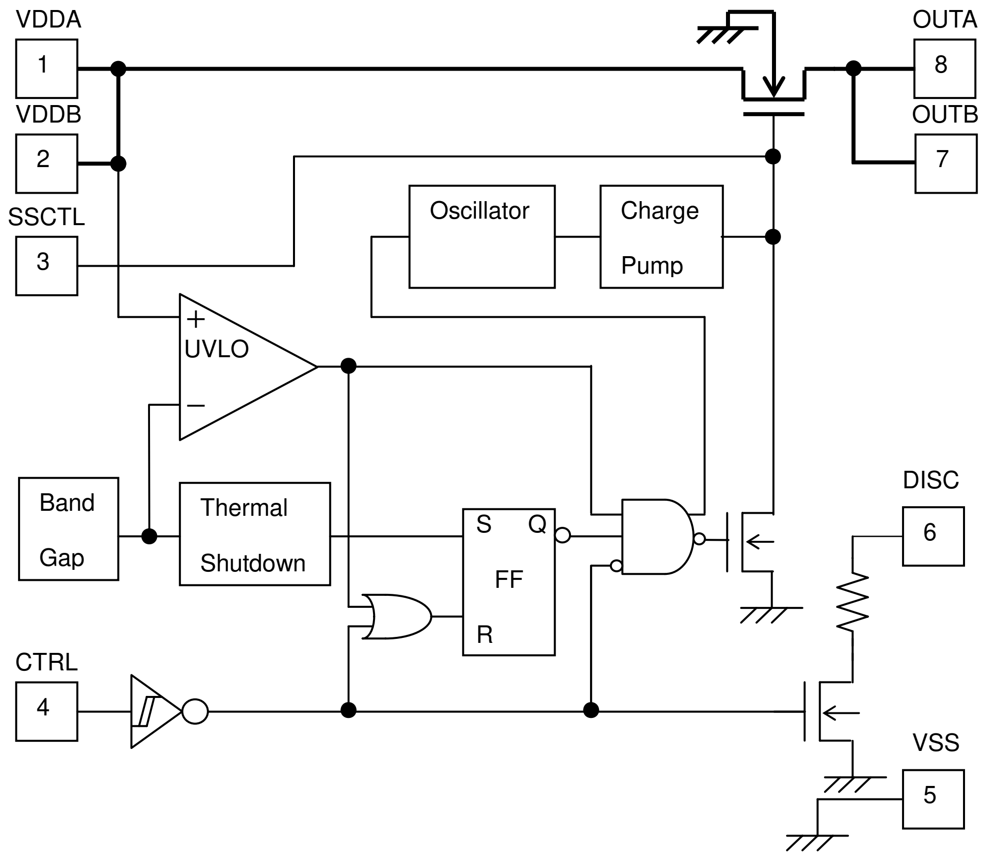
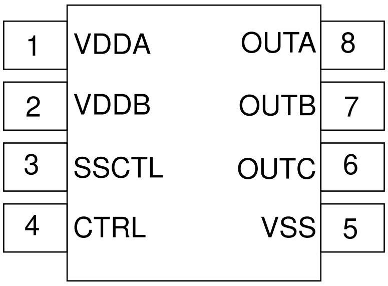


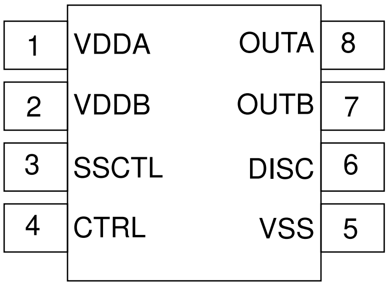
Figure 2. Block Diagram (BD6522F)

●Pin Configurations

BD6520F
TOP VIEW



BD6522F
TOP VIEW



●Pin Descriptions

○BD6520F

Pin No.	Symbol	Pin Function
1,2	VDDA, VDDB	SWITCH INPUT pin When in use, connect each pin externally
3	SSCTL	SOFT START setting pin Adding external capacitor makes it possible to delay switch On or Off time.
4	CTRL	CONTROL input pin Switch On at High level, switch Off at Low level.
5	VSS	GROUND
6,7,8	OUTA, OUTB, OUTC	SWITCH OUTPUT pin When in use, connect each pin externally

○BD6522F

Pin No.	Symbol	Pin Function
1,2	VDDA, VDDB	SWITCH INPUT pin When in use, connect each pin externally
3	SSCTL	SOFT START setting pin Adding external capacitor makes it possible to delay switch On or Off time.
4	CTRL	CONTROL input pin Switch On at High level, switch Off at Low level.
5	VSS	GROUND
6	DISC	DISCHARGE pin
7,8	OUTA, OUTB	SWITCH OUTPUT pin When in use, connect each pin externally

●Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	-0.3 to 6.0	V
CTRL Input Voltage	V_{CTRL}	-0.3 to 6.0	V
Switch Output Voltage	V_{OUT}	-0.3 to V_{DD} + 0.3 (BD6520F)	V
		-0.3 to 6.0 (BD6522F)	V
Storage temperature	T_{STG}	-55 to 150	℃
Power dissipation	Pd	560[*1]	mW

*1 This value decreases by 4.48mW/℃ above Ta=25℃

●Recommended Operating Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	3.0 to 5.5	V
Switch current	I_{OUT}	0 to 2	A
Operating Temperature	T_{OPR}	-25 to 85	℃

●Electrical Characteristics

◎BD6520F(Unless otherwise specified, Ta = 25℃, V_{DD} = 5V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
On Resistance	$R_{ON}1$	-	50	70	mΩ	V_{DD} = 5V, V_{CTRL} = 5V
	$R_{ON}2$	-	60	85	mΩ	V_{DD} = 3V, V_{CTRL} = 3V
Operating Current	I_{DD}	-	110	220	μA	V_{CTRL} = 5V, OUT = OPEN
	I_{DDST}	-	-	2	μA	V_{CTRL} = 0V, OUT = OPEN
Control Input voltage	$V_{CTRL}L$	-	-	0.7	V	V_{CTRL} L = Low Level
	$V_{CTRL}H$	2.5	-	-	V	V_{CTRL} H = High Level
Control Input current	I_{CTRL}	-1	0	1	μA	V_{CTRL} = L, H
Turn On Delay	Trd	200	1000	2000	us	RL = 10Ω,SSCTL = OPEN CTRL = L→H → OUT=50%
Turn On Rise Time	Tr	500	2000	7500	us	RL = 10Ω,SSCTL = OPEN OUT = 10% → 90%
Turn Off Delay	Tfd	-	3	20	us	RL = 10Ω,SSCTL = OPEN CTRL = H→L → OUT=50%
Turn Off Fall Time	Tf	-	1	20	us	RL = 10Ω,SSCTL = OPEN OUT = 90% → 10%
Discharge Resistance	R_{SWDC}	-	350	600	Ω	V_{DD} = 5V, V_{CTRL} = 0V, V_{OUT} = 5V
UVLO Threshold Voltage	$V_{UVLO}H$	2.3	2.5	2.7	V	V_{DD} increasing
	$V_{UVLO}L$	2.1	2.3	2.5	V	V_{DD} decreasing
UVLO Hysteresis Voltage	V_{HYS}	100	200	300	mV	V_{HYS} = $V_{UVLO}H$ - $V_{UVLO}L$
Thermal Shutdown Threshold	T_{TS}	-	135	-	℃	V_{CTRL} = 5V
SSCTL Output Voltage	V_{SSCTL}	-	13.5	-	V	V_{CTRL} = 5V

●Electrical Characteristics - continued

◎BD6522F(Unless otherwise specified, Ta = 25℃, V_{DD} = 5V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
On Resistance	$R_{ON}1$	-	50	70	mΩ	V_{DD} = 5V, V_{CTRL} = 5V
	$R_{ON}2$	-	60	85	mΩ	V_{DD} = 3.3V, V_{CTRL} = 3.3V
Operating Current	I_{DD}	-	110	220	μA	V_{CTRL} = 5V, OUT = OPEN
	I_{DDST}	-	-	2	μA	V_{CTRL} = 0V, OUT = OPEN
Control Input Voltage	$V_{CTRL}L$	-	-	0.7	V	$V_{CTRL}L$ = Low Level
	$V_{CTRL}H$	2.5	-	-	V	$V_{CTRL}H$ = High Level
Control Input Current	I_{CTRL}	-1	0	1	μA	V_{CTRL} = L, H
Turn On Time	T_{ON}	-	1000	3500	us	RL = 10Ω,SSCTL = OPEN CTRL = H → OUT =90%
Turn Off Time	T_{OFF}	-	4	20	us	RL = 10Ω,SSCTL = OPEN CTRL = L → OUT = 10%
Discharge Resistance	R_{SWDC}	-	350	600	Ω	V_{DD} = 5V,V_{CTRL} = 0V
UVLO Threshold Voltage	$V_{UVLO}H$	2.3	2.5	2.7	V	V_{DD} increasing
	$V_{UVLO}L$	2.1	2.3	2.5	V	V_{DD} decreasing
UVLO Hysteresis Voltage	V_{HYS}	100	200	300	mV	V_{HYS} = $V_{UVLO}H$ - $V_{UVLO}L$
Thermal Shutdown Threshold	T_{TS}	-	135	-	℃	V_{CTRL} = 5V
SSCTL Output Voltage	V_{SSCTL}	-	13.5	-	V	V_{CTRL} = 5V

●Measurement Circuit

◎BD6520F ◎BD6522F

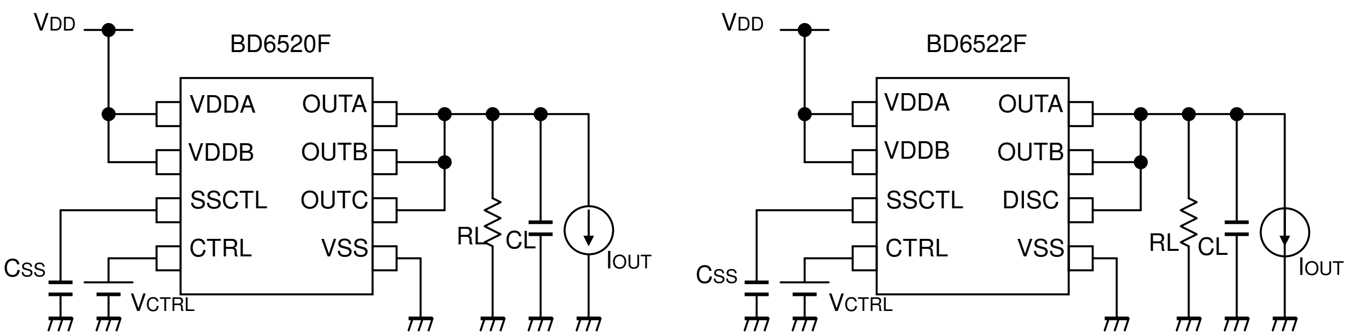


Figure 3. Measurement circuits

●Timing Diagram

◎BD6520F ◎BD6522F

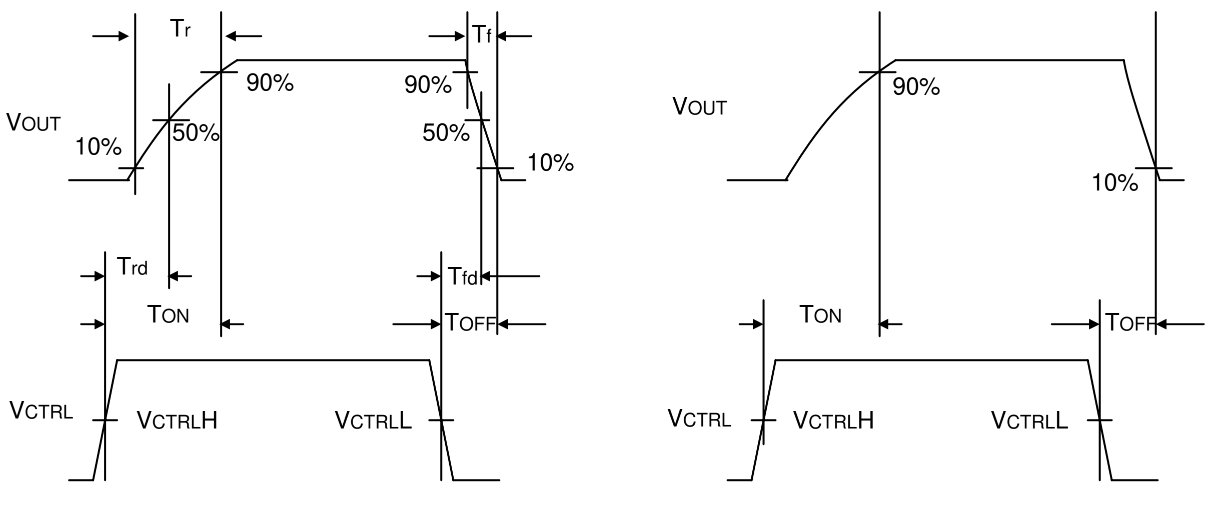


Figure 4. Timing diagram

●**Typical Performance Curves**

◎BD6520F

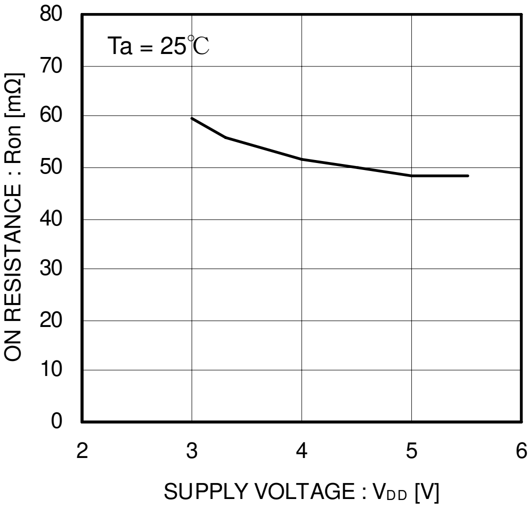


Figure 5. On resistance

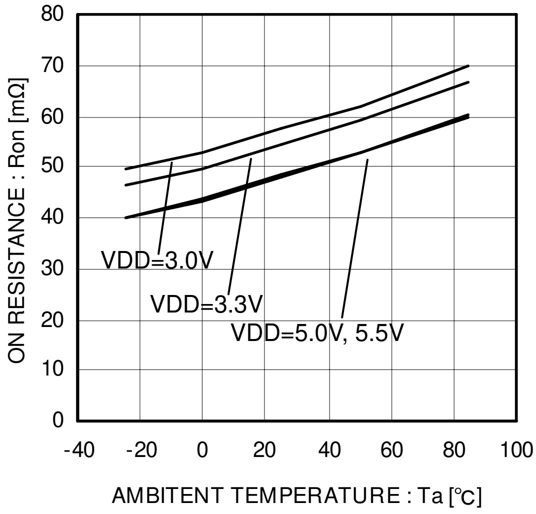


Figure 6. On resistance

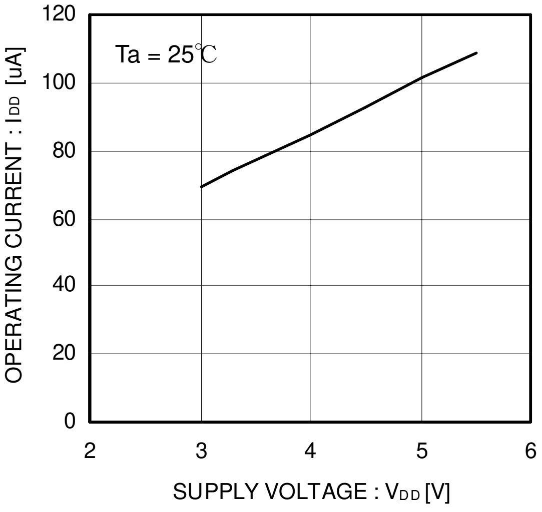


Figure 7. Operating current
(CTRL enable)

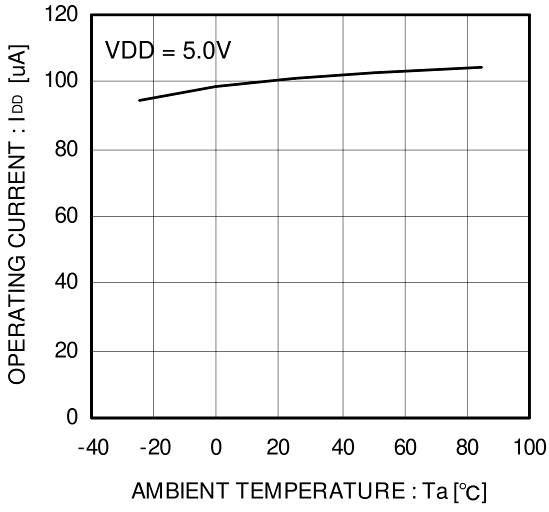


Figure 8. Operating current
(CTRL enable)

●Typical Performance Curves - continued

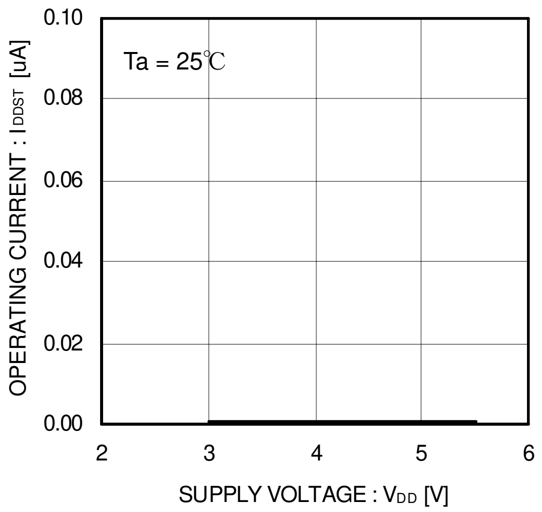


Figure 9. Operating current
(CTRL disenable)

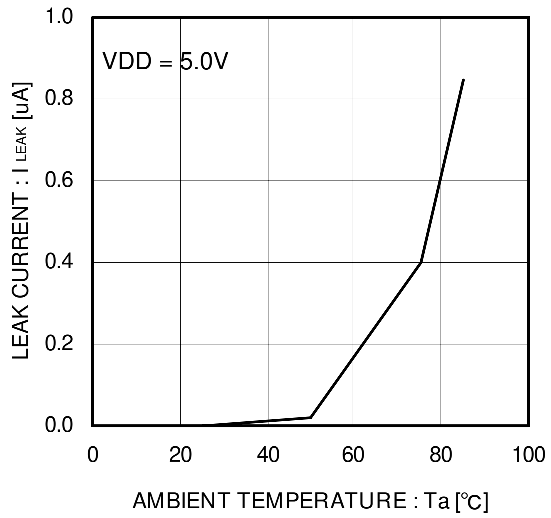


Figure 10. Leak current

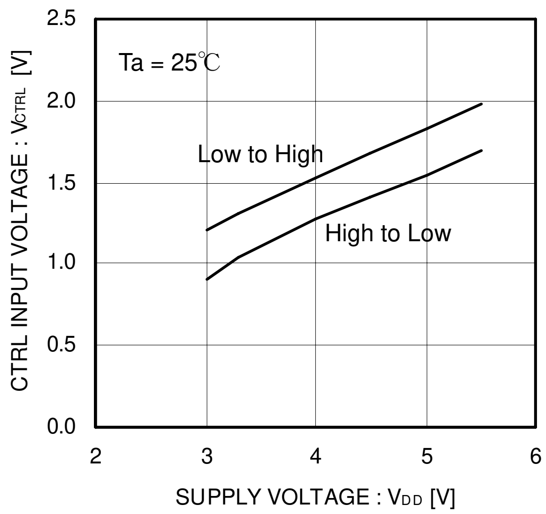


Figure 11. CTRL input voltage

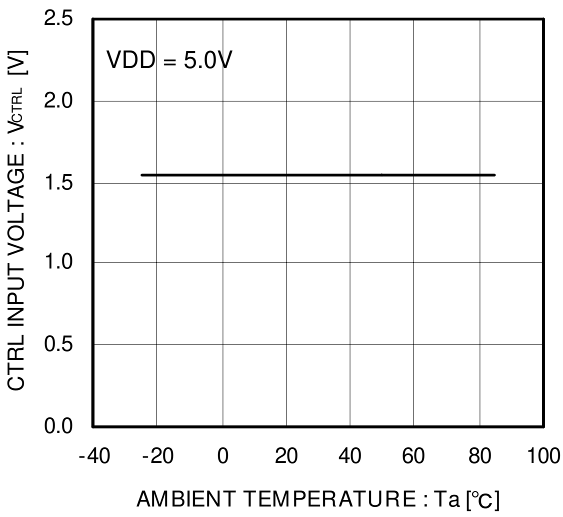


Figure 12. CTRL input voltage
H→L

●Typical Performance Curves - continued

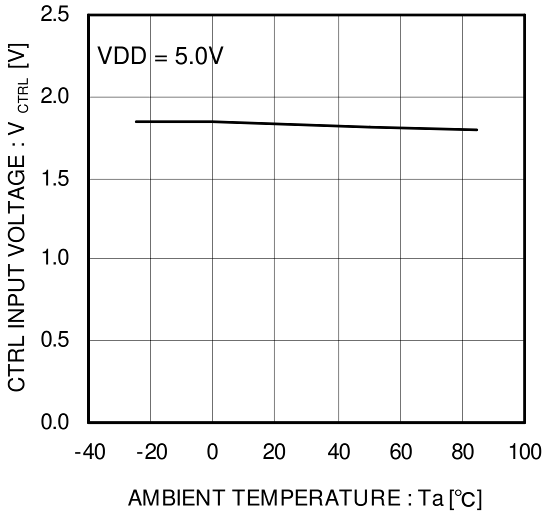


Figure 13. CTRL input voltage
L→H

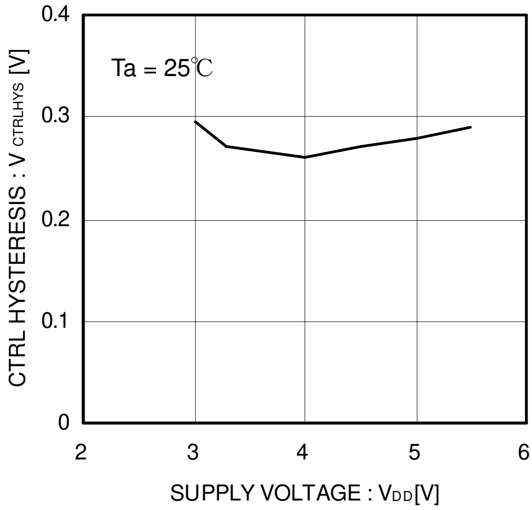


Figure 14. CTRL hysteresis voltage

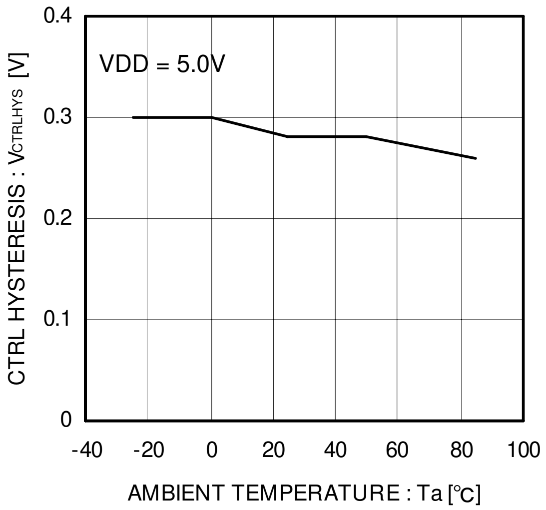


Figure 15. CTRL hysteresis voltage

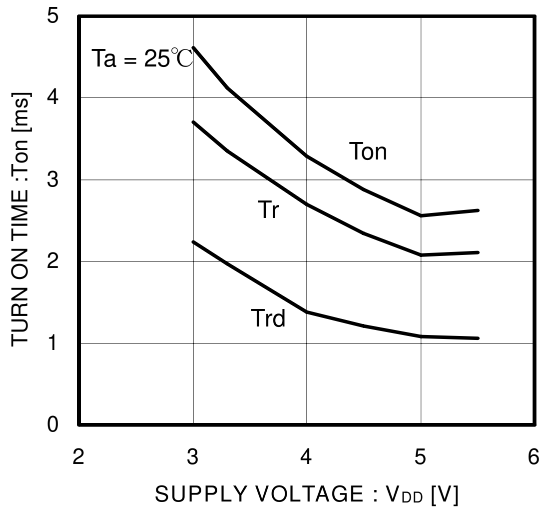


Figure 16. Turn On Rise time

●**Typical Performance Curves - continued**

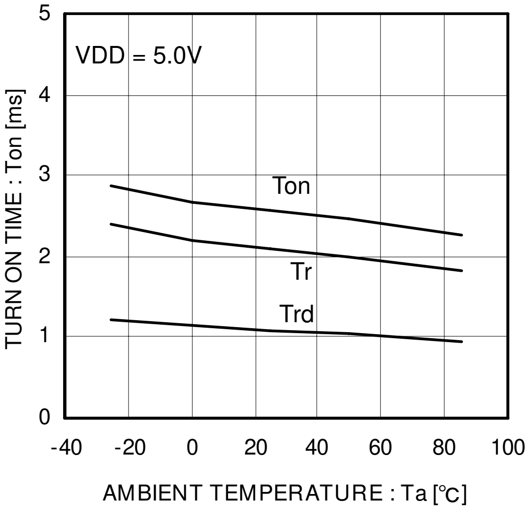


Figure 17. Turn On Rise time

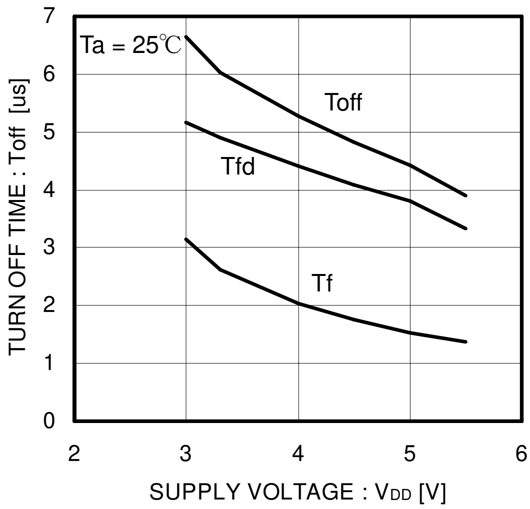


Figure 18. Turn Off Fall time

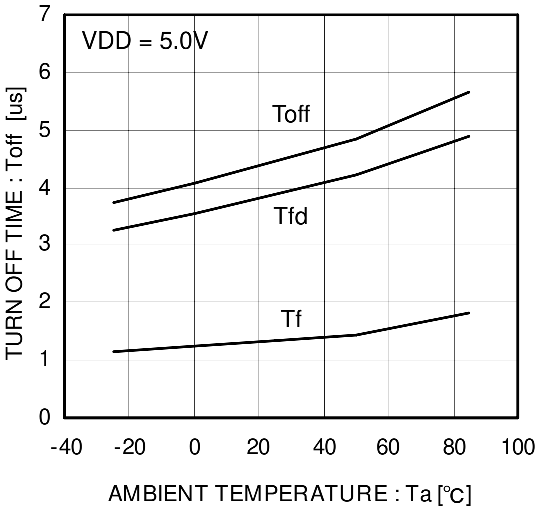


Figure 19. Turn Off Fall time

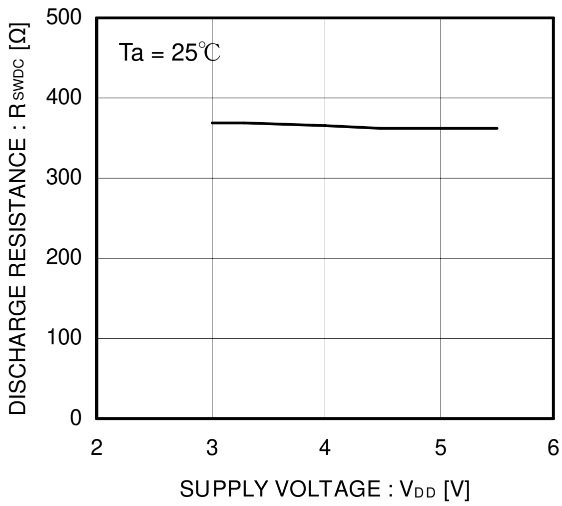


Figure 20. Switch discharge resistance

● **Typical Performance Curves - continued**

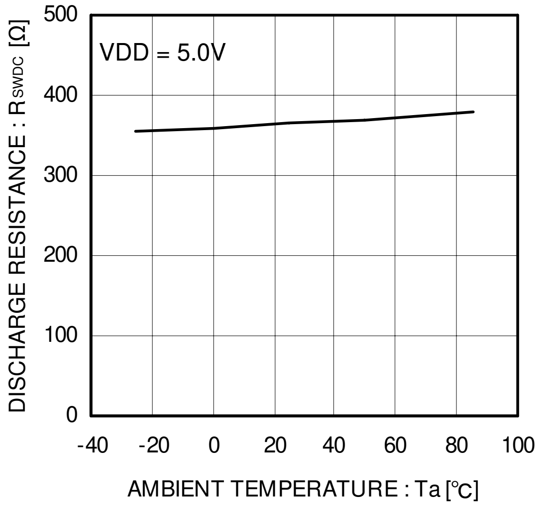


Figure 21. Switch discharge resistance

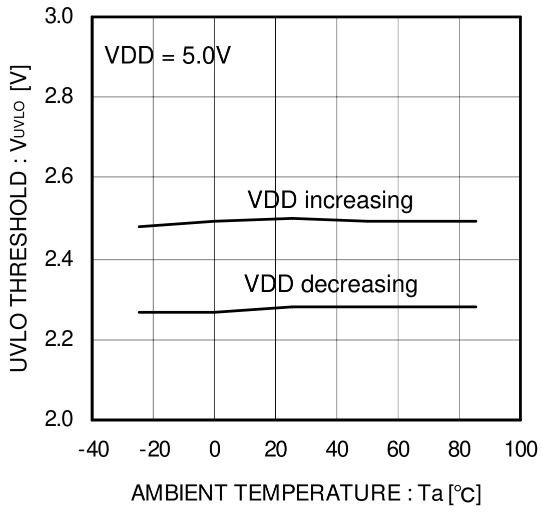


Figure 22. UVLO threshold voltage

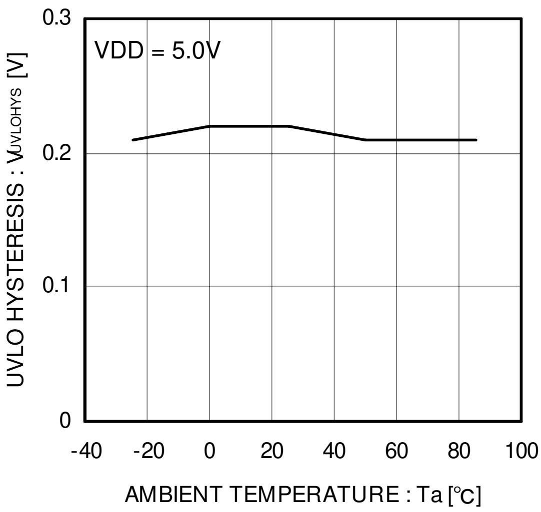


Figure 23. UVLO hysteresis voltage

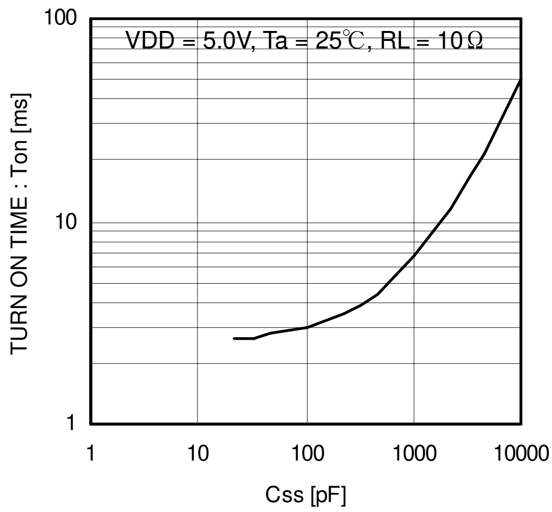


Figure 24. Turn On Rise time (vs. Css)

●**Typical Performance Curves - continued**

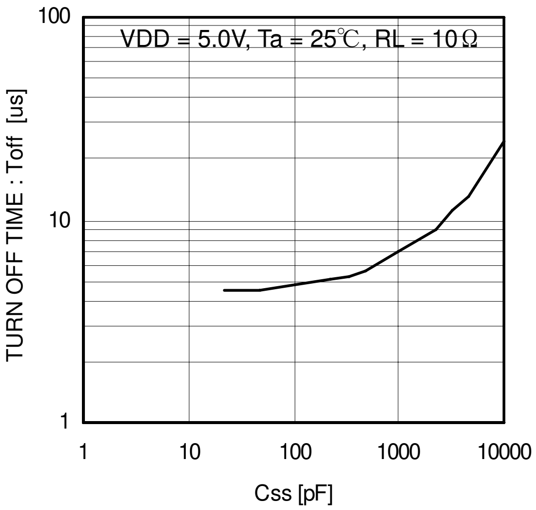


Figure 25. Turn Off Fall time (vs. Css)

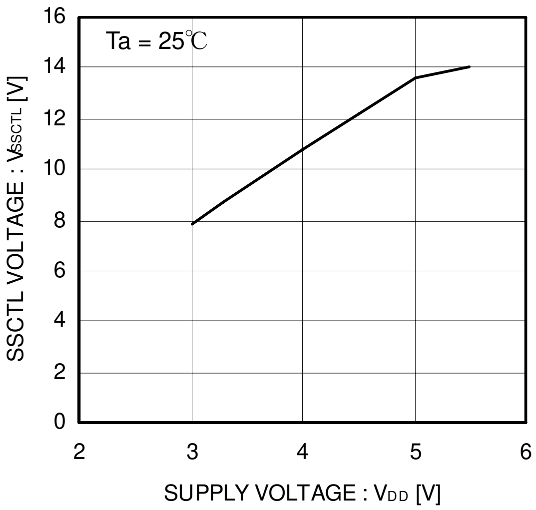


Figure 26. SSCTL output voltage

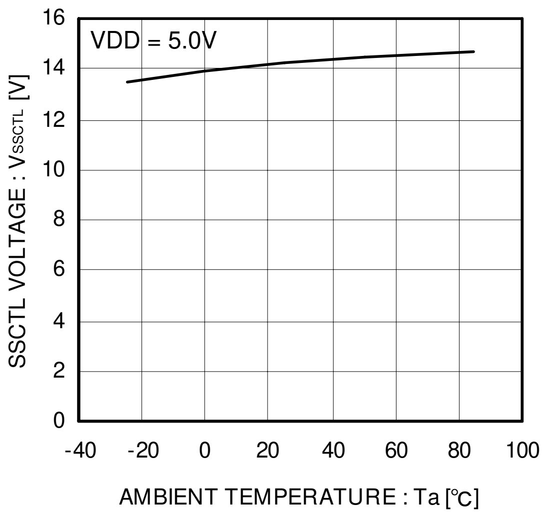


Figure 27. SSCTL output voltage

●**Typical Performance Curves – continued**

◎BD6522F

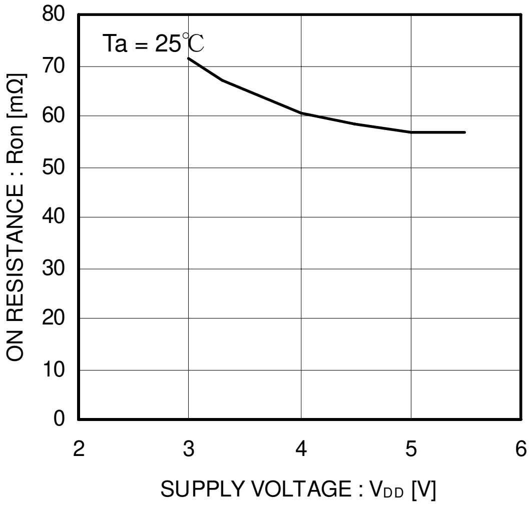


Figure 28. ON resistance

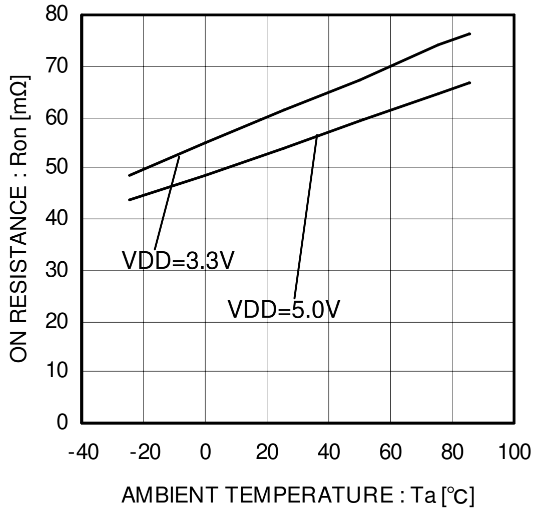


Figure 29. ON resistance

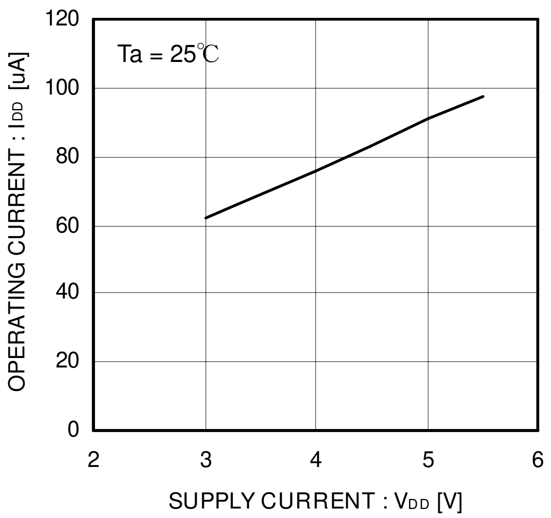


Figure 30. Operating current
(CTRL enable)

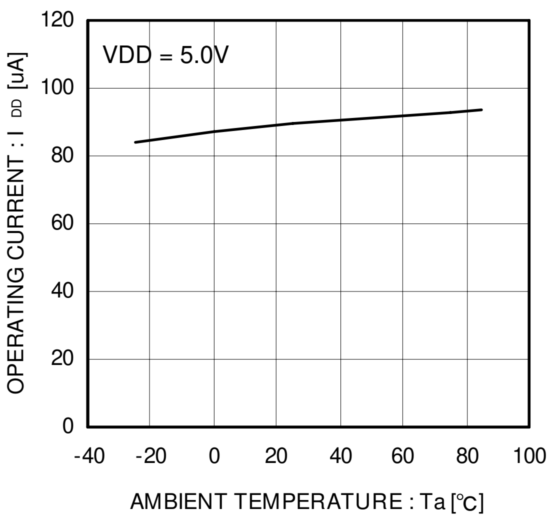


Figure 31. Operating current
(CTRL enable)

●**Typical Performance Curves - continued**

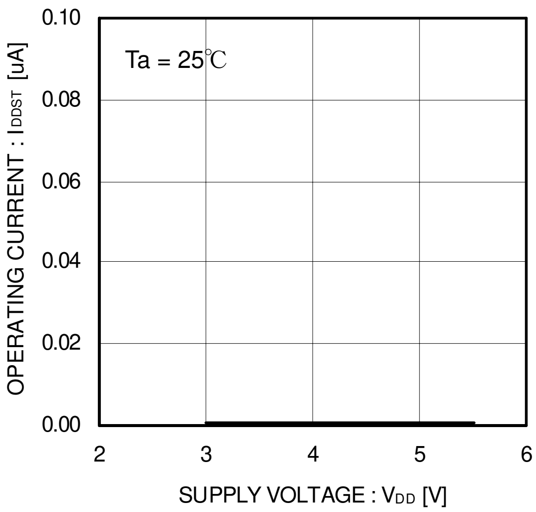


Figure 32. Operating current
(CTRL disenable)

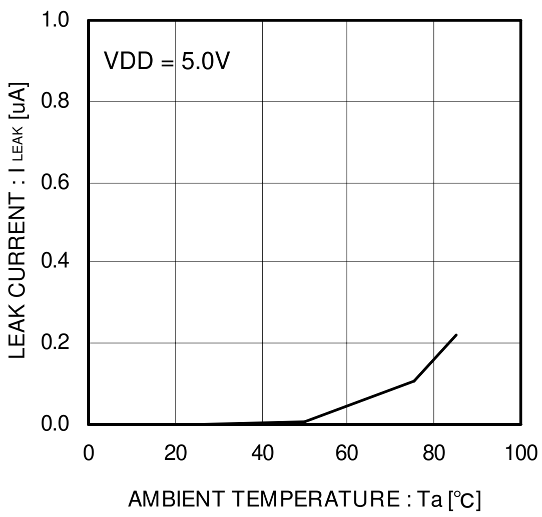


Figure 33. Leak current

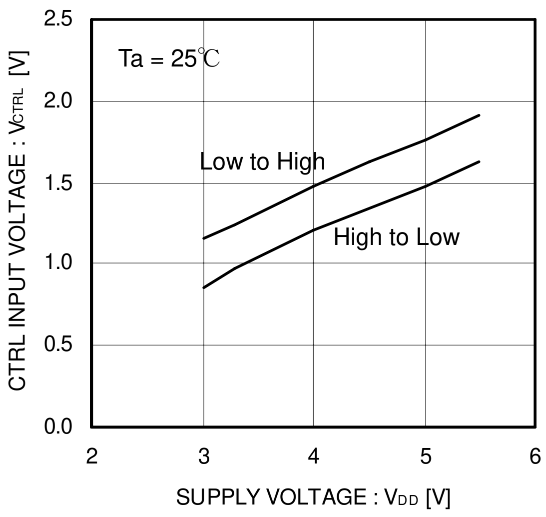


Figure 34. CTRL input voltage

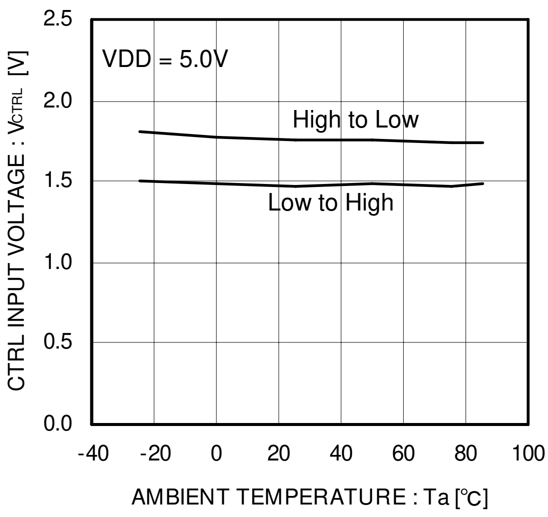


Figure 35. CTRL input voltage

●**Typical Performance Curves - continued**

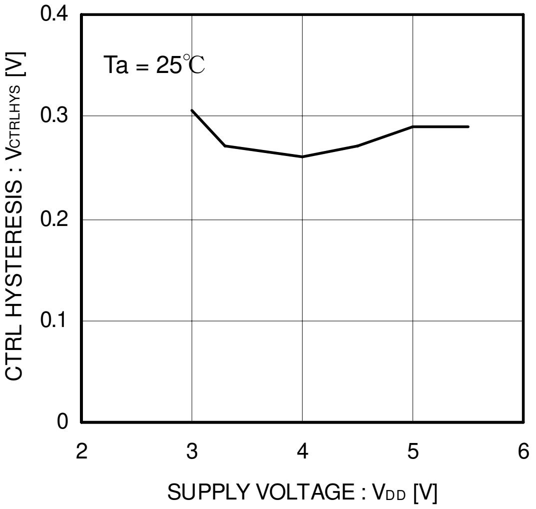


Figure 36. CTRL hysteresis voltage

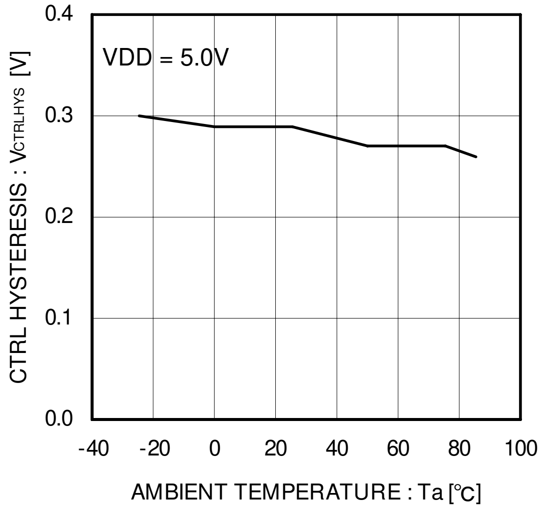


Figure 37. CTRL hysteresis voltage

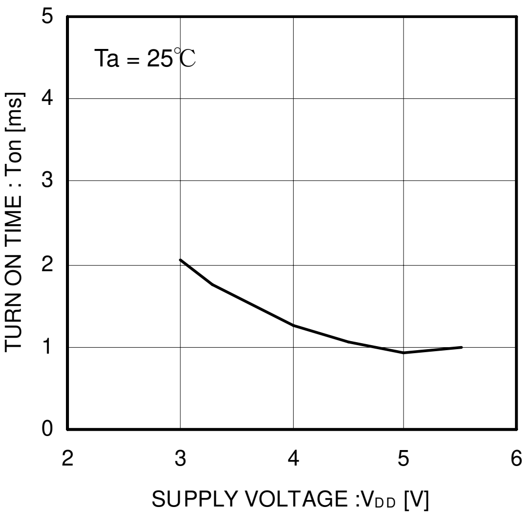


Figure 38. Turn On time

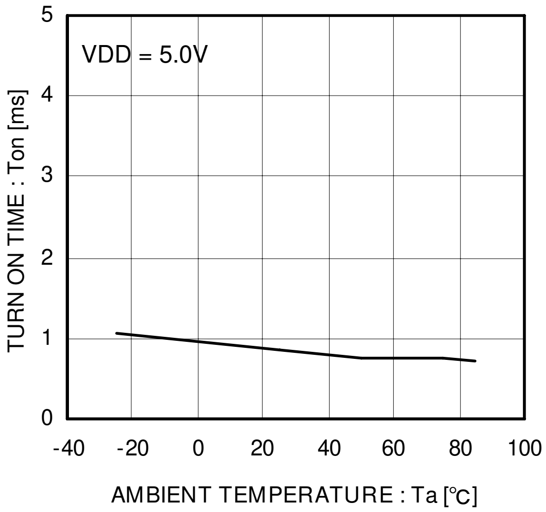


Figure 39. Turn On time

●**Typical Performance Curves - continued**

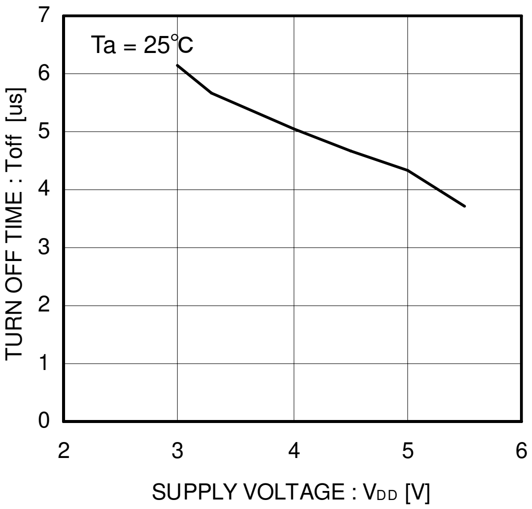


Figure 40. Turn Off time

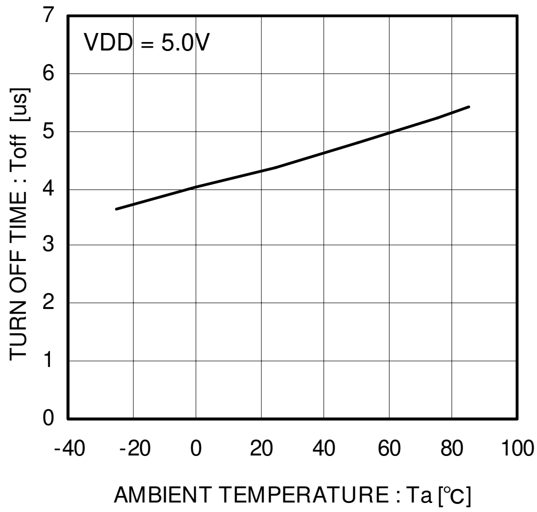


Figure 41. Turn Off time

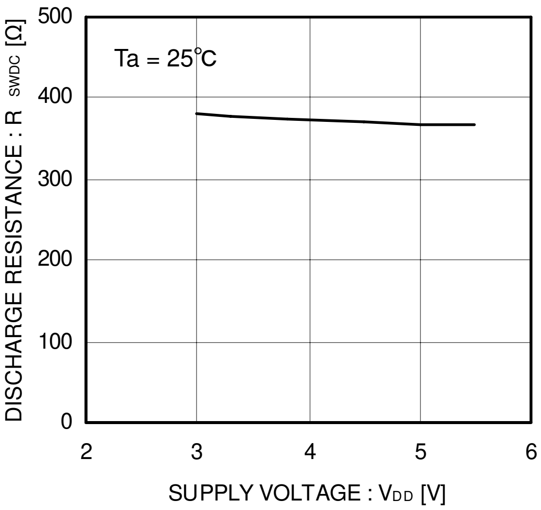


Figure 42. Switch discharge resistance

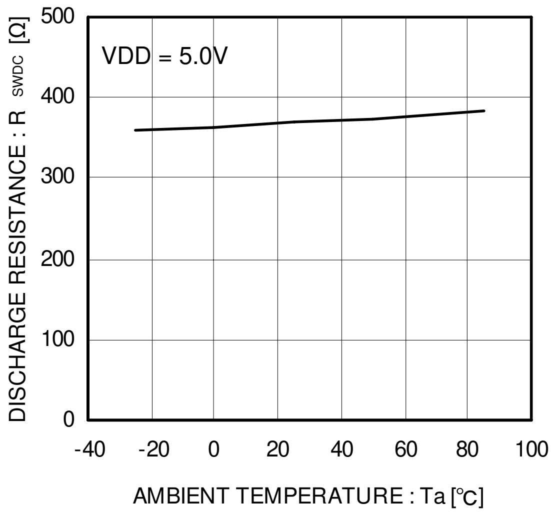


Figure 43. Switch discharge resistance

●Typical Performance Curves - continued

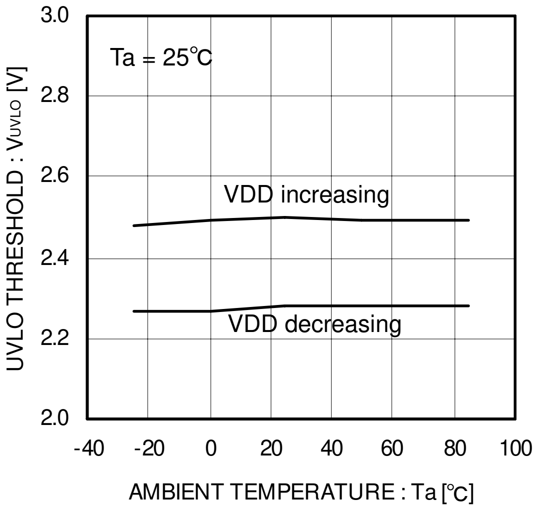


Figure 44. UVLO threshold voltage

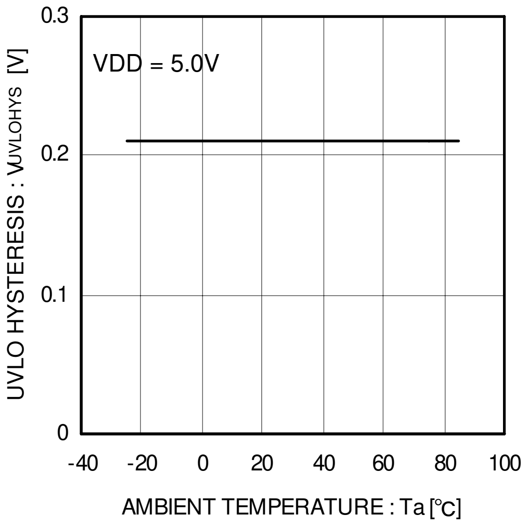


Figure 45. UVLO hysteresis voltage

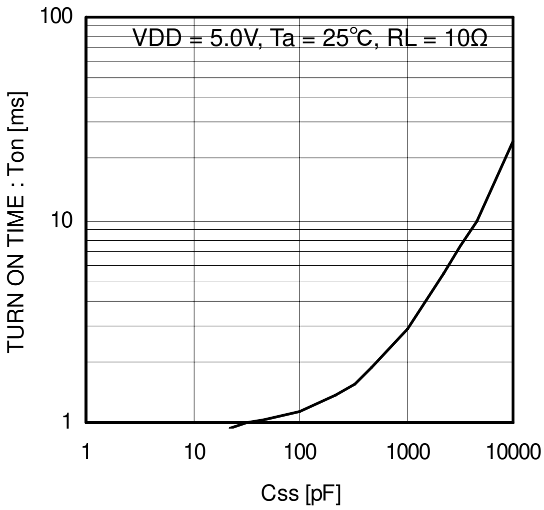


Figure 46. Turn On time (vs. Css)

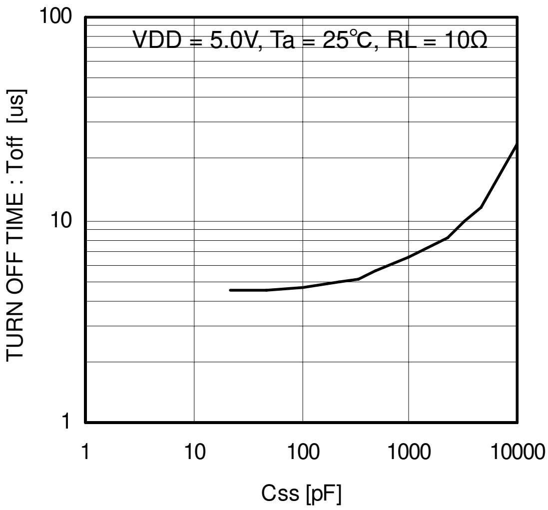


Figure 47. Turn Off time (vs. Css)

● **Typical Performance Curves - continued**

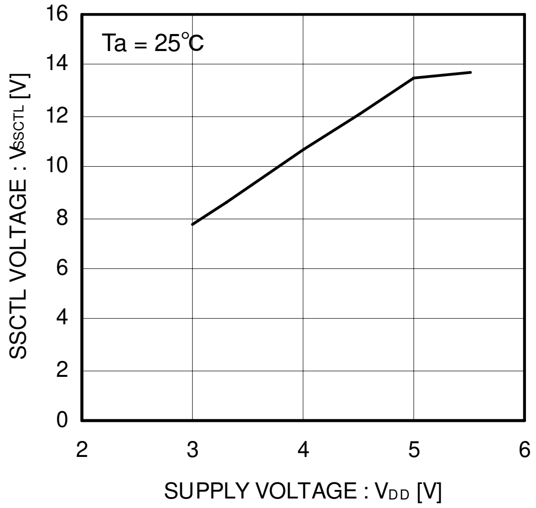


Figure 48. SSCTL output voltage

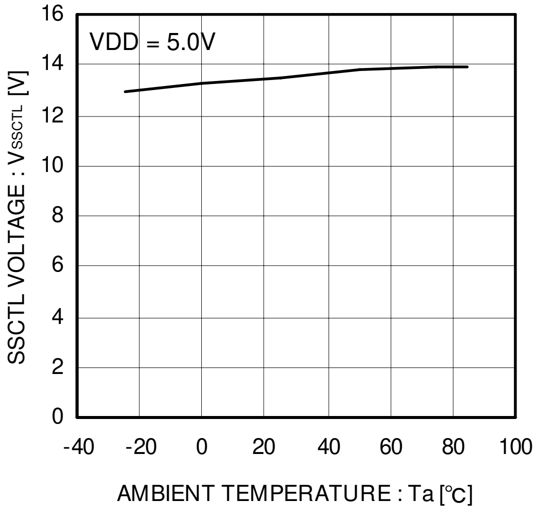


Figure 49. SSCTL output voltage

●Typical Wave Forms

V_{DD} = 5V, CL = 47µF, RL = 47Ω, unless otherwise specified.

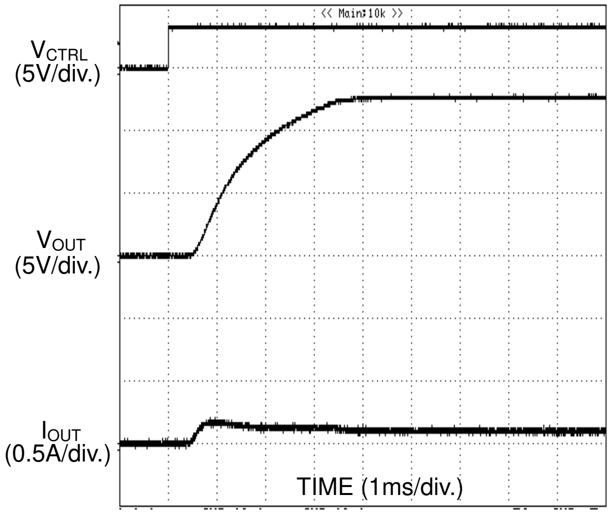


Figure 50. Turn On Rise Time (BD6520F)

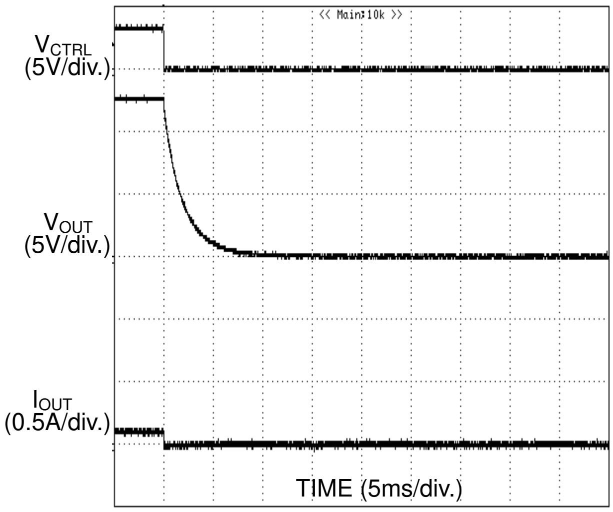


Figure 51. Turn Off Fall Time (BD6520F)

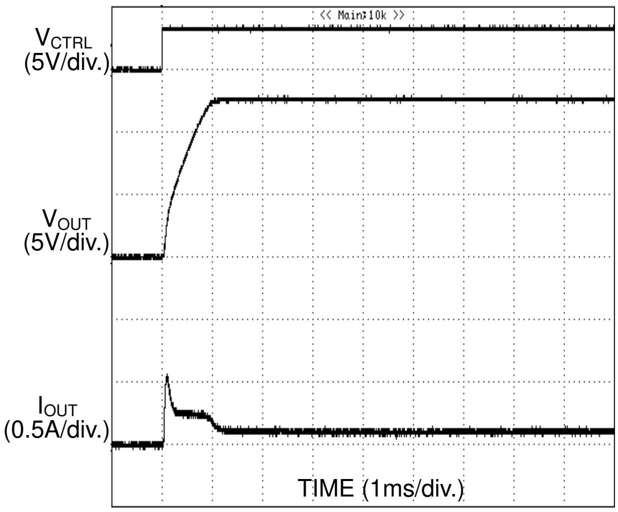


Figure 52. Turn On Rise Time (BD6522F)

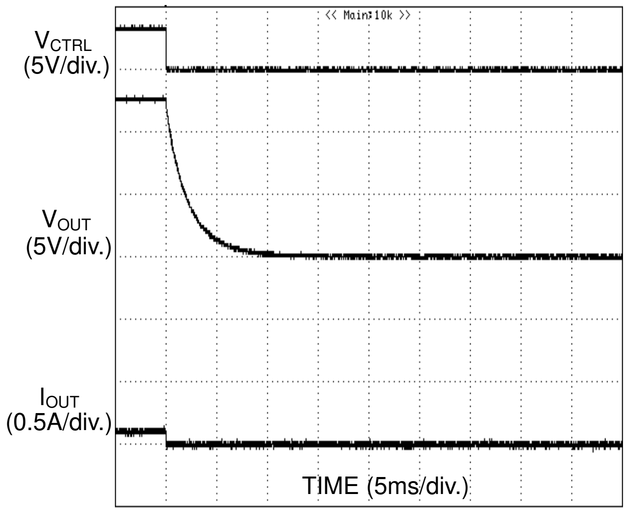


Figure 53. Turn Off Fall Time (BD6522F)

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●**Typical Wave Forms - continued**

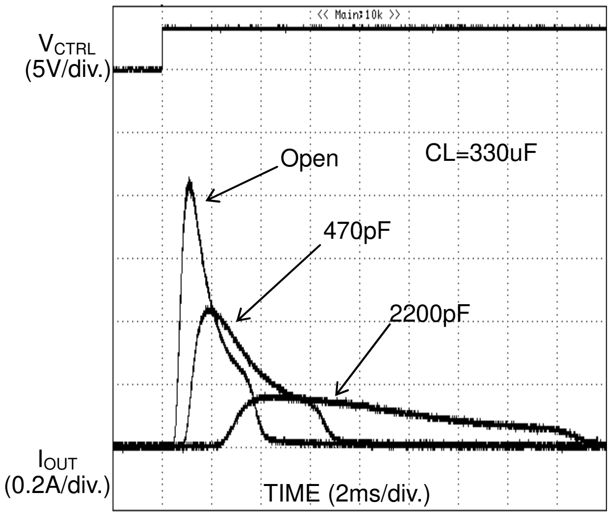


Figure 54. Inrush current vs. Css
(BD6520F)

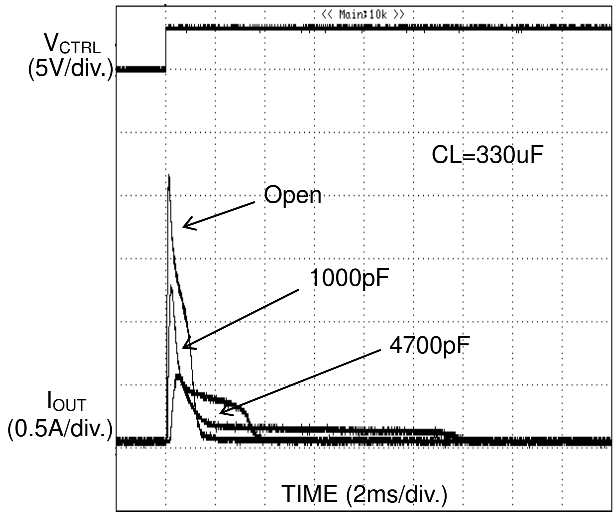


Figure 55. Inrush current vs. Css
(BD6522F)

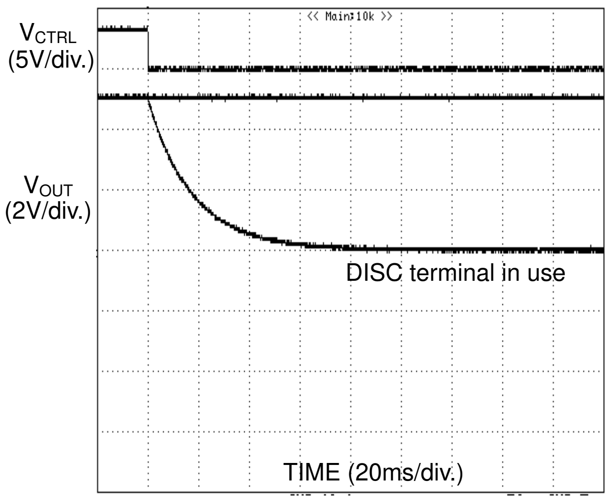


Figure 56. Discharge: CL = 47uF, RL = Open
(BD6522F)

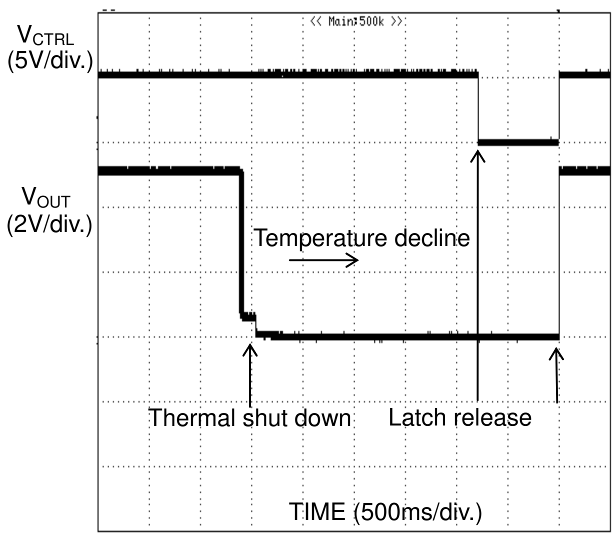


Figure 57. Thermal shutdown

●**Typical Wave Forms - continued**

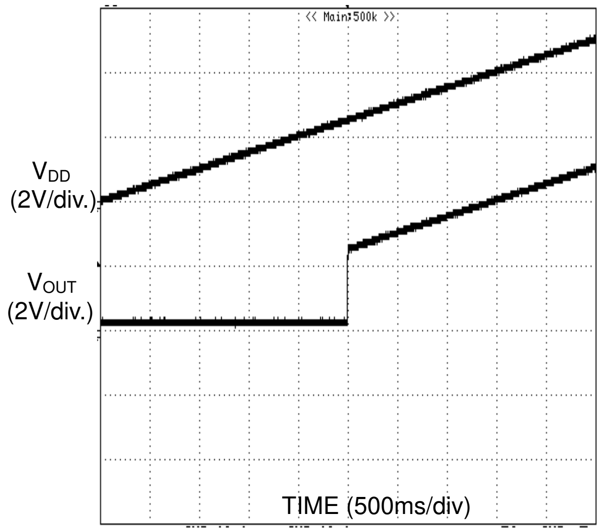


Figure 58. UVLO (at VDD increase)

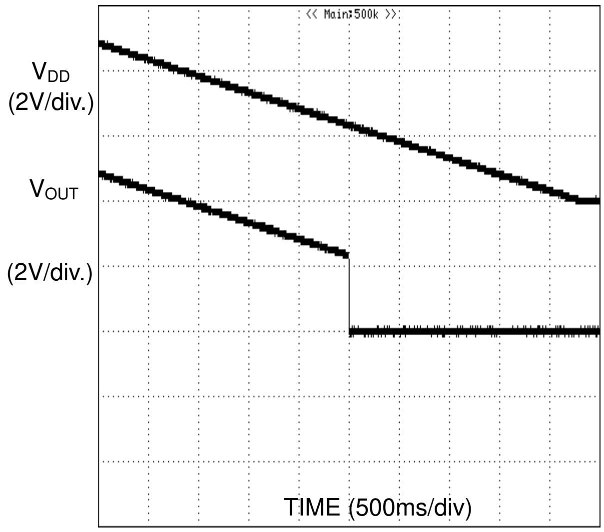


Figure 59. UVLO (at VDD decrease)

●**Typical Application Circuits**

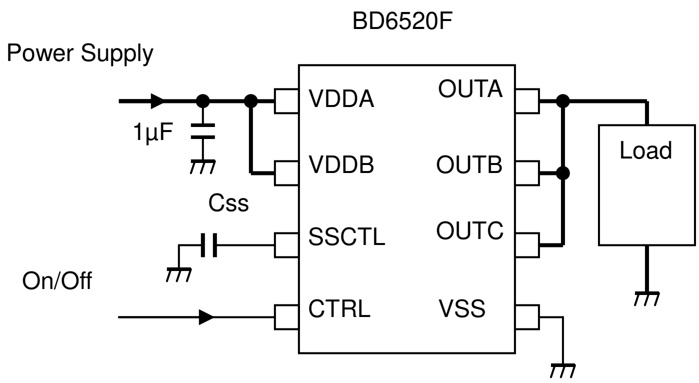


Figure 60. Power supply switch circuit (BD6520F)

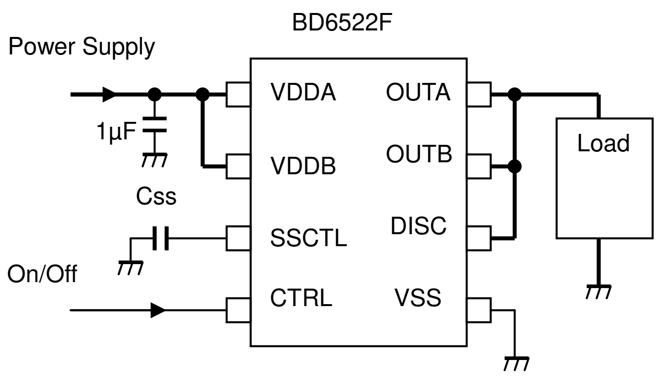


Figure 61. Power supply switch circuit (BD6522F)

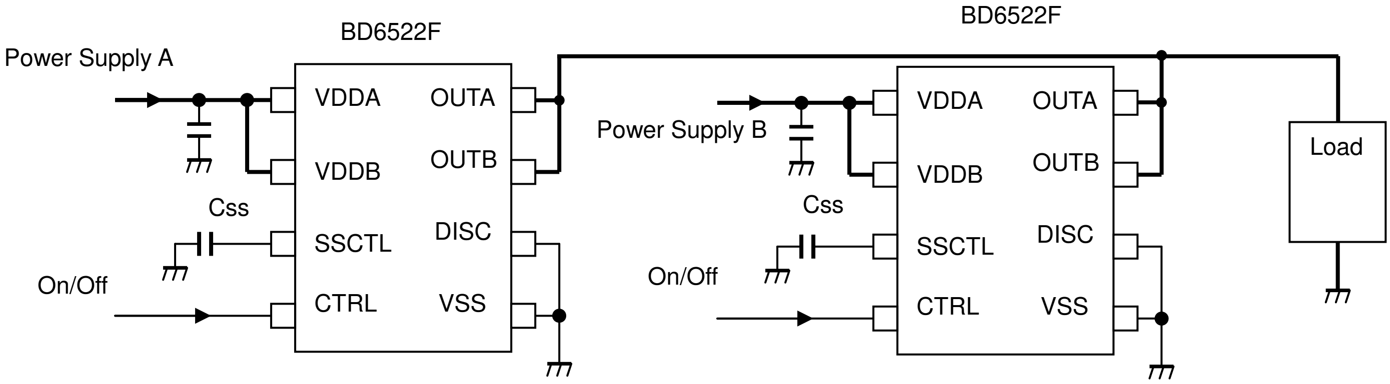


Figure 62. 2 power supply changeover switch circuit (BD6522F)

●Functional Description

1. Switch operation

VDD pin and OUT pin are connected to the drain and source of switch MOSFET respectively. VDD also serves as the power source input to internal control circuit.

When CTRL input is set to High level and the switch is turned on, VDD and OUT is connected by a 50mΩ switch. In a normal condition, current flows from VDD to OUT. If voltage of OUT is higher than VDD, current flows from OUT to VDD, since the switch is bidirectional.

In BD6520F, there is a parasitic diode between the drain and the source of switch MOSFET. Therefore, even when the switch is off and the voltage of OUT is higher than that of VDD, current will flow from OUT to VDD. In BD6522F, there is no parasitic diode and it is possible to prevent current from flowing reversely from OUT to VDD.

2. Thermal shutdown

Thermal shut down circuit turns off the switch of the circuit when the junction temperature exceeds 135℃(Typ.).

The switch off status of the thermal shut down is latched. Therefore, even when the junction temperature goes down, off status is maintained. To release the latch, it is necessary to input a signal to switch off by CTRL terminal or set UVLO state. When the input signal is switched on or UVLO is released, the switch output resets.

The thermal shut down circuit works when CTRL signal is active.

3. Low voltage malfunction prevention circuit (UVLO)

Other term for Under Voltage Lockout Circuit, the UVLO circuit monitors the voltage of the VDD pin when the CTRL input is active. UVLO circuit prevents the switch from turning on until the VDD exceeds 2.5V (Typ.). If the VDD drops below 2.3V (Typ.) while the switch turns on, then UVLO shuts off the switch.

4. Soft start control

In BD6520F/BD6522F, soft start is applied in order to reduce inrush current at switch on. Furthermore, in order to reduce inrush current, soft start control pin (SSCTL) is made available.

By connecting external capacitor between SSCTL and GND, it is possible to make rise time for the switch smooth. When the switch is enabled, SSCTL outputs a voltage of about 13.5V.

SSCTL terminal requires high impedance, therefore, proper packaging should be observed to avoid leak current. When a certain value of voltage is supplied to SSCTL terminal, switch on and/or off is disabled.

5. Discharge circuit

When the switch between VDD and OUT is OFF, the 350Ω(Typ.) discharge switch resistance between OUT and GND turns on. By turning on this switch, electric current at capacitive load is discharged.

In BD6522F, the input of discharge circuit is separately prepared as DISC pin. When discharge circuit is used, simply connect OUT pin and DISC pin to ensure proper operation.

●Timing diagram

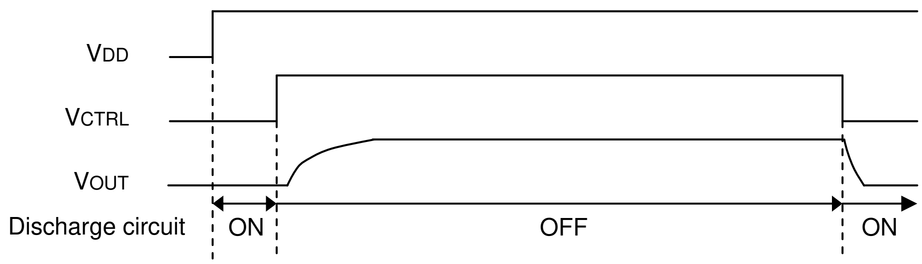


Figure 63. Normal operation

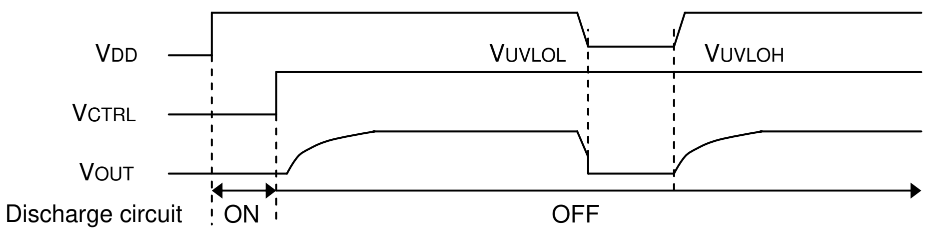


Figure 64. UVLO operation

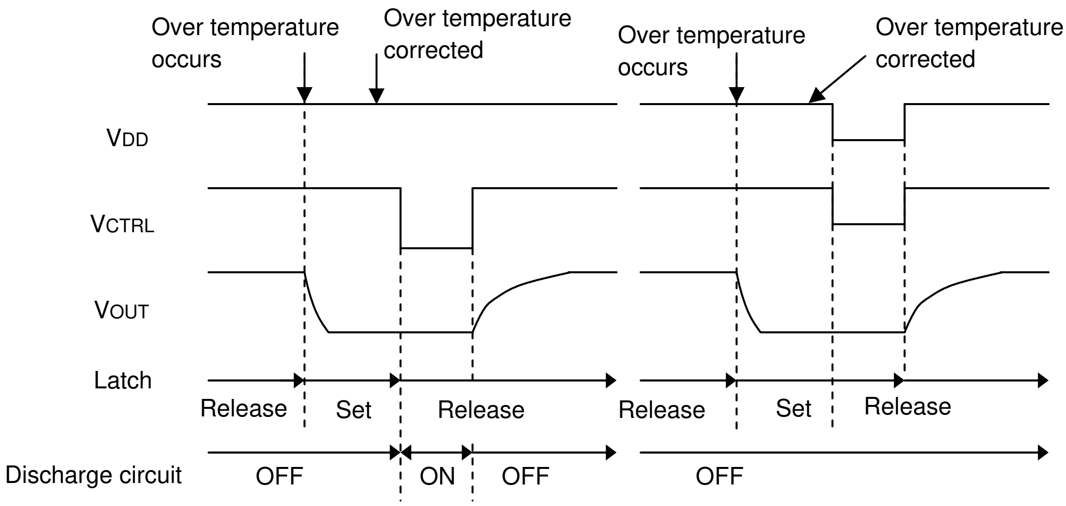


Figure 65. Thermal shutdown operation

● **Power Dissipation**

(SOP8)

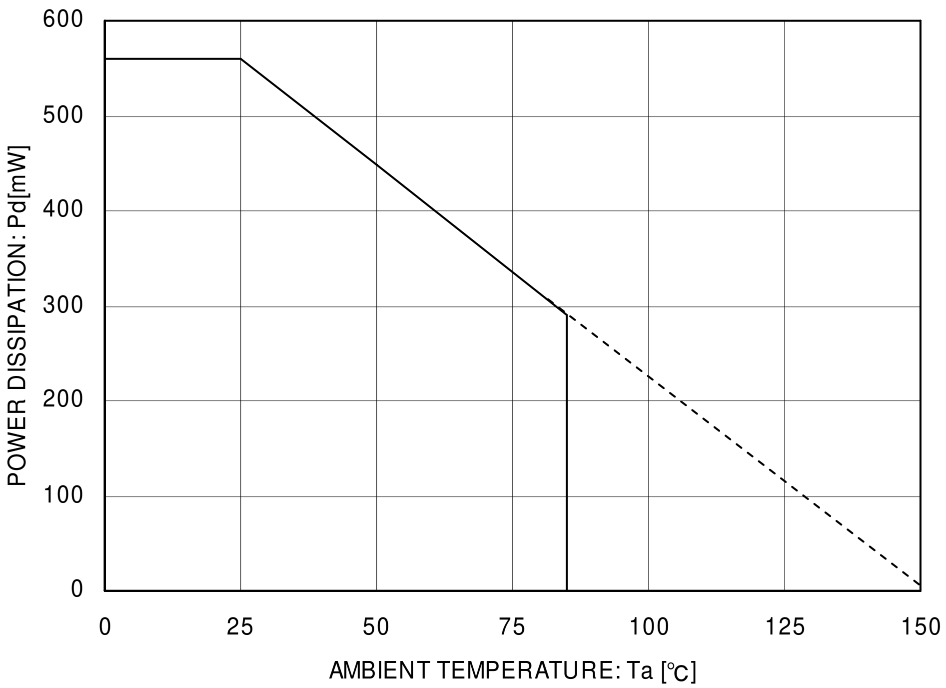
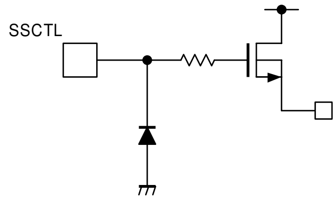
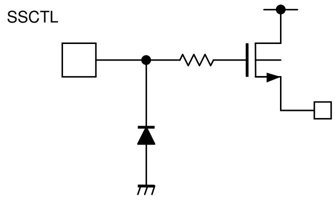
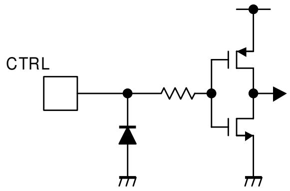
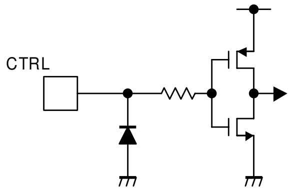
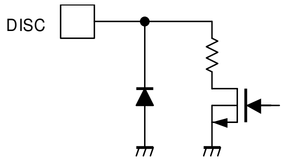
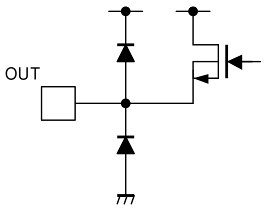
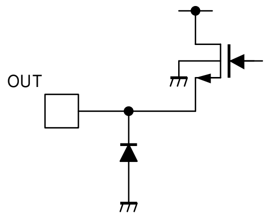


Figure 66. Power Dissipation Curve

●I/O Equivalent Circuit

Symbol	Pin No.	Equivalent circuit BD6520F	Equivalent circuit BD6522F
SSCTL	3		
CTRL	4		
DISC	6 (BD6522F)		
OUT	6 (BD6520F), 7, 8		

●Operational Notes

(1) Absolute Maximum Ratings
Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings

(2) Recommended operating conditions
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

(4) Power supply line
Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

(5) Ground Voltage
The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

(6) Short between pins and mounting errors
Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

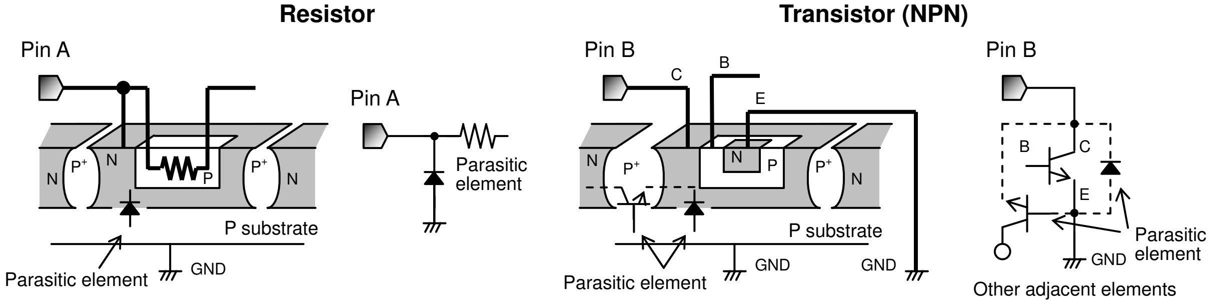
(7) Operation under strong electromagnetic field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

(8) Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(9) Regarding input pins of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of monolithic IC structure

(10) GND wiring pattern
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

(11) Capacitor between output and GND
If a large capacitor is connected between the output pin and GND pin, current from the charged capacitor can flow into the output pin and may destroy the IC when the VCC or VIN pin is shorted to ground or pulled down to 0V. Use a capacitor smaller than 10uF between output and GND.

(12) Thermal shutdown circuit (TSD)
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn off the IC when the internal temperature of the IC reaches a specified value. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.

(13) Thermal consideration
Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions. Consider Pc that does not exceed Pd in actual operating conditions (Pc≥Pd).

Package Power dissipation : Pd (W)=(Tjmax－Ta)/θja
Power dissipation : Pc (W)=(Vcc－Vo)×Io+Vcc×Ib

(Tjmax : Maximum junction temperature=150℃, Ta : Peripheral temperature[℃] ,
θja : Thermal resistance of package-ambience[℃/W], Pd : Package Power dissipation [W],
Pc : Power dissipation [W], Vcc : Input Voltage, Vo : Output Voltage, Io : Load, Ib : Bias Current)