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DC Brushless Fan Motor Drivers

Three-Phase Full-Wave Fan Motor Driver

BD67173NUX

General Description

BD67173NUX is a three-phase sensorless fan motor driver used to cool off notebook PCs. It is controlled by a variable speed provided through the PWM input signal. Its feature is sensorless drive which doesn't require a hall device as a location detection sensor and motor downsizing can be achieved by limiting the number of external components as much as possible.
Furthermore, introducing a direct PWM soft switched driving mechanism achieves silent operations and low vibrations.

Features

- Speed controllable by PWM input signal
- Sensorless drive
- Soft switched drive Quick start
- Power save function
- Internal RNF resistance
- Quick start function

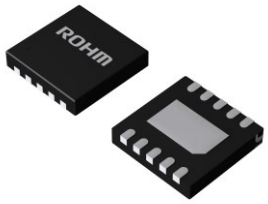
Applications

- Small fan motor for notebook PCs etc.

Key Specifications

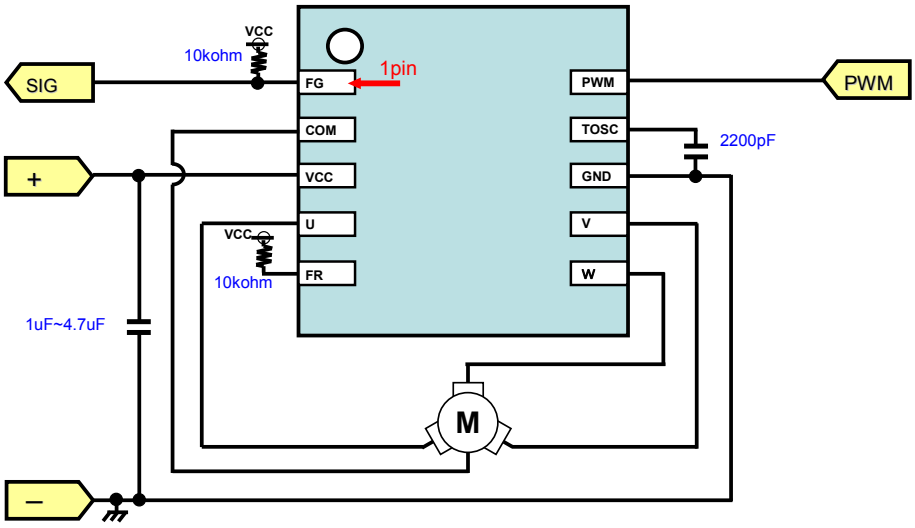
- Operating Supply Voltage Range: 2.2V to 5.5V
- Operating Temperature Range: -25°C to +95°C

Package(s)	W(Typ) x D(Typ) x H(Max)
VSON010X3030	3.00mm x 3.00mm x 0.60mm



VSON010X3030

Typical Application Circuit(s)



Contents

Pin Configuration

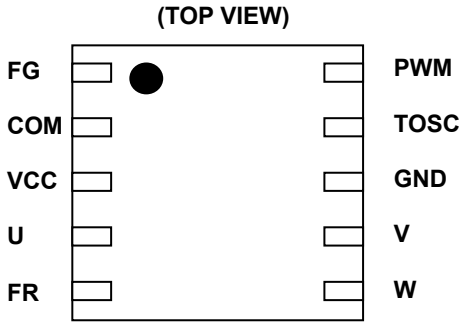


Figure 1. Pin Configuration

Pin Description(s)

Pin No.	Pin Name	Function
1	FG	FG output pin
2	COM	Coil midpoint pin
3	VCC	Power supply pin
4	U	U phase output pin
5	FR	Motor rotation direction select pin
6	W	W phase output pin
7	V	V phase output pin
8	GND	GND pin
9	TOSC	Start-up oscillation pin
10	PWM	PWM signal input pin

Block Diagram

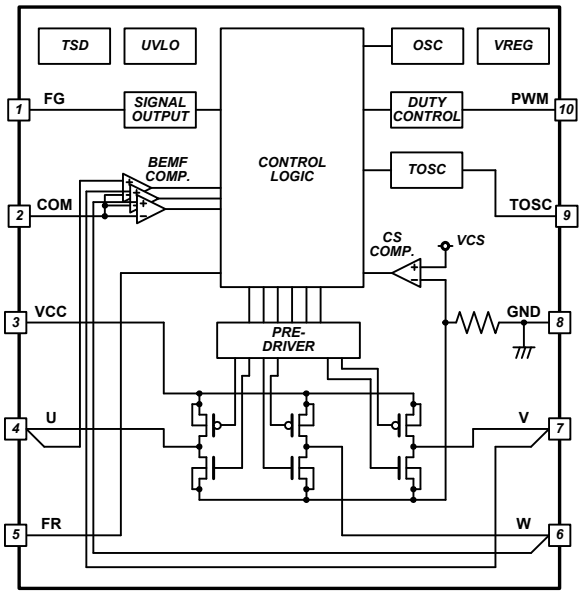


Figure 2. Block Diagram

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Limit	Unit
Supply voltage	VCC	7	V
Power dissipation	Pd	0.58 *1	W
Operating temperature	Topr	–25 to +95	°C
Storage temperature	Tstg	–55 to +150	°C
Output voltage	Vomax	7	V
Output current	Iomax	700*2	mA
FG signal output voltage	VFG	7	V
FG signal output current	IFG	10	mA
Junction temperature	Tj	150	°C

*1 Reduce by 4.64mW/°C over Ta=25°C. (On 74.2mm×74.2mm×1.6mm glass epoxy board)
*2 This value is not to exceed Pd

Recommended Operating Conditions (Ta= -25°C to +95°C)

Parameter	Symbol	Min	Typ	Max	Unit
Operating supply voltage range	V_{CC}	2.2	5	5.5	V
Input voltage range(PWM, FR)	V_{IN}	0	-	VCC	V

Electrical Characteristics (Unless otherwise specified V_{CC}=5V Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions	Ref. Data
<OVERALL>							
Circuit current STB	I_{CST}	-	15	30	uA	FR=Open	Fig. 3
Circuit current	I_{CC}	1.8	4.2	6.6	mA		Fig. 4
<PWM>							
PWM input H level	V_{PH}	2.5	-	VCC	V		
PWM input L level	V_{PL}	0	-	0.7	V		
PWM input current H	I_{PH}	-	0	1	uA	PWM=VCC	Fig. 5
PWM input current L	I_{PL}	-30	-15	-	uA	PWM=GND	Fig. 6
Input frequency	F_{PWM}	10	-	50	kHz		
<FR>							
FR input H level	V_{FRH}	2.5	-	VCC	V	FR=H : Normal rotation	
FR input L level	V_{FRL}	0	-	0.5	V	FR=L; Reverse rotation	
FR input current H	I_{FRH}	-	0	1	uA	FR=VCC	Fig. 7
FR input current L	I_{FRL}	-50	-25	-	uA	FR=GND	Fig. 8
<TOSC >							
TOSC frequency	F_{TOSC}	28	40	52	kHz	TOSC-GND 2200pF	
TOSC charge current	I_{CTOSC}	-125	-100	-75	uA	TOSC=0.5V	Fig. 9
TOSC discharge current	I_{DTOSC}	75	100	125	uA	TOSC=1.0V	Fig. 10
<FG>							
FG low voltage	V_{FGL}	-	0.12	0.3	V	IFG＝5mA	Fig.11 12
<Output >							
Output voltage	V_O	-	0.25	0.325	V	Io＝250mA (H.L. total)	Fig.13 14 Fig.15 16
PWM off time	t_{POFF}	0.5	1.0	2.0	ms		
Lock protection det. Time	t_{ON}	0.7	1.0	1.3	s		Fig. 17
Lock protection rel. time	t_{OFF}	3.3	5.0	8.3	s		Fig 18

About a current item, define the inflow current to IC as a positive notation, and the outflow current from IC as a negative notation.

Typical Performance Curves

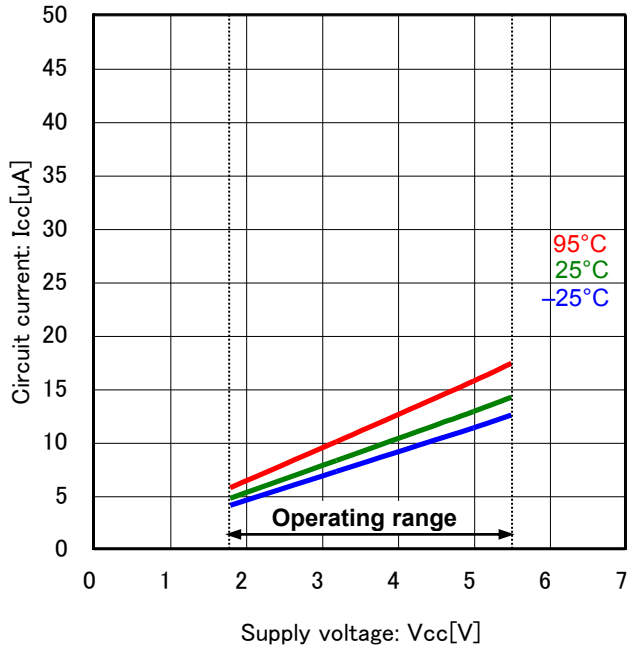


Figure 3 Circuit current STB

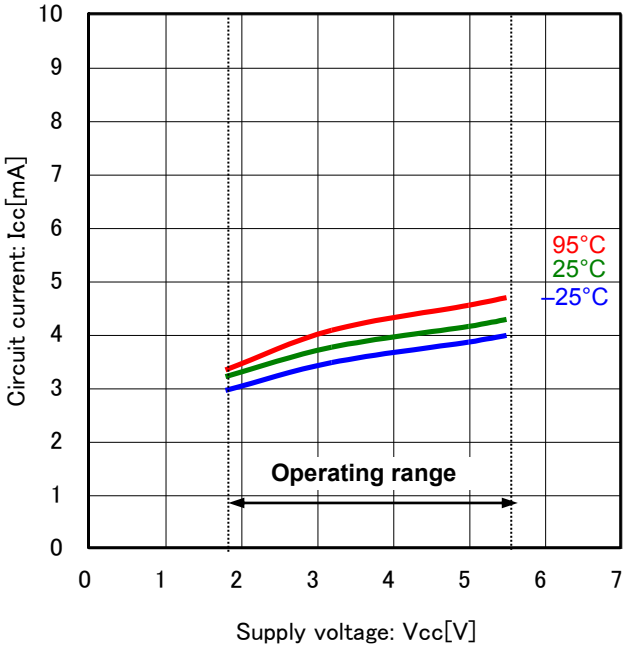


Figure 4 Circuit current

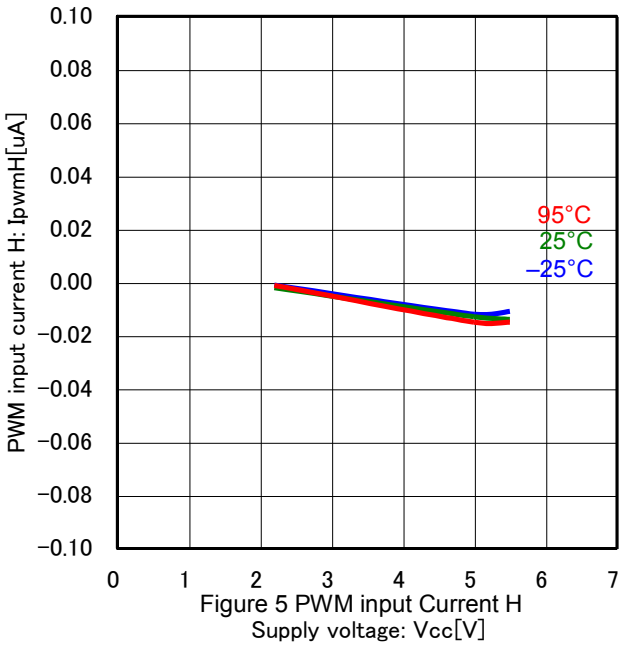


Figure 5 PWM input Current H

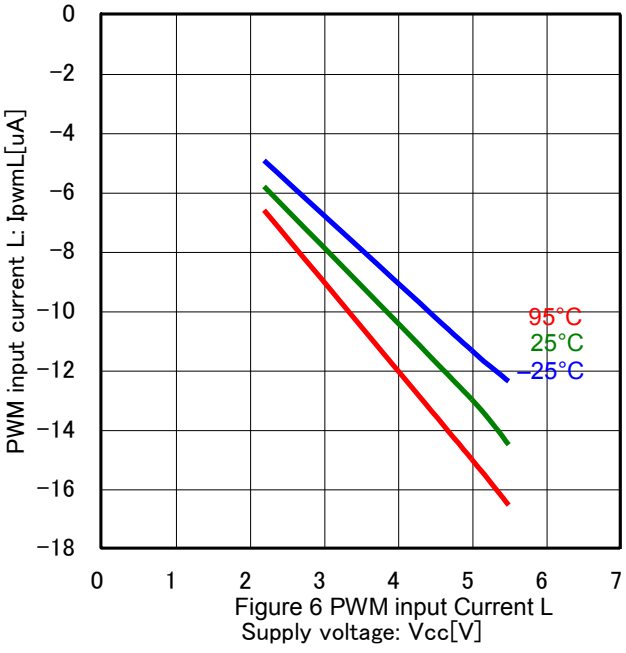


Figure 6 PWM input Current L

Typical Performance Curves2

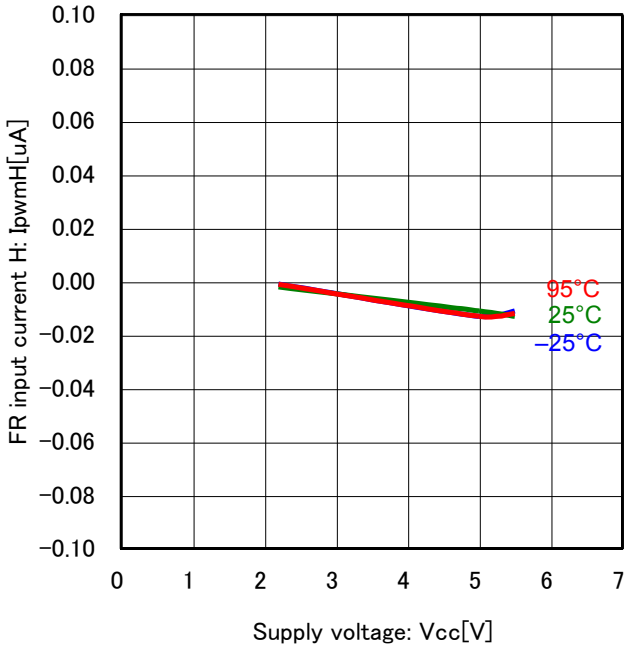


Figure 7 FR input Current H

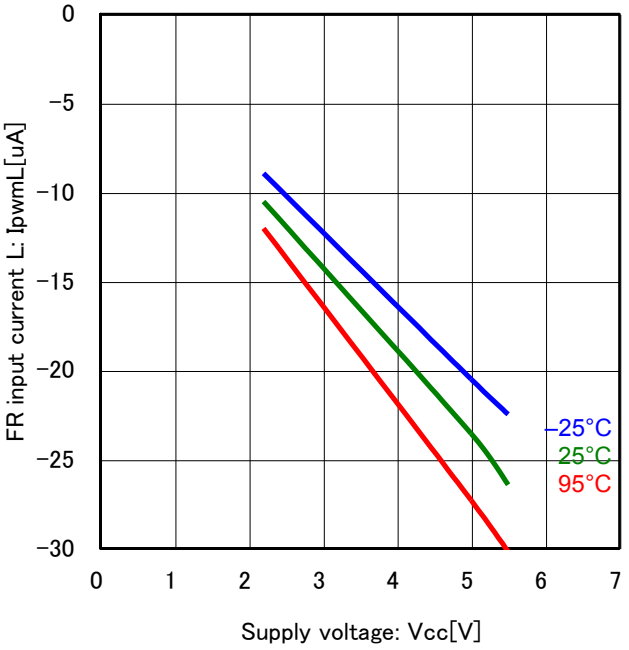


Figure 8 FR input Current L

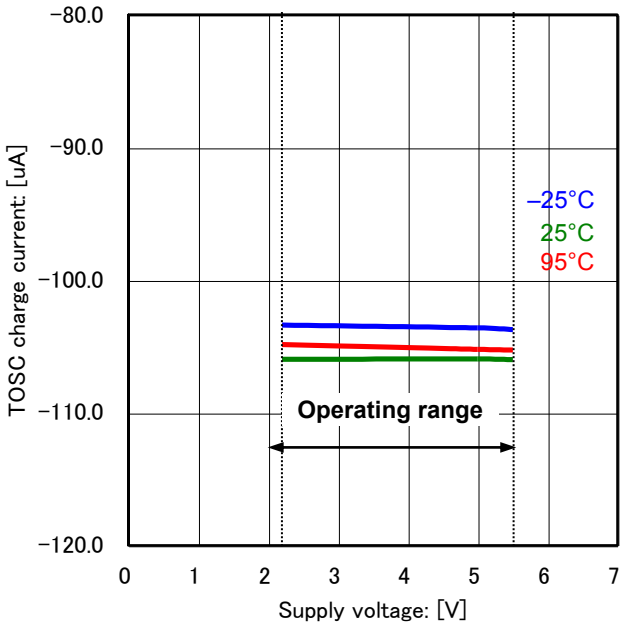


Figure 9 TOSC charge current

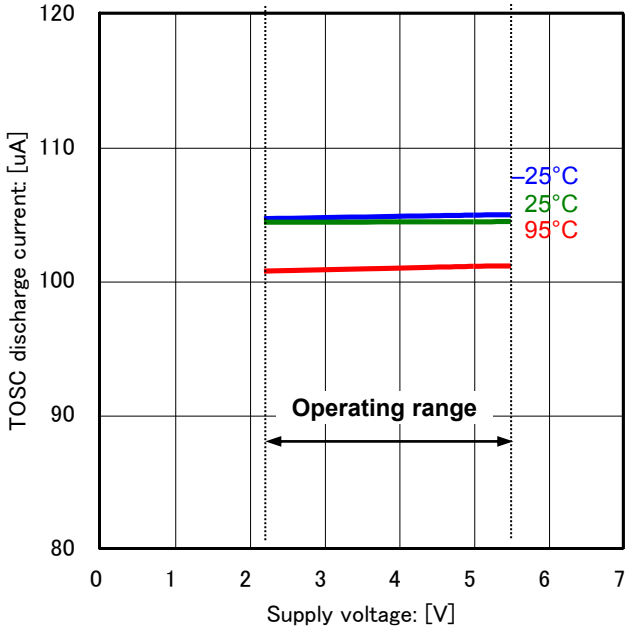


Figure 10 TOSC discharge current

Typical Performance Curves3

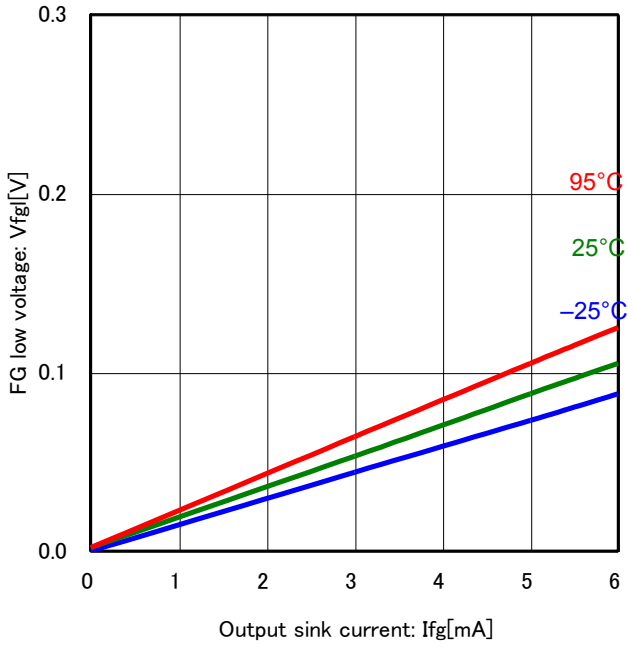


Figure 11 FG output low voltage (Vcc=5V)

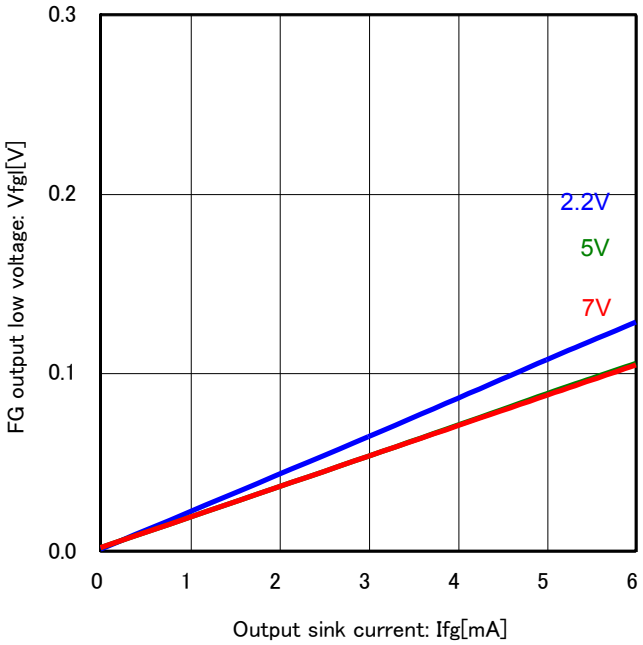


Figure 12 FG output low voltage (Ta=25°C)

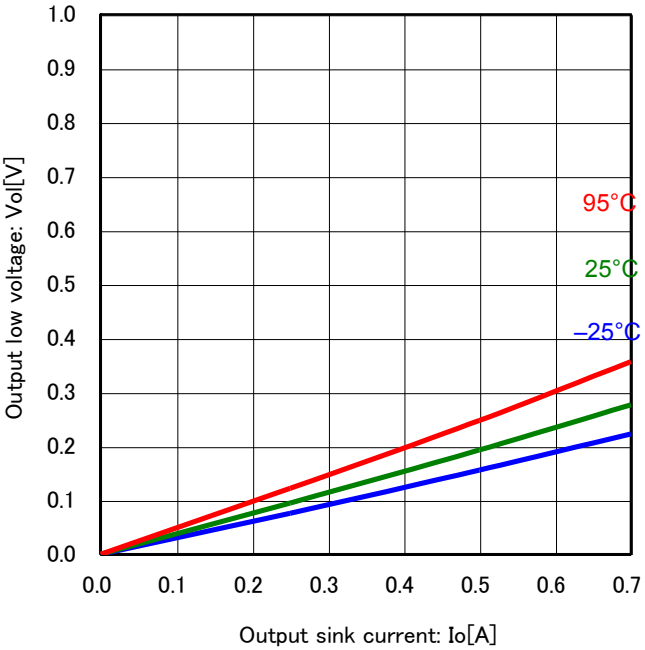


Figure 13 Output Low voltage (Ta=25°C)

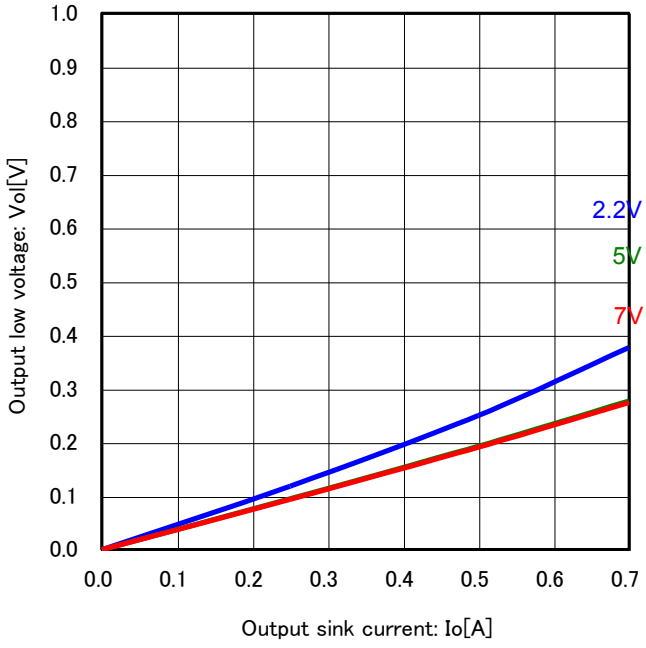


Figure 14 Output Low voltage (Vcc=5V)

Typical Performance Curves4

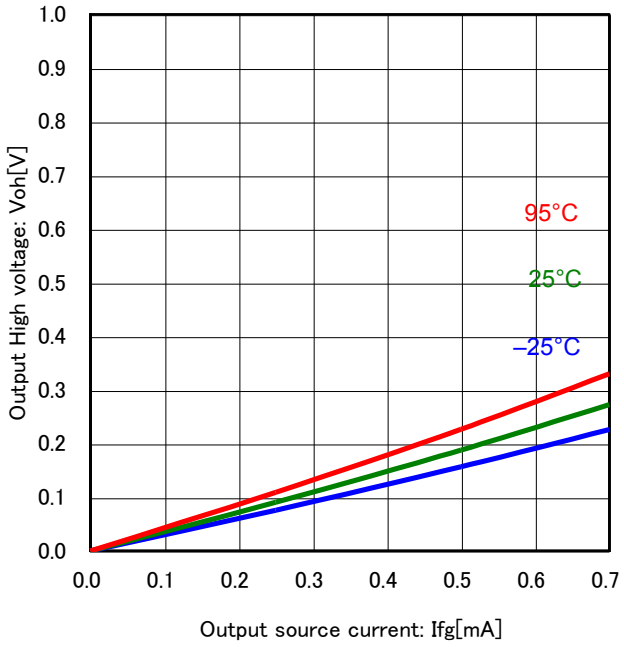


Figure 15 Output high voltage (Vcc=5V)

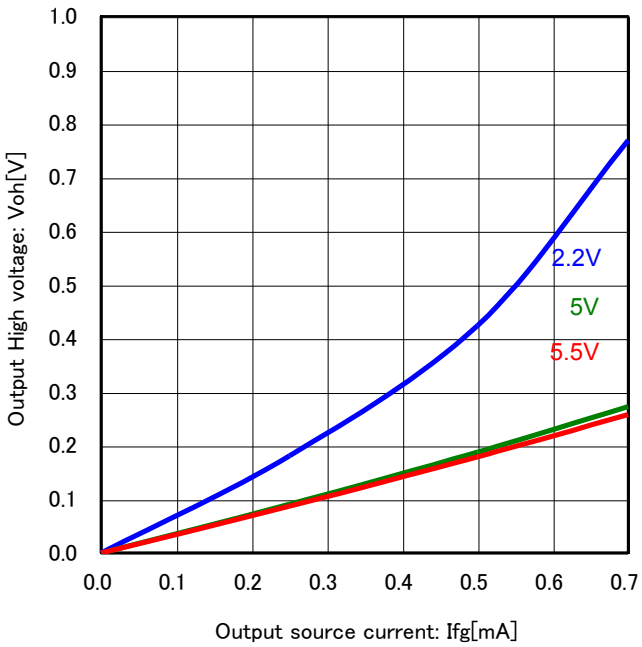


Figure 16 Out high voltage (Ta=25°C)

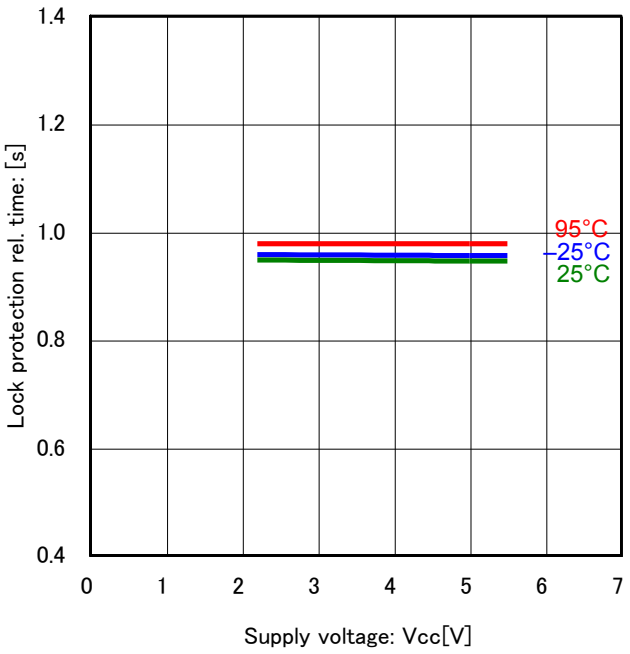


Figure 17 Lock protection det. Time

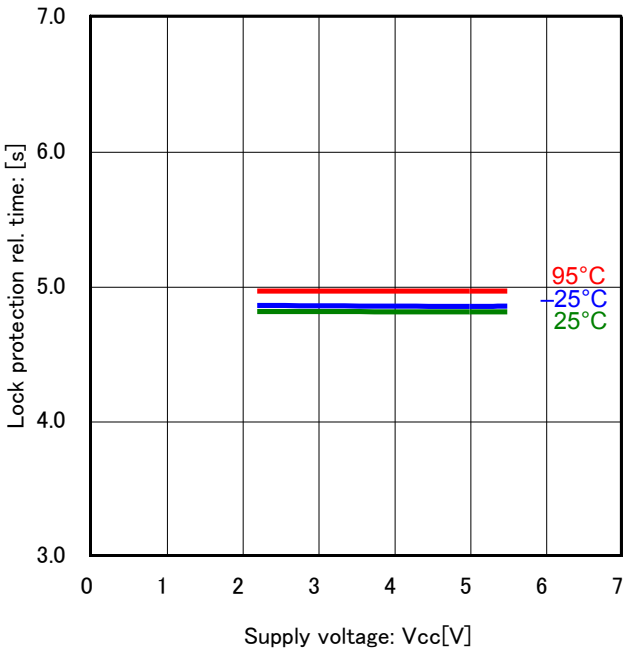


Figure 18 Lock protection rel. time

Application circuit example (Constant values are for reference)

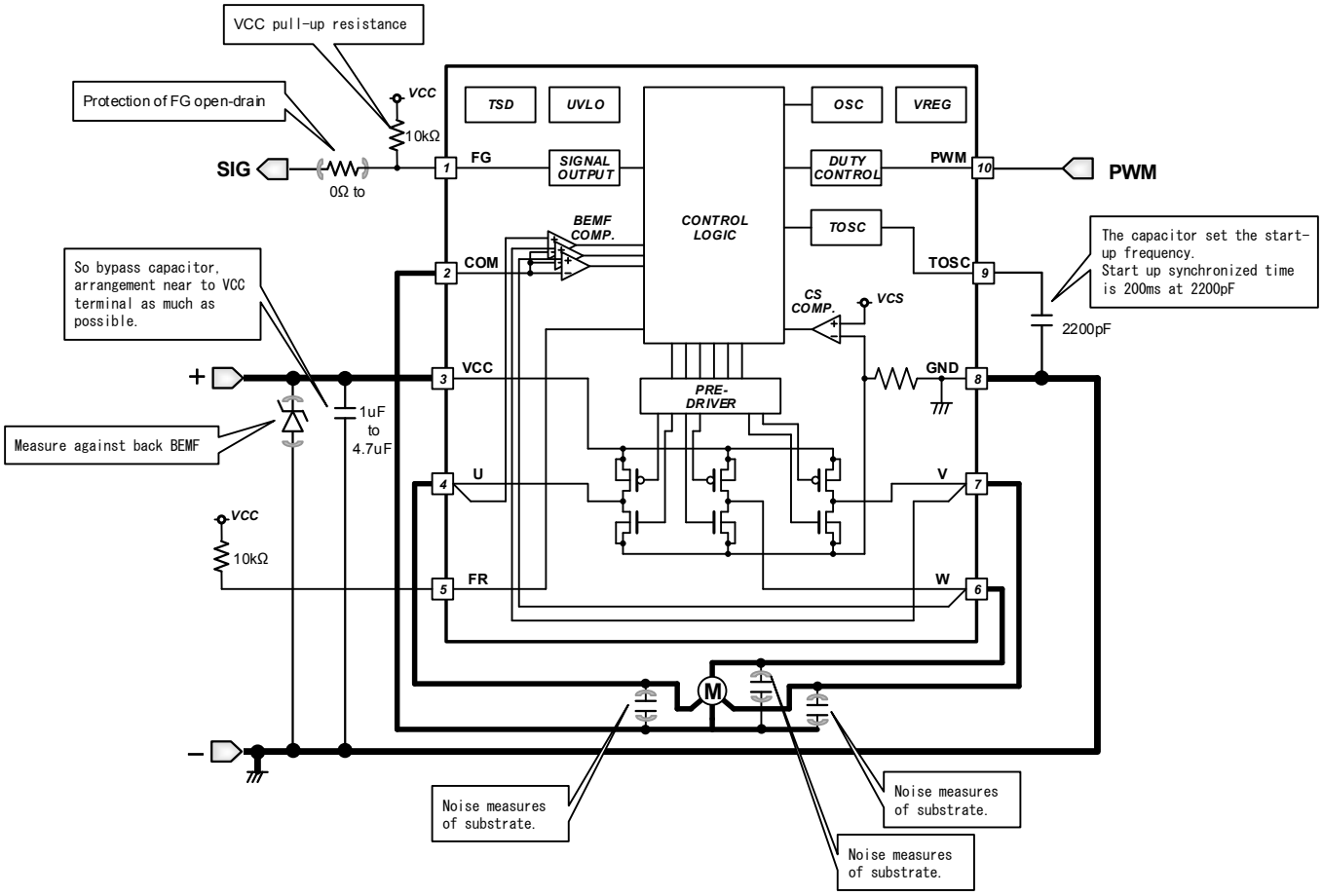


Figure 19. PWM Controllable 4 Wires Type (FG) Motor Application Circuit

- The wiring patterns from the VCC terminal and GND terminal to the bypass capacitor must be routed as short as possible. Because full PMW driving becomes the factor of the noise in BD67173NUX , the value of bypass capacitor set to 4.7uF,2.2uF or 1uF. With respect to the wiring pattern, It has been confirmed that 0.03Ω for 4.7uF,2.2uF or 1uF at the bypass capacitor doesn't cause problems under our operation environment. This can be used as a reference value to check for validity.
- When it is noisy, Capacitance should be inserted between U-COM, V-COM, and W-COM.
- Connect a capacitor between TOSC terminal and GND. Start-up frequency can be adjusted.
  When TOSC terminal is opened and is connected to GND, start –up operation becomes unstable.

Substrate design note

a) IC power, motor outputs, and motor ground lines are made as fat as possible.
b) IC ground (signal ground) line arranged near to (–) land.
c) The bypass capacitor is arrangement near to VCC terminal.
d) When substrates of outputs are noisy, add capacitor as needed.
e) When back EMF is large, add zener diode as needed.

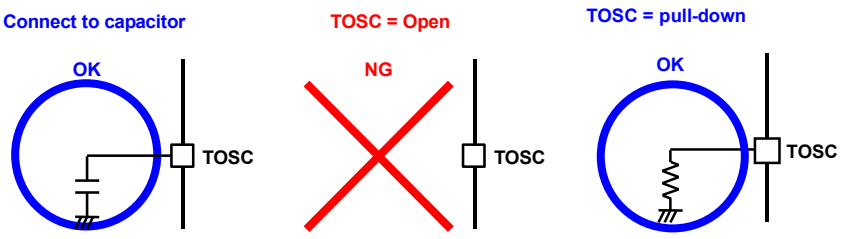


Figure 20. TOSC Function Setting

Description of Function Operation

1. State Transition

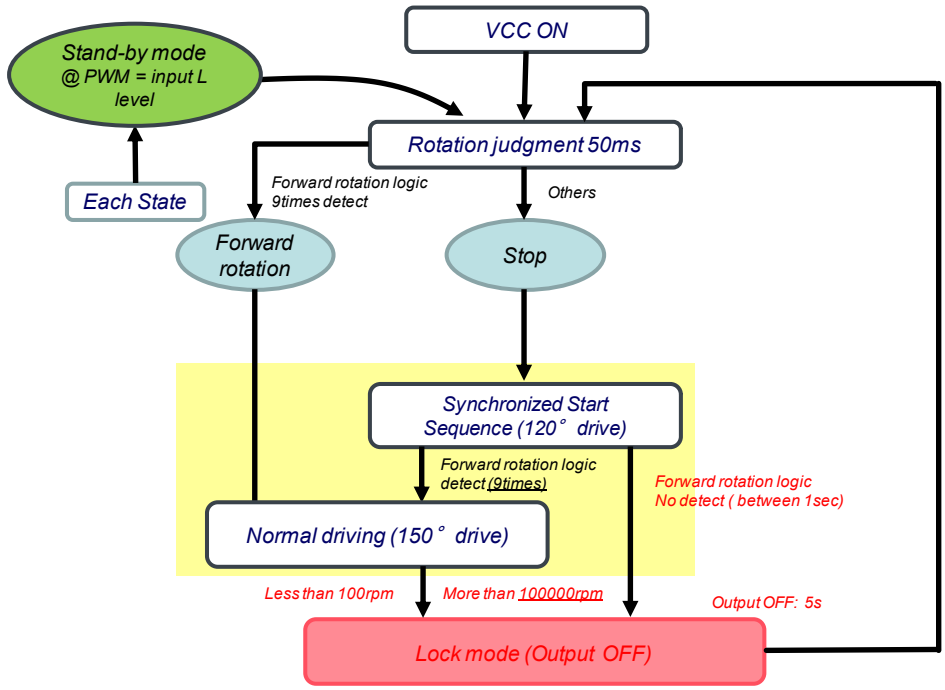
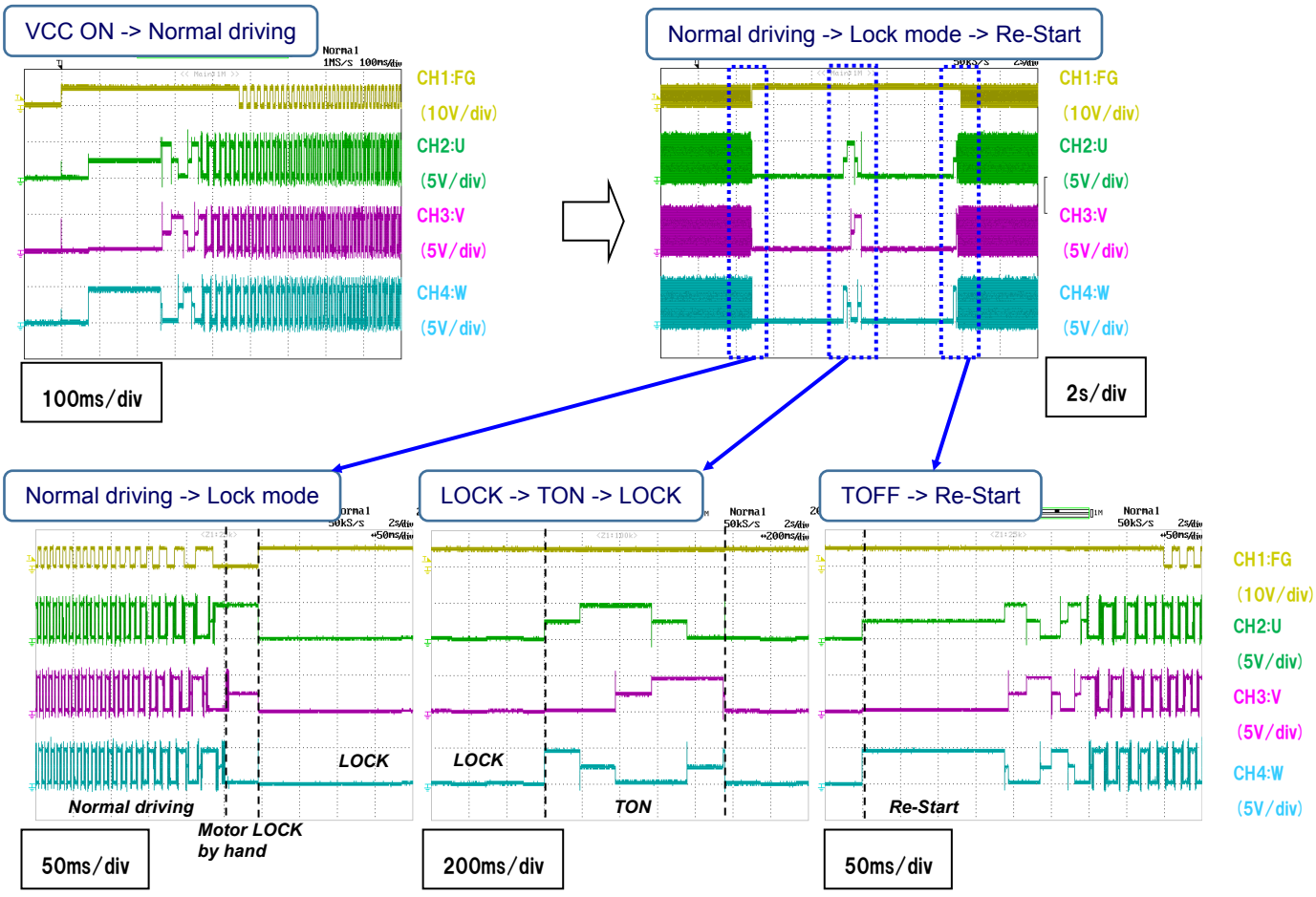


Figure 21. Flow chart



2. Sensorless Drive

BD67173NUX is a motor driver IC for driving a three-phase brushless DC motor without a hall sensor. Detecting a rotor location firstly at startup, an appropriate logic for the rotation direction is obtained using this information and given to each phase to rotate the motor. Then, the rotation of the motor induces electromotive voltage in each phase wiring and the logic based on the induced electromotive voltage is applied to the each phase to continue rotating.

2.1 Motor Drive Output Voltage and Current U, V, and W

The timing charts of the output signals from the U, V and W output is shown (Figure 6.).
The detection of the BEMF voltage does with output U, V, and W (for rise and fall zero-cross) and detects the position of the motor rotation.

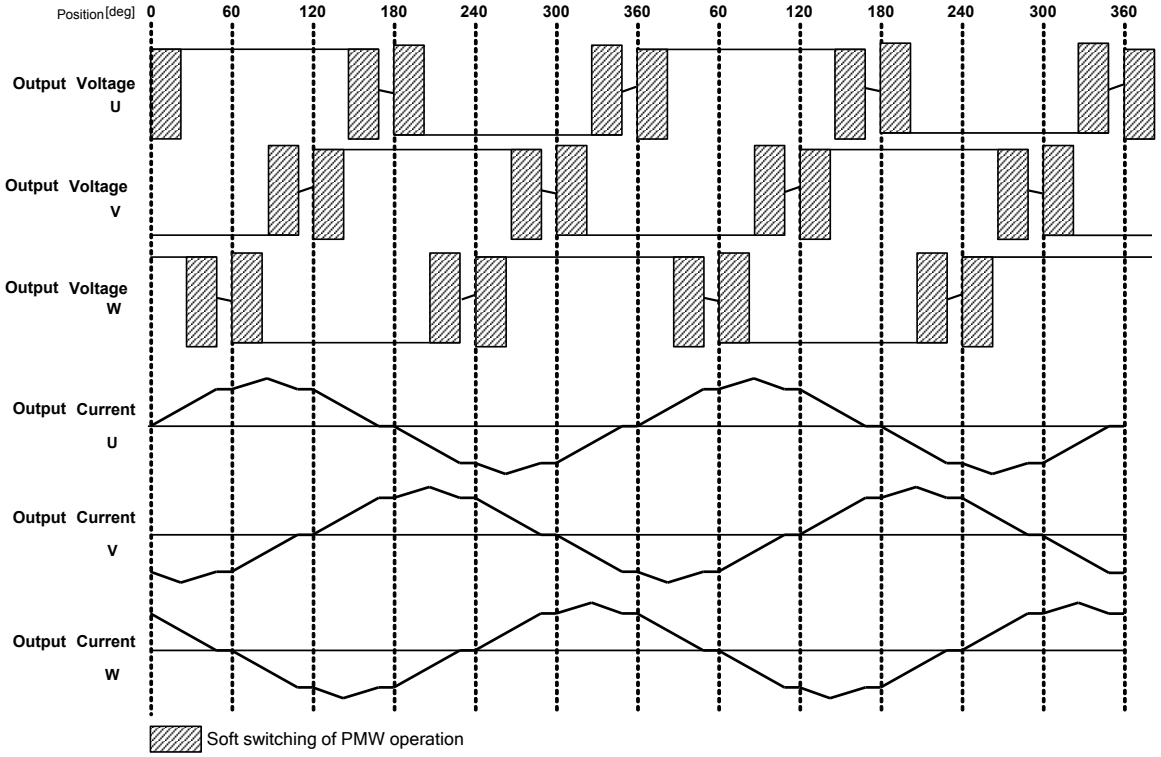


Figure 22. Motor Drive Output Timing Chart

2.2 BEMF Detection Driving Mechanism (Synchronized Start-up Mechanism)

BD67173NUX's start mechanism is synchronized start-up mechanism. BD67173NUX as BEMF detection driving starts by set output logic and monitors BEMF voltage of motor. Driving mechanism changes to BEMF detection driving after detect BEMF signal. When BEMF signal isn't detected for constant time at start-up, synchronized start-up mechanism outputs output logic forcibly by using standard synchronized signal (sync signal) and makes motor forward drive. This assistance of motor start-up as constant cycle is synchronized driving mechanism. Synchronized frequency is standard synchronized signal. Figure 23, the timing chart (outline) is shown. "Motor start-up frequency setting" generation of synchronized period is shown.

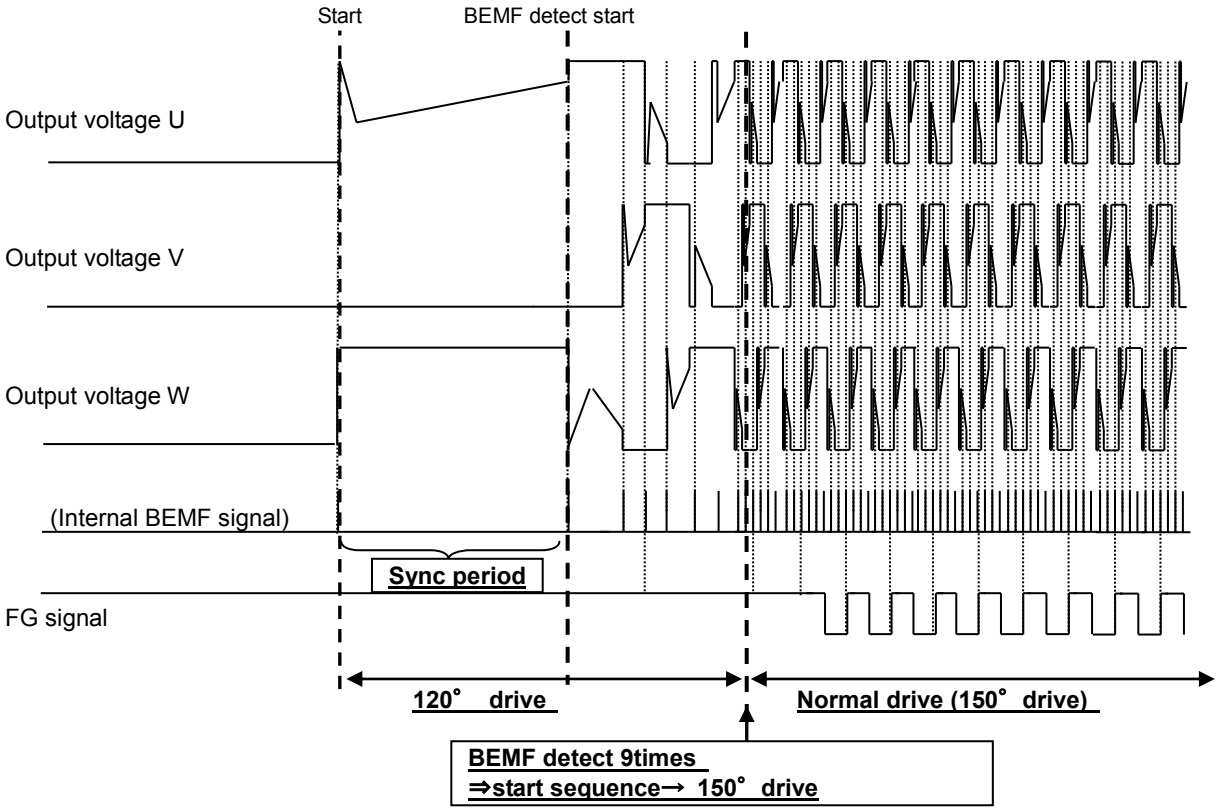
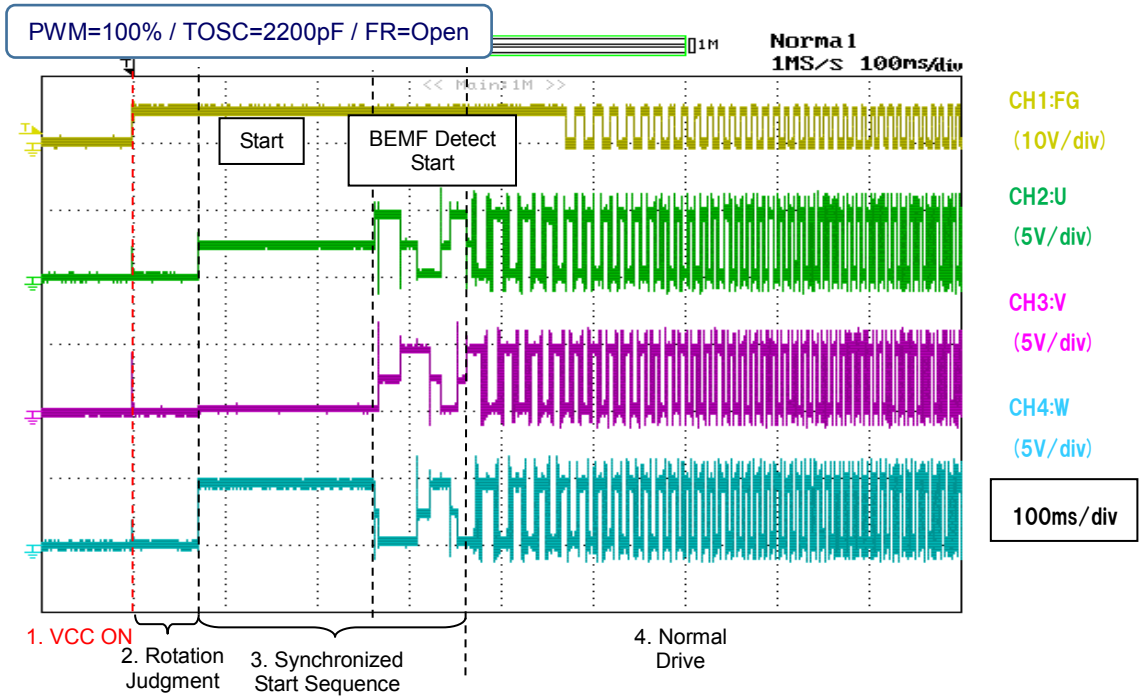


Figure 23. Synchronized Start-up Output Timing Chart



	Number of BEMF detection (from start-up)		
	Start-up	Until BEMF detection 9 times successively	after BEMF detection 9 times successively
Synchronized time	8000 × TOSC		
PWM duty	PWM = fixed 100%		PWM = same as external PWM duty
Electrify angle	120° drive		150° drive

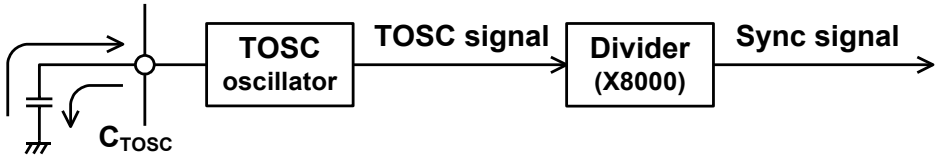
*Disagree with above timing chart

Table 1. Setting of Electrify Angle and Output Duty While Start-up

2.3 Synchronized Start-up Frequency Setting (TOSC capacitor)

The TOSC terminal starts a self-oscillation by connecting a capacitor between the TOSC terminal and GND. It becomes a start-up frequency, and synchronized time. Synchronized time can be adjusted by changing external capacitor. When the capacitor value is small, synchronized time becomes short. It is necessary to choose the best capacitor value for optimum start-up operation. For example external capacitor is 2200pF, synchronized time is 200ms (typ.). 2200pF is recommended for setting value at first. Relationship between external capacitor and synchronized time is shown in below. When connect TOSC terminal to GND, synchronized time is fixed and synchronized time is same as 2200pF.

Diagram of Relationship between TOSC terminal and synchronized time



Synchronized time = 8000 x TOSC period

Charge current : 100uA discharge current : 100uA

Example

C_{TOSC} = 2200pF

TOSC frequency = 40kHz (typ.). TOSC period = 25usec.

Synchronized time = 200msec.

External capacitor	Synchronized time
3300pF	300ms
2200pF (Recommendation)	200ms
1000pF	90ms

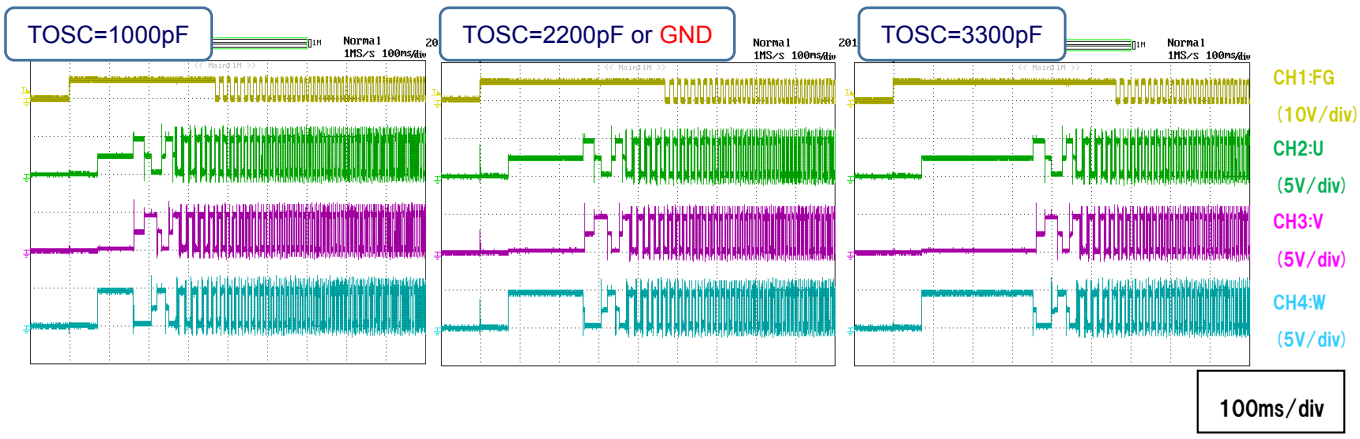
Equation

$$Tosc = 2x\frac{C_{TOSC}V_{TSOC}}{I}$$

Ctosc: Tosc terminal capacitor value.

Vtosc: Tosc terminal Hi voltage – Lo voltage= 0.57V (typ.).

I: Tosc terminal charge and discharge current.



*Setting of Appropriate Capacitor Value

Appropriate value of synchronized time is differ with characteristic and parameter of motor. Appropriate value decided by start-up confirmation with various capacitor value. At first confirm start-up with 2200pF, next is 2400,2700,3000,3300pF・・・,and 2000,1800,1600,1500,1300pF・・・etc. Appropriate capacitor value is decided after confirm maximum start-up NG value and minimum start-up NG value. For example, small BEMF voltage motor tends to small capacitor value. Set capacitor value after confirm sufficiently.

* About the Final Decision that Considers Each Dispersion

Please consider this dispersion before decision of optimal value of capacitor by start-up confirmation. (Figure 24.)
It is necessary to think about the dispersion of ±25% from TOSC external capacitor (±10%)and IC characteristics. Moreover, Lock ON detect time (page 5.) becomes a restriction of start-up confirmation. It is necessary to think about the dispersion of TON (0.7s: min). If necessary, it is possible to provide the evaluation samples and boards for the TON dispersion evaluation.

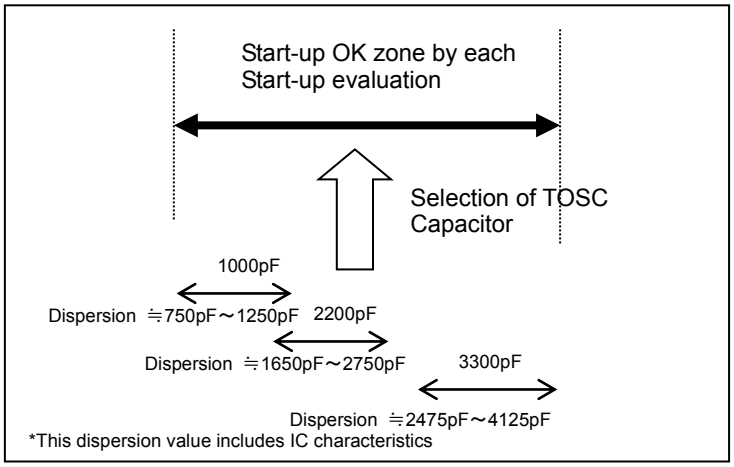


Figure 24. The Final Decision that Considers Each Dispersion

2.4 Motor Drive Output U, V, W and FG Output Signals

In Figure 25, the timing charts of the output signals from the U, V and W phases as well as the FG terminal is shown. Assuming that a three-slot tetrode motor is used, two pulse outputs of FG are produced for one motor cycle. The three phases are excited in the order of U, V and W phases.

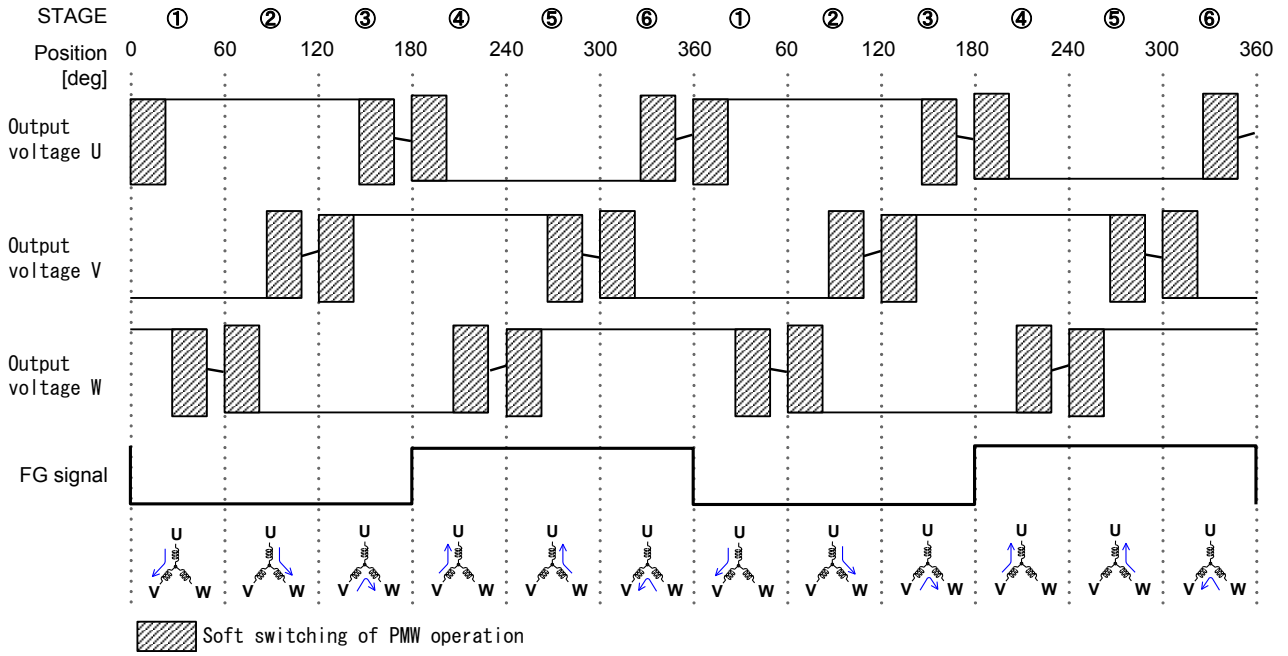
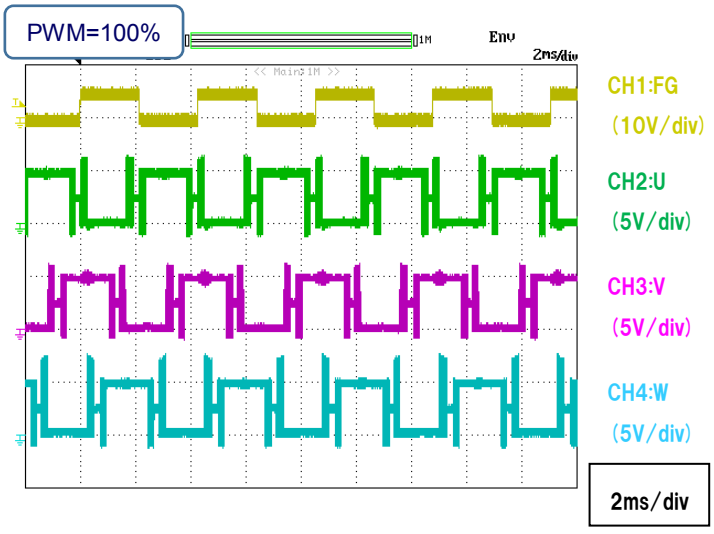


Figure 25 Timing Chart of U, V, W and FG Output (FR = Hi or No Connect)

Output pattern	Motor output		
	Motor output U	Motor output V	Motor output W
①	H	L	Hi-Z
②	H	Hi-Z	L
③	Hi-Z	H	L
④	L	H	Hi-Z
⑤	L	Hi-Z	H
⑥	Hi-Z	L	H

* About the output pattern, It changes in the flow of "1→2→3 ～ 6→1".
H; High, L; Low, Hi-Z; High impedance

Table 2. Truth Table



2.5 Variable speed operation

About Rotational speed, it changes by PWM terminal input DUTY of the output of the lower side and upper side.
(Upper and lower PWM control drive method Figure 26)

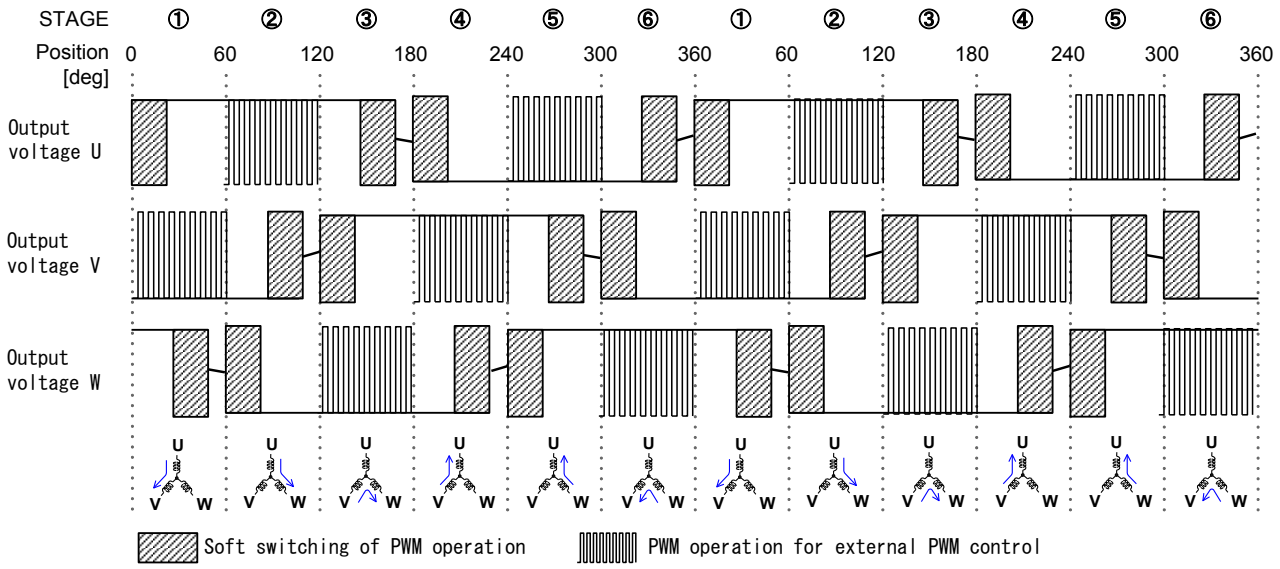
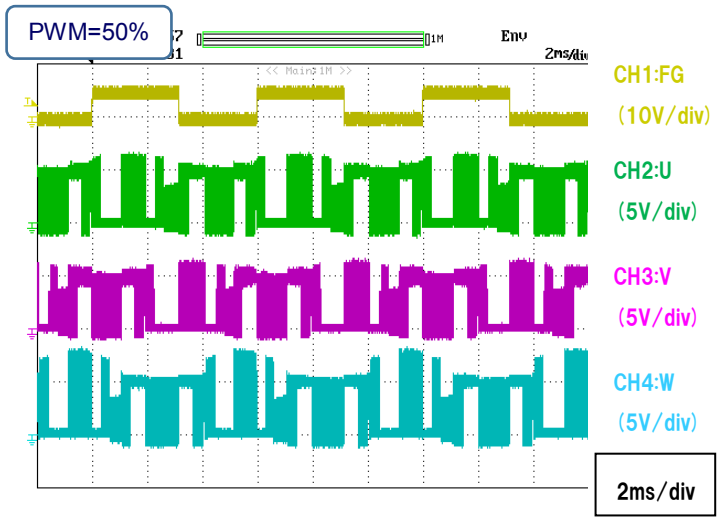


Fig.26 Timing Chart of U, V and W Output (With PWM Control)

Output pattern	Motor output		
	Motor output U	Motor output V	Motor output W
①	H	PWM	Hi-Z
②	PWM	Hi-Z	L
③	Hi-Z	H	PWM
④	L	PWM	Hi-Z
⑤	PWM	Hi-Z	H
⑥	Hi-Z	L	PWM

* About the output pattern, It changes in the flow of "1→2→3 ～ 6→1".
H; High, L; Low, Hi-Z; High impedance

Table 3. Truth Table

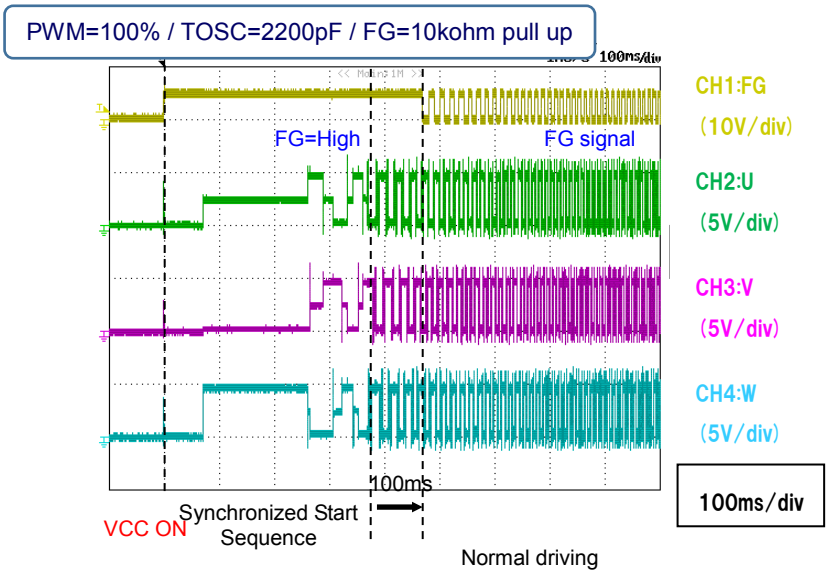


2.6 FG signal mask operation at start-up

FG signal is masked between synchronized start sequence and until 100ms at Normal driving.

	State Transition			
	Start	Synchronized Start (120° drive)	Normal driving (150° drive) Until 100ms	Normal driving After 100ms
FG Output (pull up)	Hi-Z (Hi)	Hi-Z (Hi)	Hi-Z (Hi)	FG signal

Table 4. Truth Table

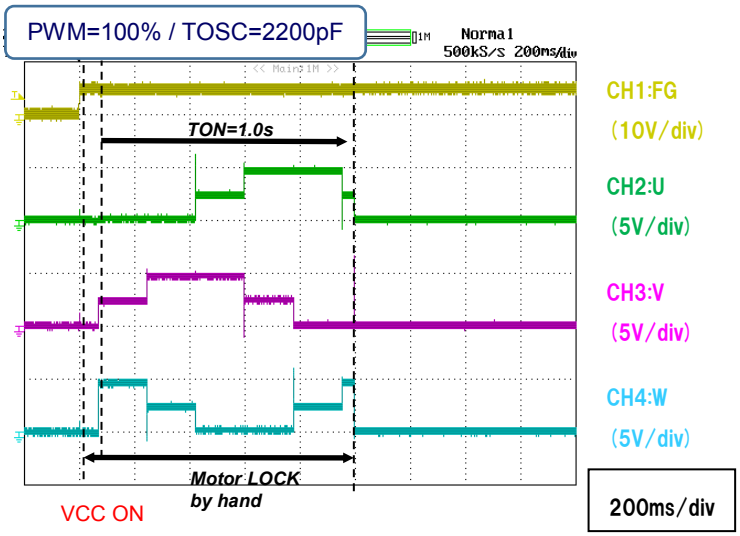


3. Lock Protection Function (Automatic Re-Start)

3.1 At Start-up Lock Detect

To prevent passing a coil current on any phase when a motor is locked, it is provided with a function which can turn OFF the output for a certain period of time and then automatically restore itself to the normal operation. During the motor rotation, an appropriate logic based on the induced electromotive voltage can be continuously given to each phase, on the other hand, when the motor is locked at no induced electromotive voltage is obtained. Utilizing this phenomenon to take a protective against locking, when the induced electromotive voltage is not detected for a predetermined period of time (TON: 1.0s), it is judged that the motor is locked and the output is turned OFF for a predetermined period of time (TOFF: 5.0s).

Moreover, If Synchronized driving doesn't change into rotational speed monitor section between TON (1.0s) at start-up, it is judged that the motor is locked.



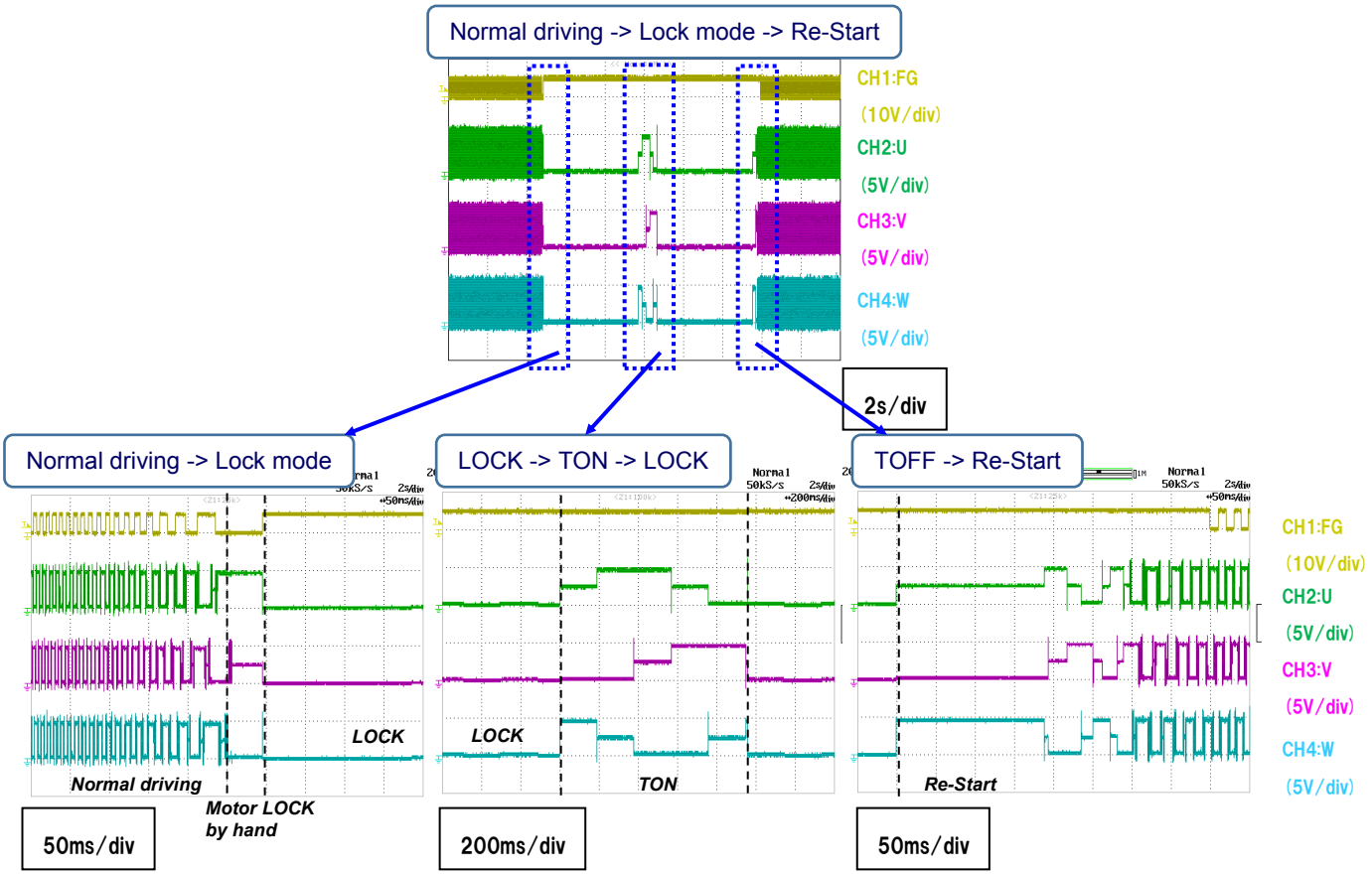
3.2 Normal Drive Lock Detect

When you stop motor in BD67173NUX normal driving, the motor settles to the high rotation speed.
Lock detect judgment of normal driving is set 2patterns (Table.4).

・Max Rotation Judgment: Motor Rotation Speed ≧ 100000rpm(typ.)
・Minimum Rotation Judgment : Motor Rotation speed ≦100rpm(typ.) (or BEMF period ≧TOSC*8000)

	Typ	Worst
Max Rotation Judgement	≧100000rpm	≧60000rpm
Min Rotation Judgment	≦100rpm	≦133rpm

Table 5. Lock Judgment Table



4. Power Saving Function / Speed control by PWM input

The power saving function is controlled by an input logic of the PWM terminal.

4.1 Operate mode when the PWM terminal is High

PWM terminal is OPEN, PWM=100% operating mode, too. (Internal circuit is 360kΩ pull up setting.)

4.2 Standby mode when the PWM terminal is Low for a time period of 1ms (typ.)

Input logic of the PWM terminal is set at Low and then the Standby mode becomes effective 1ms (typ.) (Figure 27). In the Standby mode, the lock protection function is deactivated and the lock protection is not effective. Therefore, this device can start up instantly even from the stop state when the input logic of the PWM terminal is set at High.

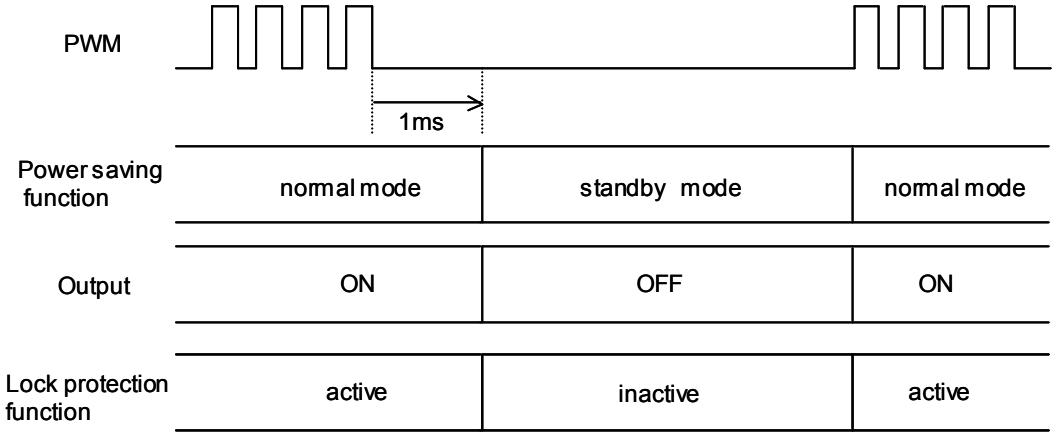


Figure 27. Power Saving Function

5. UVLO Function (Under Voltage Lock Out)

In the operation area under the guaranteed operating power supply voltage of 2.2V (typ.), the transistor on the output can be turned OFF at a power supply voltage of 1.75V (typ.). A hysteresis width of 250mV is provided and a normal operation can be performed at 1.95V (typ.). This function is installed to prevent unpredictable operations, such as a large amount of current passing through the output, by means of intentionally turning OFF the output during an operation at a very low power supply voltage which may cause an abnormal function in the internal circuit.

VCC input	UVLO	Output
0V to Sweep up	1.95V	OFF to ON
5V to Sweep down	1.75V	ON to OFF

Table 6. UVLO Judgment Table

6. Rotation Direction Select Function (FR select)

The FR select is Rotation direction select (Table .5).

FR input	Rotation
High or Open	Forward
Low	Reverse

Table 7. FR Select Table

7. Over Current Limit (Internal Current Detection Resistance)

A current passing through the motor coil can be detected on the internal current detection resistance to prohibit a current flow large than a current limit value. The current limit value is determined by setting of the IC internal limit voltage 0.2V (typ.) and the internal current detection resistance value (0.16Ω) using the following equation.

$$\text{Current limit value (1.25A)} = \frac{\text{Internal limit voltage (0.2V)}}{\text{Internal current detection resistance(0.16}\Omega\text{)}}$$

The current limit is activated at above value.

Power Dissipation

Permissible dissipation (total loss) indicates the power that can be consumed by IC at Ta = 25ºC (normal temperature). IC is heated when it consumes power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, etc, and consumable power is limited. Permissible dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is in general equal to the maximum value in the storage temperature range.

Heat generated by consumed power of IC is radiated from the mold resin or lead frame of package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called heat resistance, represented by the symbol θja [C/W]. The temperature of IC inside the package can be estimated by this heat resistance. Below Figure shows the model of heat resistance of the package.

Heat resistance θja, ambient temperature Ta, junction temperature Tj, and power consumption P can be calculated by the equation below:

$$\theta ja = (Tj - Ta) / P \quad [℃/W]$$

Thermal derating curve indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θja.

Thermal resistance θja depends on chip size, power consumption, package ambient temperature, packaging condition, wind velocity, etc even when the same package is used. Thermal derating curve indicates a reference value measured at a specified condition. Below Figure shows a thermal derating curve. (Value when mounting FR4 glass epoxy board 74.2 [mm] x 74.2 [mm] x 1.6 [mm] (copper foil area below 3 [%]))

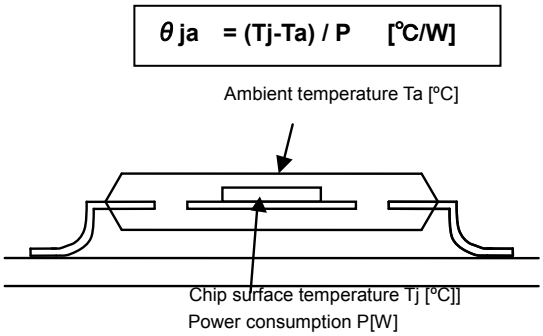
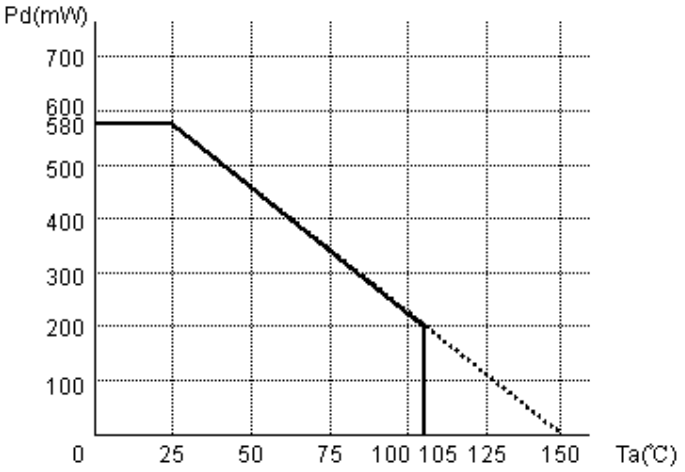


Figure 28. Thermal resistance

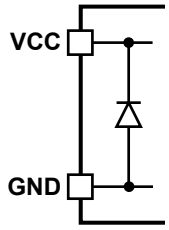


∗1 Above Ta = 25ºC, derating by 4.64 mW/ºC
(When glass epoxy board (single layer) of 74.2 mm x 74.2 mm x 1.6 mm is mounted)

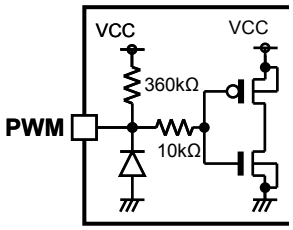
Figure 29. Thermal derating curve

I/O equivalent circuit(s)

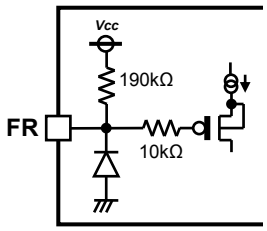
1) Power supply terminal, and ground terminal



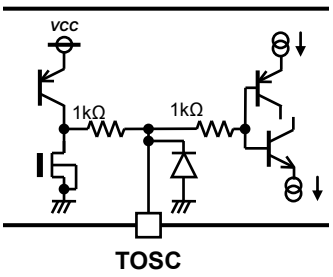
2) Output duty controllable input terminal



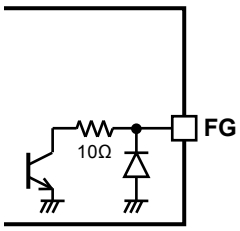
3) Motor rotation direction select input terminal



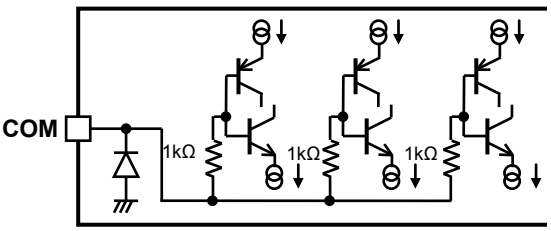
4) Start-up oscillation control terminal



5) Speed pulse signal output terminal



6) Motor coil midpoint input terminal



7) Motor output terminal

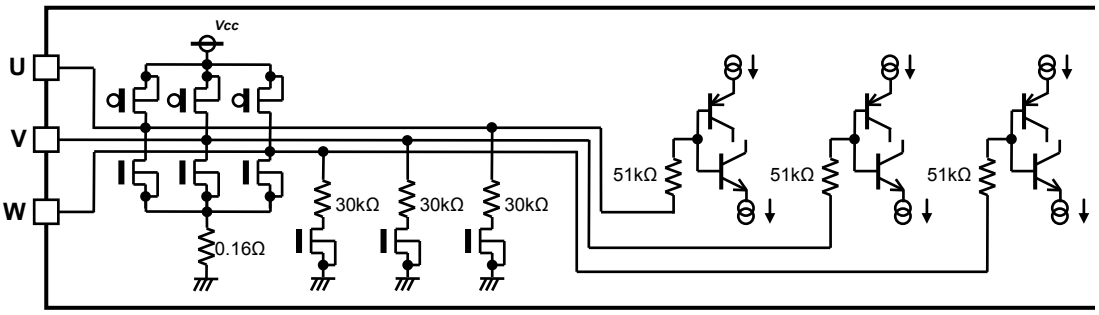


Figure 30. I/O equivalent circuits

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

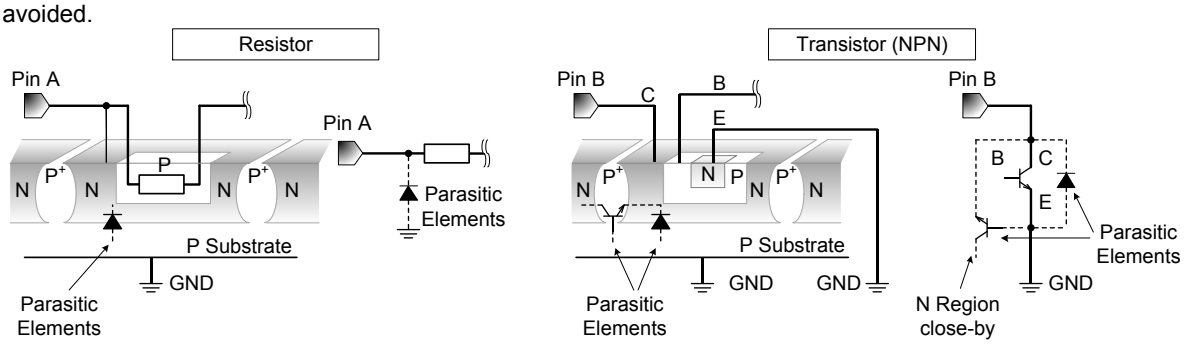


Figure 31. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

Operational Notes – continued

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

16. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.