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DC Brushless Fan Motor Drivers

Multifunction Single-phase Full-wave Fan Motor Driver

BD6995FV

General Description

BD6995FV is a 1chip driver for 12V single-phase full-wave fan motor. This IC employs the Bi-CDMOS process and soft switching drive, low power consumption and quiet drive is provided.

Key Specifications

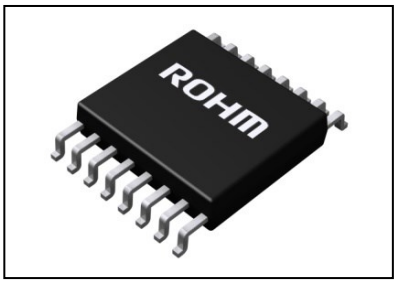
- Input Voltage Range: 4.3V to 17V
- Operating Temperature Range: -40°C to +105°C
- Output Voltage (High and Low Total): 0.6V(Typ) at 0.4A
- Output Current: 1.2A(Max)

Features

- SSOP Small Package
- PWM Soft switching Drive
- Standby Function
- Speed Controllable by DC Input
- Quick Start
- OSC Select Function (Triangle OSC or Saw OSC)
- Signal Select Function (Rotation Speed Pulse Signal: FG or Lock Alarm Signal: AL)
- Signal Output
- Lock Protection and Automatic Restart (Without External Capacitor)
- Current Limit

Package

	W(Typ) x D(Typ) x H(Max)
SSOP-B16	5.00mm x 6.40mm x 1.35mm

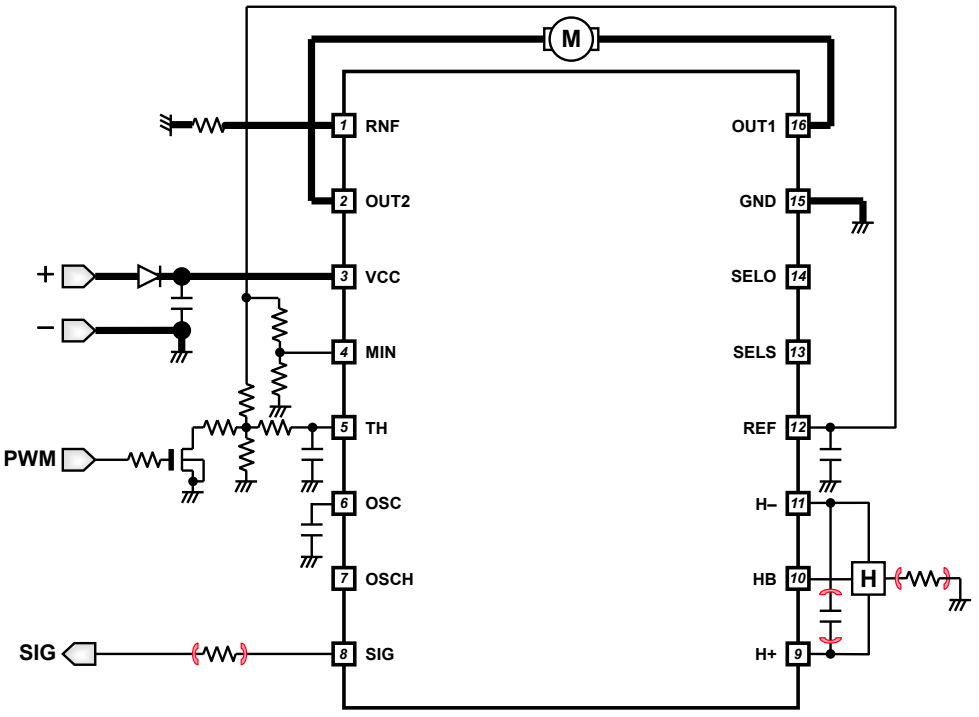


SSOP-B16

Applications

- Fan motors for general consumer equipment like Desktop PC, Projector, etc.

Typical Application Circuit



○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

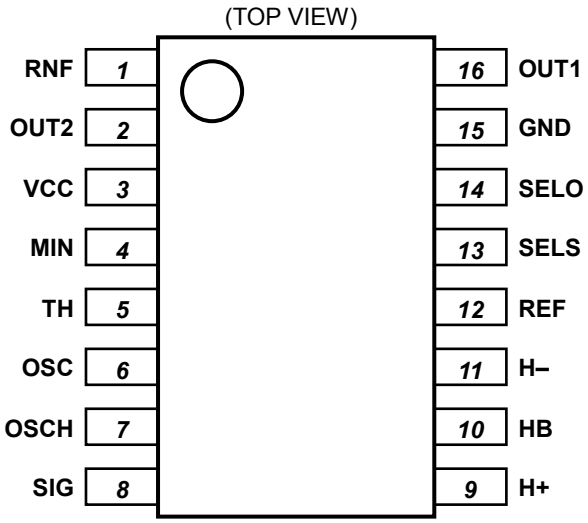


Figure 1. Pin Configuration

Pin Description

P/No.	P/Name	Function
1	RNF	Output current detecting resistor connection terminal (motor ground)
2	OUT2	Motor output 2 terminal
3	VCC	Power supply terminal
4	MIN	Minimum output duty setting terminal
5	TH	Output duty control input terminal
6	OSC	Oscillating capacitor connection terminal
7	OSCH	Resistor connection terminal for capacitor charge (use only for Saw OSC)
8	SIG	Signal output terminal (Rotation speed pulse signal: FG or Lock alarm signal: AL)
9	H+	Hall + input terminal
10	HB	Hall bias terminal
11	H–	Hall – input terminal
12	REF	Reference voltage output terminal
13	SELS	Signal select terminal (Rotation speed pulse signal: FG or Lock alarm signal: AL)
14	SELO	OSC select terminal (Triangle OSC or Saw OSC)
15	GND	Ground terminal
16	OUT1	Motor output 1 terminal

Block Diagram

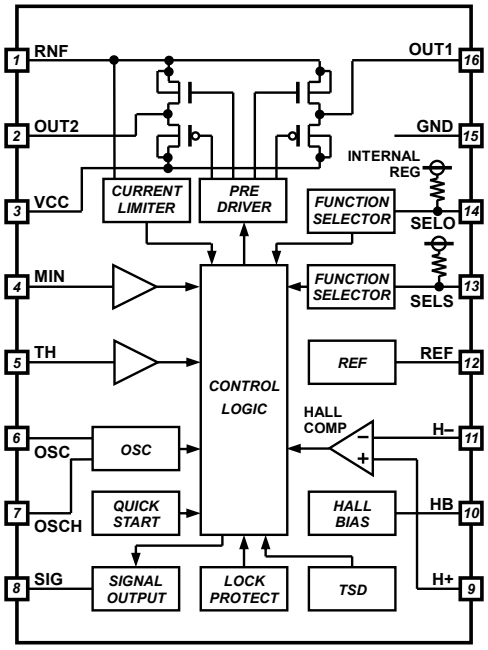


Figure 2. Block Diagram

I/O Truth Table

Hall Input		Driver Output		
H+	H–	OUT1	OUT2	SIG(FG)
H	L	L	H	Hi-Z
L	H	H	L	L

H; High, L; Low, Hi-Z; High impedance
SIG output is open-drain type.

Motor State	OUT1/2	SIG(FG)	SIG(AL)
Rotating	-	-	L
Locking	-	-	Hi-Z
Standby	Hi-Z	Hi-Z	L

L; Low, Hi-Z; High impedance
SIG output is open-drain type.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	20	V
Power Dissipation	Pd	0.88 *(Note 1)*	W
Operating Temperature Range	Topr	-40 to +105	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Output Voltage	V_O	20	V
Output Current	I_O	1.2 *(Note 2)*	A
Signal Output Voltage	V_{SIG}	20	V
Signal Output Current	I_{SIG}	10	mA
Reference Voltage(REF) Output Current	I_{REF}	5	mA
Hall Bias(HB) Output Current 1	I_{HB1}	10 *(Note 3)*	mA
Hall Bias(HB) Output Current 2	I_{HB2}	5 *(Note 4)*	mA
Input Voltage(H+, H–, TH, MIN, SELO, SELS)	V_{IN}	7	V
Junction Temperature	Tj	150	°C

(Note 1) Derate by 7.1mW/°C if operating over Ta=25°C.
(Note 2) Do not exceed Pd.
(Note 3) Ta=0°C or Higher.
(Note 4) Less than Ta=0°C.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)	Unit
		1s*(Note 3)*	
SSOP-B16			
Junction to Ambient	θ_{JA}	140.9	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	6	°C/W

(Note 1) Based on JESD51-2A(Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}	4.3	12	17	V
Input Voltage Range 1 (H+, H–) (V_{CC}≥9V)	V_{IN1}	0	-	3.0	V
Input Voltage Range 1 (H+, H–) (V_{CC}<9V)		0	-	V_{CC}/3	V
Input Voltage Range 2 (TH, MIN)	V_{IN2}	0	-	V_{REF}	V
Input Frequency Range (H+, H–)	f_{IN}	0	-	400	Hz
OSC Frequency Range	f_{OSCR}	18	-	50	kHz

(Note) Recommended motor: Single phase fan motor of 4 poles

Electrical Characteristics (Unless otherwise specified V_{CC}=12V Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit Current	I_{CC}	-	5.0	9.0	mA	
Circuit Current (Stand-by)	I_{STBY}		3.0	4.8	mA	
Hall Bias Voltage	V_{HB}	1.05	1.25	1.45	V	I_{HB}=-2mA
Output Voltage	V_O	-	0.6	0.9	V	I_O=±400mA, High and Low total
Lock Detection ON Time	t_{ON}	0.3	0.5	0.7	s	
Lock Detection OFF Time	t_{OFF}	3.0	5.0	7.0	s	
Lock Detection OFF/ON Ratio	R_{LCK}	8.5	10.0	11.5	-	$R_{LCK}=t_{OFF}$ / t_{ON}
Hall Input Hysteresis Voltage	V_{HYS}	±6	±12	±18	mV	
SIG Output Low Voltage	V_{SIGL}	-	0.2	0.3	V	I_{SIG}=5mA
SIG Output Leak Current	I_{SIGL}	-	-	10	μA	V_{SIG}=17V
OSC Frequency (Reference Data)	f_{OSC}	-	28	-	kHz	SELO=H(OPEN), C_{OSC}=100pF *(Note1)*
OSC Charge Current	I_{COSC}	-16	-11	-6	μA	V_{OSC}=2.0V
OSC Discharge Current	I_{DOSC}	6	11	16	μA	V_{OSC}=2.0V
OSC High Voltage	V_{OSCH}	2.80	3.00	3.20	V	
OSC Low Voltage	V_{OSCL}	0.85	1.05	1.25	V	
Output ON Duty	D_{OH}	38	48	58	%	V_{TH}=0.4 x V_{REF} Output 1kΩ Load SELO=H(OPEN) C_{OSC}=100pF *(Note1)*
Reference Voltage	V_{REF}	4.7	5.0	5.3	V	I_{REF}=-2mA
MIN Input Bias Current	I_{MIN}	-0.6	-	-	μA	V_{MIN}=0V
TH Input Bias Current	I_{TH}	-0.6	-	-	μA	V_{TH}=0V
SELS Input Open Voltage	V_{SELSO}	3.2	3.5	3.8	V	
SELS Input Low Level	V_{SELSL}	-0.2	-	0.7	V	
SELS Input Bias Current	I_{SELS}	-35	-25	-15	μA	V_{SELS}=0V
SELO Input Open Voltage	V_{SELOO}	3.2	3.5	3.8	V	
SELO Input Low Level	V_{SELOL}	-0.2	-	0.7	V	
SELO Input Bias Current	I_{SELO}	-35	-25	-15	μA	V_{SELO}=0V
Current Limit Voltage	V_{CL}	235	265	295	mV	

(Note1) 100pF includes parasitic capacitance of substrate and other.
For parameters involving current, positive notation means inflow of current to IC while negative notation means outflow of current from IC.
The reference data is a design guaranteed value and the numerical all shipment inspection off the subject item.

Typical Performance Curves (Reference data)

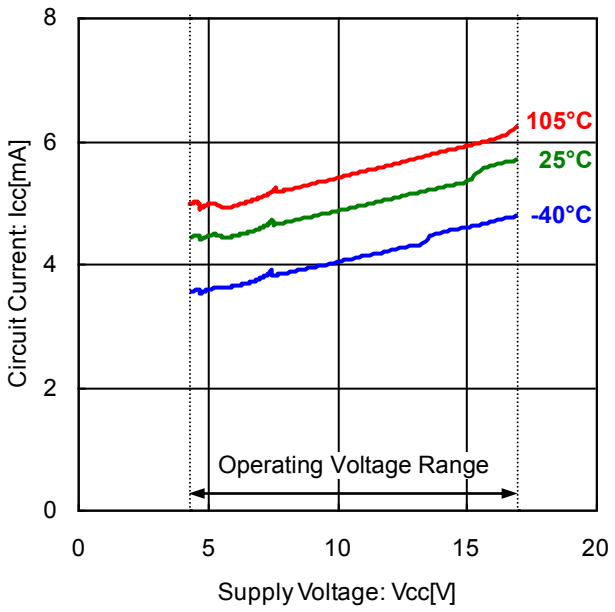


Figure 3. Circuit Current vs Supply Voltage (In Operation)

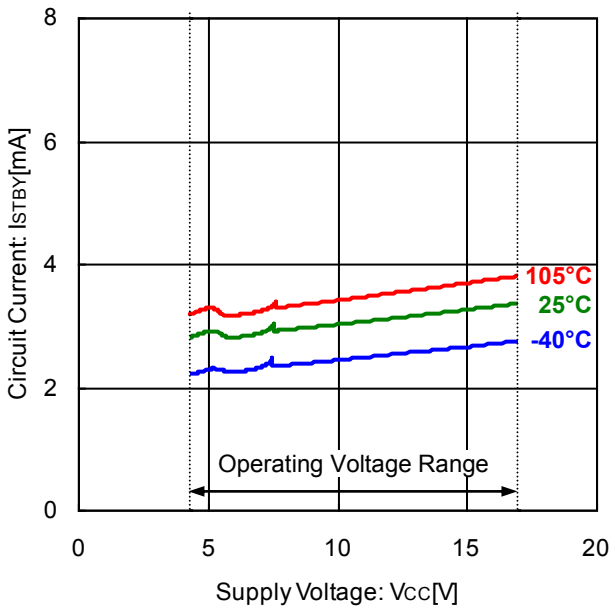


Figure 4. Circuit Current vs Supply Voltage (In Standby)

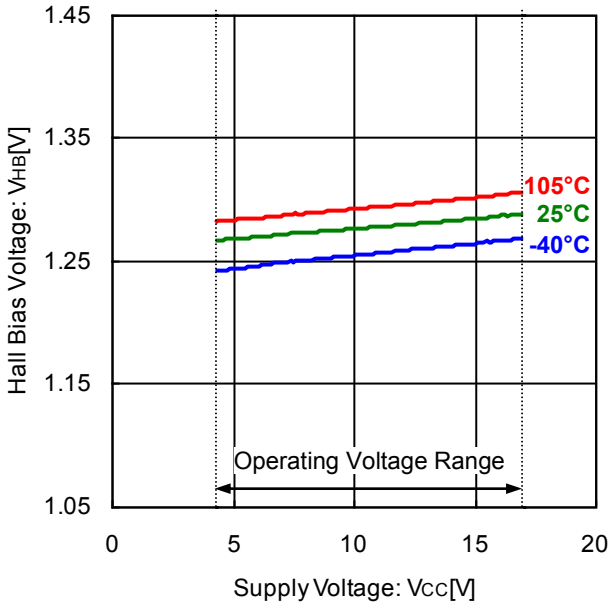


Figure 5. Hall Bias Voltage vs Supply Voltage (I_{HB}=-2mA)

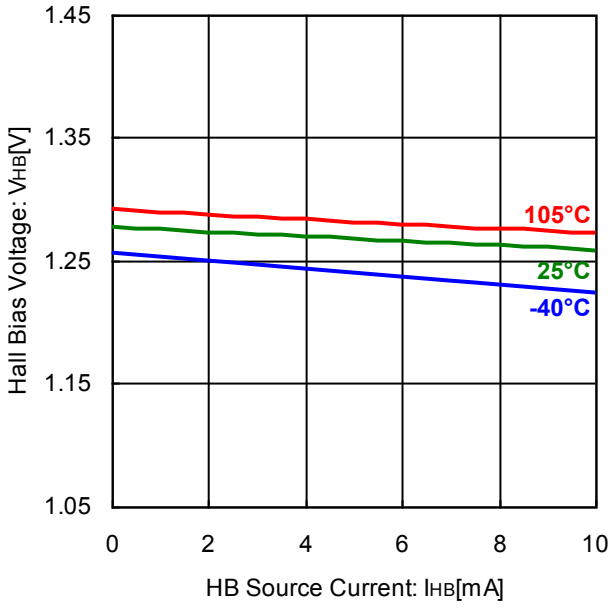


Figure 6. Hall Bias Voltage vs HB Source Current (V_{CC}=12V)

Typical Performance Curves (Reference data) - continued

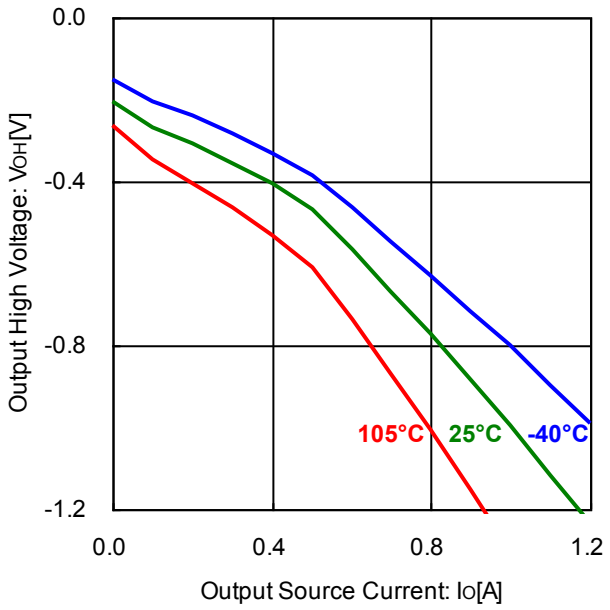


Figure 7. Output High Voltage vs Output Source Current (VCC=12V)

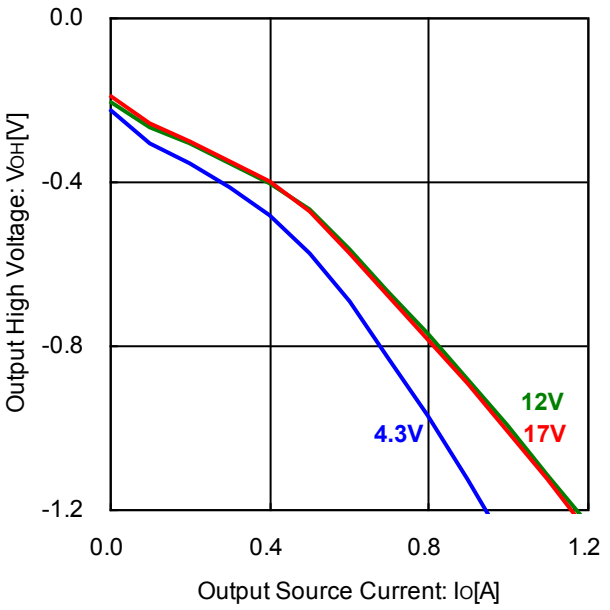


Figure 8. Output High Voltage vs Output Source Current (Ta=25°C)

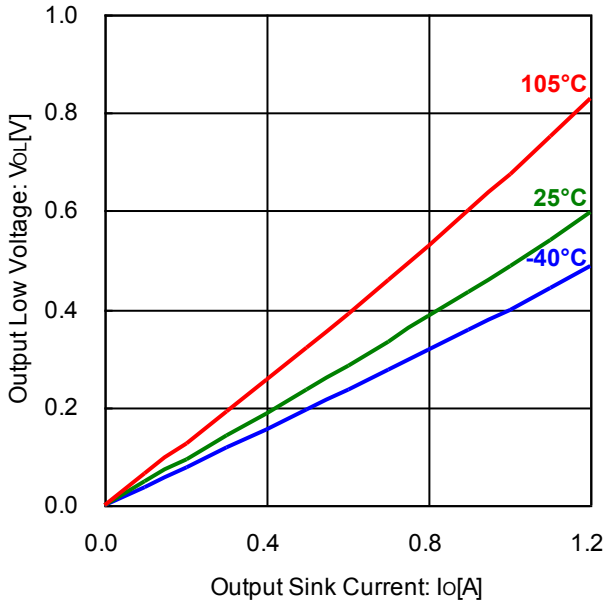


Figure 9. Output Low Voltage vs Output Sink Current (VCC=12V)

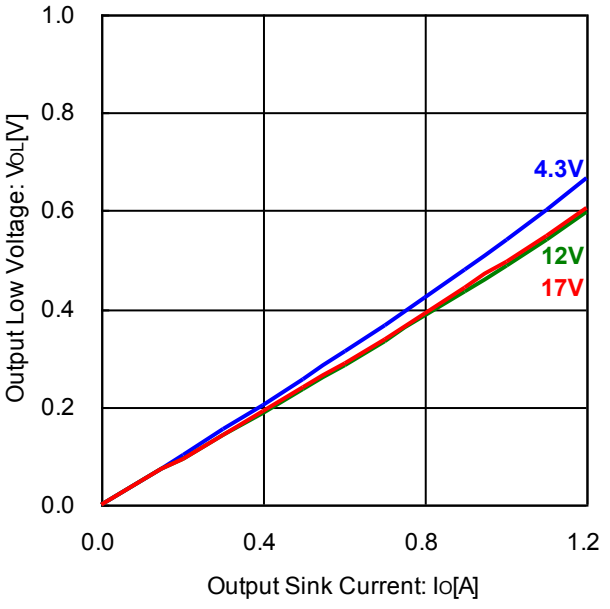


Figure 10. Output Low Voltage vs Output Sink Current (Ta=25°C)

Typical Performance Curves (Reference data) - continued

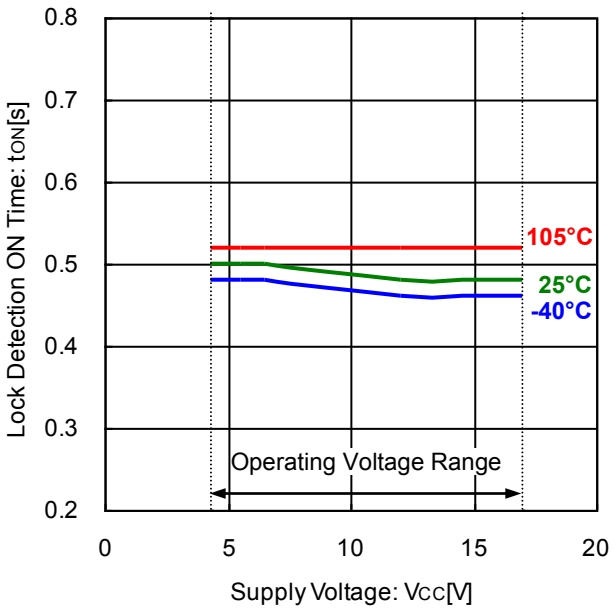


Figure 11. Lock Detection ON Time vs Supply Voltage

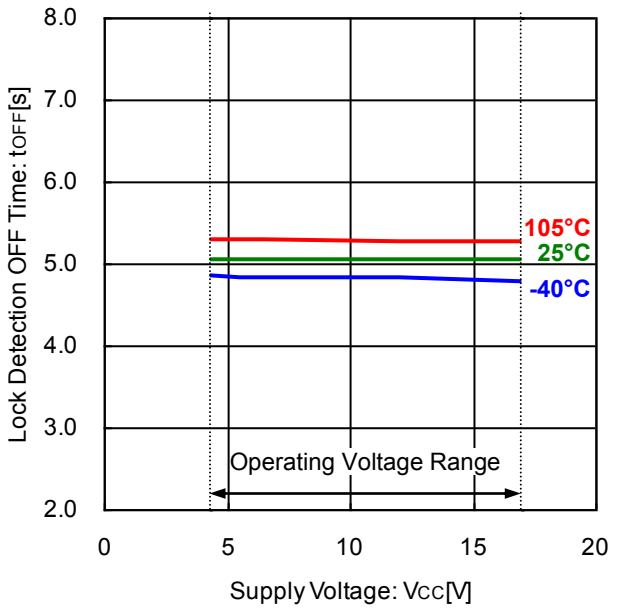


Figure 12. Lock Detection OFF Time vs Supply Voltage

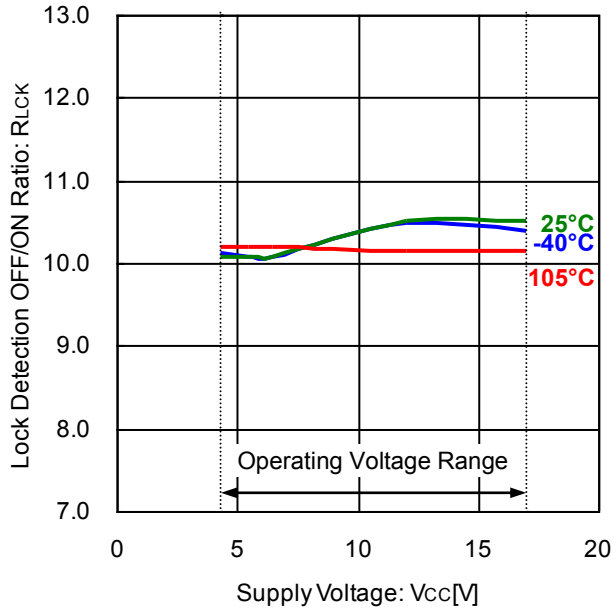


Figure 13. Lock Detection OFF/ON Ratio vs Supply Voltage

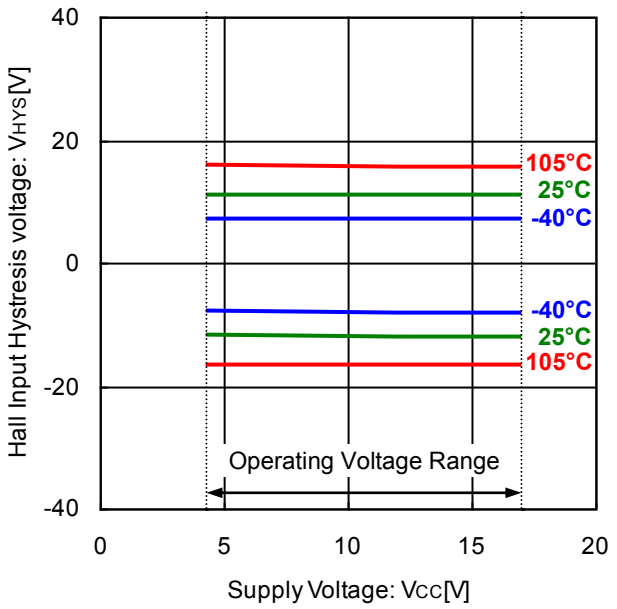


Figure 14. Hall Input Hysteresis Voltage vs Supply Voltage

Typical Performance Curves (Reference data) - continued

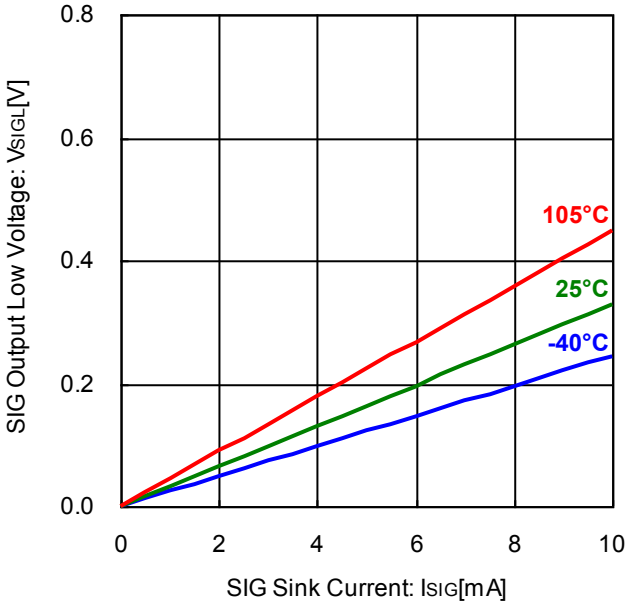


Figure 15. SIG Output Low Voltage vs SIG Sink Current (VCC=12V)

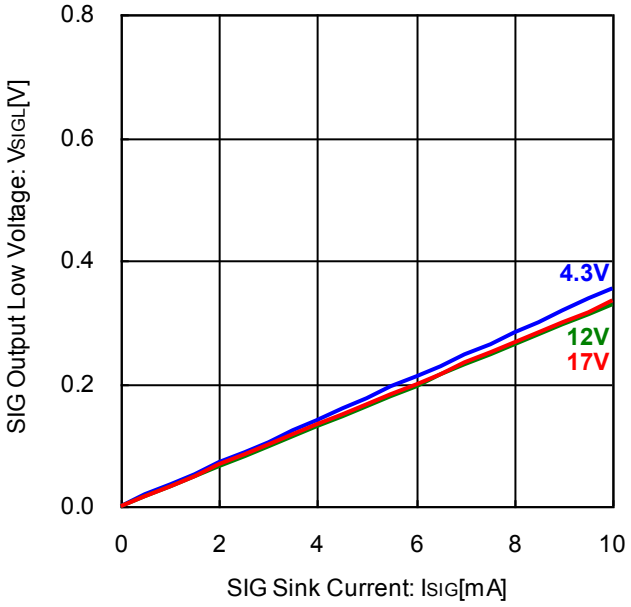


Figure 16. SIG Output Low Voltage vs SIG Sink Current (Ta=25°C)

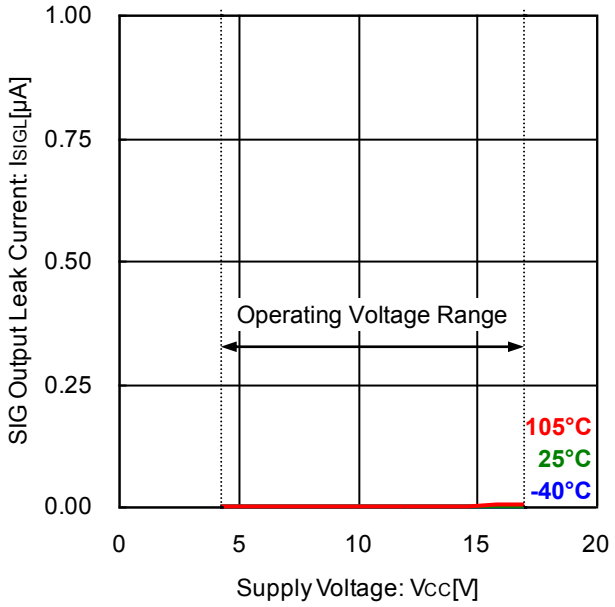


Figure 17. SIG Output Leak Current vs Supply Voltage (V_{SIG}=17V)

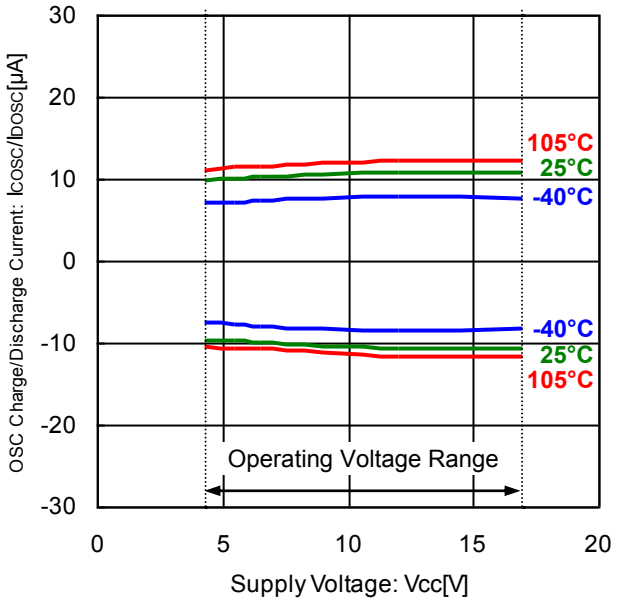


Figure 18. OSC Charge/Discharge Current vs Supply Voltage

Typical Performance Curves (Reference data) - continued

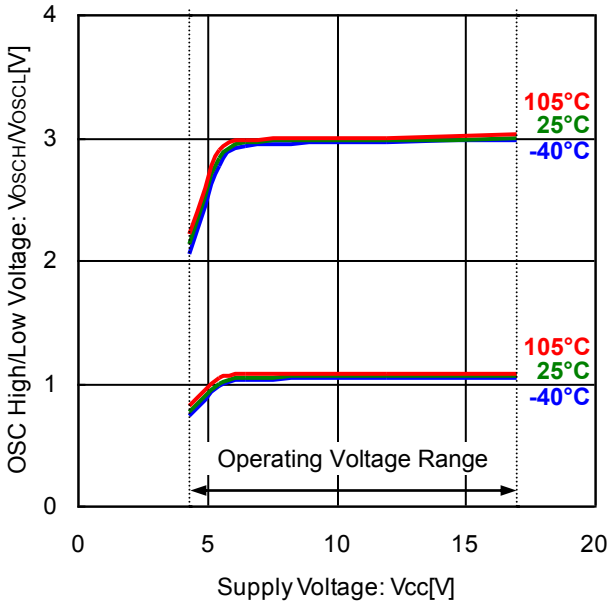


Figure 19. OSC High/Low Voltage vs Supply Voltage

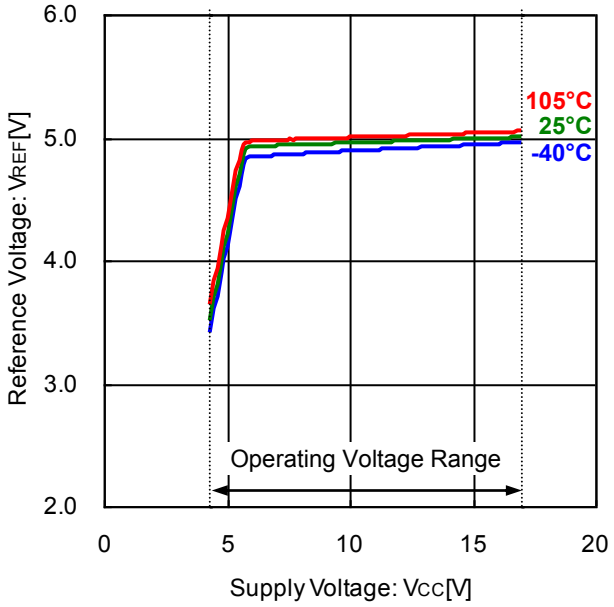


Figure 20. Reference Voltage vs Supply Voltage
(I_{REF}=-2mA)

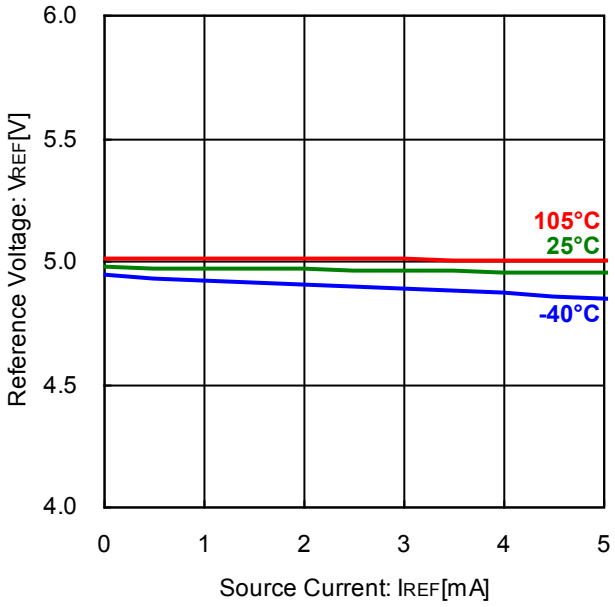


Figure 21. Reference Voltage vs Source Current
(V_{CC}=12V)

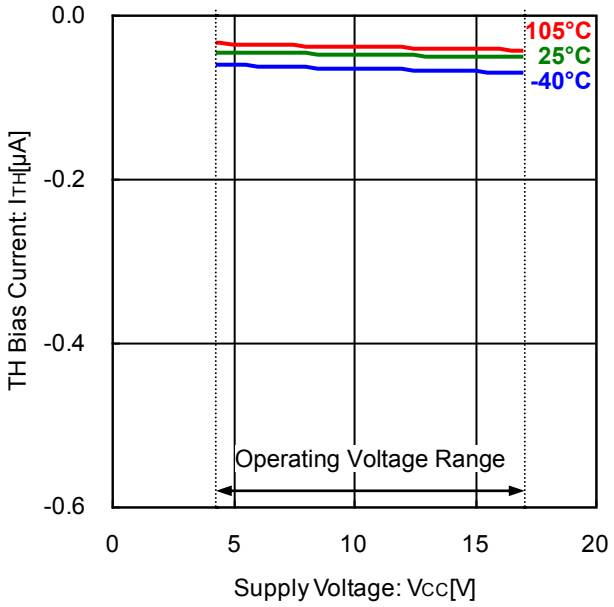


Figure 22. TH Bias Current vs Supply Voltage
(V_{TH}=0V)

Typical Performance Curves (Reference data) - continued

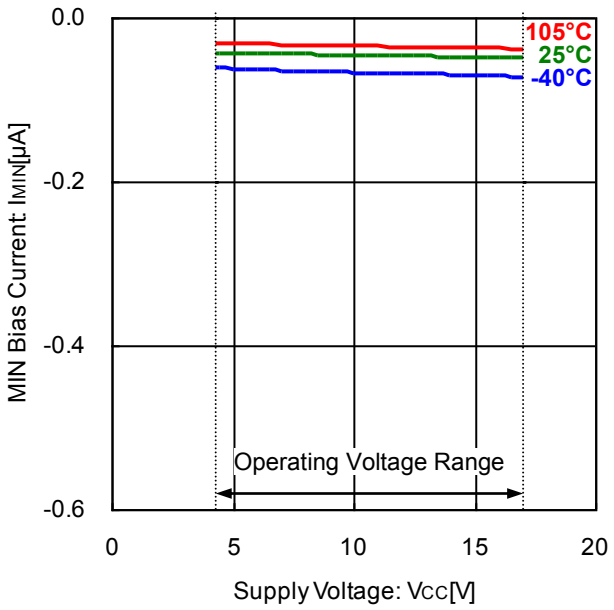


Figure 23. MIN Bias Current vs Supply Voltage (V_{MIN}=0V)

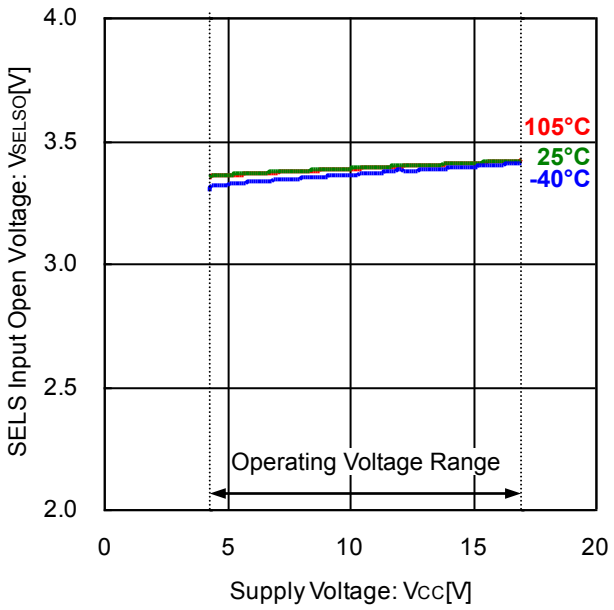


Figure 24. SELS Input Open Voltage vs Supply Voltage

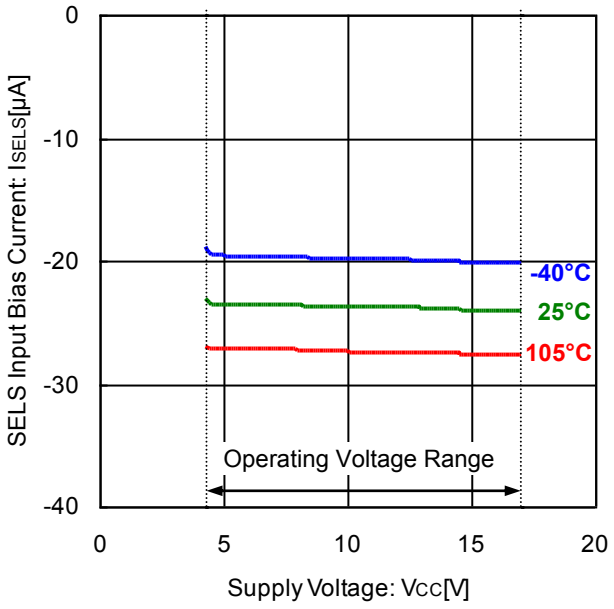


Figure 25. SELS Input Bias Current vs Supply Voltage (V_{SELS}=0V)

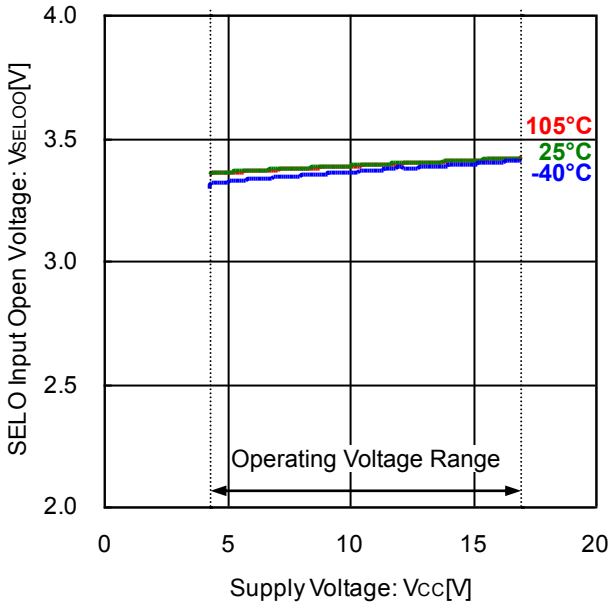


Figure 26. SELO Input Open Voltage vs Supply Voltage

Typical Performance Curves (Reference data) - continued

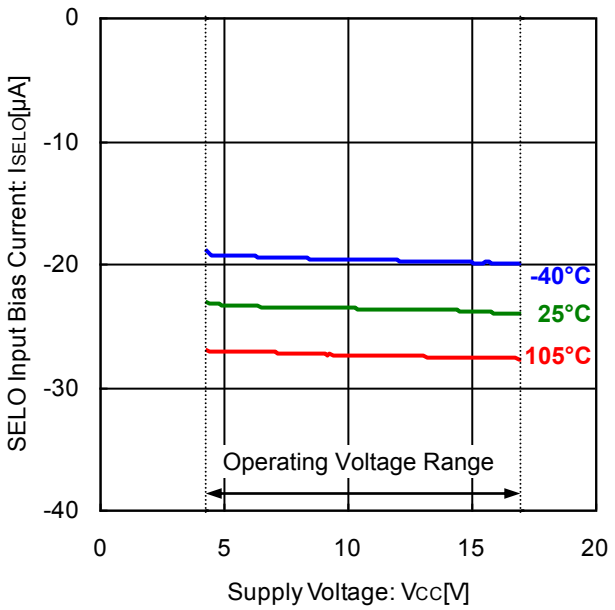


Figure 27. SELO Input Bias Current vs Supply Voltage (V_{SELO}=0V)

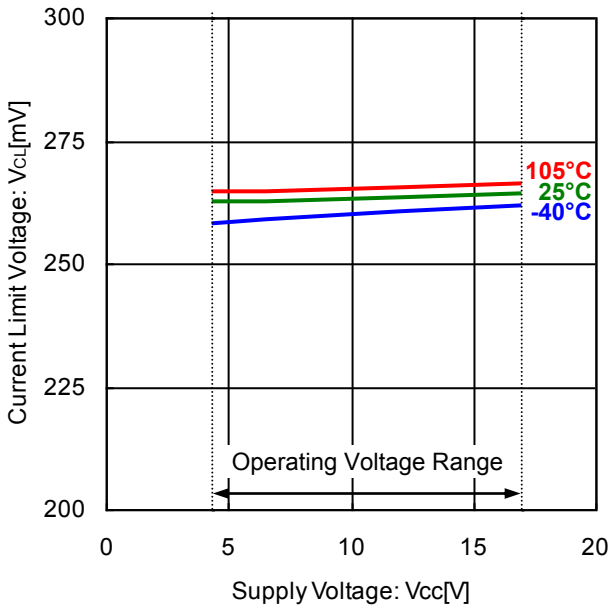


Figure 28. Current Limit Voltage vs Supply Voltage

Application Example (Constant Values are for Reference)

1. Triangle OSC Application
   Triangle OSC for controlling the speed is generated using the OSC circuit in the IC. Triangle OSC is compared with the external PWM signal converted into the DC voltage, and controlling the rotational speed.

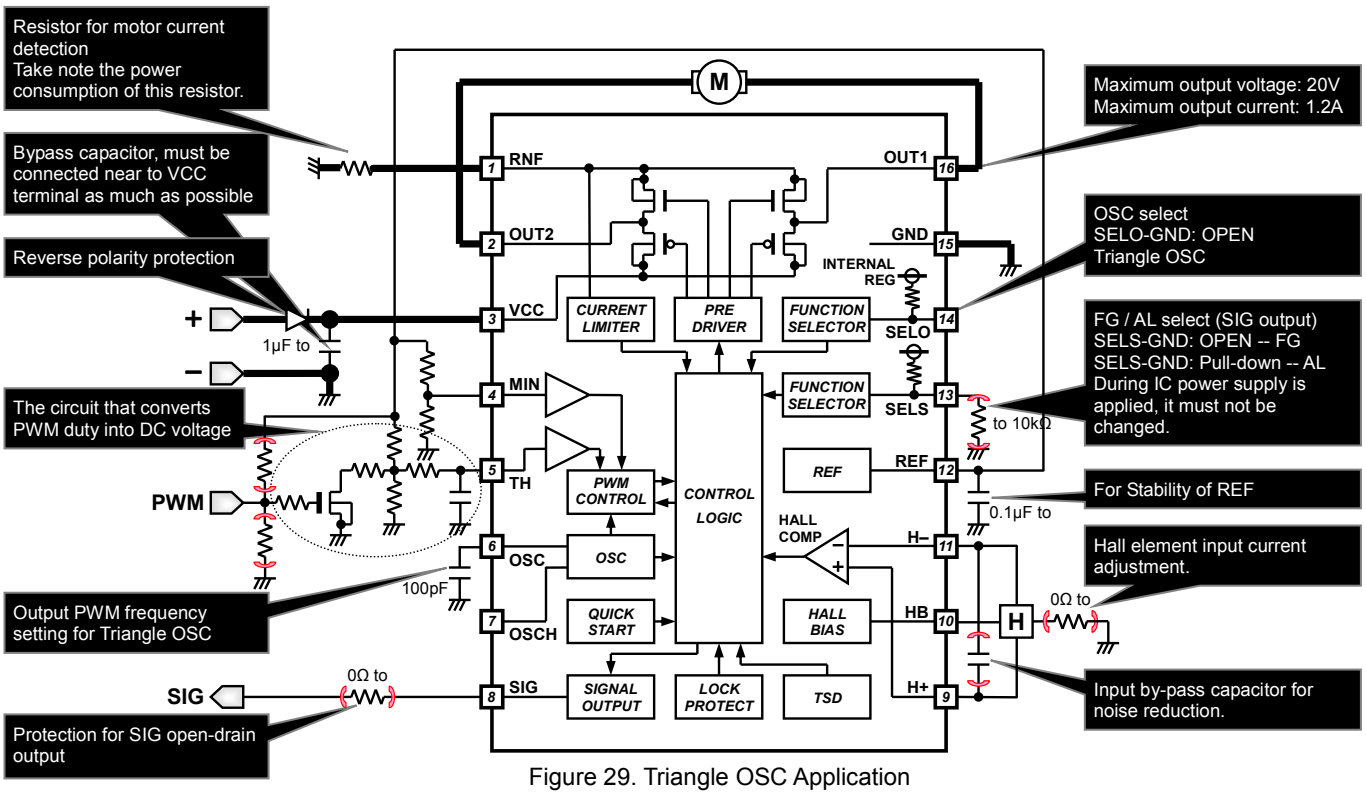


Figure 29. Triangle OSC Application

2. Saw OSC Application
   Saw OSC for controlling the speed is generated using an external capacitor and resistor. Saw OSC is compared with the external PWM signal converted into the DC voltage, and controlling the rotational speed.

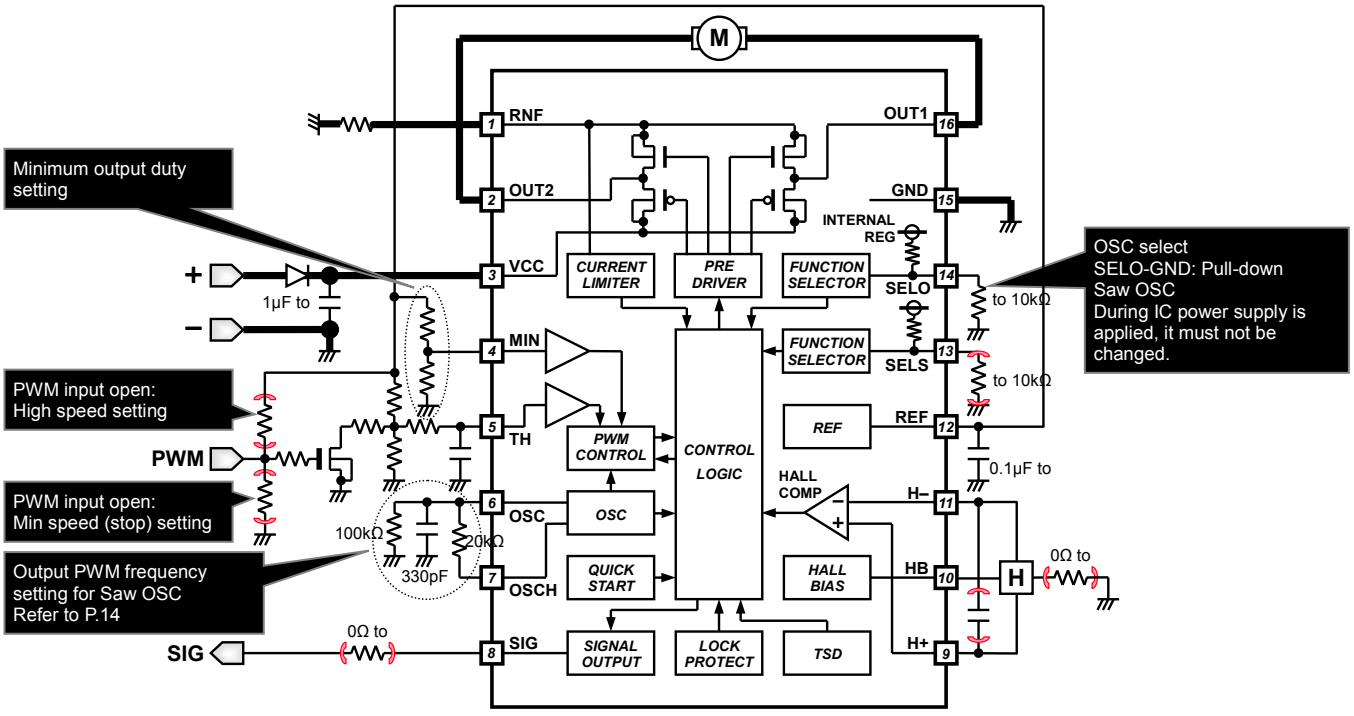


Figure 30. Saw OSC application

Substrate Design Note

1. IC power, Motor outputs, and Motor ground lines should be made as wide as possible.

2. When the absolute maximum rated voltage may be exceeded due to voltage rise by back electromotive force, place capacitor or zener diode between VCC and GND. If necessary, add both.
   The bypass capacitor and/or zener diode must be connected near to VCC terminal as much as possible.

3. H+ and H- lines are arranged side by side and connected from the hall element to the IC as short as possible, because it is easy for noise to affect the hall lines.

Functional Descriptions

1. Variable speed operation
   The rotational speed is changed by PWM duty on the motor outputs (OUT1, OUT2 terminals).

   (1) PWM Operation by DC input
   As shown in Figure 32, to change the motor output PWM duty, a DC voltage input from TH terminal is compared with triangle (saw) wave produced by internal OSC circuit. MIN terminal is used to set the minimum PWM duty. The PWM duty is determined by the lower voltage between the TH voltage and the MIN voltage.

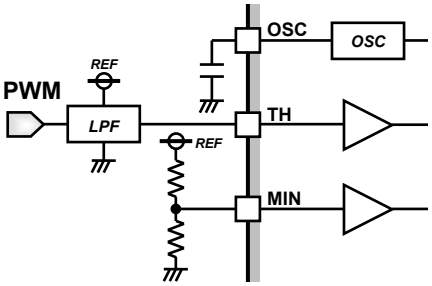


Figure 31. DC input application

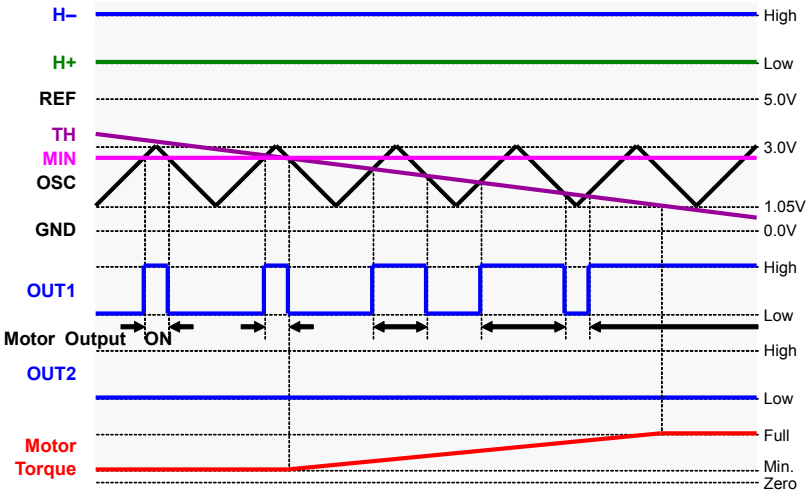


Figure 32. DC Input Operation Timing Chart

Dividing resistor of REF generates OSC high level (Typ.3.0V) and OSC low level (Typ.1.05V) voltage, and the ratio of those voltages is designed to be hard to fluctuate. For an application that requires strict precision, determine a value with sufficient margin after taking full consideration of external constants.
(Note) In BD6995FV, the speed control with the direct PWM input is impossible.

(2) Setting of TH and MIN Terminals
The voltage of the TH terminal or MIN terminal becomes irregular when it is open. Please apply voltages to both terminals when turning on IC power supply.

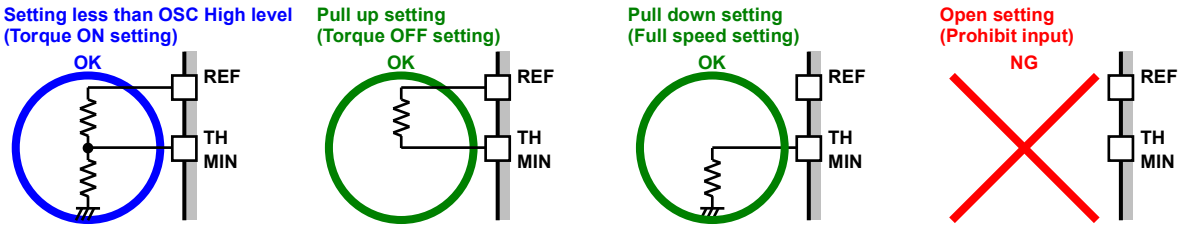


Figure 33. Setting of the Variable Speed Function

(3)-1 Output Oscillatory Frequency Setting (Triangle OSC: SELO=H or OPEN, OSCH=OPEN)

Frequency (fosc) in which the motor outputs are operated PWM by DC voltage input is set according to capacity value (Cosc) of the capacitor connected with OSC terminal.

$f_{OSC} = |I_{DOSC} \times I_{COSC}| / (C_{OSC} \times (|I_{DOSC}| + |I_{COSC}|) \times (V_{OSCH} - V_{OSCL}))$ [Hz]

f_{OSC}: OSC frequency [Hz]
C_{OSC}: Capacitance between OSC and GND [F]
I_{DOSC}: OSC discharge current [A] (Typ: 11μA)
I_{COSC}: OSC charge current [A] (Typ: -11μA)
V_{OSCH}: OSC high voltage [V] (Typ: 3.0V)
V_{OSCL}: OSC low voltage [V] (Typ: 1.05V)

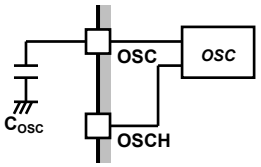


Figure 34. Triangle OSC Application

(Example.) The frequency when motor output PWM operates becomes about 28.2 kHz when assuming that Cosc is 100pF.

$f_{OSC} = |11\mu \times -11\mu| / (100p \times (|11\mu| + |-11\mu|) \times (3.0 - 1.05)) = 28.2$ [kHz]

When this application is used in a wide temperature range, fluctuation range of the frequency becomes large by individual difference and temperature characteristics of the IC. For an application that requires quiet, determine a value with sufficient margin that frequency becomes outside of audible range. When the triangle OSC is used, please set OSCH terminal open.

(3)-2 Output Oscillatory Frequency Setting (Saw OSC: SELO=L)

Frequency (fosc) in which the motor outputs are operated PWM by DC voltage input is set according to R1 and R2 and C_{OSC}.

$T_{RISE} = - \{R_H \times R2 \times C / (R_H + R2)\} \times \ln \{(V_{OSCH} - (R2 \times V_{REF}) / (R_H + R2)) / (V_{OSCL} - (R2 \times V_{REF}) / (R_H + R2))\}$ [s]
$R_H = R1 + R_{OSCH}$ [Ω]
$T_{FALL} = - R2 \times C \times \ln (V_{OSCL} / V_{OSCH})$ [s]
$f_{OSC} = 1 / (T_{RISE} + T_{FALL})$ [Hz]

R_{OSCH}: Internal resistor (Typ: 5kΩ)
T_{RISE}: OSC rise time [s]
T_{FALL}: OSC fall time [s]
f_{OSC}: OSC frequency [Hz]
C_{OSC}: Capacitance between OSC and GND [F]
V_{REF}: REF voltage [V] (Typ: 5.0V)
V_{OSCH}: OSC high voltage [V] (Typ: 3.0V)
V_{OSCL}: OSC low voltage [V] (Typ: 1.05V)

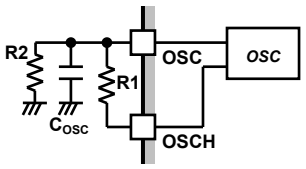


Figure 35. Saw OSC Application

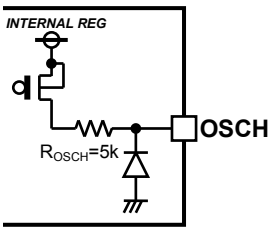


Figure 36. OSCH Circuit

(Example.) The frequency when motor output PWM operates becomes about 23.9 kHz when assuming that R_{OSCH} is 5kΩ and R1 is 20kΩ, R2=100kΩ and C_{OSC} is 330pF.

$T_{RISE} = - \{25k \times 100k \times 330p / (25k + 100k)\} \times \ln \{(3 - (100k \times 5) / (25k+100k)) / (1.05 - (100k \times 5) / (25k+100k))\}$
$= 7.14$ [μs]
$T_{FALL} = - 100k \times 330p \times \ln (1.05 / 3)$
$= 34.64$ [μs]
$f_{OSC} = 1 / (7.14\mu + 34.64\mu)$
$= 23.9$ [kHz]

When this application is comprised of external parts of good temperature characteristics, there is less frequency fluctuation compared to triangle OSC. When the frequency fluctuation needs to be suppressed, saw OSC is recommended.

2. Lock Protection and Automatic Restart
Motor rotation is detected by hall signal and the IC internal counter set lock detection ON time (t_{ON}) and OFF time (t_{OFF}). Timing chart is shown in Figure 37. The soft switching of OUT1 and OUT2 is not included in this timing chart.

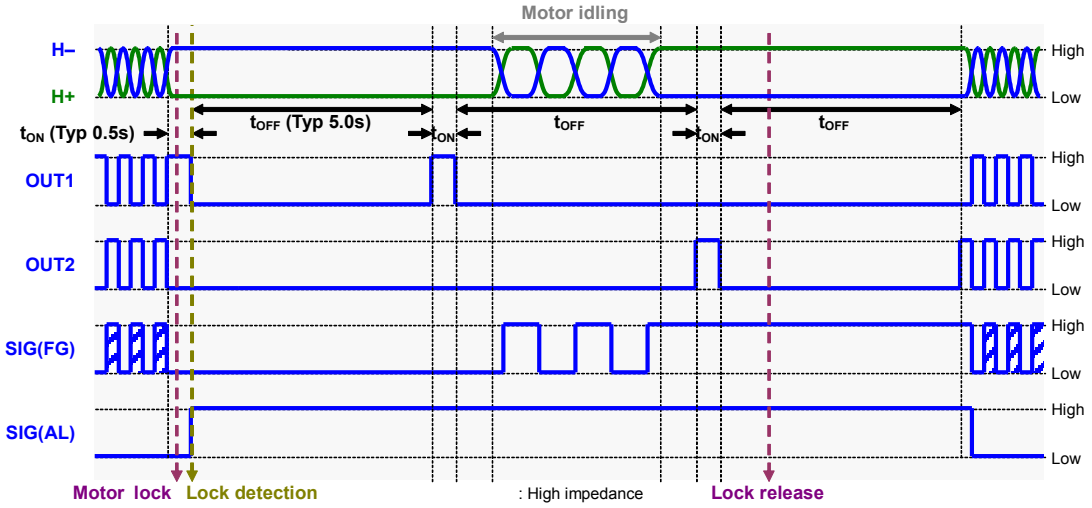


Figure 37. Timing chart of Lock Protection

3. Quick Start and Standby
When the motor stopped by torque OFF voltage (V_{TH}>V_{OSCH}) restarts by torque ON voltage (V_{TH}<V_{OSCH}), the motor is not affected by the lock protection function. The motor can restart immediately anytime.
In the case of minimum PWM duty OFF setting (V_{MIN}>V_{OSCH}), this function is enable.

(1) When torque OFF voltage is input during motor rotation:
The lock protection function is disabled. Restart failure is prevented.

(2) When torque OFF voltage is input during motor rotation and 0.5 second (Typ) passed from the last hall input signal change:
IC goes to standby mode. (Lock protection function remains disabled.)
In standby mode, OUT1 and OUT2 and SIG (FG) become Hi-Z logic and SIG (AL) becomes L logic.
When torque ON voltage is inputted at the standby mode, the motor can restart (AL logic is L).
Timing chart is shown in Figure 38.

(3) When torque OFF voltage is input during lock protection:
Since 0.5 second (Typ) passed from the last hall input signal change, IC goes to standby mode immediately.
(Note)
When torque OFF voltage is input in a timing same as lock protection, IC goes to standby mode immediately.
Because OUT1 and OUT2 become Hi-Z logic, when coil current is left, current returns to power supply. When the above mentioned timing is assumed, please take measures of item2 of safety measures or please increase the value of the filter of TH terminal in an application circuit. (More than 20kΩ, 1μF)

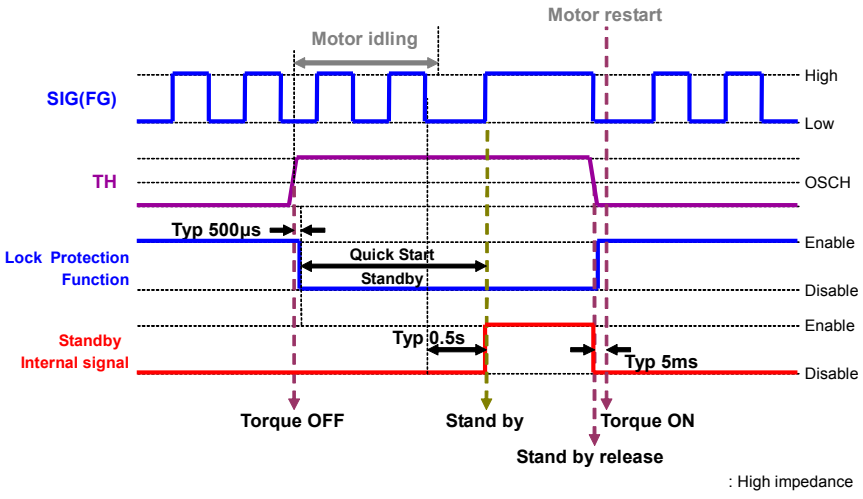


Figure 38. Timing chart of Quick start and Standby

4. Hall Input Setting

(1) Hall Input Setting

Hall input voltage range is shown in operating conditions. The input voltage of a hall comparator is input in "hall input voltage range" including signal amplitude. The input current to Hall element can be adjusted with R1 resistor.

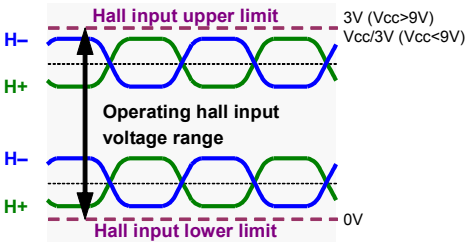


Figure 39. Hall Input Voltage Range

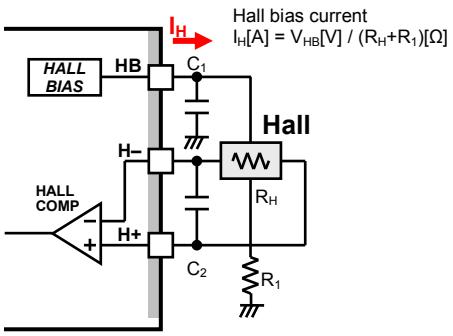


Figure 40. Hall input application

(2) Reducing the Noise of Hall Signal

VCC noise or the like depending on the wiring pattern of board may affect Hall element. In this case, place a capacitor C_1 as shown Figure 40. In addition, when wiring from the hall element output to IC hall input is long, noise may be loaded on wiring. In this case, insert a capacitor C_2.

5. Current Limit

The current limit circuit turns off the upper side output, when the current that flows to the motor coil is detected exceeding a set value. The current limit value is controlled by internal setting voltage (Typ: 265mV) and current sense resistor. In Figure 41, I_O is the current flowing to the motor coil, R_{NF} is the resistance detecting the current, and P_{RMAX} is the power consumption of RNF.

$$I_O[A] = V_{CL}[V] / R_{NF}[\Omega]$$
$$= 265[mV] / 0.33[\Omega]$$
$$= 0.803[A]$$

$$P_{RMAX}[W] = V_{CL}[V] \times I_O[A]$$
$$= 265[mV] \times 0.803[A]$$
$$= 0.213[W]$$

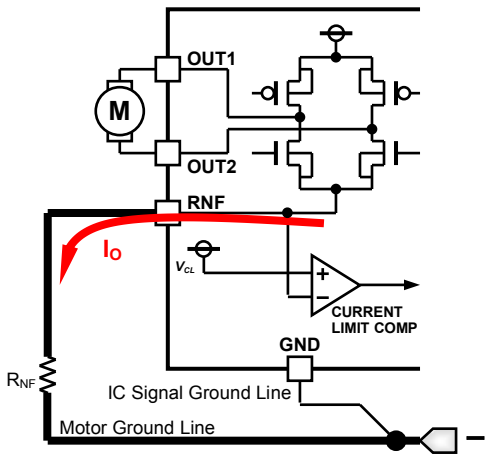


Figure 41. Setting of current limit and ground lines

6. Soft Switching Period and Recirculating Period
BD6995FV has the soft switching period (Note1) and the recirculating period (Note2). The width of each period is set as follows. The soft switching period is approximately 28 degrees (5 steps). The recirculating period is approximately 11 degrees. Timing chart is shown in Figure 42.
(Note1) The soft switching period is the period when a duty of the output changes to a target duty from 0% or 0% from a target duty.
(Note2) The recirculating period is the period when coil current recirculates before phase switching of output.

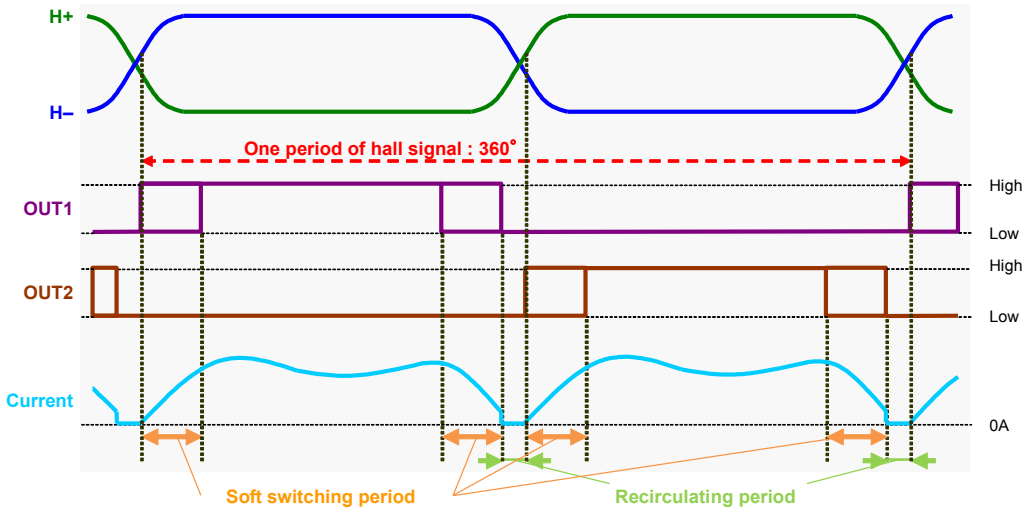
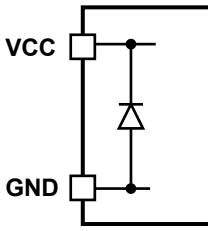


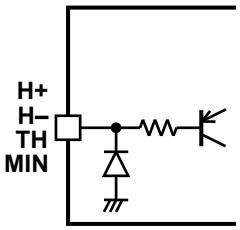
Figure 42. Timing Chart of Soft switching period and Recirculating period

I/O Equivalence Circuit (Resistance Values are Typical)

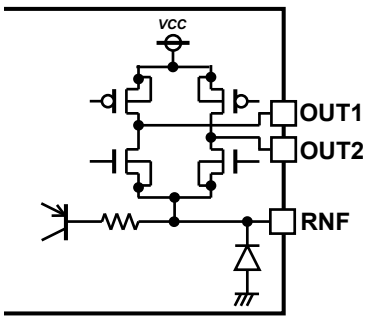
1. Power supply terminal, Ground terminal



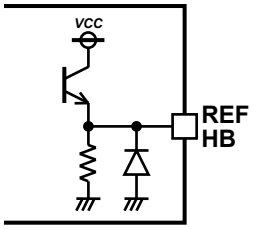
2. Hall+, Hall- terminals, TH, MIN terminals



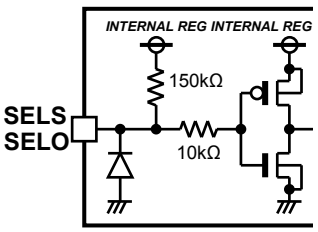
3. OUT1, OUT2 terminals, RNF terminal



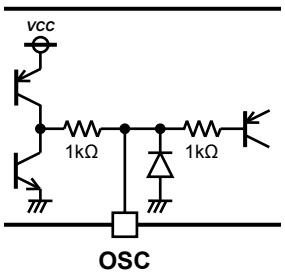
4. REF terminal HB terminal



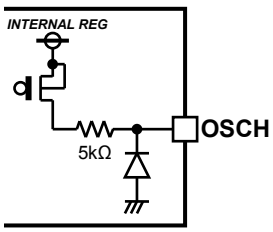
5. SELS, SELO terminals



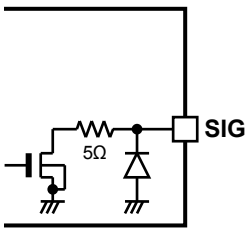
6. OSC terminal



7. OSCH terminal



8. SIG terminal



Safety Measure

1. Reverse Connection Protection Diode
Reverse connection of power results in IC destruction as shown in Figure 43. When reverse connection is possible, reverse connection protection diode must be added between power supply and VCC.

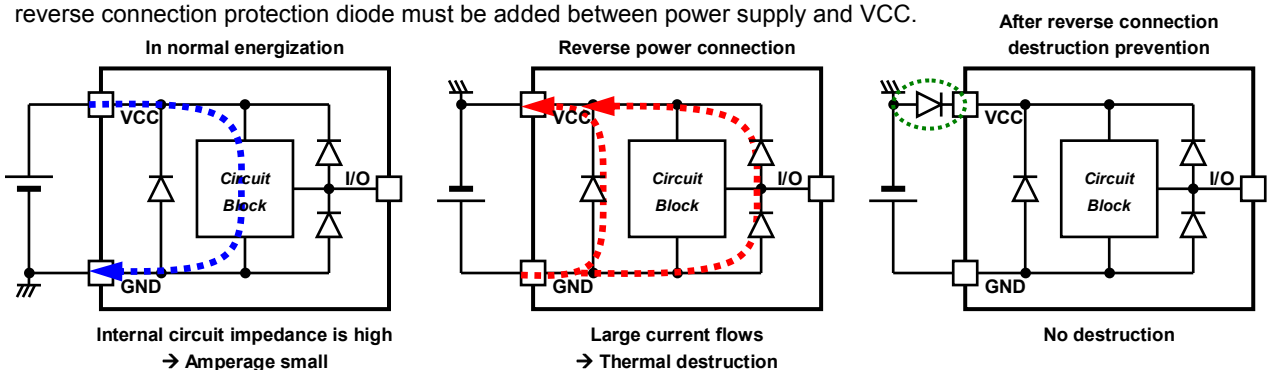


Figure 43. Flow of Current When Power is Connected Reversely

2. Measure against V_{CC} Voltage Rise by Back Electromotive Force
Back electromotive force (Back EMF) generates regenerative current to power supply. However, when reverse connection protection diode is connected, V_{CC} voltage rises because the diode prevents current flow to power supply.

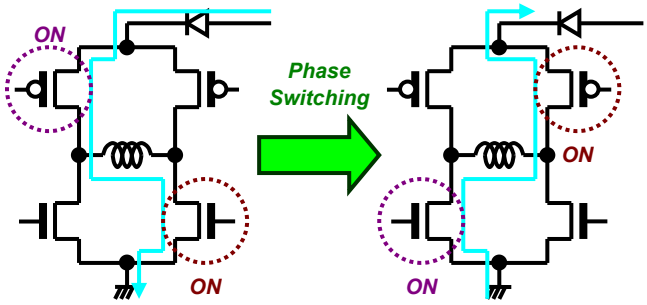


Figure 44. V_{CC} Voltage Rise by Back Electromotive Force

When the absolute maximum rated voltage may be exceeded due to voltage rise by back electromotive force, place (A) Capacitor or (B) Zener diode between VCC and GND. If necessary, add both (C).

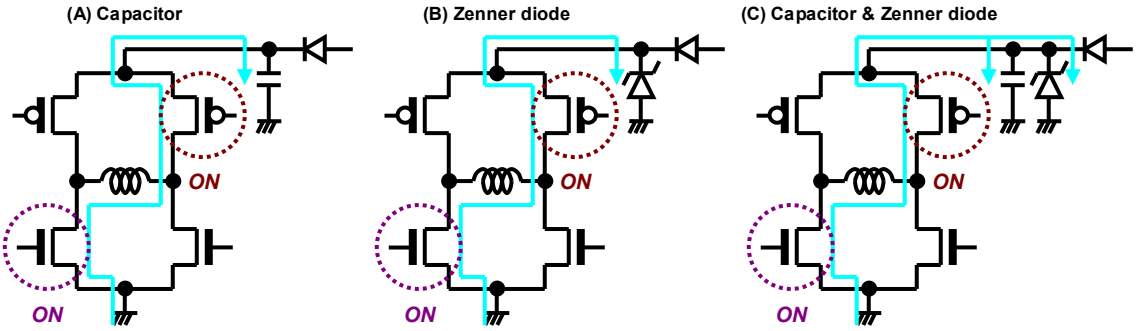


Figure 45. Measure against Vcc and Motor Driving Outputs Voltage

3. Problem of GND line PWM Switching
Do not perform PWM switching of GND line because GND terminal potential cannot be kept to a minimum.

4. Protection of SIG Open-Drain Output
SIG output is an open drain and requires pull-up resistor. Adding resistor can protect the IC. When SIG terminal is directly connected to power supply, it will exceed the absolute maximum rating that could damage the IC.

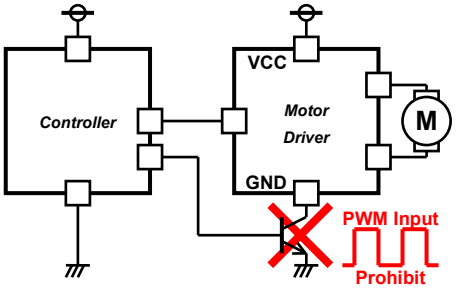


Figure 46. GND Line PWM Switching Prohibited

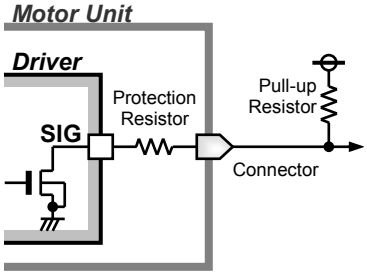


Figure 47. Protection of SIG Terminal

Power Consumption

1. Current Pathway

The current pathways that is related to heat generation of driver IC are the following, and shown in Figure 48.

(1) Circuit Current (I_{CC})
(2) Motor Driving Current (I_M)
(3) Reference Current (I_{REF})
(4) Hall Bias Current (I_{HB})
(5) SIG Output Sink Current (I_{SIG})
(6) Coil Current at the time of Phase Change (I_{CH})
(It is added only when coil current is left at the time of phase change like Figure 49.)

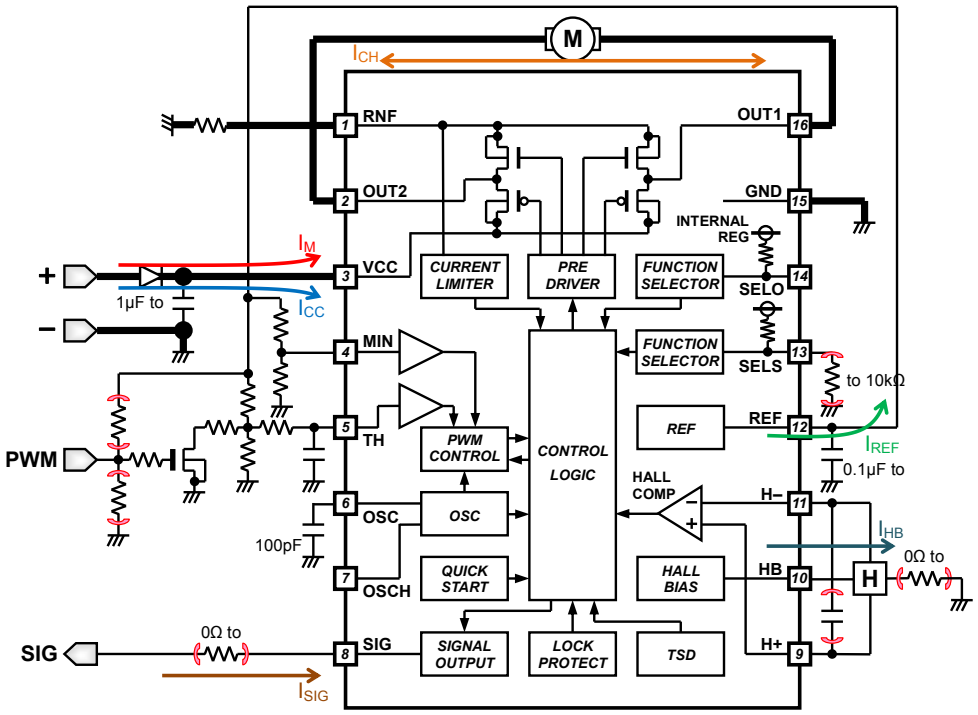


Figure 48. Current Pathway

2. Calculation of Power Consumption

(1) Circuit Current (I_{CC})
$P_{W1} = V_{CC} \times I_{CC}$ [W]

(2) Motor Driving Current (I_M)
$P_{W2} = ((V_{OH}+V_{OL}) \times I_M)$ [W]

where:
V_{OH} is the output high voltage [V]
V_{OL} is the output low voltage [V]
I_M is the motor driving average current [A]

(3) Reference Current (I_{REF})
$P_{W3} = (V_{CC} - V_{REF}) \times I_{REF}$ [W]

(4) Hall Bias Current (I_{HB})
$P_{W4} = (V_{CC} - V_{HB}) \times I_{HB}$ [W]

(5) SIG Output Sink Current (I_{SIG})
$P_{W5} = V_{SIG} \times I_{SIG}$ [W]

(6) Coil Current at the time of Phase Change (I_{CH})
$P_{W6} = V_{CC} \times I_{CH} \times 1/2 \times T1/T$ [W]

where:
I_{CH} is the coil current at the time of phase change [A]

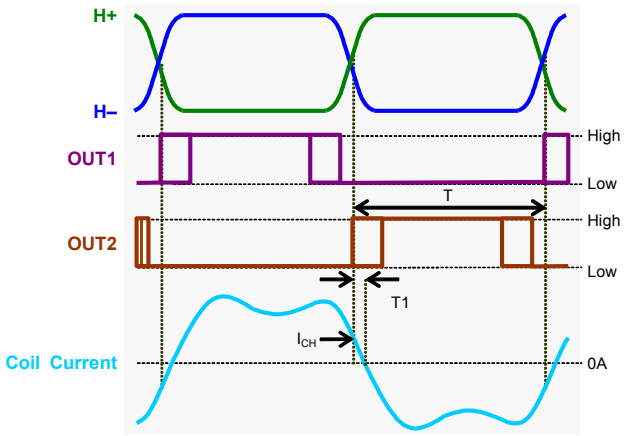


Figure 49. Waveform example
(When coil current is left at the time of phase change)

Total power consumption of driver IC becomes the following by the above (1) to (6).
$P_{W(ttl)} = P_{W1} + P_{W2} + P_{W3} + P_{W4} + P_{W5} + (P_{W6})$ [W]

Refer to next page to calculate the chip surface temperature (Tj) from the power consumption value.

Power Dissipation

1. Power Dissipation

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25°C (normal temperature). IC is heated when it consumes power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be allowed by IC chip into the package is the absolute maximum rating of the junction temperature, and depends on circuit configuration, manufacturing process, etc. Power dissipation is determined by this maximum junction temperature, the thermal resistance in the state of the substrate mounting, and the ambient temperature. Therefore, when the power dissipation exceeds the absolute maximum rating, the operating temperature range is not a guarantee. The maximum junction temperature is in general equal to the maximum value in the storage temperature range.

2. Thermal Resistance

Heat generated by consumed power of IC is radiated from the mold resin or lead frame of package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance. In the state of the substrate mounting, thermal resistance from the chip junction to the ambient is shown in θ_{JA} [°C/W], and thermal characterization parameter from junction to the top center of the outside surface of the component package is shown in Ψ_{JT} [°C/W]. Thermal resistance is classified into the package part and the substrate part, and thermal resistance in the package part depends on the composition materials such as the mold resins and the lead frames. On the other hand, thermal resistance in the substrate part depends on the substrate heat dissipation capability of the material, the size, and the copper foil area etc. Therefore, thermal resistance can be decreased by the heat radiation measures like installing a heat sink etc. in the mounting substrate.
The thermal resistance model is shown in Figure 50, and Equation is shown below.

$\theta_{JA} = (Tj - Ta) / P$ [ºC/W]
$\Psi_{JT} = (Tj - Tt) / P$ [ºC/W]

where:
θ_{JA} is the thermal resistance from junction to ambient [ºC/W]
Ψ_{JT} is the thermal characterization parameter from junction to the top center of the outside surface of the component package [ºC/W]
Tj is the junction temperature [ºC]
Ta is the ambient temperature [ºC]
Tt is the package outside surface (top center) temperature [ºC]
P is the power consumption [W]

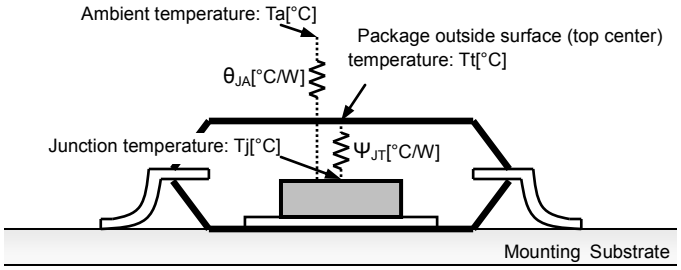


Figure 50. Thermal Resistance Model of Surface Mount

Even if it uses the same package, θ_{JA} and Ψ_{JT} are changed depending on the chip size, power consumption, and the measurement environments of the ambient temperature, the mounting condition, and the wind velocity, etc.

3. Thermal De-rating Curve

Thermal de-rating curve indicates power that can be consumed by the IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature (25°C), and becomes 0W at the maximum junction temperature (150°C). The inclination is reduced by the reciprocal of thermal resistance θja. The thermal de-rating curve under a condition of thermal resistance (P.3) is shown in Figure 51.

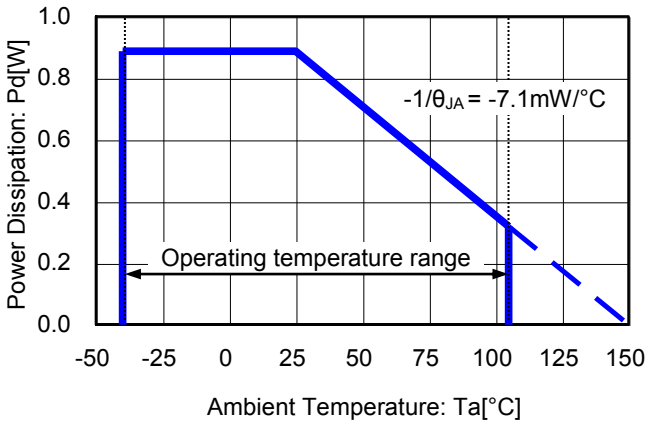


Figure 51. Power Dissipation vs Ambient Temperature

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

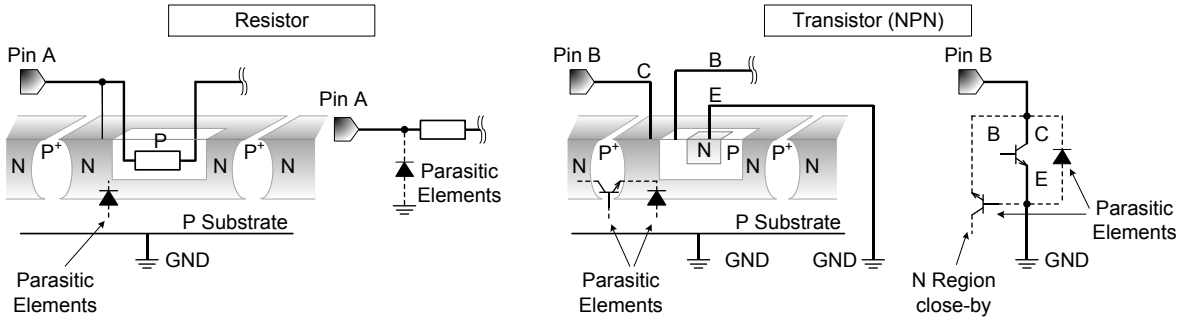


Figure 52. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

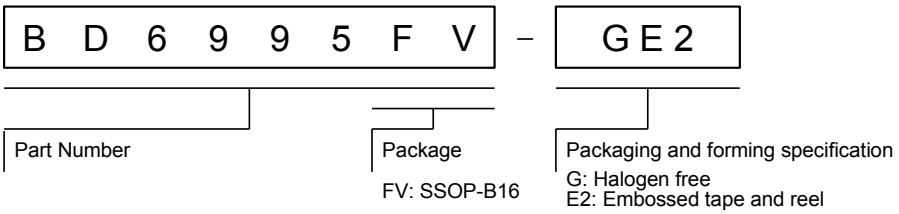
14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

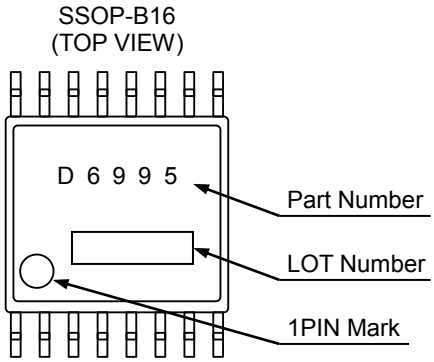
15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

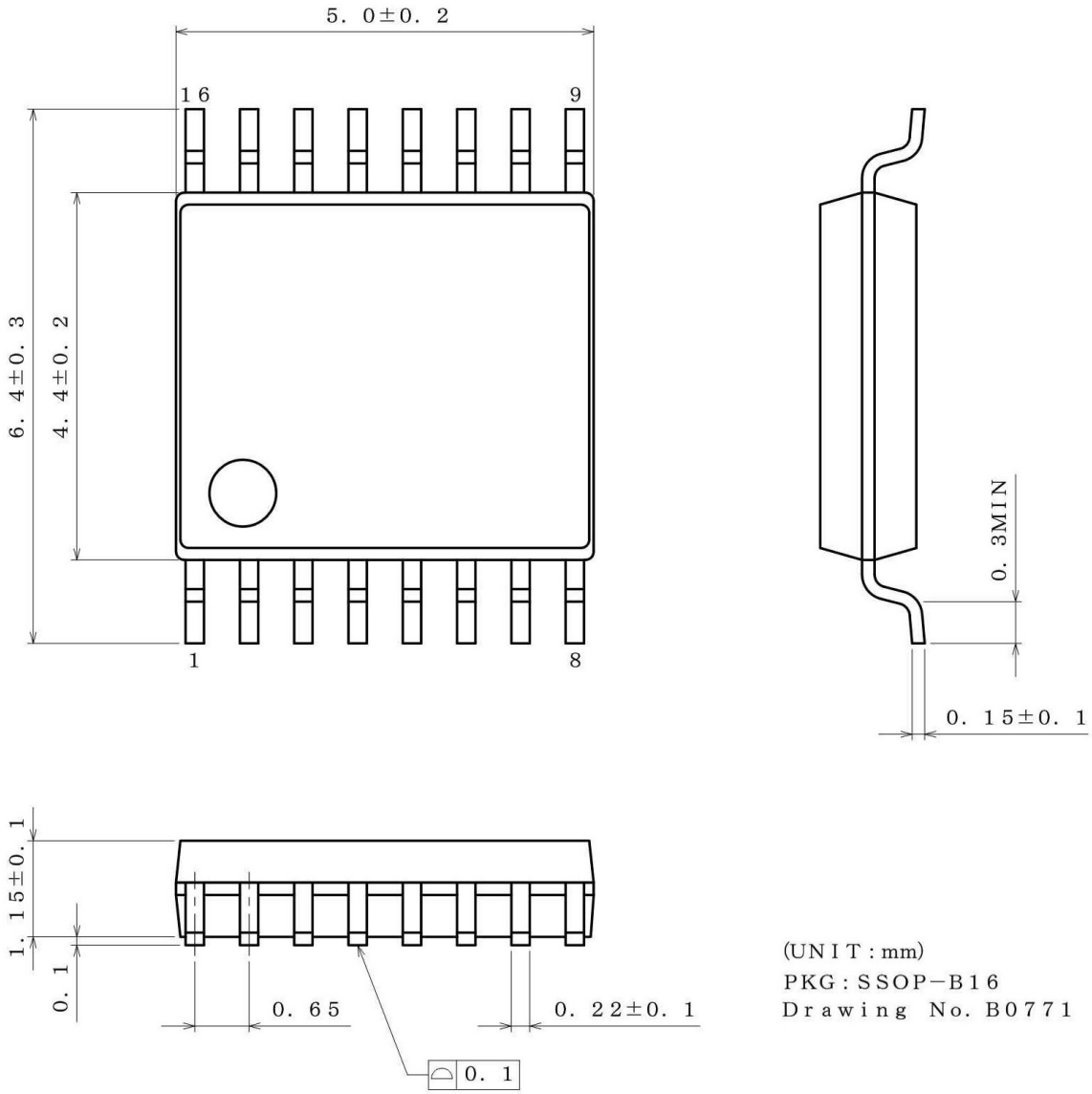


Marking Diagrams



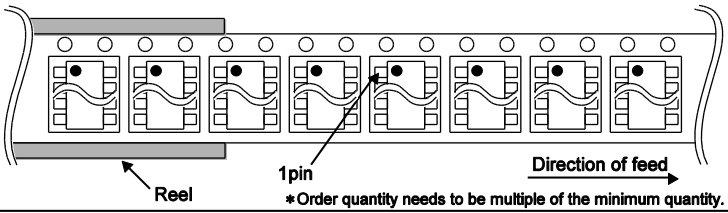
Physical Dimension, Tape and Reel Information

Package Name	SSOP-B16



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
24.Jun.2016	001	New Release