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Power Management LSI for Mobile Phone

BD71801GWL

General Description

The BD71801GWL is an integrated Power Management LSI available in a small 80-pins 0.4mm-pitch 3.8mm-by-3.8mm Wafer-level CSP package, which is designed to meet demands for space-constrained Smart phones.

The device provides 5-Buck Converters. The device also includes 12 general-purpose LDOs providing a wide range of voltage and current capabilities.

All Buck Converters and LDOs are fully controllable by the I2C interface. The BD71801GWL is very easy to use in any mobile platforms.

Features

- 5-Channel High Efficiency Step-down Converters. (Adjustable Voltage Options by I2C) (Switching frequency 2MHz(TYP))
- All Buck Converters Support PFM/PWM Auto Mode.
- 12-Channel LDOs are Programmable to Voltage Options by I2C.
- LDOs and all Buck Converters Power ON/OFF Control Enabled by I2C Interface or External pin.
- 2ch NMOS output LDOs (LDO11, 12) for Optimized Efficiency.
- Power ON/OFF Sequence.
- Support TCXO Buffer (26MHz) and 32KHz crystal oscillator.
- I2C Compatible Interface. (I2C Clock Support : Full Speed Mode 400kHz) (Device Address is "1001011","1001100")

Applications

- Smart Phones
- Tablets
- Mobile Router
- Data Transmitter

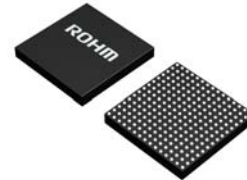
Key Specifications

- Input Voltage Range: 2.6V to 5.5V
- Output Voltage Range: 1.0V to 3.4V
- Switching Frequency: 2.0MHz(Typ)
- OFF Current: 0.3μA (Typ)
- Operating Temperature Range: -35°C to +85°C

Package

UCSP50L3C

W(Typ) x D(Typ) x H(Max)
3.80mm x 3.80mm x 0.57mm



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Maximum Supply Voltage 1 (VBATREF, VBAT, VIN1)	VBATMAX	7.0	V
Maximum Supply Voltage 2 (PBAT1,2,3,4,5)	VPBATMAX	7.0	V
Maximum Supply Voltage 3 (VIN2)	VIN2MAX	4.2	V
Maximum Input Voltage 1 (OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, OUT8, OUT9, OUT10, LX1, LX2, LX3, LX4, LX5, PSET, ADRS, EN_O7, PWRON, PWRHOLD, POR, TCXO_IN, OSC_IN, DVDD ^(Note 1) , OSC_OUT, SIMRSTIN, SIMCLKIN, SIMIODBB, SIMIO)	VINMAX1	7.0	V
Maximum Input Voltage 2 (SDA, SCL)	VINMAX2	DVDD + 0.3	V
Maximum Input Voltage 3 (OUT11,12, REFC)	VINMAX3	VIN2MAX + 0.3	V
Power Dissipation	Pd	1.38 ^(Note 2)	W
Operating Temperature Range	Topr	-35 ~ +85	°C
Storage Temperature Range	Tstg	-55 ~ +125	°C

(Note 1) The DVDD Voltage must be under the Battery voltage VBAT, PBAT anytimes.

(Note 2) Derate by 13.8mW/ when operation above Ta=25 (when mounted in ROHM's standard board(54mm × 62mm)).

Caution: Operation the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, likes adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Range	Unit
VBAT Voltage	VBAT	2.70 ~ 5.50 ^(Note3)	V
PBAT Voltage	VPBAT	2.70 ~ 5.50 ^(Note3)	V
VIN1 Voltage	VIN1	2.70 ~ 5.50 ^(Note4)	V
VIN2 Voltage	VIN2	1.40 ~ 1.80 ^(Note5)	V

(Note 3) Whenever the VBAT or PBAT or VIN1 or VIN2 voltage is under the LDO, SWREG output voltage, or under certain levels, the LDO and SWREG output is not guaranteed to meet its published specifications. It is necessary to supply the same voltage to PBAT and VBAT.

(Note 4) To achieve the best efficiency performance, SWREG5 output is recommended to be connected to VIN1 externally.

(Note 5) To achieve the best efficiency performance, SWREG4 output is recommended to be connected to VIN2 externally.

Block Diagram

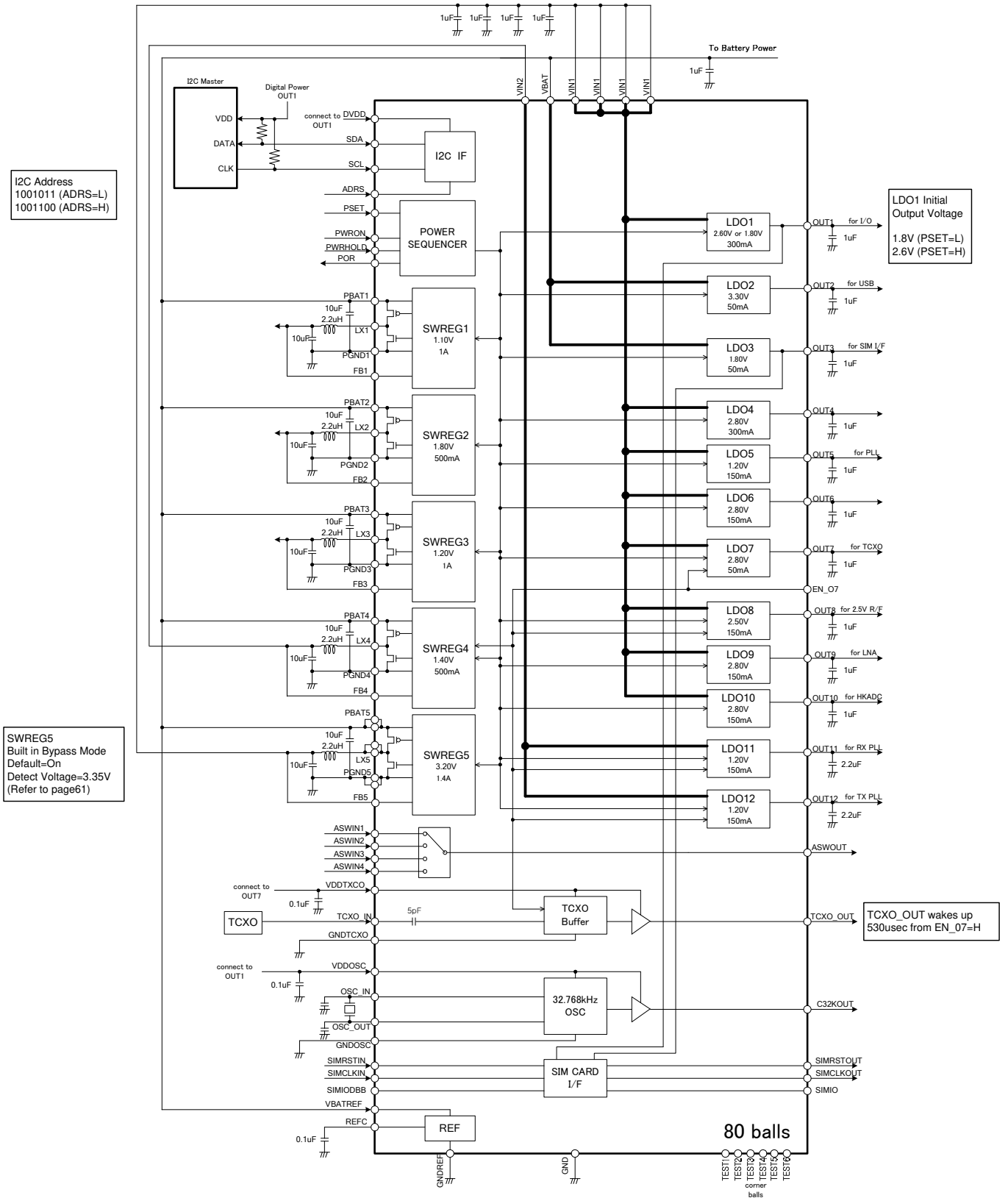


Figure 1. Block Diagram

(Note1) Recommend Parts

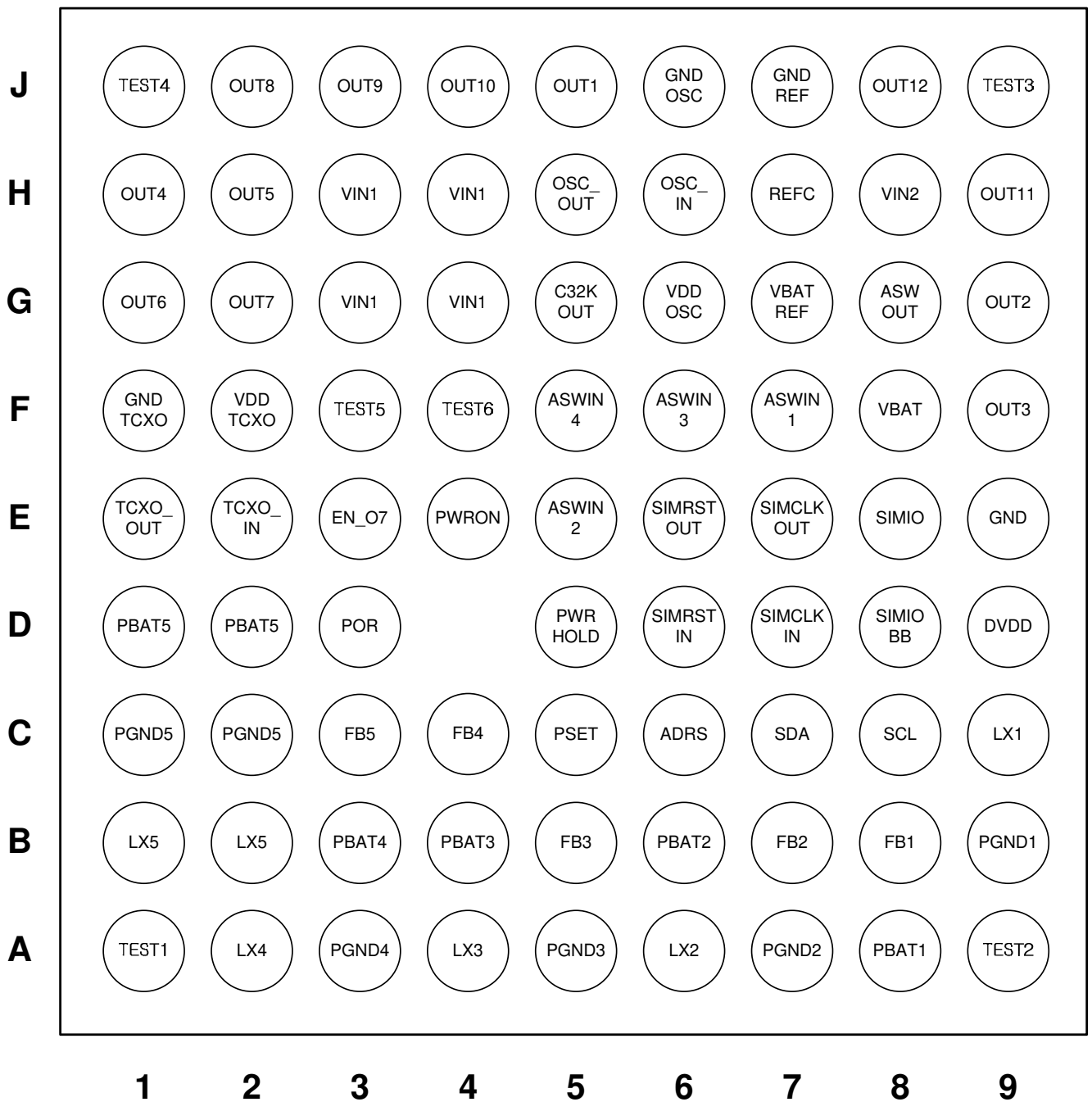
- 1. Coil : SWREG2, SWREG4 → DFE201612R-H-2R2N (TOKO)
SWREG1, SWREG3, SWREG5 → DFE252012R-H-2R2N (TOKO)
- 2. X_{tal} : FC135 (EPSON TOYOCOM)
CM7V-T1A (MICRO CRYSTAL SWITZERLAND)

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

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Pin Configurations



Bottom View

Figure 2. Pin Configuration

Pin Descriptions

Ball No.	Pin Name	A/D	I/O	Equivalent Circuit Eigure	Function	Diode		Initial Condition	Function
						+ side	- side		
A1	TEST1	-	-	-	Non connect pin (Open or connected to GND.)	VBAT	GND	-	(Note1)
A2	LX4	A	O	A	Inductor Connection for SWREG4	PBAT4	PGND4	HiZ	
A3	PGND4	-	-	-	Ground for SWREG4	PBAT4	GND	-	
A4	LX3	A	O	A	Inductor Connection for SWREG3	PBAT3	PGND3	HiZ	
A5	PGND3	-	-	-	Ground for SWREG3	PBAT3	GND	-	
A6	LX2	A	O	A	Inductor Connection for SWREG2	PBAT2	PGND	HiZ	
A7	PGND2	-	-	-	Ground for SWREG2	PBAT2	GND	-	
A8	PBAT1	-	-	-	Power Supply for SWREG1	-	PGND1	-	
A9	TEST2	-	-	-	Non connect pin (Open or connected to GND)	VBAT	GND	-	(Note1)
B1	LX5	A	O	A	Inductor Connection for SWREG5	PBAT5	PGND5	HiZ	
B2	LX5	A	O	A	Inductor Connection for SWREG5	PBAT5	PGND5	HiZ	
B3	PBAT4	-	-	-	Power Supply for SWREG4	-	PGND4	-	
B4	PBAT3	-	-	-	Power Supply for SWREG3	-	PGND3	-	
B5	FB3	A	I/O	B	Voltage Feed back pin for SWREG3	PBAT3	GND	-	
B6	PBAT2	-	-	-	Power Supply for SWREG2	-	PGND2	-	
B7	FB2	A	I/O	B	Voltage Feed back pin for SWREG2	PBAT2	GND	-	
B8	FB1	A	I/O	B	Voltage Feed back pin for SWREG1	PBAT1	GND	-	
B9	PGND1	-	-	-	Ground for SWREG1	PBAT1	GND	-	
C1	PGND5	-	-	-	Ground for SWREG5	PBAT5	GND	-	
C2	PGND5	-	-	-	Ground for SWREG5	PBAT5	GND	-	
C3	FB5	A	I/O	B	Voltage Feed back pin for SWREG5	PBAT5	GND	-	
C4	FB4	A	I/O	B	Voltage Feed back pin for SWREG4	PBAT4	GND	-	
C5	PSET	D	I	C	LDO1 Initial voltage set pin (L=1.8V, H=2.6V)	PBAT3	GND	-	Connect to GND
C6	ADRS	D	I	C	Logic Selector	PBAT4	GND	-	I2C Address 1001011 (ADRS=L) 1001100 (ADRS=H)
C7	SDA	D	I	D	I2C data input	VBAT	GND	-	
C8	SCL	D	I	E	I2C clock input	VBAT	GND	-	
C9	LX1	A	O	A	Inductor Connection for SWREG1	PBAT1	PGND1	HiZ	

(Note 1) The TEST1, 2, 3, 4, 5, 6 pin are used for factory test mode. Please keep these pin "OPEN" or GND at all times.

Ball No.	Pin Name	A/D	I/O	Equivalent Circuit Eigure	Function	Diode		Initial Condition	Function
						+ side	- side		
D1	PBAT5	-	-	-	Power Supply for SWREG5	-	PGND5	-	
D2	PBAT5	-	-	-	Power Supply for SWREG5	-	PGND5	-	
D3	POR	D	O	F	Power on reset signal output	VBAT	GND	L	(Note2)
D5	PWRHOLD	D	I	G	Power enable signal	VBAT	GND	-	
D6	SIMRSTIN	D	I	H	SIM clock input from DBB	VBAT	GND	-	
D7	SIMCLKIN	D	I	H	SIM reset input from DBB	VBAT	GND	-	
D8	SIMIOBB	D	I/O	I	SIM data input / output from DBB	VBAT	GND	-	Pull up 20KΩ to OUT1
D9	DVDD	-	-	-	VDD for I2C block	VBAT	GND	-	
E1	TCXO_OUT	D	O	K	TCXO_Buffer input frequency	VDDTCXO	GND	L	
E2	TCXO_IN	A	I	J	TCXO_Buffer output frequency	VBAT	GND	-	
E3	EN_07	D	I	L	TCXO Buffer, SWREG4, LDO7,8,11,12 control	VBAT	GND	Pull Down	Pull down 1.5MΩ
E4	PWRON	D	I	L	Start up signal input	VBAT	GND	Pull Down	Pull down 1.5MΩ
E5	ASWIN2	A	I	M	Analog SW input selector2	VBAT	GND	-	
E6	SIMRSTOUT	D	O	N	SIM CARD side reset output	VBAT OUT3	GND	L	
E7	SIMCLKOUT	D	O	N	SIM CARD side clock output	VBAT OUT3	GND	L	
E8	SIMIO	D	I/O	I	SIM CARD side data input/output	VBAT	GND	Pull Up	Pull up 10KΩ to OUT3
E9	GND	-	-	-	Ground Pin	VBAT	-	-	
F1	GNDTCXO	-	-	-	Ground for TCXO Buffer	VBAT	GND	-	
F2	VDDTCXO	-	-	-	Power Supply for TCXO Buffer	-	GND	-	
F3	TEST5	-	-	-	Non connect pin (Open or connected to GND.)	VBAT	GND	-	(Note1)
F4	TEST6	-	-	-	Non connect pin (Open or connected to GND.)	VBAT	GND	-	(Note1)
F5	ASWIN4	A	I	M	Analog SW input selector4	VBAT	GND	-	
F6	ASWIN3	A	I	M	Analog SW input selector3	VBAT	GND	-	
F7	ASWIN1	A	I	M	Analog SW input selector1	VBAT	GND	-	
F8	VBAT	-	-	-	Power Supply for IC	-	GND	-	
F9	OUT3	A	O	O	LDO3 output	VBAT	GND		

(Note 1) The TEST1, 2, 3, 4, 5, 6 pin are used for ROHM factory test mode. Please keep these pin "OPEN" or tied to GND at all times.

(Note 2) POR pin needs a pull up resistor in PCB layout.

Ball No.	PIN名	A/D	I/O	Equivalent Circuit Eigure	Function	Diode		Initial Condition	Function
						+ side	- side		
G1	OUT6	A	O	P	LDO6 output	VIN1	GND	-	
G2	OUT7	A	O	P	LDO7 output	VIN1	GND	-	
G3	VIN1	-	-	-	Power Supply input for LDO	-	GND	-	
G4	VIN1	-	-	-	Power Supply input for LDO	VBAT	GND	-	
G5	C32KOUT	A	O	Q	32.768kHz output	VBAT	GND	-	
G6	VDDOSC	-	-	-	Power Supply for RTC Block	-	GND	-	
G7	VBATREF	-	-	-	Power Supply for Reference Block	-	GND	-	
G8	ASWOUT	A	O	M	Analog SW selector Output	VBAT	GND	-	
G9	OUT2	A	O	O	LDO2 output	VBAT	GND	-	
H1	OUT4	A	O	P	LDO4 output	VIN1	GND	-	
H2	OUT5	A	O	P	LDO5 output	VIN1	GND	-	
H3	VIN1	-	-	-	Power Supply input for LDO	VBAT	GND	-	
H4	VIN1	-	-	-	Power Supply input for LDO	VBAT	GND	-	
H5	OSC_OUT	A	I/O	R	32.768kHz crystal connect terminal	-	GND	-	
H6	OSC_IN	A	I/O	R	32.768kHz crystal connect terminal	-	GND	-	
H7	REFC	A	O	S	Reference Voltage output	VBAT	GND	-	
H8	VIN2	-	-	-	Power Supply input for LDO	VBAT	GND	-	
H9	OUT11	A	O	T	LDO11 output	VIN2	GND	-	
J1	TEST4	-	-	-	Non connect pin (Open or connected to GND.)	VBAT	GND	-	(Note1)
J2	OUT8	A	O	P	LDO8 output	VIN1	GND	-	
J3	OUT9	A	O	P	LDO9 output	VIN1	GND	-	
J4	OUT10	A	O	P	LDO10 output	VIN1	GND	-	
J5	OUT1	A	O	P	LDO1 output	VIN1	GND	-	
J6	GNDOSC	-	-	-	GND for RTC block	VBAT	-	-	
J7	GNDREF	-	-	-	Ground for Reference Block	VBAT	-	-	
J8	OUT12	A	O	T	LDO12 output	VIN2	GND	-	
J9	TEST3	-	-	-	Non connect pin (Open or connected to GND.)	VBAT	GND	-	(Note1)

(Note 1) The TEST1, 2, 3, 4, 5, 6 pin are used for factory test mode. Please keep these pin "OPEN" or tied to GND at all times.

I/O Equivalence Circuits

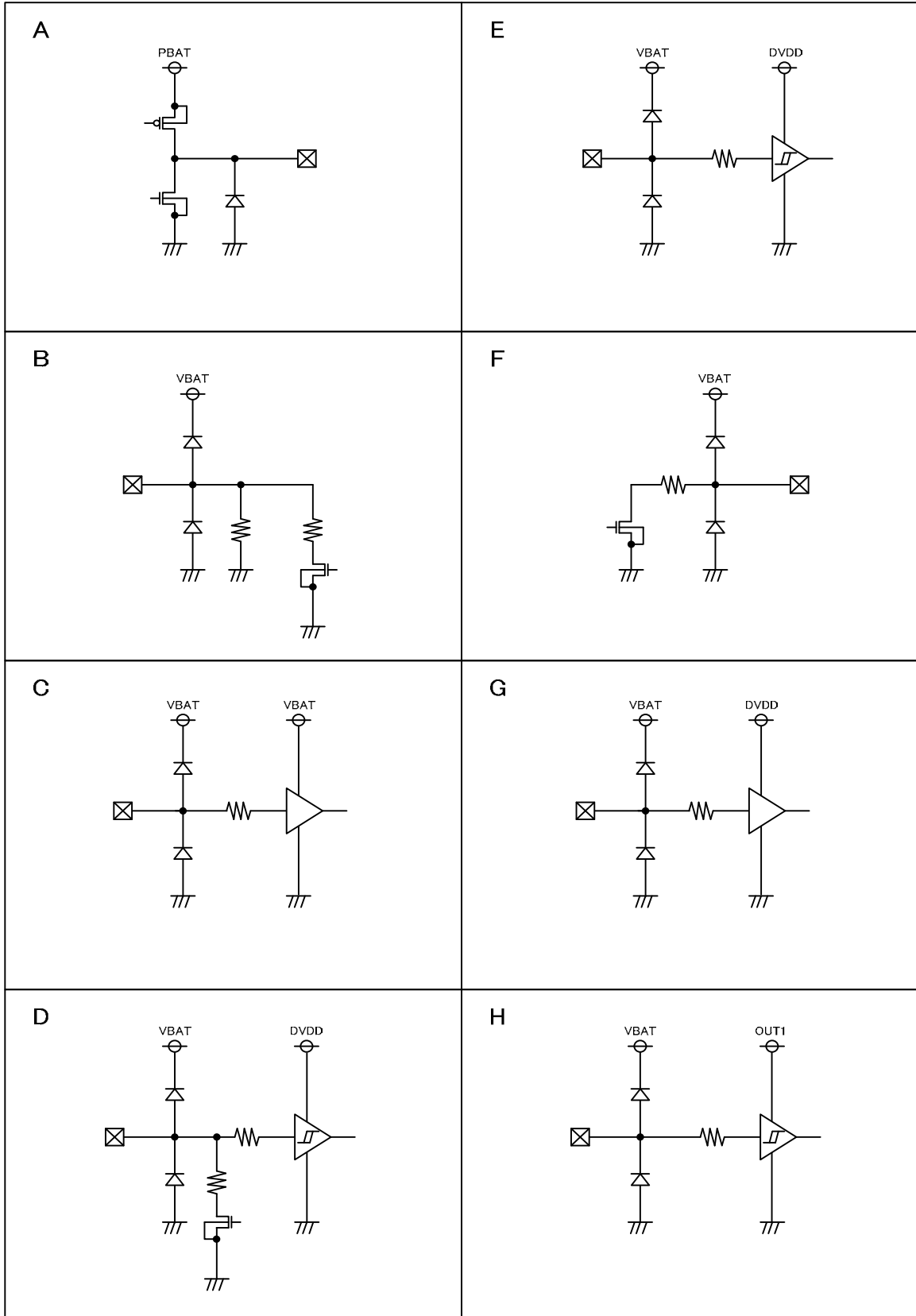


Figure 3. I/O Equivalence Circuits

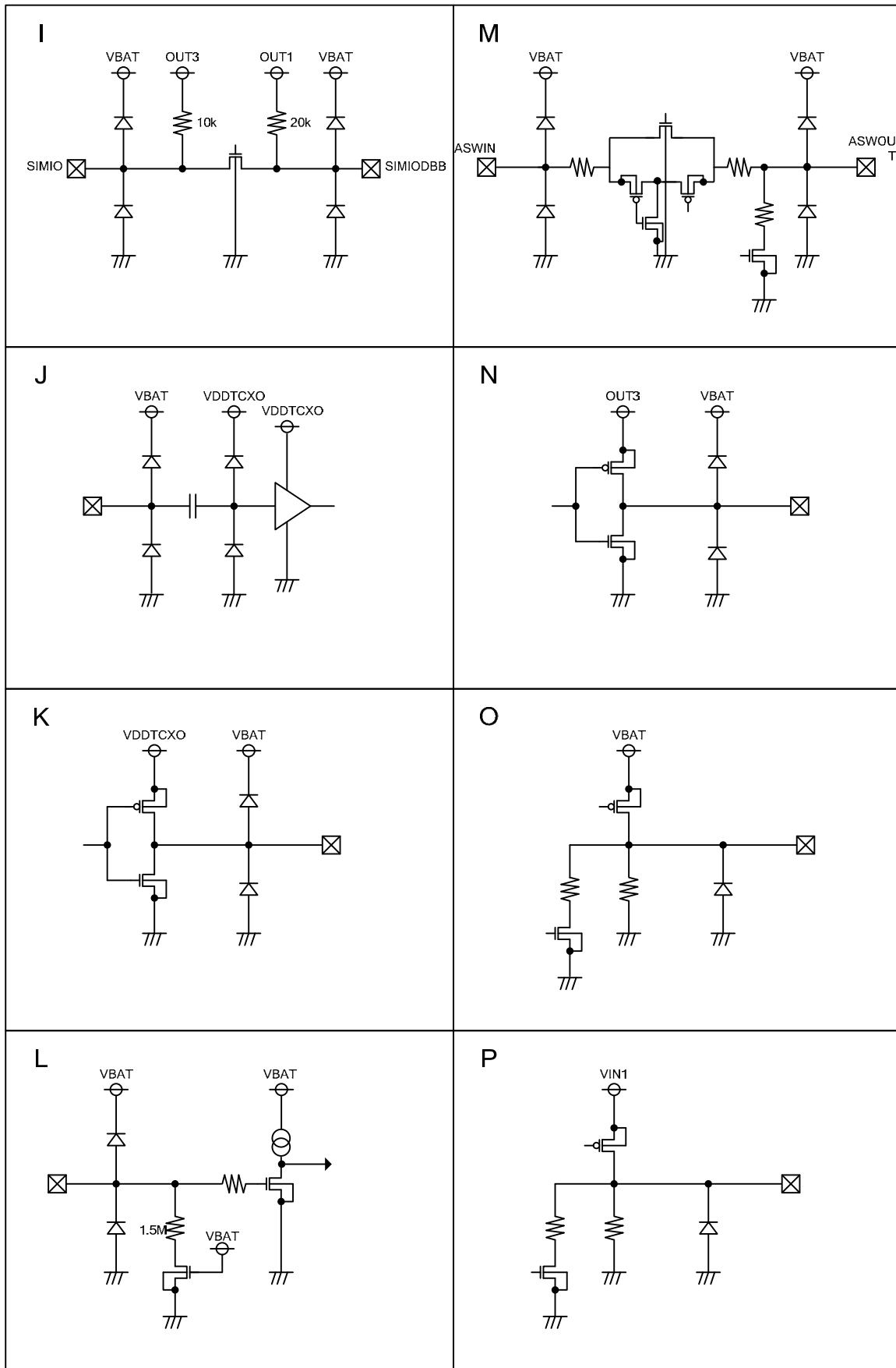


Figure 4. I/O Equivalence Circuits

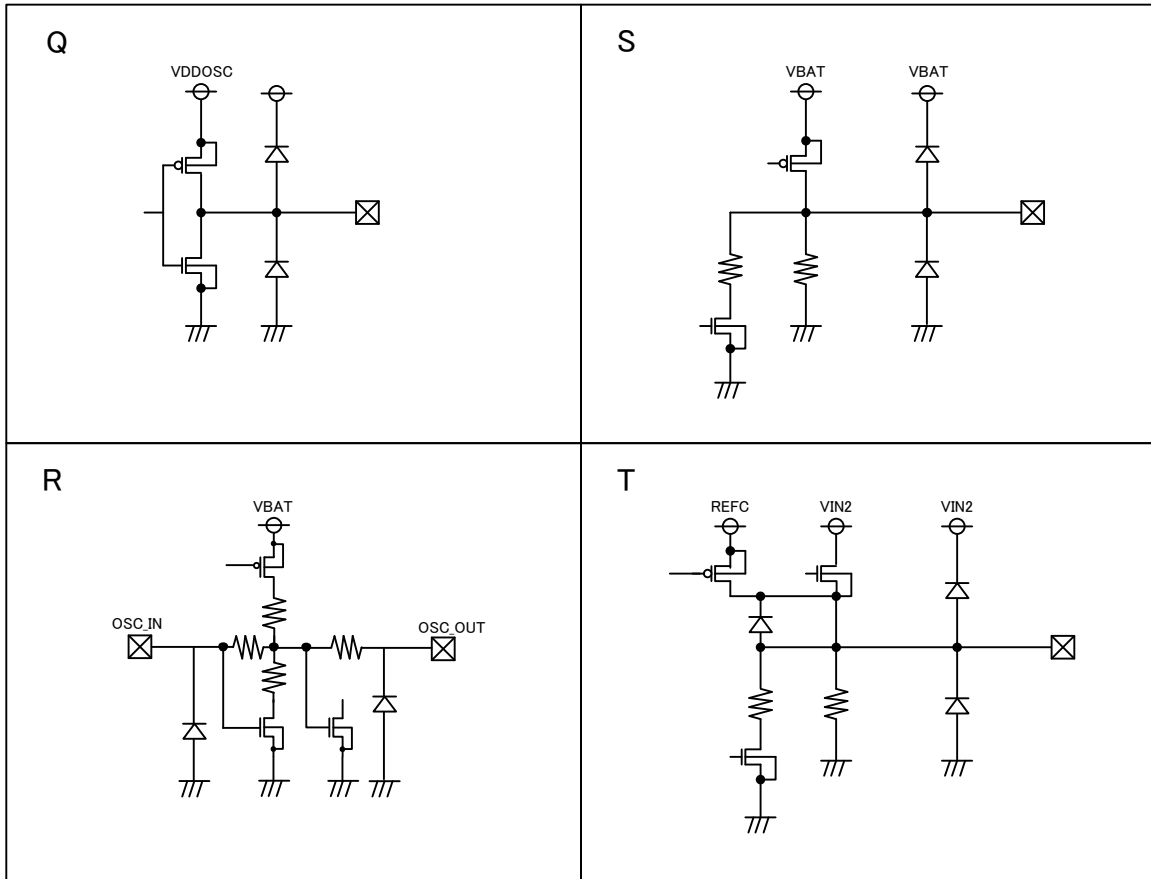


Figure 5. I/O Equivalence Circuits

Initial Output Voltage Summary

	Usage example	Power Supply	Initial Output Voltage	Load max	Adjustable range
SWREG1	CORE	PBAT1	1.10V	1.0A	±50,100mV
SWREG2	MEMORY	PBAT2	1.80V	0.5A	±50,100mV
SWREG3	ANALOG	PBAT3	1.20V	1.0A	±50,100mV
SWREG4	For VIN2 power supply (efficiency improvement)	PBAT4	1.40V	0.5A	±50,100mV
SWREG5	For VIN1 power supply (efficiency improvement)	PBAT5	3.20V	1.4A	±50,100mV
LDO1	I/O	VIN1	2.60V / 1.80V (Note 1)	300mA	±50,100mV
LDO2	USB	VBAT	3.30V	50mA	±50,100mV
LDO3	SIM I/F	VBAT	1.80V	50mA	±50,100mV
LDO4	Reserved	VIN1	2.80V	300mA	±50,100mV
LDO5	SYS PLL	VIN1	1.20V	150mA	±50,100mV
LDO6	Reserved	VIN1	2.80V	150mA	±50,100mV
LDO7	TCXO	VIN1	2.80V	50mA	±50,100mV
LDO8	2.5V R/F	VIN1	2.50V	150mA	±50,100mV
LDO9	LNA	VIN1	2.80V	150mA	±50,100mV
LDO10	HKADC	VIN1	2.80V	150mA	±50,100mV
LDO11	RX PLL	VIN2	1.20V	150mA	±50,100mV
LDO12	TX PLL	VIN2	1.20V	150mA	±50,100mV

(Note1) Depend on PSET pin setting.

SWREG Output Voltage Step Table

	SWREG1	SWREG2	SWREG3	SWREG4	SWREG5
Voltage step [V]	1.00	1.00	1.00	1.00	1.20
	1.05	1.05	1.05	1.05	1.40
	1.10	1.10	1.10	1.10	1.70
	1.15	1.15	1.15	1.15	1.75
	1.20	1.20	1.20	1.20	1.80
	1.25	1.25	1.25	1.25	1.85
	1.30	1.30	1.30	1.30	1.90
	1.35	1.35	1.35	1.35	3.00
	1.40	1.40	1.40	1.40	3.05
	1.45	1.45	1.45	1.45	3.10
	1.50	1.50	1.50	1.50	3.15
	1.70	1.70	1.70	1.70	3.20
	1.75	1.75	1.75	1.75	3.25
	1.80	1.80	1.80	1.80	3.30
	1.85	1.85	1.85	1.85	3.35
1.90	1.90	1.90	1.90	3.40	

	LDO1	LDO2	LDO3	LDO4	LDO5	LDO6	LDO7	LDO8	LDO9	LDO10	LDO11	LDO12
Voltage step [V]	1.70	2.55	1.70	1.10	1.00	1.10	1.10	1.20	1.10	1.10	1.00	1.00
	1.75	2.60	1.75	1.20	1.05	1.20	1.20	1.30	1.20	1.20	1.05	1.05
	1.80	2.65	1.80	1.30	1.10	1.30	1.30	1.70	1.30	1.30	1.10	1.10
	1.85	2.75	1.85	1.70	1.15	1.70	1.70	1.80	1.70	1.70	1.15	1.15
	1.90	2.80	1.90	1.80	1.20	1.80	1.80	2.40	1.80	1.80	1.20	1.20
	2.50	2.85	2.50	1.90	1.25	1.90	1.90	2.45	1.90	1.90	1.25	1.25
	2.55	2.90	2.60	2.50	1.30	2.50	2.50	2.50	2.50	2.50	1.30	1.30
	2.60	2.95	2.70	2.55	1.70	2.55	2.55	2.55	2.55	2.55	1.35	1.35
	2.65	3.00	2.80	2.60	1.80	2.60	2.60	2.60	2.60	2.60		
	2.70	3.05	2.90	2.65	1.90	2.65	2.65	2.65	2.65	2.65		
	2.80	3.10	2.95	2.70	2.60	2.70	2.70	2.70	2.70	2.70		
	2.90	3.20	3.00	2.75	2.70	2.75	2.75	2.75	2.75	2.75		
	2.95	3.25	3.05	2.80	2.80	2.80	2.80	2.80	2.80	2.80		
	3.00	3.30	3.10	2.85	2.90	2.85	2.85	2.85	2.85	2.85		
	3.05	3.35	3.20	2.90	3.00	2.90	2.90	2.90	2.90	2.90		
	3.10	3.40	3.30	3.00	3.10	3.00	3.00	3.00	3.00	3.00		

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

Power On Sequence

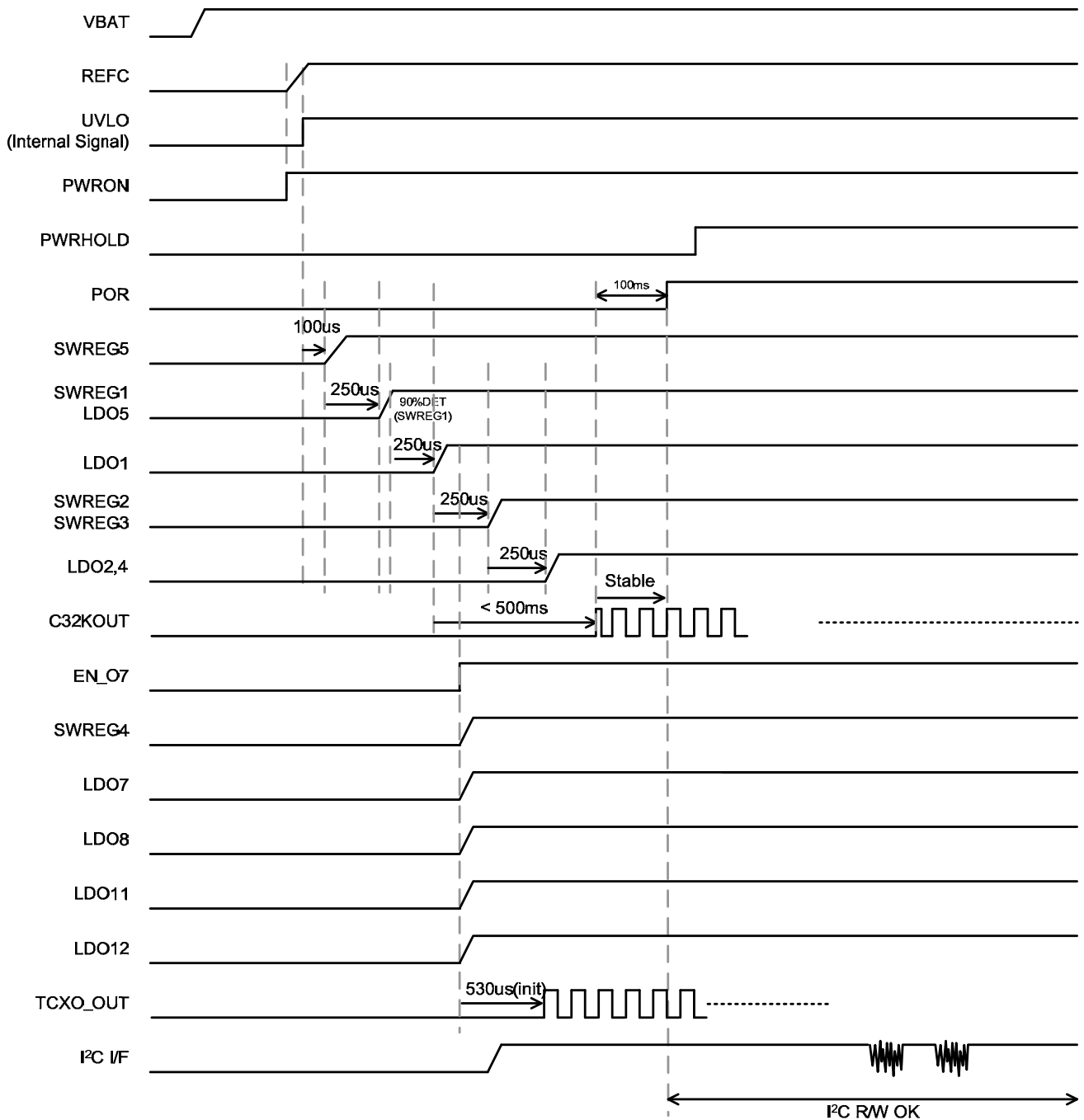


Figure 6. Power ON sequence (Start factor is PWRON)

The short detection circuit is built in the SWREG1,2,3,4 and 5 outputs.

When the output shorted state continued more than 100ms, the all LDO and SWREG will be OFF.

If the LDO and SWREG are turned off by the external pin (EN_O7) or I2C command, the short detection circuit is not detected.

The SWREG1, 2, 3, and 4 must be used external parts when not used SWREG's output voltage.

If it is not used the external parts in these SWREG, the short detector will detect when running the start up sequence.

(It is possible when these SWREG turn off by the I2C command after start up sequence.)

Power Off Sequence

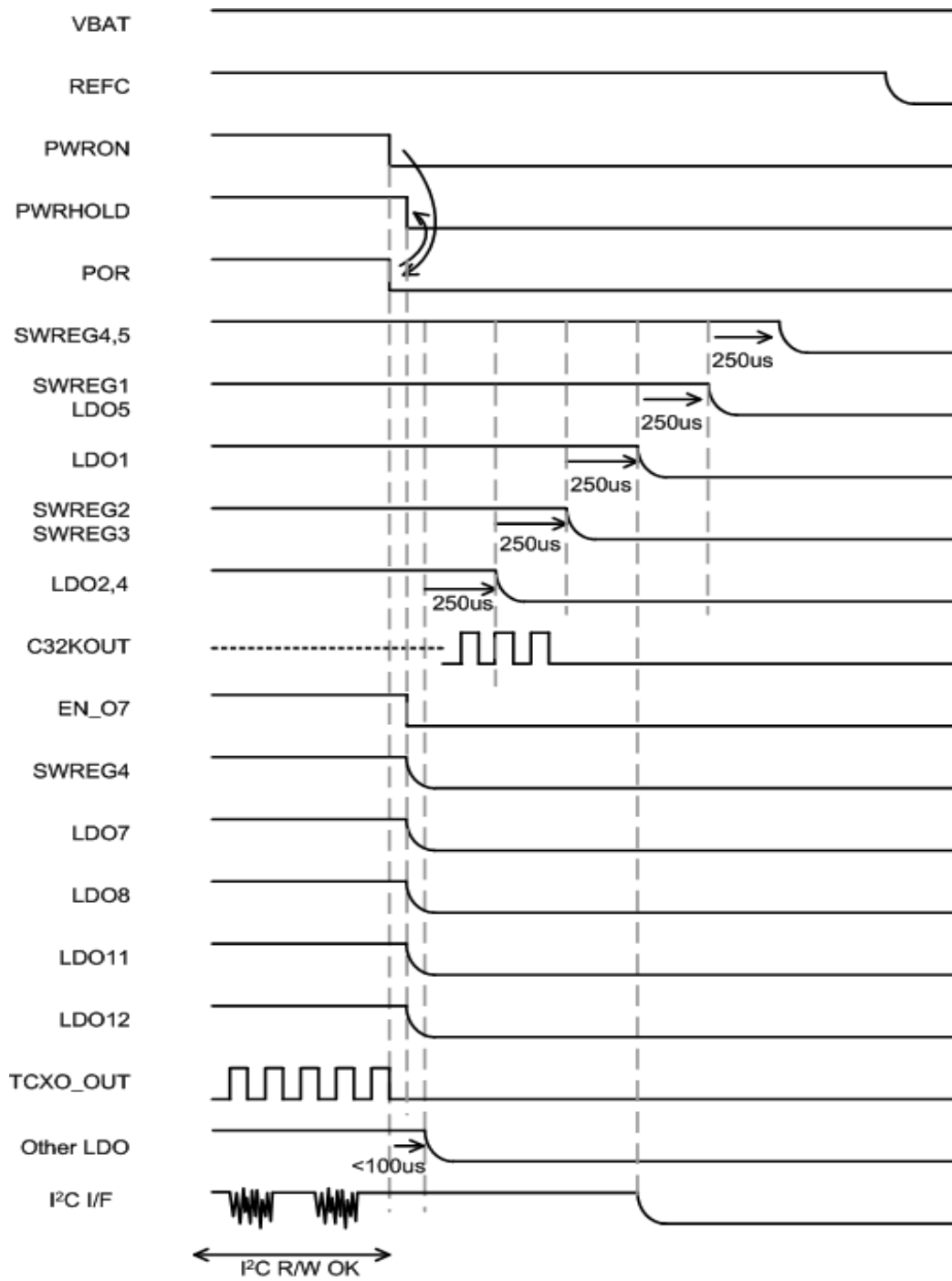


Figure 7. Power OFF sequence

Electrical Characteristics (Current Consumption)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT1, 2, 3, 4, 5=VIN1=VIN2=3.6V, DVDD=VDDOSC=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Circuit Current						
VBAT Circuit Current 1 (OFF)	IQVB1	-	0.3	1.0	μA	All LDO=OFF All SWREG=OFF DVDD=0V PWRON=L PWRHOLD=L EN_O7=L
VBAT Circuit Current 2 (Sleep)	IQVB2	-	280	475	μA	PWRON=H PWRHOLD=H LDO1,2,4,5=ON SWREG1,2,3,5=ON POR=H All SWREG=PFM/PWM auto mode All LDO, SWREG=No load 32kHz Buffer=ON EN_O7=L
VBAT Circuit Current 3 (All on)	IQVB3	-	580	1160	μA	PWRON=H PWRHOLD=H LDO1,2,3,4,5,6,7,8,9,10,11,12=ON SWREG1,2,3,4,5=ON POR=H All SWREG=PFM/PWM auto mode All LDO, SWREG=No load EN_O7=H

Electrical Characteristics (Logic Interface)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT1, 2, 3, 4, 5=VIN1=VIN2=3.6V, DVDD=OUT1)

Parameter	Symbol	Rating			Unit	Conditions
		Min	Typ	Max		
Digital characteristics (Digital Pins: EN_07, PWRON as NMOS input) ^(Note1)						
Input "H" level	VIH1	1.44	-	-	V	
Input "L" level	VIL1	-	-	0.4	V	
Pull Down Resistance	RPD1	-	1.5	-	MΩ	PWRON, EN_07
Digital characteristics (Digital Pins: SCL, SDA, PWRHOLD) ^(Note1)						
Input "H" level	VIH2	0.7× DVDD	-	DVDD+0.3	V	
Input "L" level	VIL2	-0.3	-	0.3× DVDD	V	
Input leak current	IIC2	-1	0	1	μA	
Digital characteristics (Digital Pins: PSET, ADRS)						
Input "H" level	VIH3	0.7× VBAT	-	VBAT+0.3	V	
Input "L" level	VIL3	-0.3	-	0.3× VBAT	V	
Input leak current	IIC3	-1	0	1	μA	
Digital characteristics (Digital Pins: SDA, POR)						
SDA output "L" level voltage	VOL1	-	-	0.4	V	IOL = 6mA
POR output "L" level voltage	VOL2	-	-	0.4	V	IOL = 1mA

(Note 1) The EN_07, PWRON, PWRHOLD and POR pin can be use under the Max VBAT+0.3V.

Electrical Characteristics (32 kHz Buffer)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT1, 2, 3, 4, 5=VIN1=VIN2=3.6V, DVDD=VDDOSC=OUT1)

Parameter	Symbol	Rating			Unit	Conditions
		Min	Typ	Max		
Digital characteristics (Digital Pins: C32KOUT)						
C32KOUT Output High Level	VOH_32K	0.8× OUT1	-	-	V	IO= -2mA
C32KOUT Output Low Level	VOL_32K	-	-	0.2× OUT1	V	IO= 2mA
32.768kHz Duty	DUTY	30	50	70	%	

Electrical Characteristics (SWREG1)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SWREG1						
Output Voltage	VOSW1	1.067	1.100	1.133	V	initial value Io=100mA
Programmable Output Voltage	VOSW10 VOSW11 VOSW12 VOSW13	-3%	1.00 1.05 1.15 1.20	+3%	V	Io=100mA
Output Current	IOSW1	-	-	1000	mA	
Efficiency	ηSW1	-	86	-	%	Io=400mA, Vo=1.20V, VBAT=3.6V
Oscillating Frequency	FOSC1	-	2.0	-	MHz	Vo=1.10V (PWM mode, Io=100mA)
Output Inductance	LSWREG1	1.5	2.2	-	μH	Ta= -35~85°C
Output Capacitance	CSWREG1	4.7	10	-	μF	Ta= -35~85°C, with SWREG's DC bias

Electrical Characteristics (SWREG2)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SWREG2						
Output Voltage	VOSW2	1.746	1.800	1.854	V	initial value Io=100mA
Programmable Output Voltage	VOSW20 VOSW21 VOSW22 VOSW23	-3%	1.70 1.75 1.85 1.90	+3%	V	Io=100mA
Output Current	IOSW2	-	-	500	mA	
Efficiency	ηSW2	-	86	-	%	Io= 200mA, Vo=1.80V, VBAT=3.6V
Oscillating Frequency	FOSC2	-	2.0	-	MHz	Vo=1.80V (PWM mode, Io=100mA)
Output Inductance	LSWREG2	1.5	2.2	-	μH	Ta= -35~85°C
Output Capacitance	CSWREG2	4.7	10	-	μF	Ta= -35~85°C, with SWREG's DC bias

Electrical Characteristics (SWREG3)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SWREG3						
Output Voltage	VOSW3	1.164	1.200	1.236	V	initial value Io=100mA
Programmable Output Voltage	VOSW30 VOSW31 VOSW32 VOSW33	-3%	1.10 1.15 1.25 1.30	+3%	V	Io=100mA
Output Current	IOSW3	-	-	1000	mA	
Efficiency	η SW3	-	86	-	%	Io=200mA, Vo=1.20V, VBAT=3.6V
Oscillating Frequency	FOSC3	-	2.0	-	MHz	Vo=1.20V (PWM mode, Io=100mA)
Output Inductance	LSWREG3	1.5	2.2	-	μ H	Ta= -35~85°C
Output Capacitance	CSWREG3	4.7	10	-	μ F	Ta= -35~85°C, with SWREG's DC bias

Electrical Characteristics (SWREG4)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SWREG4						
Output Voltage	VOSW4	1.358	1.400	1.442	V	initial value Io=100mA
Programmable Output Voltage	VOSW40 VOSW41 VOSW42 VOSW43	-3%	1.50 1.45 1.35 1.30	+3%	V	Io=100mA
Output Current	IOSW4	-	-	500	mA	
Efficiency	η SW4	-	87	-	%	Io=200mA, Vo=1.40V, VBAT=3.6V
Oscillating Frequency	FOSC4	-	2.0	-	MHz	Vo=1.40V (PWM mode, Io=100mA)
Output Inductance	LSWREG4	1.5	2.2	-	μ H	Ta= -35~85°C
Output Capacitance	CSWREG4	4.7	10	-	μ F	Ta= -35~85°C, with SWREG's DC bias

Electrical Characteristics (SWREG5)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SWREG5						
Output Voltage	VOSW5	3.104	3.200	3.296	V	initial value Io=100mA
Programmable Output Voltage	VOSW50 VOSW51 VOSW52 VOSW53	-3%	3.300 3.250 3.150 3.100	+3%	V	Io=100mA
Output Current	IOSW5	-	-	1400	mA	
Efficiency	η SW5	-	92	-	%	Io=400mA, Vo=3.20V, VBAT=3.6V
Oscillating Frequency	FOSC5	-	2.0	-	MHz	Vo=3.20V (PWM mode, Io=100mA)
Output Inductance	LSWREG5	1.5	2.2	-	μ H	Ta= -35~85°C
Output Capacitance	CSWREG5	4.7	10	-	μ F	Ta= -35~85°C, with SWREG's DC bias

Electrical Characteristics (LDO1)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO1						
Output Voltage A	VOM1A0	2.548	2.600	2.652	V	Initial setting, PSET=H Io=50mA
Output Voltage B	VOM1B0	1.764	1.800	1.836	V	Initial setting, PSET=L Io=50mA
Output Current	VOM1C	-	-	300	mA	
Dropout Voltage	VOM1DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.1V setting)
Input Voltage Stability	ΔVIM1	-	2	-	mV	VIN1=3~4.5V, Io=50mA
Load Stability	ΔVLM1	-	20	-	mV	Io=1mA ~ 300mA
Programmable Output Voltage A	VOM1A1	-2%	2.70	+2%	V	Io=50mA
	VOM1A2		2.65			
	VOM1A3		2.55			
	VOM1A4		2.50			
Programmable Output Voltage B	VOM1B1	-2%	1.90	+2%	V	Io=50mA
	VOM1B2		1.85			
	VOM1B3		1.75			
	VOM1B4		1.70			
Discharge Resistance	RDCHG1	-	100	-	ohm	
Ripple Rejection Ratio	RRM1	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=120Hz Io=50mA, Vo=2.60V BW=20Hz~20kHz
Output Capacitor	COUT1	0.47	1.0	-	μF	Ta=-35~85°C, with LDO's DC bias

Electrical Characteristics (LDO2)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO2						
Output Voltage	VOM20	3.234	3.300	3.366	V	Io=50mA
Output Current	VOM2C	-	-	50	mA	
Dropout Voltage	VOM2DP	-	0.05	-	V	Io=50mA VBAT=2.8V(Vo=3.4V setting)
Input Voltage Stability	ΔV_{IM2}	-	2	-	mV	VBAT=3.6~4.5V, Io=50mA
Load Stability	ΔV_{LM2}	-	20	-	mV	Io=1mA ~ 50mA
Programmable Output Voltage	VOM21	-2%	3.40	+2%	V	Io=50mA
	VOM22		3.35			
	VOM23		3.25			
	VOM24		3.20			
Discharge Resistance	RDCHG2	-	100	-	ohm	
Ripple Rejection Ratio	RRM2	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=120Hz Io=50mA, Vo=3.3V BW=20Hz~20kHz
Output Capacitor	COUT2	0.47	1.0	-	μ F	Ta=-35~85°C, with LDO's DC bias

Electrical Characteristics (LDO3)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO3						
Output Voltage	VOM30	1.764	1.800	1.836	V	Io=50mA
Output Current	VOM3C	-	-	50	mA	
Dropout Voltage	VOM3DP	-	0.05	-	V	Io=50mA VBAT=2.8V (Vo=3.3V setting)
Input Voltage Stability	Δ VIM3	-	2	-	mV	VBAT=3.3~4.5V, Io=50mA
Load Stability	Δ VLM3	-	20	-	mV	Io=1mA ~ 50mA
Programmable Output Voltage B	VOM31	-2%	1.90	+2%	V	Io=50mA
	VOM32		1.85			
	VOM33		1.75			
	VOM34		1.70			
Discharge Resistance	RDCHG3	-	100	-	ohm	
Ripple Rejection Ratio	RRM3	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=120Hz Io=50mA, Vo=3.0V BW=20Hz~20kHz
Output Capacitor	COUT3	0.47	1.0	-	μ F	Ta=-35~85°C, with LDO's DC bias

Electrical Characteristics (LDO4)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO4						
Output Voltage	VOM40	2.744	2.800	2.856	V	Io=50mA
Output Current	VOM4C	-	-	300	mA	
Dropout Voltage	VOM4DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.0V setting)
Input Voltage Stability	Δ VIM4	-	2	-	mV	VBAT=3.2~4.5V, Io=50mA
Load Stability	Δ VLM4	-	20	-	mV	Io=1mA ~ 300mA
Programmable Output Voltage	VOM41 VOM42 VOM43 VOM44	-2%	2.90 2.85 2.75 2.70	+2%	V	Io=50mA
Discharge Resistance	RDCHG4	-	100	-	ohm	
Ripple Rejection Ratio	RRM4	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=120Hz Io=50mA, Vo=2.80V BW=20Hz~20kHz
Output Capacitor	COUT4	0.47	1.0	-	μ F	Ta=-35~85°C, with LDO's DC bias

Electrical Characteristics (LDO5)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO5						
Output Voltage	VOM50	1.176	1.200	1.224	V	Io=50mA
Output Current	VOM5C	-	-	150	mA	
Dropout Voltage	VOM5DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.1V setting)
Input Voltage Stability	Δ VIM5	-	2	-	mV	VIN1=3.0~4.5V, Io=50mA
Load Stability	Δ VLM5	-	20	-	mV	Io=1mA ~ 150mA
Programmable Output Voltage	VOM51	-2%	1.30	+2%	V	Io=50mA
	VOM52		1.25			
	VOM53		1.15			
	VOM54		1.10			
Discharge Resistance	RDCHG5	-	100	-	ohm	
Ripple Rejection Ratio	RRM5	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=10kHz Io=50mA, Vo=1.20V BW=20Hz~20kHz
Output Noise Level	VON5	-	60	-	μ Vrms	Io=50mA, Vo=1.20V BW=20Hz~20kHz
Output Capacitor	COU5	0.47	1.0	-	μ F	Ta=-35~85°C, with LDO's DC bias

Electrical Characteristics (LDO6)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO6						
Output Voltage	VOM60	2.744	2.800	2.856	V	Io=50mA
Output Current	VOM6C	-	-	150	mA	
Dropout Voltage	VOM6DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.0V setting)
Input Voltage Stability	Δ VIM6	-	2	-	mV	VIN1=3.2~4.5V, Io=50mA
Load Stability	Δ VLM6	-	20	-	mV	Io=1mA ~ 150mA
Programmable Output Voltage	VOM61	-2%	2.90	+2%	V	Io=50mA
	VOM62		2.85			
	VOM63		2.75			
	VOM64		2.70			
Discharge Resistance	RDCHG6	-	100	-	ohm	
Ripple Rejection Ratio	RRM6	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=10kHz Io=50mA, Vo=1.20V BW=20Hz~20kHz
Output Noise Level	VON6	-	60	-	μ Vrms	Io=50mA, Vo=1.20V BW=20Hz~20kHz
Output Capacitor	COUT6	0.47	1.0	-	μ F	Ta=-35~85°C, with LDO's DC bias

Electrical Characteristics (LDO7)

(Unless otherwise specified, Ta=25°C, VBAT=PBAT*=3.6V, VIN1=3.2V(FB5), VIN2=1.4V(FB4), DVDD=OUT1)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LDO7						
Output Voltage	VOM70	2.744	2.800	2.856	V	Io=50mA
Output Current	VOM7C	-	-	50	mA	
Dropout Voltage	VOM7DP	-	0.05	-	V	Io=50mA VIN1=2.7V(Vo=3.0V setting)
Input Voltage Stability	Δ VIM7	-	2	-	mV	VIN1=3.2~4.5V, Io=50mA
Load Stability	Δ VLM7	-	20	-	mV	Io=1mA ~ 50mA
Programmable Output Voltage	VOM71	-2%	2.90	+2%	V	Io=50mA
	VOM72		2.85			
	VOM73		2.75			
	VOM74		2.70			
Discharge Resistance	RDCHG7	-	100	-	ohm	
Ripple Rejection Ratio	RRM7	-	60	-	dB	VBAT=4.2V+0.2Vpp fR=10kHz Io=50mA, Vo=1.20V BW=20Hz~20kHz
Output Noise Level	VON7	-	60	-	μ Vrms	Io=50mA, Vo=1.20V BW=20Hz~20kHz
Output Capacitor	COUT7	0.47	1.0	-	μ F	Ta=-35~85°C, with LDO's DC bias