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System PMIC for Battery Powered Systems

BD71815AGW

General Description

BD71815AGW is a single-chip power management IC for battery-powered portable devices. The IC integrates 5 buck converters, 8 LDOs, a boost driver for LED, and a 500mA single-cell linear charger. Also included is a Coulomb counter, a real-time clock (RTC), a 32 kHz crystal oscillator and a general-purpose output (GPO).

The IC's buck converters supply power to the application processor as well as system peripherals such as DDR memory, wireless modules, and touch controllers. These regulators maintain high efficiency over a wide range of current loads by supporting both PFM and PWM modes. They also operate at a high switching frequency of 6MHz, which allows the use of smaller and cheaper inductors and capacitors. The regulator supplying the processor core also supports Dynamic Voltage Scaling (DVS).

Features

- 5 buck converters:
  - 3 1000mA buck converters
  - 1 800mA buck converter
  - 1 500mA buck converter
- 3 general-purpose LDOs
  - 2 100mA LDOs
  - 1 50mA LDO
- LDO for DDR Reference Voltage (DVREF)
- LDO for Secure Non-Volatile Storage (SNVS)
- LDO for Low-Power State Retention (LPSR)
- LDO for SD Card with dedicated enable terminal
- LDO for SD Card Interface with dedicated terminal to dynamically change output voltage
- White LED Boost Converter
  -25mA LED Boost Converter
- Single-cell Linear LIB Charger with 30V OVP
  -Selectable charging voltage: 3.72 to 4.34 V
  -Programmable charge current: 100 to 500mA
  -Support for up to 2000mA charge current using external MOSFET
  -DCIN over voltage protection
  -Battery over voltage protection
  -Battery Supplement Mode support
  -Battery Short Circuit Detection
- Voltage Measurement for Thermistor
  -Bias voltage output for External Thermistor
- Embedded Coulomb Counter for Battery Fuel Gauging
  -15-bit ΔΣ-ADC with External Current Sense Resistor (10 mΩ, ±1% or 30mΩ, ±1%)
  -1-sec cycle, 28-bit accumulation
  -Coulomb count while charging/discharging
- Battery Monitoring and Alarm Output
  -Under Voltage Alarm while discharging
  -Over Current Alarm
  -Over/Under Temperature Alarm
  -Programmable thresholds and time durations
- Real Time Clock with 32.768kHz crystal oscillator
  -32.768kHz clock output (Open Drain or CMOS Output Selectable)
- 1 GPO (Open Drain or CMOS Output Selectable)
- Power Control I/O
  -Power On/Off control input
  -Standby Input for switching RUN/SUSPEND State
  -Reset Input to reset hung PMIC
  -Power On Reset output
- 1 LED Indicator
  -Indicate charger status
- I2C interface

Applications

- E-Book reader
- Media players with smart devices, wearables
- Portable Navigation Devices with Home POS, Human Machine Interfaces

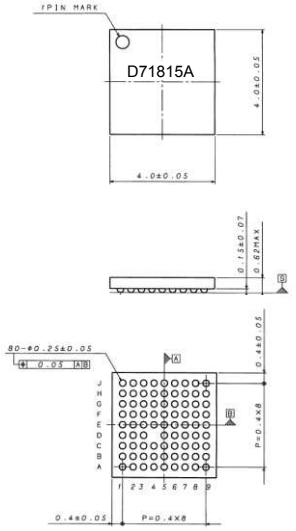
Key Specifications

- Input Voltage Range (DCIN): 3.5V to 28V
- Input Voltage Range (VIN, VSYS): 2.9V to 5.5V
- Input Voltage Range (DVDD): 1.5V to 3.4V
- Off Current: 20 µA (Typ)
  [RTC+ Coulomb counter+ LDO_SNVS only]
- Operating temperature range: -40°C to +85°C

Package

W(Typ) x D(Typ) x H(Max)

UCSP55M4C 4.0mm x 4.0mm x 0.62mm



(Unit :mm)

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Contents

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Typical Application Circuit

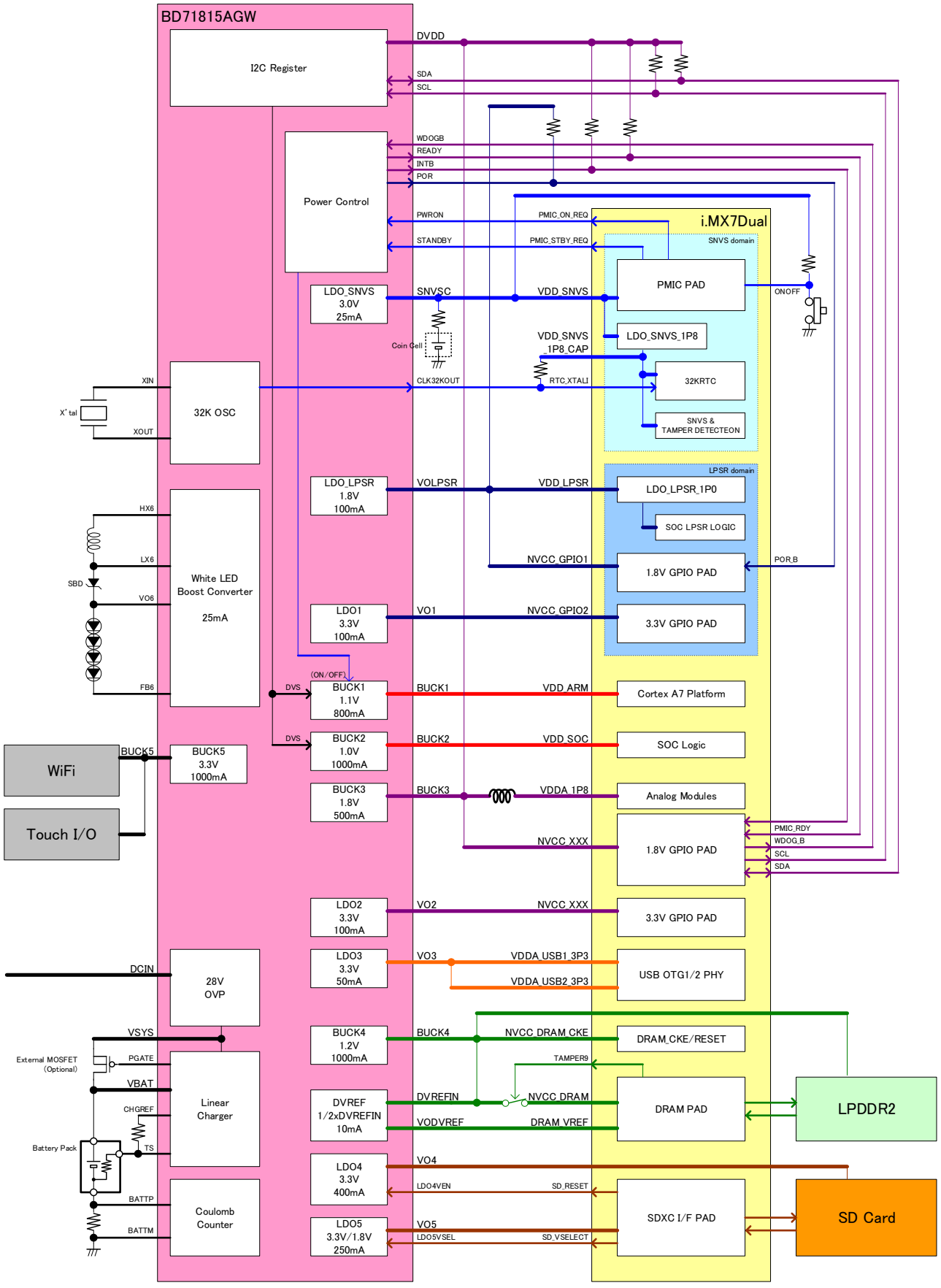

Figure 1. Typical Application (E-Book Reader with i.Mx7D)

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Block Diagram

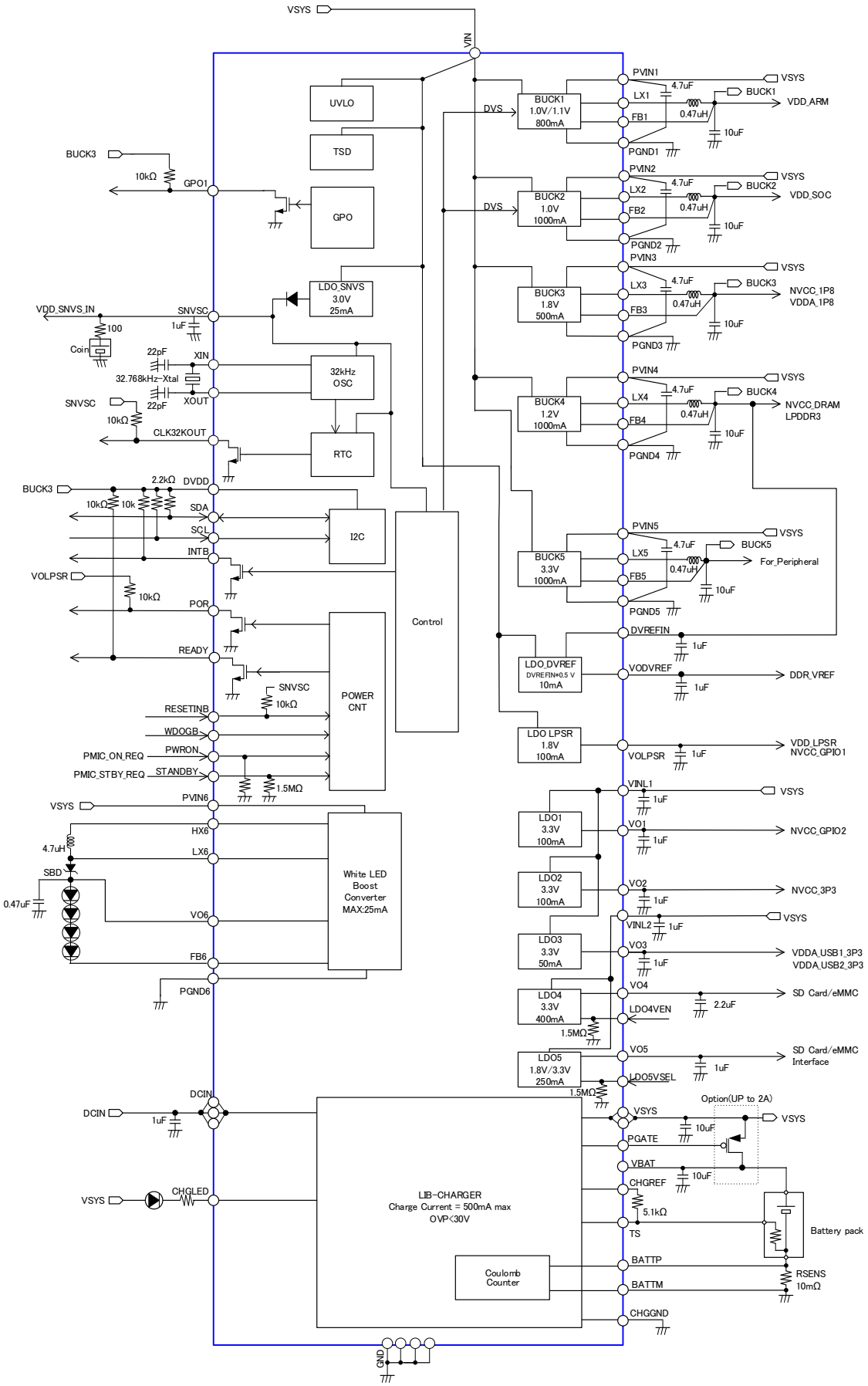

Figure 2. IC Block Diagram

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Pin Configuration

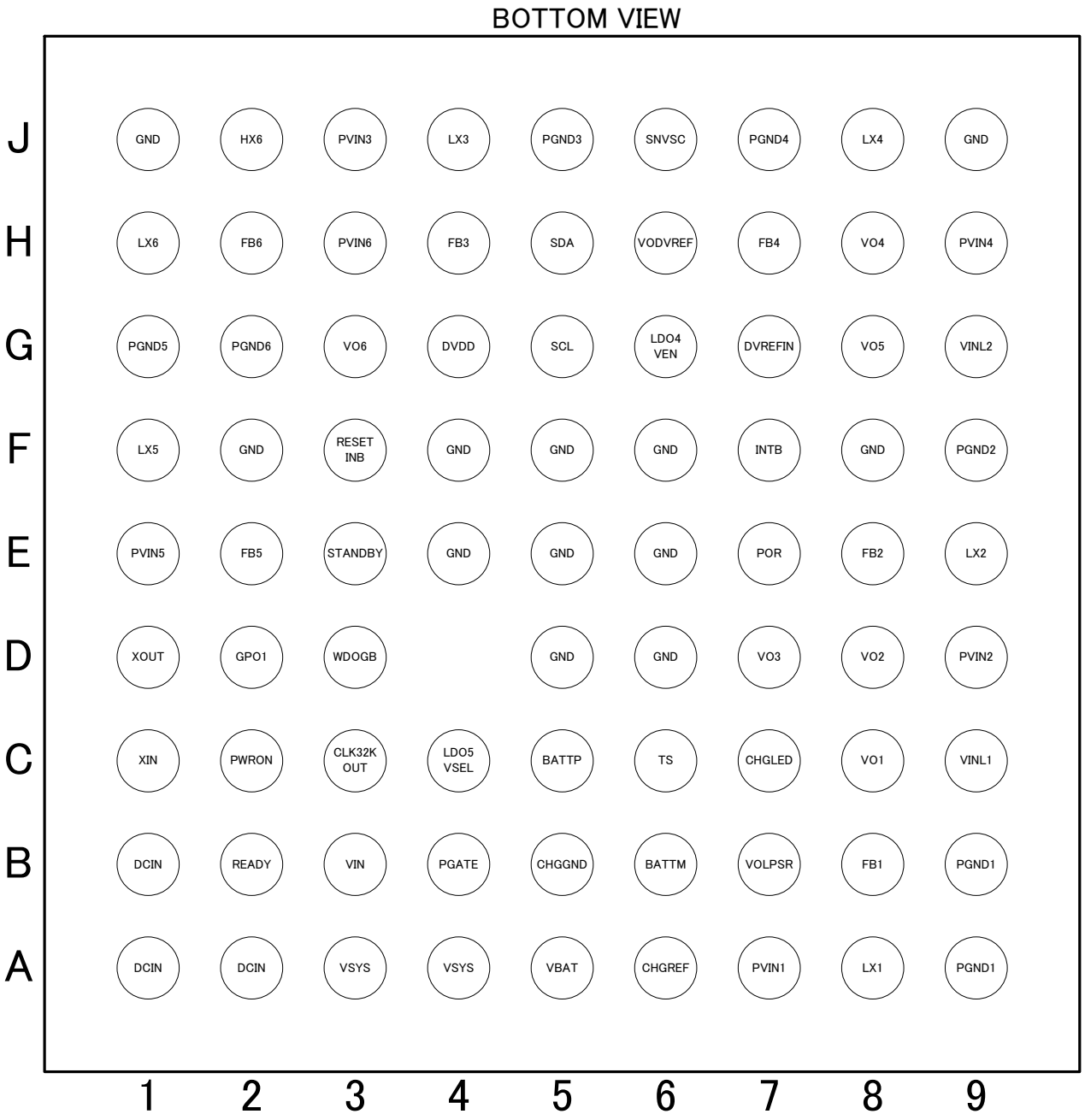

Figure 3. Pin Configuration (Bottom View)

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Pin Descriptions

Table 1. BD71815AGW Pin Descriptions

Ball No.	Block Name	Terminal Name	I/O	Explanation	Internal Pull up/down
A7	BUCK1	PVIN1	I	Input power supply for BUCK1	
A8		LX1	O	Switch node connection for BUCK1	
B8		FB1	I	Output voltage feedback for BUCK1	
E3		STANDBY	I	Standby input signal	Pull down 1.5MΩ to GND
A9		PGND1	-	Power ground for BUCK1	
B9		PGND1	-	Power ground for BUCK1	
D9	BUCK2	PVIN2	I	Input power supply for BUCK2	
E9		LX2	O	Switch node connection for BUCK2	
E8		FB2	I	Output voltage feedback for BUCK2	
F9		PGND2	-	Power ground for BUCK2	
J3	BUCK3	PVIN3	I	Input power supply for BUCK3	
J4		LX3	O	Switch node connection for BUCK3	
H4		FB3	I	Output voltage feedback for BUCK3	
J5		PGND3	-	Power ground for BUCK3	
H9	BUCK4	PVIN4	I	Input power supply for BUCK4	
J8		LX4	O	Switch node connection for BUCK4	
H7		FB4	I	Output voltage feedback for BUCK4	
J7		PGND4	-	Power ground for BUCK4	
E1	BUCK5	PVIN5	I	Input power supply for BUCK5	
F1		LX5	O	Switch node connection for BUCK5	
E2		FB5	I	Output voltage feedback for BUCK5	
G1		PGND5	-	Power ground for BUCK5	
H3	LED Driver	PVIN6	I	Input power supply for BOOST	
J2		HX6	O	Switch node connection for BOOST	
H1		LX6	O	Switch node connection for BOOST	
G3		VO6	O	BOOST output	
H2		FB6	I	Output voltage feedback for BOOST	
G2		PGND6	-	Power ground for BOOST	
B7	LDOLPSR	VOLPSR	O	LDO output for LPSR	
C9	LDO	VINL1	I	LDO input for LDO1, LDO2 and LDO3	
C8		VO1	O	LDO output for LDO1	
D8		VO2	O	LDO output for LDO2	
D7		VO3	O	LDO output for LDO3	
G9		VINL2	I	LDO input for LDO4 and LDO5	
H8		VO4	O	LDO output for LDO4	
G8		VO5	O	LDO output for LDO5	
G6		LDO4VEN	I	LDO4 Enable	Pull down 1.5MΩ to GND
C4		LDO5VSEL	I	LDO5 Output Voltage select	Pull down 1.5MΩ to GND
G7	DVREF	DVREFIN	I	LDO input for DVREF/CLK32KOUT H-level(note3)	
H6		VODVREF	O	LDO output for DVREF	
J6	SNVS	SNVSC	O	LDO output for SNVS (requires capasitor)	

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Table 2. BD71815AGW Pin Descriptions (continued)

Ball No.	Block Name	Terminal Name	I/O	Explanation	Pull up/down
G4	I2C	DVDD	I	Power Supply for I2C interface	
H5		SDA	I/O	I2C data line (Open drain)	note1
G5		SCL	I	I2C clock	note1
C1	RTC	XIN	I	32.768kHz-Xtal input	
D1		XOUT	O	32.768kHz-Xtal output	
C3		CLK32KOUT	O	32.768kHz clock output (Open drain/CMOS)	
C2	POWRCNT	PWRON	I	Power on/off control input	Pull down 1.5MΩ to GND
F3		RESETINB	I	Reset input to shutdown this device	Pull up 10kΩ to SNVSC
E7		POR	O	Power on reset output (Open drain)	note2
F7		INTB	O	Interrupt signal to processor (Open drain)	note2
D3		WDOGB	I	Watchdog input from processor	Pull up 1.5MΩ to VIN
B2		READY	O	PMIC ready output	note2
A1	OVP	DCIN	I	DCIN input	
A2		DCIN	I	DCIN input	
B1		DCIN	I	DCIN input	
A3		VSYS	O	System supply output	
A4		VSYS	O	System supply output	
A5	CHARGER	VBAT	I/O	Charger output / Battery input	
B4		PGATE	O	External power MOS gate control output	
C6		TS	I	Battery pack thermistor voltate sense	
A6		CHGREF	O	Internal reference for the Lib charger	
C5		BATTP	I	Current sense input (battery pack side)	
B6		BATTM	I	Current sense input (ground side)	
B5		CHGGND	-	Ground for Charger	
C7		CHGLED	O	Charging status indication output (Open drain)	
D2	GPO	GPO1	O	Output for general purpose	
B3	Power/GND	VIN	I	Input power supply	
J1		GND	-	Signal ground	
J9		GND	-	Signal ground	
F2		GND	-	Signal ground	
F8		GND	-	Signal ground	
D5		GND	-	Signal ground	
D6		GND	-	Signal ground	
E4		GND	-	Signal ground (for reduce Thermal resistance)	
E5		GND	-	Signal ground (for reduce Thermal resistance)	
E6		GND	-	Signal ground (for reduce Thermal resistance)	
F4		GND	-	Signal ground (for reduce Thermal resistance)	
F5		GND	-	Signal ground (for reduce Thermal resistance)	
F6		GND	-	Signal ground (for reduce Thermal resistance)	

note1 : SDA and SCL need pull up resistance to DVDD.

note2 : POR, INTB and READY need pull up resistance.

note3 : When CLK32KOUT is selected to CMOS output mode.

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PCB Layout Recommendations

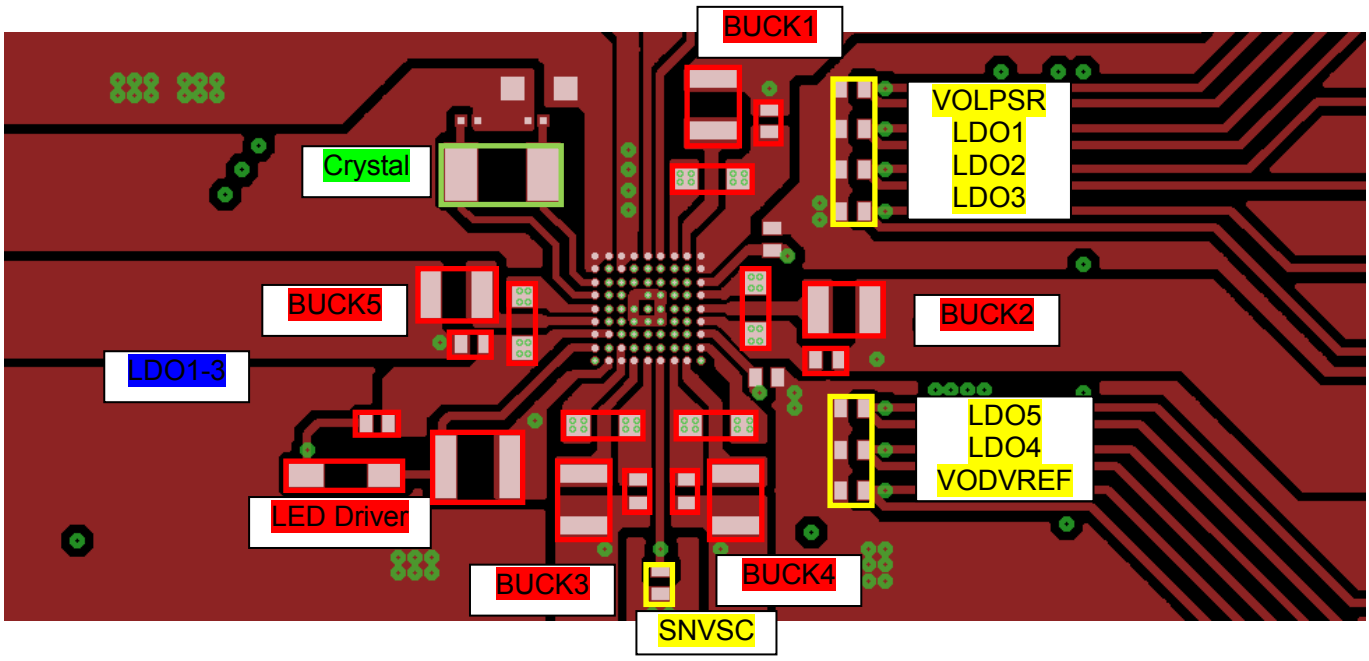

Figure 4. PCB Layout Recommendations (Top View)

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Description of Blocks

1. High Efficiency Buck Converters (BUCK1 – 5) and LDOs

BD71815AGW step down converters operate at a fixed frequency of 6MHz. These converters employ Pulse Width Modulation (PWM) under moderate to heavy load and enter Power Save Mode when used under light load. In Power Save Mode, the step down converters operate using Pulse Frequency Modulation (PFM).

Table 3. BD71815AGW Output Power Rails

BD71815AGW Function	i.MX7 Dual Usage example	Power Supply	Initial Output Voltage	Load max	Adjustable range
BUCK1	VDD_ARM	PVIN1	1.1V	800mA	0.8 to 2.000V (25mV step) [DVS]
BUCK2	VDD_SOC	PVIN2	1.0V	1000mA	0.8 to 2.000V (25mV step) [DVS]
BUCK3	NVCC_1P8 / VDDA_1P8	PVIN3	1.8V	500mA	1.2V to 2.7V (50mV step)
BUCK4	NVCC_DRAM / LPDDR3	PVIN4	1.2V	1000mA	1.1 to 1.85V (25mV step)
BUCK5	Peripheral	PVIN5	3.3V	1000mA	1.8 to 3.3V (50mV step)
LDO1	NVCC_GPIO2	VINL1	3.3V	100mA	0.8 to 3.3V (50mV step)
LDO2	NVCC_3P3	VINL1	3.3V	100mA	0.8 to 3.3V (50mV step)
LDO3	VDDA_USB1_3P3 / VDDA_USB2_3P3	VINL1	3.3V	50mA	0.8 to 3.3V (50mV step)
LDO4	SD Card / eMMC	VINL2	3.3V	400mA	0.8V to 3.3V(50mV step)
LDO5	SD Card / eMMC	VINL2	1.8V / 3.3V	250mA	0.8V to 3.3V(50mV step)
VODVREF	LPDDR3	VIN	0.5*DVREFIN	10mA	0.55 to 0.925V (DVREFIN= BUCK4)
SNVSC	VDD_SNVS	VIN	3.0V	25mA	Fixed
LDO LPSR	VDD_LPSR / NVCC_GPIO1	VIN	1.8V	100mA	Fixed
White LED Driver	-	VIN	up to 18V	25mA	10uA to 25mA
I2C	-	DVDD	-	-	-
RTC	-	SNVS	-	-	-
Charger	-	VSYS	-	-	-
Coulomb Counter	-	SNVS	-	-	-
SNVS/VSYS Voltage monitor	-	VIN	-	-	-

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Table 4. Voltage Identification Code for BD71815AGW Output Power Rails

#	I2C Register	BUCK1	BUCK2	BUCK3	BUCK4	BUCK5	LDO1	LDO2	LDO3	LDO4	LDO5
0	00 0000	0.800	0.800	1.200	1.100	1.800	0.80	0.80	0.80	0.80	0.80
1	00 0001	0.825	0.825	1.250	1.125	1.850	0.85	0.85	0.85	0.85	0.85
2	00 0010	0.850	0.850	1.300	1.150	1.900	0.90	0.90	0.90	0.90	0.90
3	00 0011	0.875	0.875	1.350	1.175	1.950	0.95	0.95	0.95	0.95	0.95
4	00 0100	0.900	0.900	1.400	1.200(note1)	2.000	1.00	1.00	1.00	1.00	1.00
5	00 0101	0.925	0.925	1.450	1.225	2.050	1.05	1.05	1.05	1.05	1.05
6	00 0110	0.950	0.950	1.500	1.250	2.100	1.10	1.10	1.10	1.10	1.10
7	00 0111	0.975	0.975	1.550	1.275	2.150	1.15	1.15	1.15	1.15	1.15
8	00 1000	1.000	1.000(note1)	1.600	1.300	2.200	1.20	1.20	1.20	1.20	1.20
9	00 1001	1.025	1.025	1.650	1.325	2.250	1.25	1.25	1.25	1.25	1.25
10	00 1010	1.050	1.050	1.700	1.350	2.300	1.30	1.30	1.30	1.30	1.30
11	00 1011	1.075	1.075	1.750	1.375	2.350	1.35	1.35	1.35	1.35	1.35
12	00 1100	1.100(note1)	1.100	1.800(note1)	1.400	2.400	1.40	1.40	1.40	1.40	1.40
13	00 1101	1.125	1.125	1.850	1.425	2.450	1.45	1.45	1.45	1.45	1.45
14	00 1110	1.150	1.150	1.900	1.450	2.500	1.50	1.50	1.50	1.50	1.50
15	00 1111	1.175	1.175	1.950	1.475	2.550	1.55	1.55	1.55	1.55	1.55
16	01 0000	1.200	1.200	2.000	1.500	2.600	1.60	1.60	1.60	1.60	1.60
17	01 0001	1.225	1.225	2.050	1.525	2.650	1.65	1.65	1.65	1.65	1.65
18	01 0010	1.250	1.250	2.100	1.550	2.700	1.70	1.70	1.70	1.70	1.70
19	01 0011	1.275	1.275	2.150	1.575	2.750	1.75	1.75	1.75	1.75	1.75
20	01 0100	1.300	1.300	2.200	1.600	2.800	1.80	1.80	1.80	1.80	1.80(note1)
21	01 0101	1.325	1.325	2.250	1.625	2.850	1.85	1.85	1.85	1.85	1.85
22	01 0110	1.350	1.350	2.300	1.650	2.900	1.90	1.90	1.90	1.90	1.90
23	01 0111	1.375	1.375	2.350	1.675	2.950	1.95	1.95	1.95	1.95	1.95
24	01 1000	1.400	1.400	2.400	1.700	3.000	2.00	2.00	2.00	2.00	2.00
25	01 1001	1.425	1.425	2.450	1.725	3.050	2.05	2.05	2.05	2.05	2.05
26	01 1010	1.450	1.450	2.500	1.750	3.100	2.10	2.10	2.10	2.10	2.10
27	01 1011	1.475	1.475	2.550	1.775	3.150	2.15	2.15	2.15	2.15	2.15
28	01 1100	1.500	1.500	2.600	1.800	3.200	2.20	2.20	2.20	2.20	2.20
29	01 1101	1.525	1.525	2.650	1.825	3.250	2.25	2.25	2.25	2.25	2.25
30	01 1110	1.550	1.550	2.700	1.850	3.300(note1)	2.30	2.30	2.30	2.30	2.30
31	01 1111	1.575	1.575				2.35	2.35	2.35	2.35	2.35
32	10 0000	1.600	1.600				2.40	2.40	2.40	2.40	2.40
33	10 0001	1.625	1.625				2.45	2.45	2.45	2.45	2.45
34	10 0010	1.650	1.650				2.50	2.50	2.50	2.50	2.50
35	10 0011	1.675	1.675				2.55	2.55	2.55	2.55	2.55
36	10 0100	1.700	1.700				2.60	2.60	2.60	2.60	2.60
37	10 0101	1.725	1.725				2.65	2.65	2.65	2.65	2.65
38	10 0110	1.750	1.750				2.70	2.70	2.70	2.70	2.70
39	10 0111	1.775	1.775				2.75	2.75	2.75	2.75	2.75
40	10 1000	1.800	1.800				2.80	2.80	2.80	2.80	2.80
41	10 1001	1.825	1.825				2.85	2.85	2.85	2.85	2.85
42	10 1010	1.850	1.850				2.90	2.90	2.90	2.90	2.90
43	10 1011	1.875	1.875				2.95	2.95	2.95	2.95	2.95
44	10 1100	1.900	1.900				3.00	3.00	3.00	3.00	3.00
45	10 1101	1.925	1.925				3.05	3.05	3.05	3.05	3.05
46	10 1110	1.950	1.950				3.10	3.10	3.10	3.10	3.10
47	10 1111	1.975	1.975				3.15	3.15	3.15	3.15	3.15
48	11 0000	2.000	2.000				3.20	3.20	3.20	3.20	3.20
49	11 0001						3.25	3.25	3.25	3.25	3.25
50	11 0010						3.30(note1)	3.30(note1)	3.30(note1)	3.30(note1)	3.30(note1)
51	11 0011										
52	11 0100										
53	11 0101										
54	11 0110										
55	11 0111										
56	11 1000										
57	11 1001										
58	11 1010										
59	11 1011										
60	11 1100										
61	11 1101										
62	11 1110										
63	11 1111										
Voltage step		25mV	25mV	50mV	25mV	50mV	50mV	50mV	50mV	50mV	50mV

(note1) Default output voltage setting

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2. Power ON/OFF Sequence

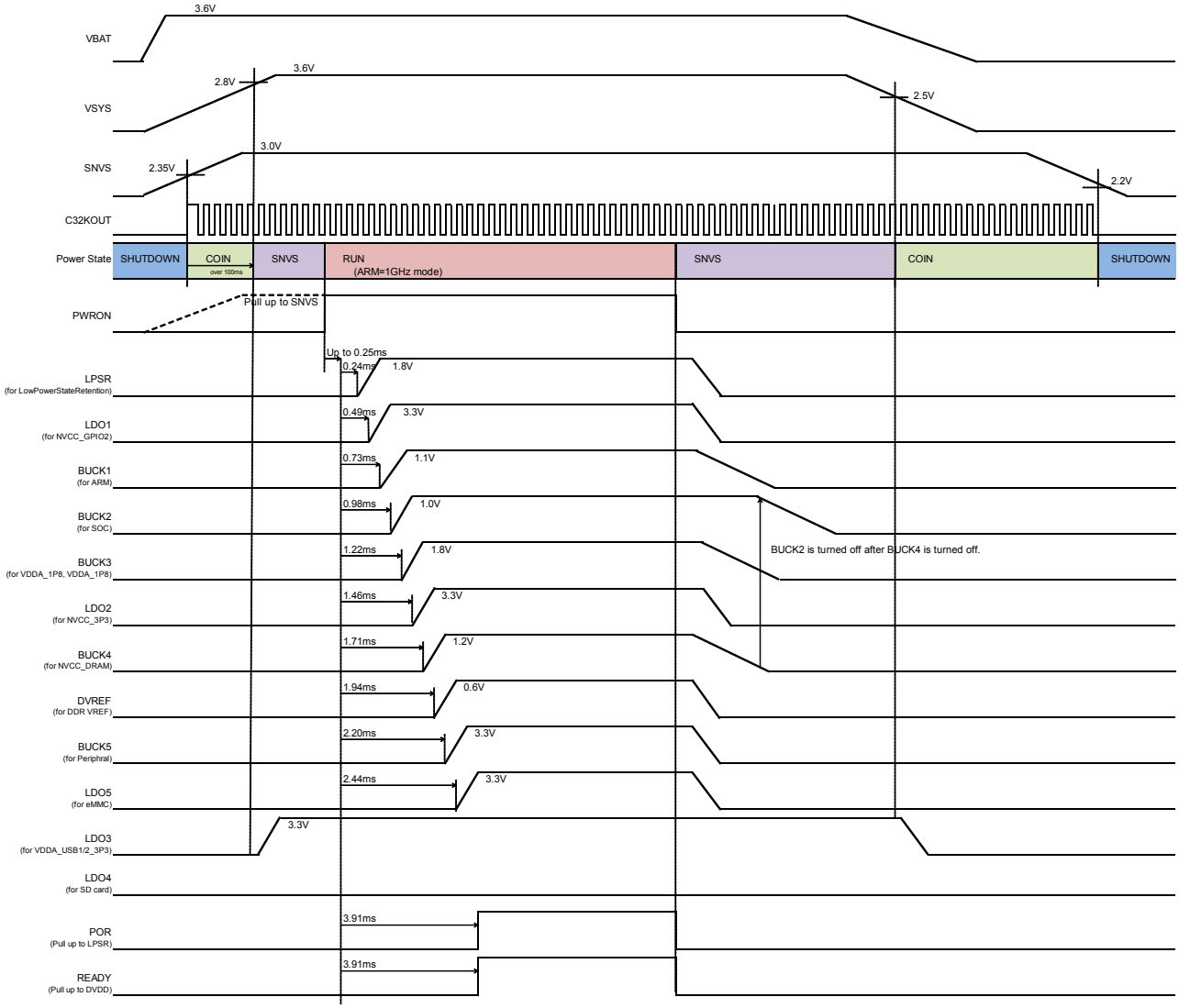

Figure 5. Power ON/OFF Sequence

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3. States of Operation

BD71815AGW has six power states: RUN, SUSPEND, LPSR, SNVS, Coin, and Shutdown. Figure 6 shows the state transition diagram along with the conditions to enter and exit each state.

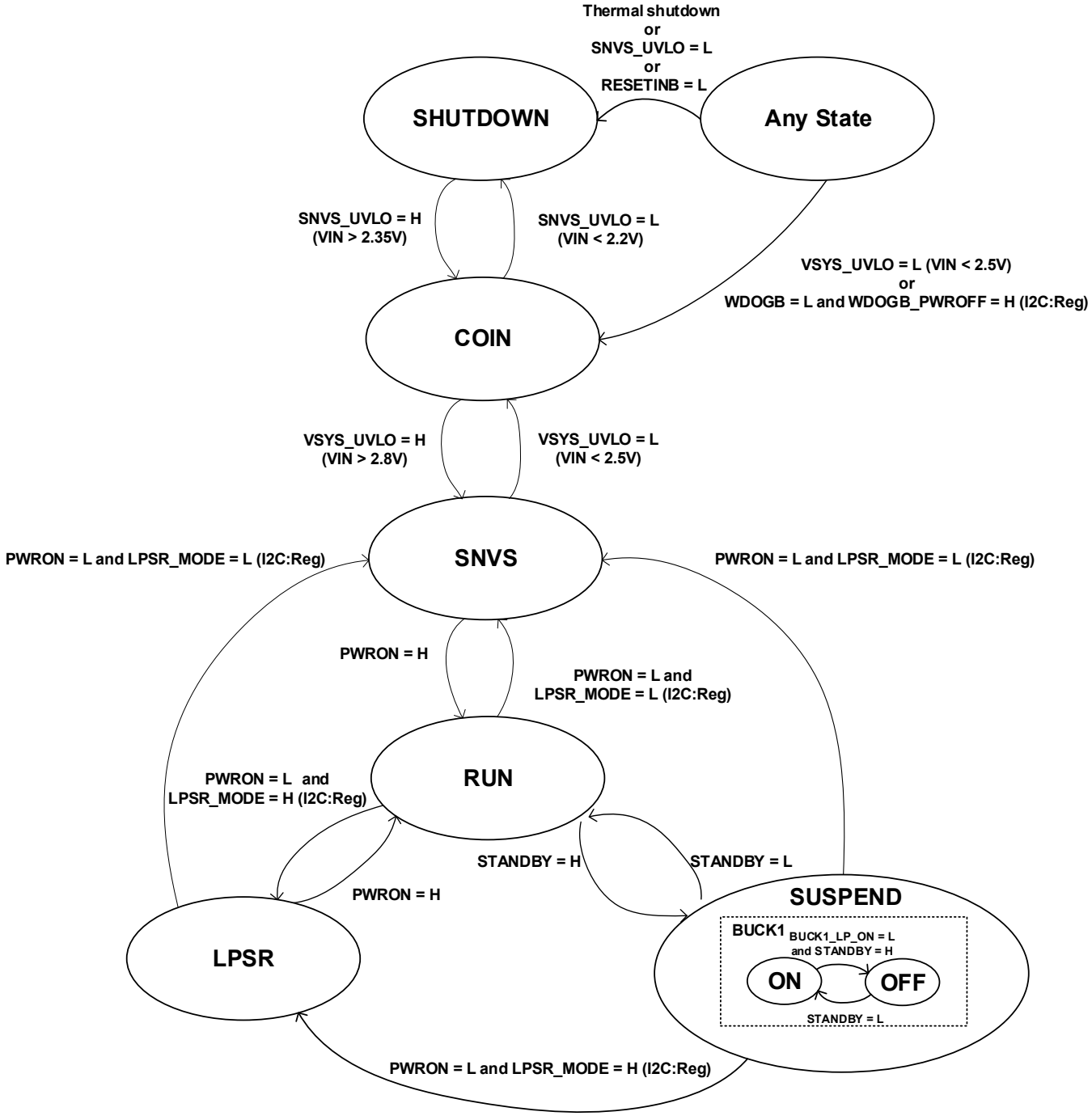

Figure 6. Power States Transitions

Description of states is provided in the following section. I2C Control is not possible in Shutdown state. However, the interrupt signal INTB is active during RUN and SUSPEND states.

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Table 5. Voltage Rails ON/OFF for Respective Power States

BD71815AGW Function	Power Mode						Output Control	
	Shutdown	Coin	SNVS	LPSR	RUN	SUSPEND	ON/OFF	Sequence order
BUCK1	OFF	OFF	OFF	OFF	Auto	Auto	State or I2C register	2
BUCK2	OFF	OFF	OFF	OFF	Auto	Auto	State or I2C register	3
BUCK3	OFF	OFF	OFF	OFF	Auto	Auto	State or I2C register	4
BUCK4	OFF	OFF	OFF	OFF	Auto	Auto	State or I2C register	6
BUCK5	OFF	OFF	OFF	OFF	Auto	Auto	State or I2C register	8
LDO1	OFF	OFF	OFF	ON	ON	ON	State or I2C register	1
LDO2	OFF	OFF	OFF	OFF	ON	ON	State or I2C register	5
LDO3	OFF	OFF	ON	ON	ON	ON	State or I2C register	9
LDO4	OFF	OFF	OFF	OFF/ON	OFF/ON	OFF/ON	LDO4VEN	9
LDO5	OFF	OFF	OFF	OFF	ON	ON	State or I2C register	9
VODVREF	OFF	OFF	OFF	OFF	ON	ON	State or I2C register	7
SNVSC	OFF	ON	ON	ON	ON	ON	State or I2C register	-
LDO LPSR	OFF	OFF	OFF	ON	ON	ON	State or I2C register	0
White LED Driver	OFF	OFF	OFF	OFF	OFF	OFF	State or I2C register	-
I2C	Reset	Disable	Disable	Disable	Enable	Enable	State	-
RTC	OFF	ON	ON	ON	ON	ON	State	-
Charger	OFF	OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	DCIN	-
Coulomb Counter	OFF	OFF	ON	ON	ON	ON	State	-
SNVS/VSYS Voltage monitor	ON	ON	ON	ON	ON	ON	-	-

(Note) Auto : PWM/PFM mode change automatically depending on the load current

(1) Power Control States

(a) Shutdown State

BD71815AGW enters Shutdown State when SNVS falls below 2.2V or when BD71815AGW encounters a thermal shutdown event. In case of system hang-up, setting RESETINB to LOW will cause the IC to shut down. Only the SNVS and VSYS voltage measurement block (UVLO) is powered during Shutdown state. Data in all registers are reset to their initial settings. To exit Shutdown state, SNVS must exceed 2.35V.

(b) Coin State

BD71815AGW enters Coin State when SNVS exceeds 2.35V or VSYS falls below 2.5V. BD71815AGW also enters Coin State when only the coin battery is connected to SNVSC, or when WDOGB is asserted low. BD71815AGW starts the Off Sequence in this case.

UVLO, RTC, Battery measurement (Coulomb Counter), and SNVS blocks are powered in Coin State. All BUCK blocks and other LDOs are powered off. Registers cannot be accessed when BD71815AGW enters this state, but register data is retained.

(c) SNVS State

BD71815AGW enters SNVS State if PWRON is asserted low while LPSR_MODE registers are set low. SNVS State can also be accessed from Coin State when VSYS exceeds 2.8V.

In SNVS State, BUCKs and LDOs which have the SNVS_ON register set High are turned ON. Charger is also started when DCIN input is supplied with the appropriate voltage. These blocks are turned on in addition to blocks powered in Coin State.

(d) LPSR State

BD71815AGW enters LPSR state if PWRON is asserted Low while LPSR_MODE registers are set high.

In LPSR State, BUCKs and LDOs which have the LPSR_ON register set high are turned ON.

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(d) RUN State

BD71815AGW enters RUN state when PWRON is asserted High. POR is negated in this state.
In RUN State, BUCKs and LDOs which have the RUN_ON register set High are turned ON. I2C registers can be accessed in this state.

(e) SUSPEND State

BD71815AGW enters SUSPEND State from RUN State when STANDBY is asserted high.
In SUSPEND State, BUCKs and LDOs which have the LP_ON register set low are turned OFF. I2C registers can be accessed in this state.

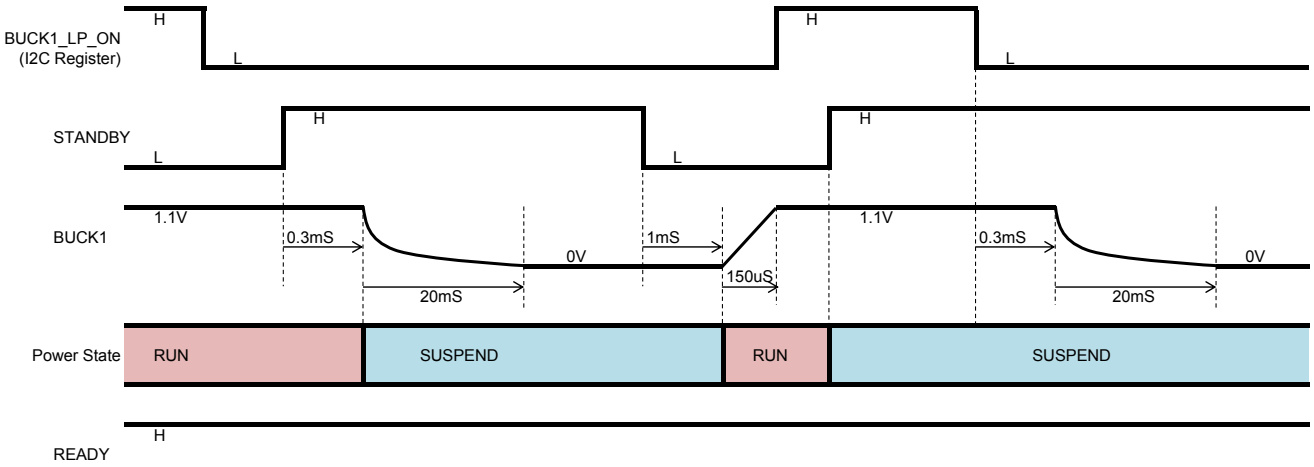

Figure 7 – SUSPEND State Control Timing Diagram

4. Dynamic Voltage Scaling (DVS) Control

BUCK1 and BUCK2 support Dynamic Voltage Scaling (DVS). BUCK1_DVSSEL and BUCK2_DVSSEL registers control the output voltage of BUCK1 and BUCK2, respectively. BUCK#_H controls the output voltage for when BUCK#_DVSSEL is set high, and BUCK#_L for when BUCK#_DVSSEL is set low. Slew rate is also set via the BUCK#_RAMPRATE register.

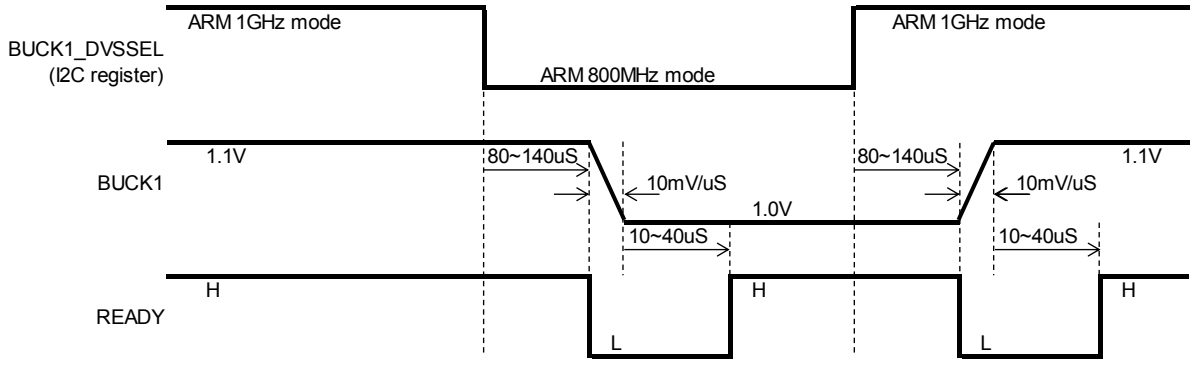

Figure 8 - DVS Control Timing Diagram

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5. LDO4 and LDO5 Control (for SD Card)

LDO4 and LDO5 support High Speed SD Card and SD Card Interface power rails, respectively.

LDO4 is turned on and off by LDO4VEN. This function is for High Speed SD Card Reset operation.

LDO5 supports Dynamic Voltage Scaling (DVS). LDO5_H register controls the output voltage for when LDO5VSEL pin is set high, and LDO5_L register for when LDO5VSEL pin is set low. This function supplies dynamically changing output voltages for Normal to High Speed operation.

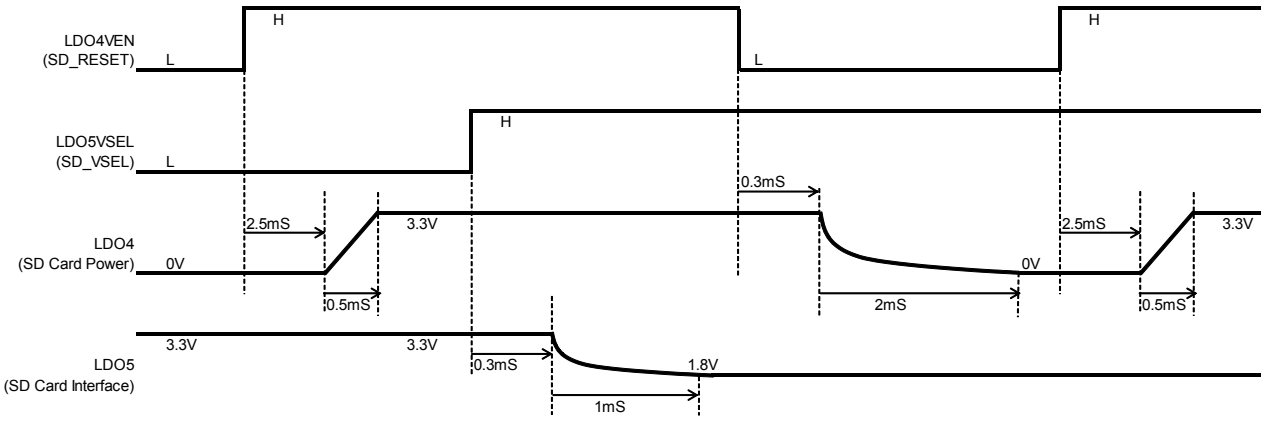

Figure 9 – SD Card Interface Control Timing Diagram

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6. Real Time Clock (RTC) Block

Features

- RTC is driven by a 32.768 kHz oscillator and provides alarm and timekeeping functions to the nearest second.
- Time information is provided in seconds, minutes, and hours.
- Calendar information is provided in day, month, year, and day of the week.
- Alarm interrupt is sent at the time and day programmed into registers.
- Leap year compensation up to 2099
- Selectable 12-hour and 24-hour modes
- RTC calibration support
- Oscillator failure detection

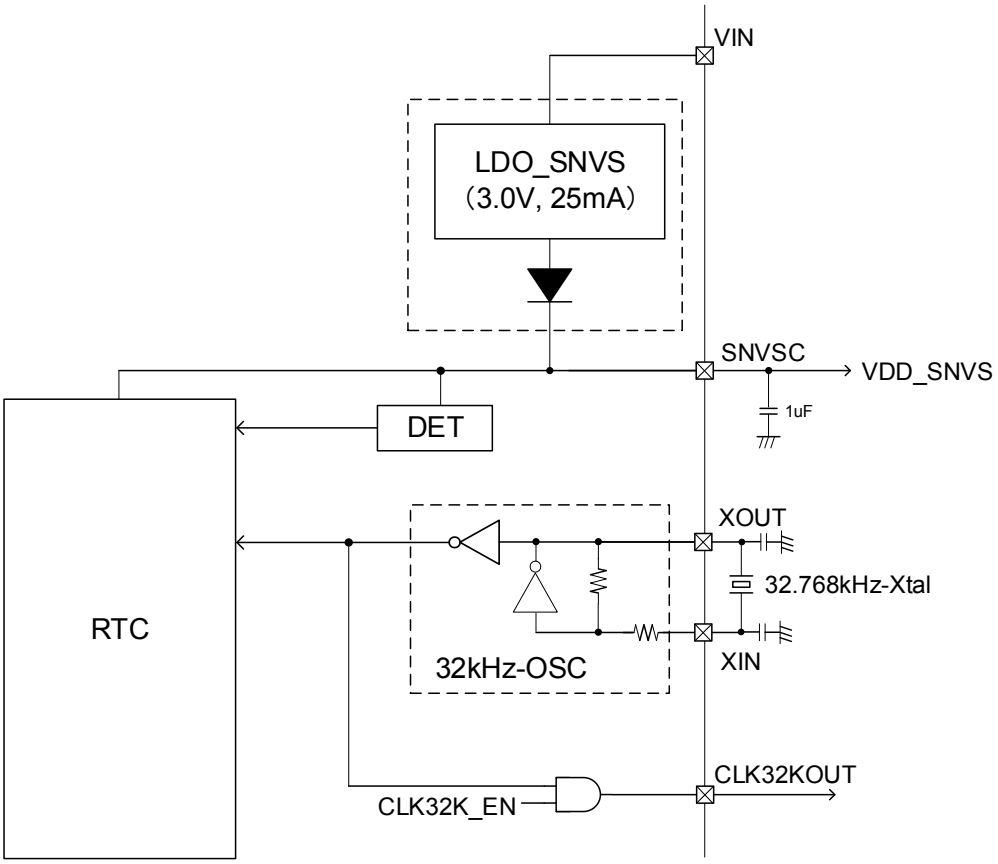

Figure 10. RTC Block Diagram

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(1) Oscillation Adjustment

The oscillation adjustment circuit can be used to correct a time count gain or loss with high precision.
This is done by varying the number of 1-second clock pulses once every 20 or 60 seconds.
When DEV bit in the TRIM Register is set to "0", the Oscillation Adjustment Circuit varies the number of 1-second clock pulses once every 20 seconds. When the DEV bit in the TRIM Register is set to "1", the Oscillation Adjustment Circuit varies the number of 1-second clock pulses once every 60 seconds.
The Oscillation Adjustment Circuit can be disabled by writing the settings "*,0,0,0,0,0,*" ("*" represents "0" or "1") to the TRIM[6:0] bits of the TRIM Register. Conversely, when such oscillation adjustment is to be made, an appropriate oscillation adjustment value can be calculated using the equation below.

(a) When oscillation frequency is higher than target frequency

When setting DEV bit to 0:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency} + 0.1)}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$
$$\approx (\text{Oscillation frequency - Target Frequency}) \times 10 + 1$$

When setting DEV bit to 1:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency} + 0.0333)}{\text{Oscillation frequency} \times 1.017 \times 10^{-6}}$$
$$\approx (\text{Oscillation frequency - Target Frequency}) \times 30 + 1$$

Oscillation frequency: Frequency of clock pulse output from CLK32KOUT pin
Target frequency: Desired frequency to be set
Generally, a 32.768kHz quartz crystal unit has temperature characteristics that support the highest oscillation frequency at normal temperature. Consequently, the quartz crystal unit is recommended to have target frequency settings ranging from 32.768 to 32.76810 kHz (+3.05ppm relative to 32.768kHz).
Oscillation adjustment value: Value that is to be written to the TRIM[6:0] bits of the TRIM register
This value is represented in 7-bit coded decimal notation.

(b) When oscillation frequency is equal to target frequency

Oscillation adjustment value = 0, +1, -64, or -63.

(c) When oscillation frequency is lower than target frequency

When setting DEV bit to 0:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency})}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$
$$\approx (\text{Oscillation frequency - Target Frequency}) \times 10$$

When setting DEV bit to 1:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency})}{\text{Oscillation frequency} \times 1.017 \times 10^{-6}}$$
$$\approx (\text{Oscillation frequency - Target Frequency}) \times 30$$

Sample oscillation adjustment value calculations follow.

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(ex.A) For an oscillation frequency = 32768.85Hz and a target frequency = 32768.05Hz

When setting DEV bit to 0:

$$\begin{aligned}\text{Oscillation adjustment value} &= \frac{32768.85 - 32768.05 + 0.1}{32768.85 \times 3.051 \times 10^{-6}} \\ &\approx (32768.85 - 32768.05) \times 10 + 1 \\ &= 9\end{aligned}$$

In this instance, write the settings "00001001" in the TRIM register. Thus, an appropriate oscillation adjustment value in the presence of any time count gain represents a distance from 01h.

When setting DEV bit to 1:

$$\begin{aligned}\text{Oscillation adjustment value} &= \frac{32768.85 - 32768.05 + 0.0333}{32768.85 \times 1.017 \times 10^{-6}} \\ &\approx (32768.85 - 32768.05) \times 30 + 1 \\ &= 25\end{aligned}$$

In this instance, write the settings "10011001" in the TRIM register.

(ex.B) For an oscillation frequency = 32762.22Hz and a target frequency = 32768.05Hz

When setting DEV bit to 0:

$$\begin{aligned}\text{Oscillation adjustment value} &= \frac{32762.22 - 32768.05}{32762.22 \times 3.051 \times 10^{-6}} \\ &\approx (32762.22 - 32768.05) \times 10 \\ &= -58\end{aligned}$$

To represent an oscillation adjustment value of -58 in 7bit coded decimal notation, subtract 58 (3Ah) from 128 (80h) to obtain 46h. In this instance, write the settings of "01000110" in the TRIM register. Thus, an appropriate oscillation adjustment value in the presence of any time count loss represents a distance from 80h.

When setting DEV bit to 1:

$$\begin{aligned}\text{Oscillation adjustment value} &= \frac{32762.22 - 32768.05}{32762.22 \times 1.017 \times 10^{-6}} \\ &\approx (32762.22 - 32768.05) \times 30 \\ &= -175\end{aligned}$$

Oscillation adjustment value can be set from -62 to 63. Then, in this case, Oscillation adjustment value is out of range.

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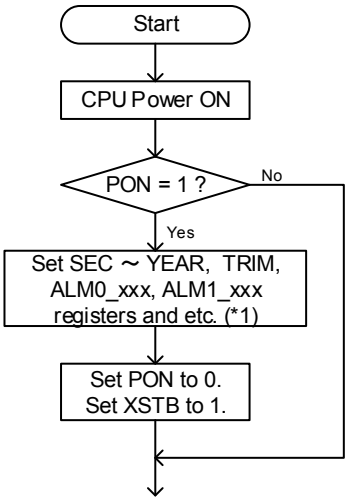
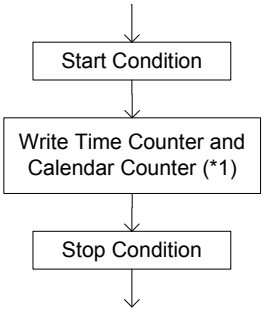
(3) Typical software-based operation

Initialization at Power-on



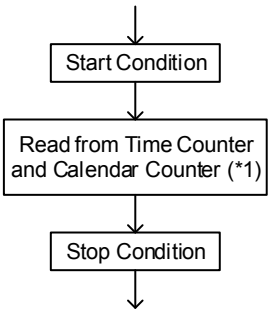
*1) This step involves ordinary initialization including, but not limited to, the Oscillation Adjustment Register and interrupt cycle settings.

Writing Time and Calendar Data



*1) It is recommended to also modify the sec register when one writes to the min~year registers.
When the seconds digit goes up while accessing I2C, the clock could assume an unpredictable value.
Writing to the sec register prevents the above behavior because less than 1Hz counter is cleared.

Reading Time and Calendar Data



*1) When reading clock and calendar counters, do not insert Stop Condition.

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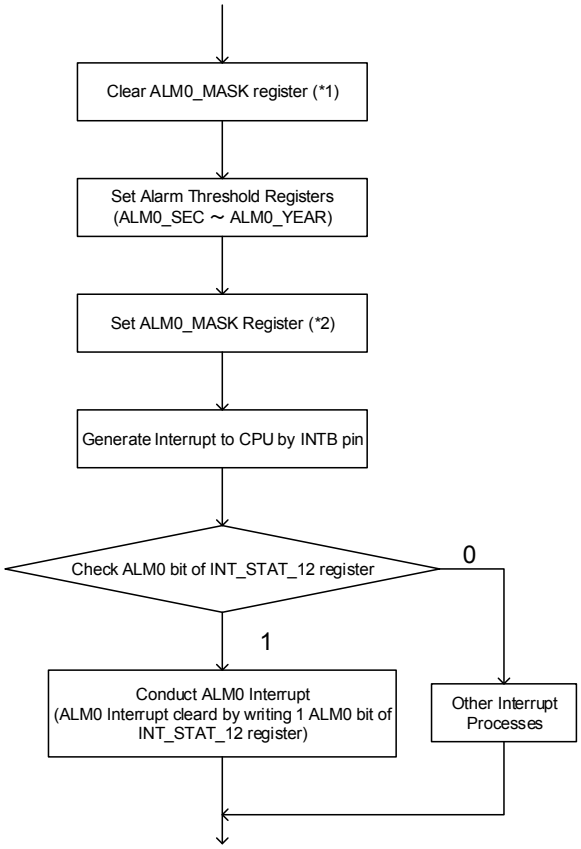
ALARM0 Interrupt Process



*1) This step is intended to disable the alarm interrupt circuit once by clearing ALM0_MASK register, in anticipation of a coincidental match between current time and preset alarm time as the alarm interrupt function is set.

*2) This step is intended to enable the alarm interrupt function after completion of all alarm interrupt settings.

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7. Over Voltage Protection (OVP) Block

Features

- Single-input for the battery charger source: DCIN
- 30V over voltage protection for DCIN input.

8. Battery Charger Block

Features

- Supports battery insertion and removal detection
- JEITA-compliant Battery Charging Profile with thermal control of charging current and voltage settings. This is achieved by measuring the temperature of an external thermistor (The Initial setting of BD71815AGW is adjusted to TDK NTCG163JF103FT1S).
- Supports battery supplement mode
- Automatic or manual (software) control of Watch Dog Timer while Pre–charging and Fast-charging
- Charger statuses or Error conditions are indicated on CHGLED output (for LED lighting)

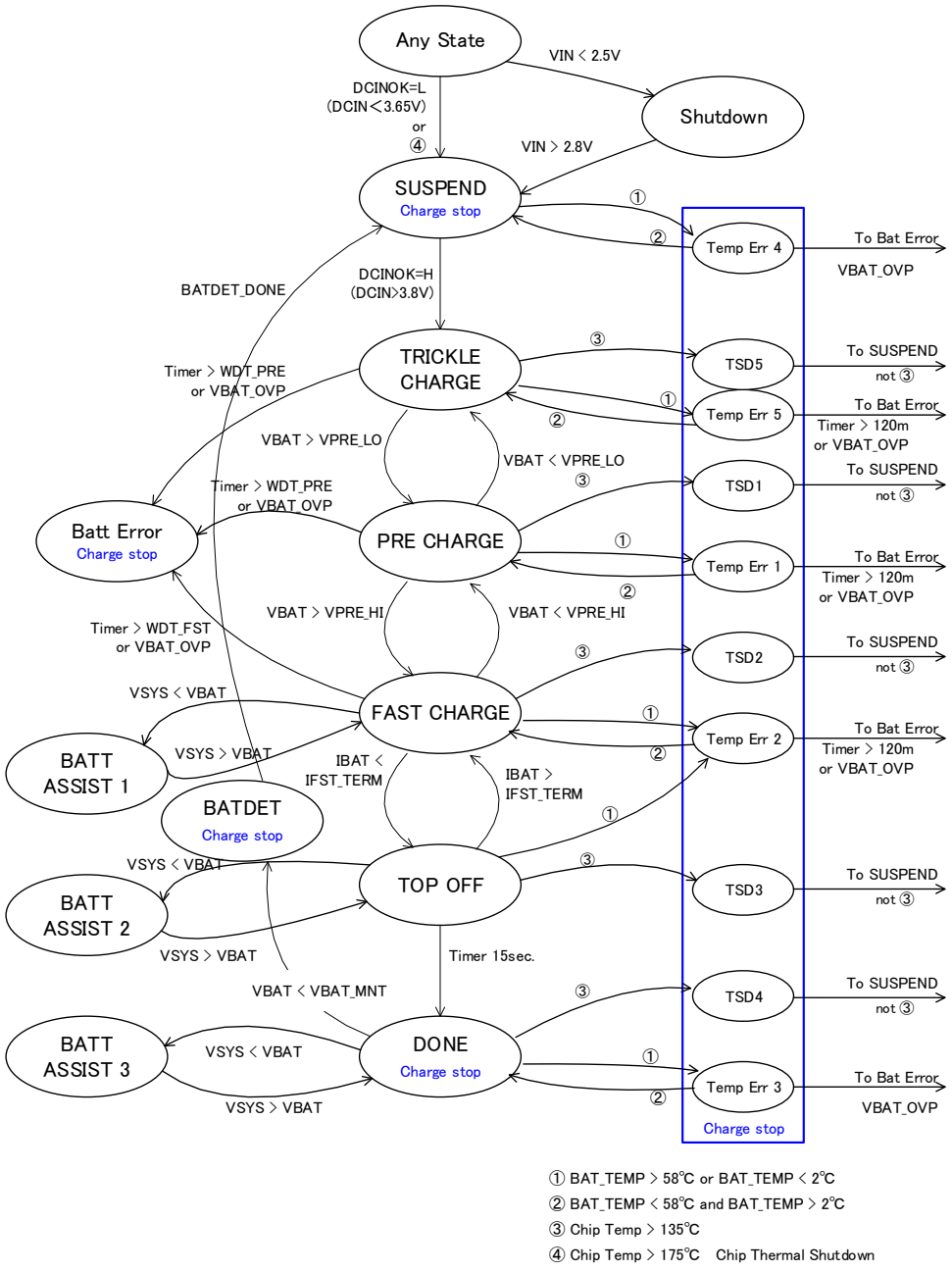

Figure 11. State Diagram of Battery Charger

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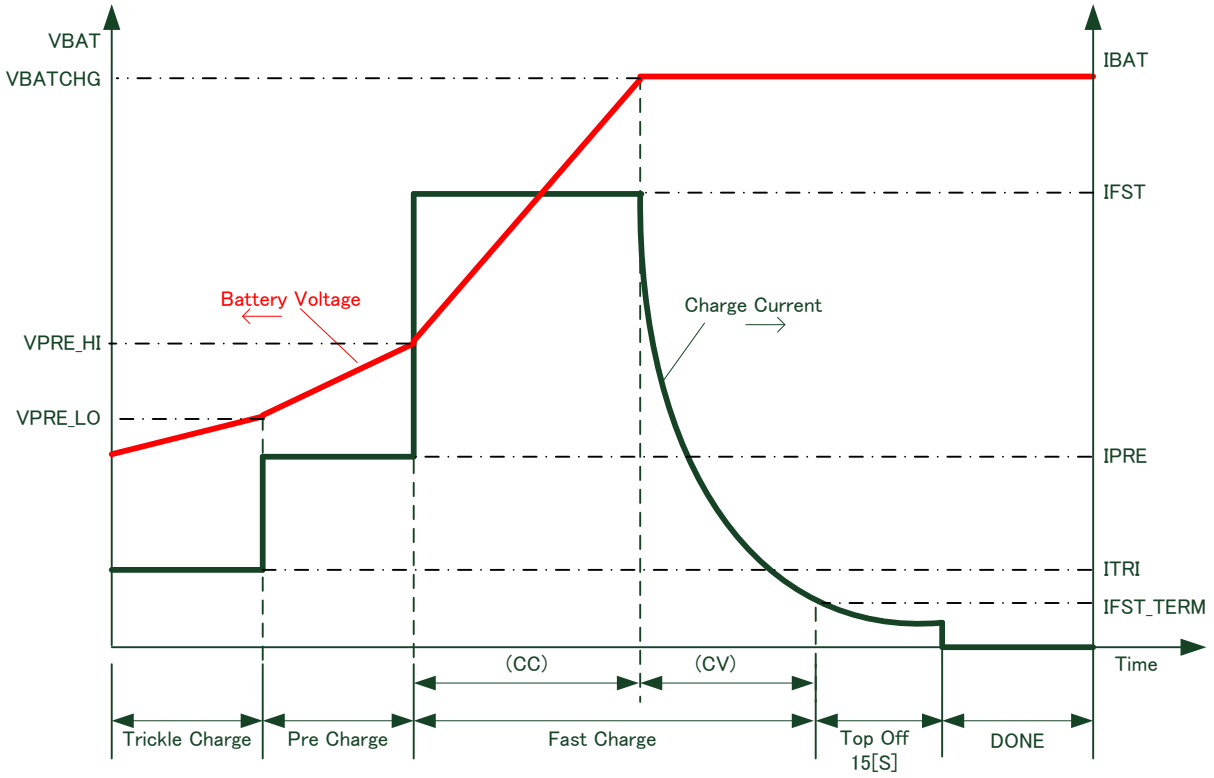

Figure 12. Battery Charger Output Control

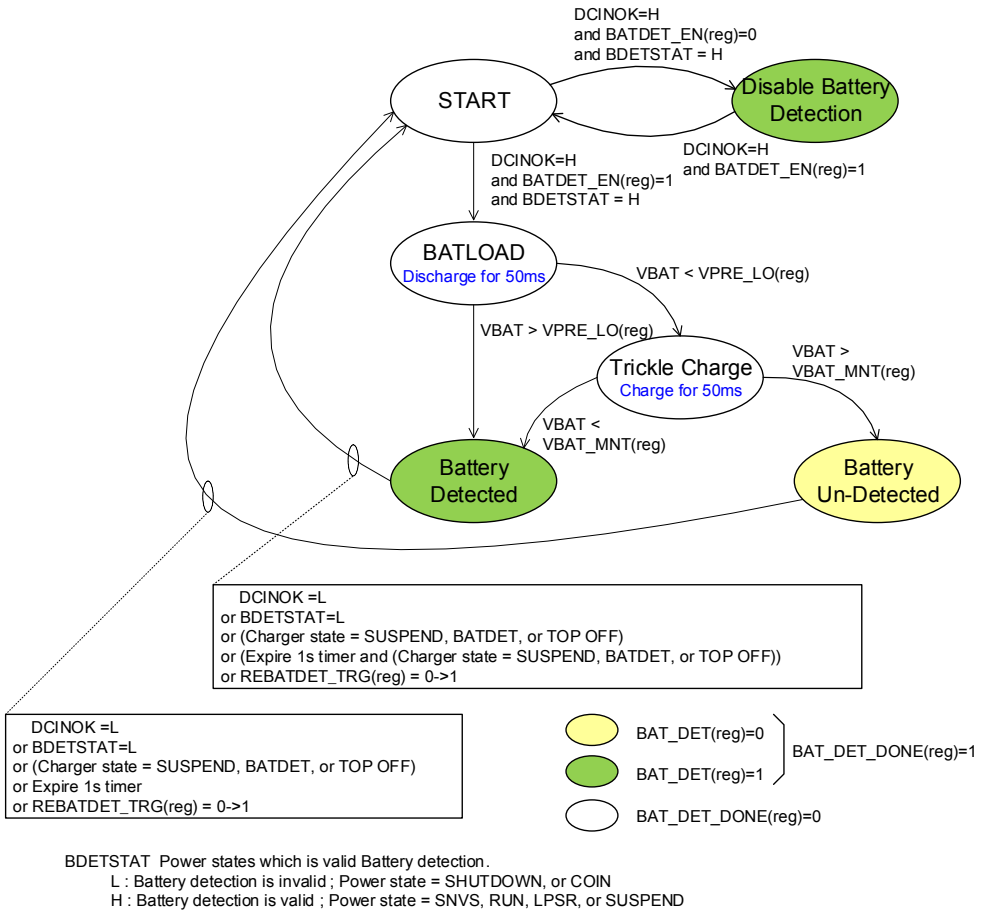

Figure 13. State Diagram of Battery Detection

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BD71815AGW has four Watch Dog Timers.

(a) High Temperature Protection Timer
The High Temperature Protection Timer is a timer to count the duration that battery temperature is higher than T4 (default 58°C) (BAT_TEMP[2:0]=3h) at Temp_err1, Temp_err2 or Temp_err5 state. This timer counts down 1 in every 64 seconds and shifts to Batt Error state after 121 counts.

(b) Low Temperature Protection Timer
The Low Temperature Protection Timer is a timer to count the duration that battery temperature is less than T2 (default 2°C) (BAT_TEMP[2:0]=5h) at Temp_err1, Temp_err2 or Temp_err5 state. This timer counts down 1 in every 64 seconds and shifts to Batt Error state after 121 counts.

(c) Watch Dog Timer for TRICKLE CHARGE and PRE CHARGE states
During Trickle-charge or Pre-charge, this timer counts down once every 64 seconds and shifts to Batt Error state after 121 counts by default. The number of counts can be changed by register settings (WDT_AUTO and WDT_PRE).

Table 6. Watch Dog Timer for Pre-charging and Trickle-charging

39h: CHG_STATE	40h: BAT_TEMP[2:0]	47h: CHG_SET1		Initial set value	countdown value	threshold to Batt Error
		[7] WDT_DIS	[6] WDT_AUTO			
TRICKLE CHARGE(01h) or PRE CHARGE(02h)	ROOM(0h) or HOT1(1h) or HOT2(2h) or Temp. Disable(6h)	0	0	49h: WDT_PRE	-1	1
		0	1	122	-1	1

(d) Watch Dog Timer for FAST CHAREGE and TOP OFF states
During Fast-charge or TOPOFF, this timer counts down in every 512 seconds or 64 seconds, and shifts to Batt Error state after 601 counts. The counter speed depends on the battery temperature. The number of the counts can be changed by register settings (WDT_AUTO, WDT_FST, and COLD_ERR_EN).

Table 7. Fast-charging and TOPOFF Watch Dog Timer

39h:CHG_STATE	40h:BAT_TEMP[2:0]	47h: CHG_SET1			Initial set value	countdown value	threshold to Batt Error
		WDT_DIS	WDT_AUTO	COLD_ERR_EN			
FAST CHARGE(03h) or TOP OFF(0Eh)	COLD1(4h)	0	0	1	1442	-1	3
		0	1	1	1442	-1	3
		0	0	0	WDT_FST * 8	-2	3
		0	1	0	1442	-2	3
	ROOM(0h) or HOT1(1h) or HOT2(2h) or Temp. Disable(6h)	0	0	1	WDT_FST * 8	-2	240
		0	1	1	1442	-2	240
		0	0	0	WDT_FST * 8	-2	240
		0	1	0	1442	-2	240

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(1) Thermal Control for Charging

Charging current is controlled by the battery temperature, measured using an external thermistor.
In low-temperature condition, charging current is reduced to half of the set value ICHG.

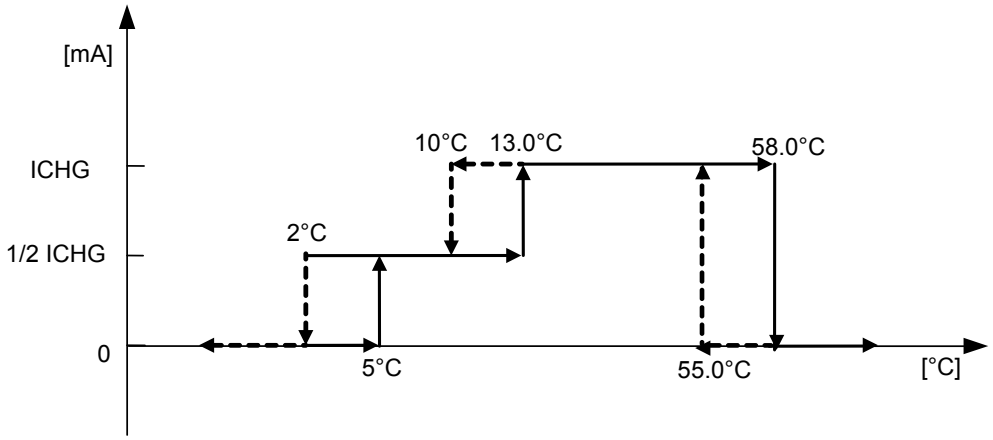

Figure 14. Charging Current vs. Battery Temperature

Charging voltage is also reduced by temperature and set by control registers.

Table 8. Charging Voltage vs. Battery Temperature

JEITA Temperature Range		Voltage Setting Register
T2 – T3	2°C to 45°C, (typ)	VBAT_CHG1
T3 – T5	45°C to 50°C, (typ)	VBAT_CHG2
T5 – T4	50°C to 58°C, (typ)	VBAT_CHG3

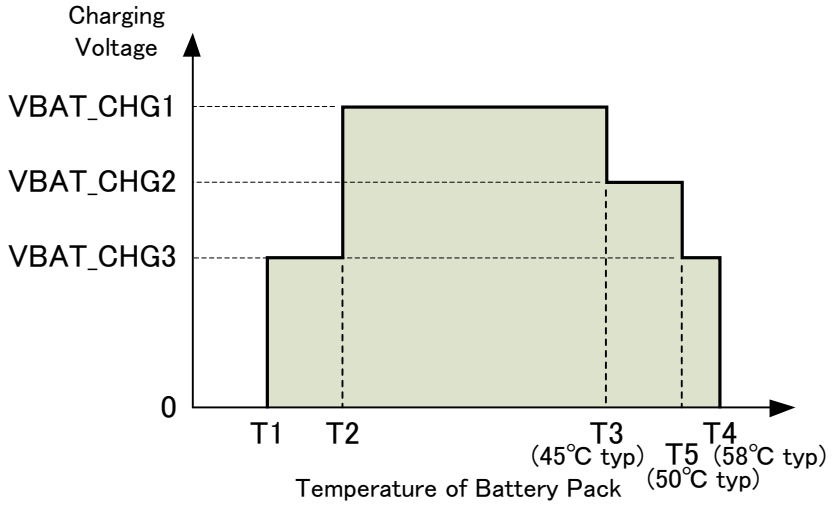

Figure 15. Charging Voltage vs. Battery Temperature

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9. Coulomb Counter Block

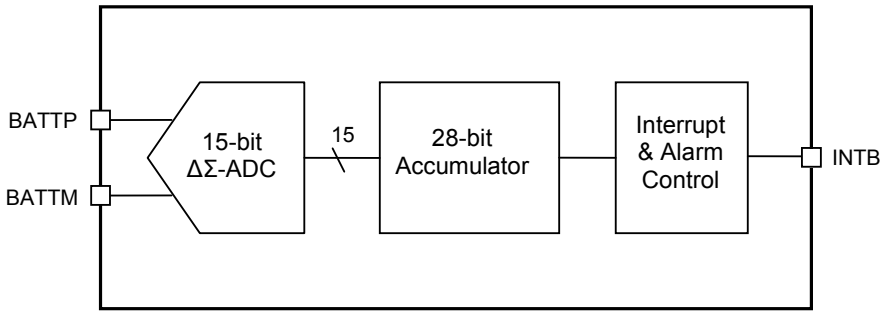

Figure 16. Coulomb Counter Block Diagram

Features

- 28-bit Coulomb Counter for battery fuel gauging
- 15-bit ΔΣ-ADC measures the battery's charge and discharge current by means of an external current sense resistor (10mΩ, ±1% or 30mΩ, ±1%).
- Charging/Discharging amount integration period : 1sec
- There are three programmable battery capacity thresholds for interrupt.

(1) Functions and Programmabilites

(a) 28-bit accumulator features

28-bit accumulator accumulates 15-bit ΔΣ-ADC results by each 1sec. The accumulated value is shown in CCNTD register. CCNTD value is accumulated when CCNTENB is set to 1. CCNTD value is held when CCNTENB is set to 0. When CCNTRST is set to 1, CCNTD value is cleared to 0.

(b) Three programmable Event Alarm outputs from INTB pin

BD71815AGW has alarm events using Coulomb Counter. The elements are shown in Table 9.

Table 9. Alarm events using Coulomb Counter

Status register name	Interrupt register name	Event	Condition
CC_MON1	CC_MON1_DET	Coulomb counter near full capacity alarm (AMBLED is turned off and GRNLED is turned on when CHGDONE_LED_EN(reg)=1)	0 : CCNTD ≤ CC_BATCAP1_TH(reg) 1 : CCNTD > CC_BATCAP1_TH(reg)
CC_MON2	CC_MON2_DET	Coulomb counter general alarm 2	0 : CCNTD ≥ CC_BATCAP2_TH(reg) 1 : CCNTD < CC_BATCAP2_TH(reg)
CC_MON3	CC_MON3_DET	Coulomb counter general alarm 3	0 : CCNTD ≥ CC_BATCAP3_TH(reg) 1 : CCNTD < CC_BATCAP3_TH(reg)
OCUR1	OCUR1_DET OCUR1_RES	Battery over current alarm 1	0 : CURCD < OCURTHR1_TH(reg) 1 : CURCD ≥ OCURTHR1_TH(reg) more than OCURDUR1(reg) time
OCUR2	OCUR2_DET OCUR2_RES	Battery over current alarm 2	0 : CURCD < OCURTHR2_TH(reg) 1 : CURCD ≥ OCURTHR2_TH(reg) more than OCURDUR2(reg) time
OCUR3	OCUR3_DET OCUR3_RES	Battery over current alarm 3	0 : CURCD < OCURTHR3_TH(reg) 1 : CURCD ≥ OCURTHR3_TH(reg) more than OCURDUR3(reg) time

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