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Power Management ICs for Automotive Body Control

LED Indicator Driver



BD8105FV

No.11039ECT01

●Description

The BD8105FV is a serial parallel control LED driver with 35V input voltage rating. Responding to the 3-line serial data, it turns the 12ch open drain output on/off. Due to its compact size, it is optimal for small spaces.

●Features

- 1) Open Drain Output
- 2) 3-line Serial Control + Enable Signal
- 3) Internal Temperature Protection Circuit (TSD)
- 4) Cascade Connection Compatible
- 5) SSOP-B20W
- 6) Internal 12 ch Power Transistor

●Applications

These ICs can be used with car and consumer electronic.

●Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Ratings | Unit |
|---|--------|----------|------|
| Power Supply Voltage | VCC | 7 | V |
| Output Voltage(Pin No : 4~9, 11~16) | VDmax | 35 | V |
| Input Voltage(Pin No : 1, 2, 3, 17, 18) | VIN | -0.3~VCC | V |
| Power Dissipation | Pd | 1187* | mW |
| Operating Temperature Range | Topr | -40~+105 | °C |
| Storage Temperature Range | Tstg | -55~+150 | °C |
| Drive Current (DC) | IomaxD | 50 | mA |
| Drive Current(Pulse) | IomaxP | 150** | mA |
| Junction Temperature | Tjmax | 150 | °C |

* Pd decreased at 9.50mW/°C for temperatures above Ta=25°C, mounted on 70×70×1.6mm Glass-epoxy PCB.

** Do not however exceed Pd. Time to impress ≤ 200msec

●Operational Conditions (Ta=-40~105°C)

| Parameter | Symbol | Ratings | | | Unit |
|----------------------|--------|---------|------|------|------|
| | | Min. | Typ. | Max. | |
| Power Supply Voltage | Vcc | 4.5 | 5 | 5.5 | V |
| Drive Current | Io | - | 20 | 40 | mA |

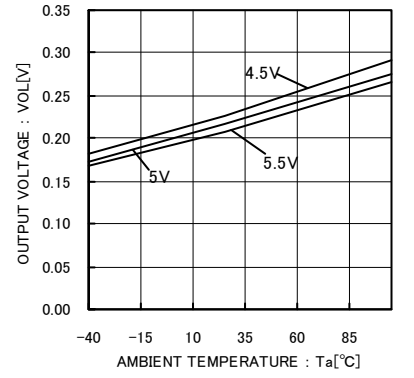
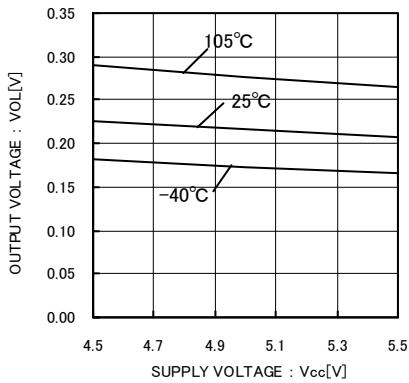
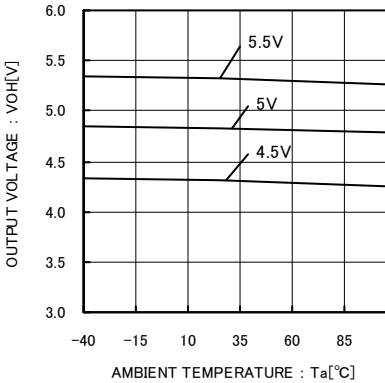
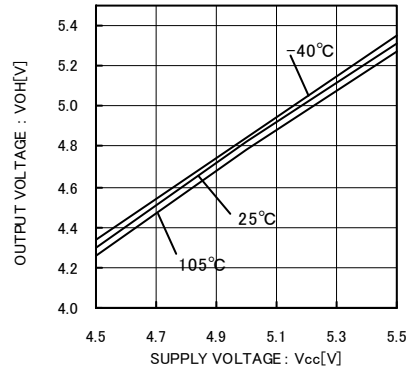
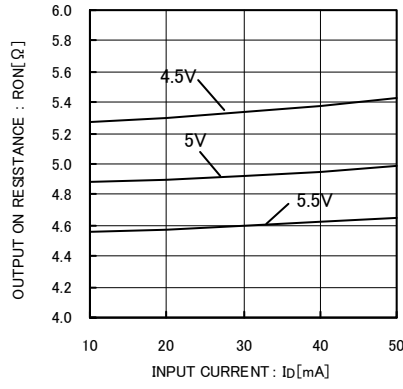
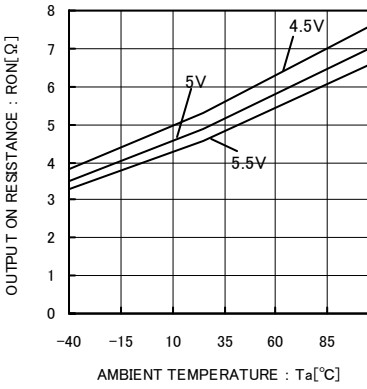
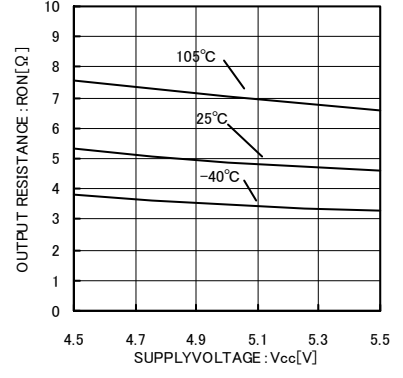
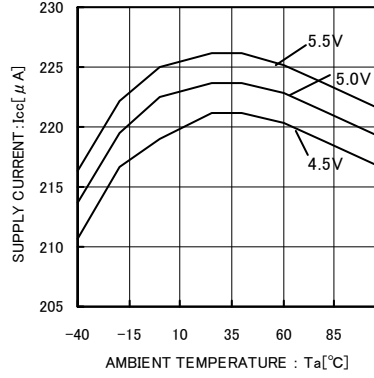
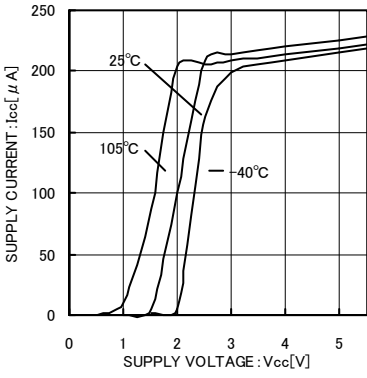
* This product is not designed for protection against radioactive rays.

●Electrical Characteristics (Unless specified, Ta=-40~105°C Vcc=4.5~5.5V)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|---|--------|-------------|------|-------------|------|---|
| | | Min. | Typ. | Max. | | |
| 【Output D0~D11】 (Pin No : 4~9, 11~16) | | | | | | |
| ON Resistor | RON | - | 6 | 12 | Ω | Id=20mA |
| Output leakage current | IDL | - | 0 | 5 | μA | V _D =34V |
| 【Logic input】 (Pin No : 1, 2, 3, 17, 18) | | | | | | |
| Upper limit threshold voltage | VTH | Vcc ×0.8 | - | - | V | |
| Bottom limit threshold voltage | VTL | - | - | Vcc ×0.2 | V | |
| Serial clock frequency | FCLK | - | - | 1 | MHz | |
| Input Current | IIN | 20 | 50 | 100 | μA | VIN=5V |
| Input leakage Current | IINL | - | 0 | 5 | μA | VIN=0V |
| 【WHOLE】 | | | | | | |
| Circuit Current | ICC | - | 0.3 | 5 | mA | Serial Data Input, VCC=5V,CLK=500KHz, SEROUT=OPEN |
| Static Current | ISTN | - | 0 | 50 | μA | RST_B=OPEN, SEROUT=OPEN |
| 【SER OUT】 (Pin No. : 20) | | | | | | |
| Output Voltage high | VOH | 4.6 | 4.8 | - | V | VCC=5V, ISO=-5mA |
| Output voltage Low | VOL | - | 0.2 | 0.4 | V | VCC=5V, ISO=5mA |

* This product is not designed for protection against radioactive rays.

● Electrical Characteristic Diagrams (Unless otherwise specified Ta=25°C)



●Block Diagram

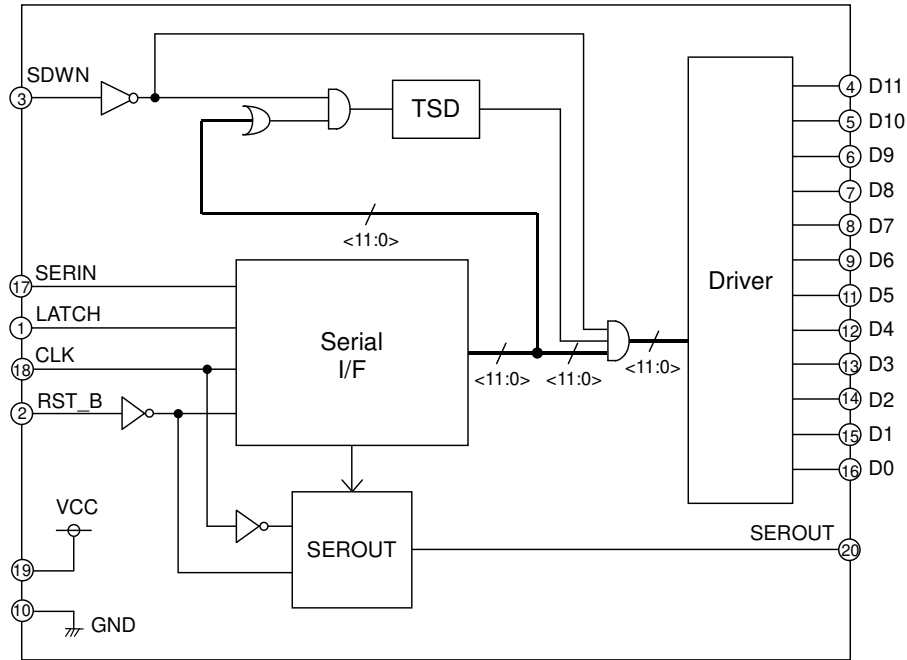


Fig.10

●Pin Setup Diagram

BD8105FV(SSOP-B20W)

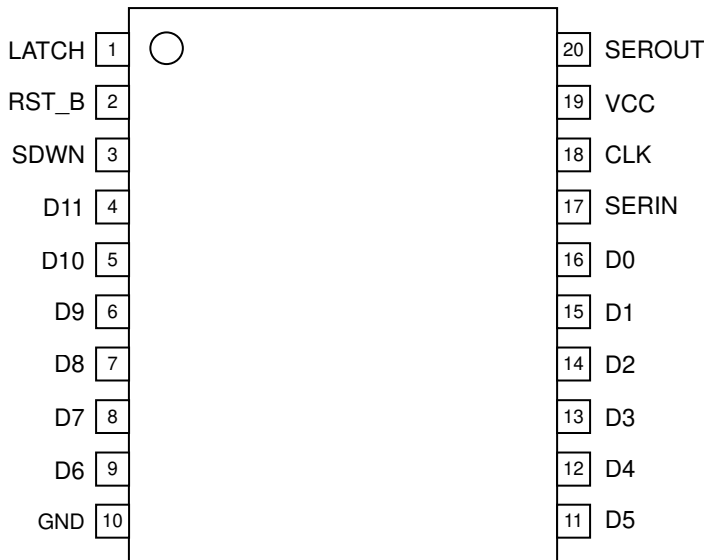


Fig.11

●Terminal Number • Terminal Name

| Pin Number | Terminal Name | Function |
|------------|---------------|---|
| 1 | LATCH | Latch Signal Input Terminal (H: Latches Data) |
| 2 | RST_B | Reset Reversal Input Terminal (L: FF Data 0) |
| 3 | SDWN | Shutdown Input Terminal (H: Output Off) |
| 4 | D11 | Drain Output Terminal 11 |
| 5 | D10 | Drain Output Terminal 10 |
| 6 | D9 | Drain Output Terminal 9 |
| 7 | D8 | Drain Output Terminal 8 |
| 8 | D7 | Drain Output Terminal 7 |
| 9 | D6 | Drain Output Terminal 6 |
| 10 | GND | Ground Terminal |
| 11 | D5 | Drain Output Terminal 5 |
| 12 | D4 | Drain Output Terminal 4 |
| 13 | D3 | Drain Output Terminal 3 |
| 14 | D2 | Drain Output Terminal 2 |
| 15 | D1 | Drain Output Terminal 1 |
| 16 | D0 | Drain Output Terminal 0 |
| 17 | SERIN | Serial Data Input Terminal |
| 18 | CLK | Clock Input Terminal |
| 19 | VCC | Supply Voltage Input Terminal |
| 20 | SEROUT | Serial Data Output Terminal |

●Block Operation

1)Serial I/F

The I/F is a 3-line serial (LATCH, CLK, SERIN) style.

12-bit output ON/OFF can be set-up. This is composed of shift register. + 12-bit register.

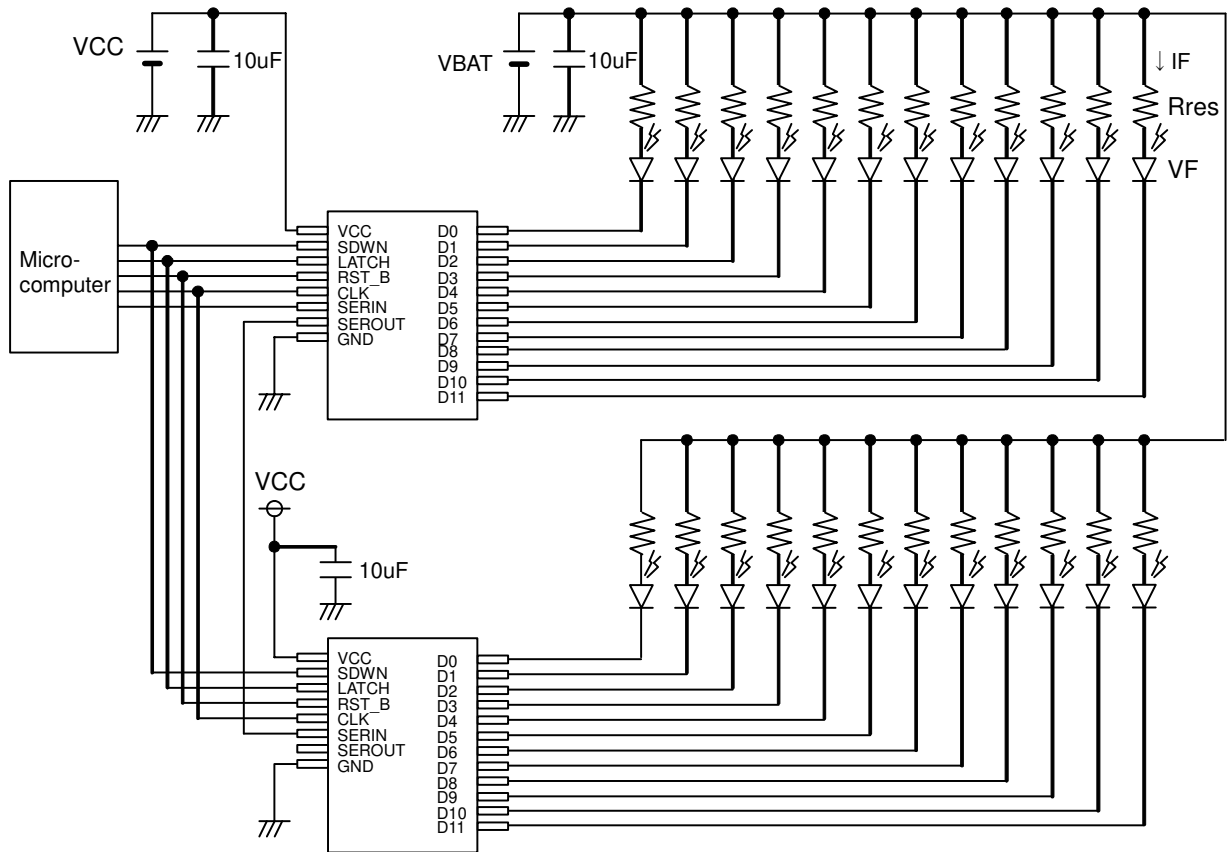
2)Driver

It is a 12-bit open drain output.

3)TSD (Thermal Shut Down)

To prevent heat damage and overheating, when the chip temperature goes over approximately 175°C, the output turns off. When the temperature goes back down, normal operation resumes. However, the intended use of the temperature protection circuit is to protect the IC, so please construct thermal design with the junction temperature Tjmax under 150°C.

●Application Circuit



$$IF = \frac{VBAT - VF}{Rres + RON}$$

Fig.12

●Serial Communication

The serial I/F is composed of a shift register which changes the CLK and SERIN serial signals to parallel signals, and a register to remember those signals with a LATCH signal. The registers are reset by applying a voltage under $VCC \times 0.2$ to the RST_B terminal or opening it, and D11~D0 become open. To prevent erroneous LED lighting, please apply voltage under $VCC \times 0.2$ to RST_B or make it open during start-up.

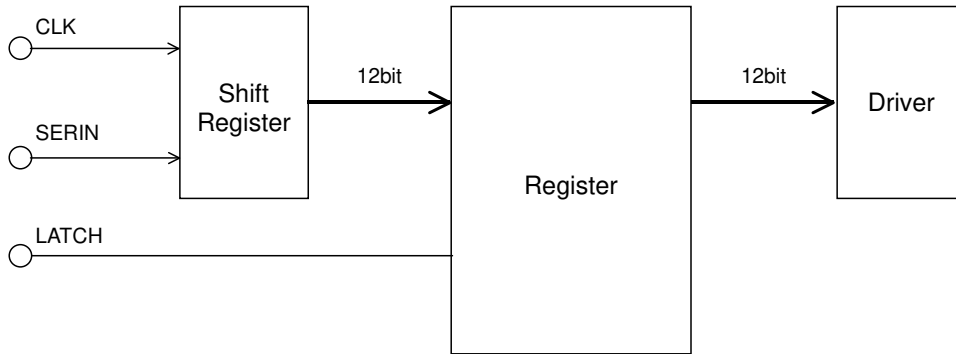


Fig.13

1)Serial Communication Timing

The 12-bit serial data input from SERIN is taken into the shift register by the rise edge of the CLK signal, and is recorded in the register by the rise edge of the LATCH signal. The recorded data is valid until the next rise edge of the LATCH signal.

2)Serial Communication Data

The serial data input configuration of SERIN terminal is shown below:

| | | | | | | | | | | | |
|---------|-----|----|----|----|----|----|----|----|----|----|-------|
| First → | | | | | | | | | | | →Last |
| d11 | d10 | d9 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| Data | | | | | | | | | | | |

| Terminal Name | Output Status | Data | | | | | | | | | | | |
|---------------|---------------|------|-----|----|----|----|----|----|----|----|----|----|----|
| | | d11 | d10 | d9 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| D11 | ON | 1 | * | * | * | * | * | * | * | * | * | * | |
| | OFF | 0 | * | * | * | * | * | * | * | * | * | * | |
| D10 | ON | * | 1 | * | * | * | * | * | * | * | * | * | |
| | OFF | * | 0 | * | * | * | * | * | * | * | * | * | |
| D9 | ON | * | * | 1 | * | * | * | * | * | * | * | * | |
| | OFF | * | * | 0 | * | * | * | * | * | * | * | * | |
| D8 | ON | * | * | * | 1 | * | * | * | * | * | * | * | |
| | OFF | * | * | * | 0 | * | * | * | * | * | * | * | |
| D7 | ON | * | * | * | * | 1 | * | * | * | * | * | * | |
| | OFF | * | * | * | * | 0 | * | * | * | * | * | * | |
| D6 | ON | * | * | * | * | * | 1 | * | * | * | * | * | |
| | OFF | * | * | * | * | * | 0 | * | * | * | * | * | |
| D5 | ON | * | * | * | * | * | * | 1 | * | * | * | * | |
| | OFF | * | * | * | * | * | * | 0 | * | * | * | * | |
| D4 | ON | * | * | * | * | * | * | * | 1 | * | * | * | |
| | OFF | * | * | * | * | * | * | * | 0 | * | * | * | |
| D3 | ON | * | * | * | * | * | * | * | * | 1 | * | * | |
| | OFF | * | * | * | * | * | * | * | * | 0 | * | * | |
| D2 | ON | * | * | * | * | * | * | * | * | * | 1 | * | |
| | OFF | * | * | * | * | * | * | * | * | * | 0 | * | |
| D1 | ON | * | * | * | * | * | * | * | * | * | * | 1 | |
| | OFF | * | * | * | * | * | * | * | * | * | * | 0 | |
| D0 | ON | * | * | * | * | * | * | * | * | * | * | * | 1 |
| | OFF | * | * | * | * | * | * | * | * | * | * | * | 0 |

* represents "Don't care".

3)Enable Signal

By applying voltage at least $VCC \times 0.8$ or more to the SDWN terminal, D0 (16 pin)~D11 (4 pin) become open forcibly. At this time, the temperature protection circuit (TSD) stops. D11~D0 become PWM operation by inputting PWM to SDWN(3 pin).

4)SEROUT

A cascade connection can be made (connecting at least 2 or more IC's in serial). Serial signal input from SERIN is transferred into receiver IC by the fall edge of the CLK signal. Since this functionality gives enough margins for the setup time prior to the rise edge of the CLK signal on the receiver IC (using the exact same CLK signal of sender IC), the application reliability can be improved as cascade connection functionality.

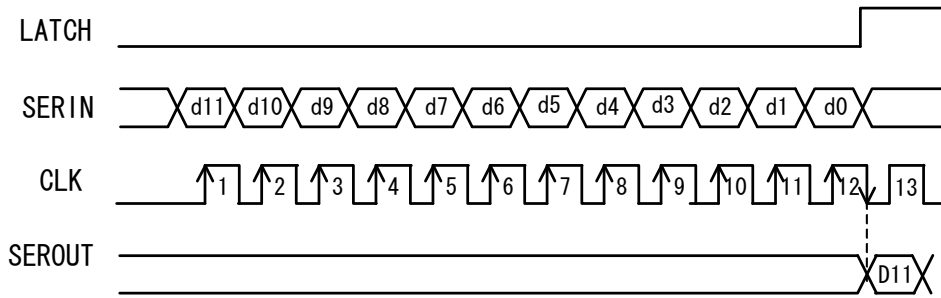


Fig.14

●Cascade Connection

By using (at least) 2 ICs, each IC's D11~D0, at (at least) 24ch, can be controlled by the 24-bit SERIN signal. The serial data input to the sender IC can be transferred to the receiver IC by inputting 12CLK to the CLK terminal.

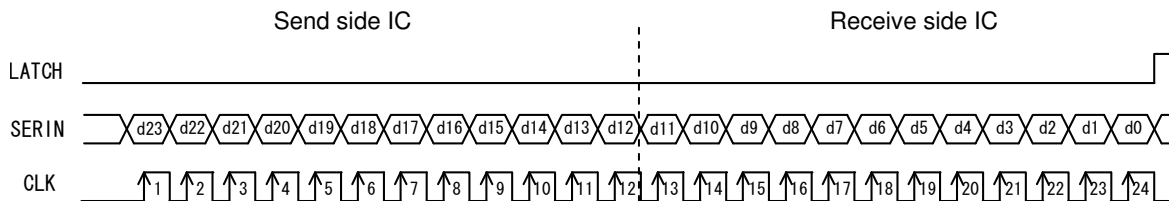


Fig.15

●INPUT SIGNAL'S TIMING CHART

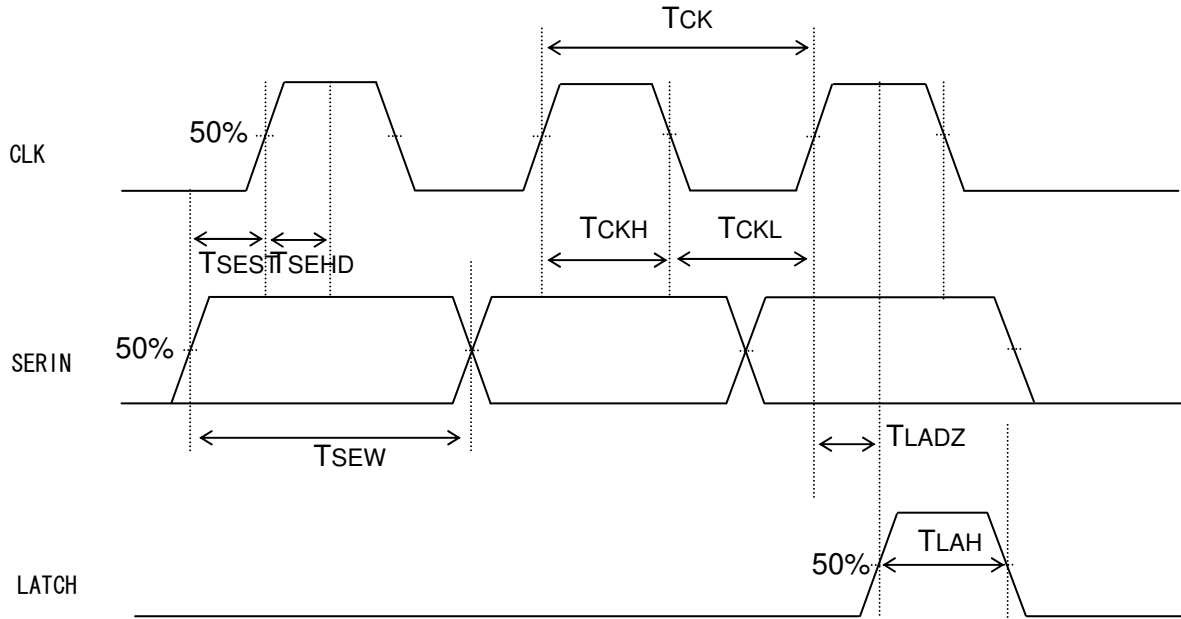


Fig.16

●INPUT SIGNAL'S TIMING RULE(Ta=-40~105°C Vcc=4.5~5.5V)

| Parameter | Symbol | Min | Unit |
|------------------------------------|--------|------|------|
| CLK period | TCK | 1000 | ns |
| CLK high pulse width | TCKH | 480 | ns |
| CLK low pulse width | TCKL | 480 | ns |
| SERIN high and low pulse width | TSEW | 980 | ns |
| SERIN setup time prior to CLK rise | TSEST | 150 | ns |
| SERIN hold time after CLK fall | TSEHD | 150 | ns |
| LATCH high pulse time | TLAH | 480 | ns |
| Last CLK rise to LATCH rise | TLADZ | 250 | ns |

●OUTPUT SIGNAL'S DELAY CHART

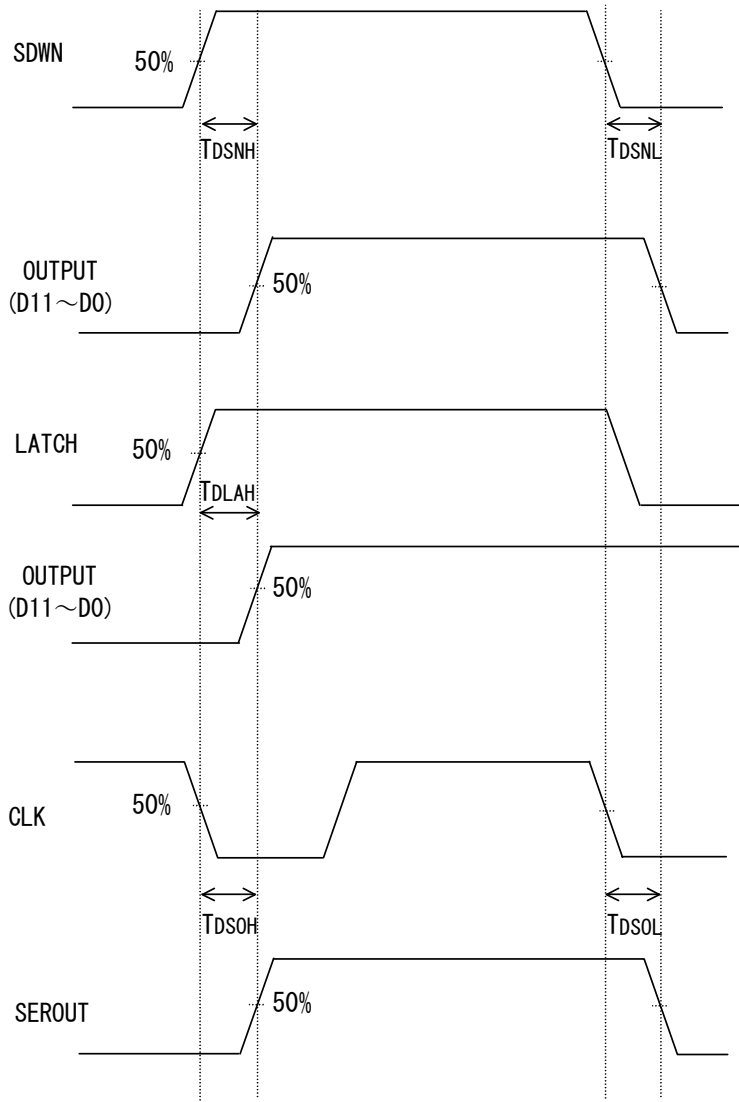


Fig.17

●OUTPUT SIGNAL'S DELAY TIME(Ta=-40~105°C Vcc=4.5~5.5V)

| Parameter | Symbol | Max | Unit |
|-------------------------------------|--------|-----|------|
| SDWN Switching Time(L→H) | TDSNH | 300 | ns |
| SDWN Switching Time(H→L) | TDSNL | 300 | ns |
| LATCH Switching Delay Time | TDLAH | 300 | ns |
| SEROUT Propagation Delay Time(L→H) | TDSOH | 350 | ns |
| SEROUT Propagation Delay Time (H→L) | TDSOL | 350 | ns |

●INPUT/OUTPUT EQUIVALENT CIRCUIT(PIN NAME)

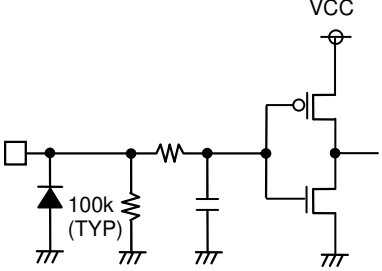
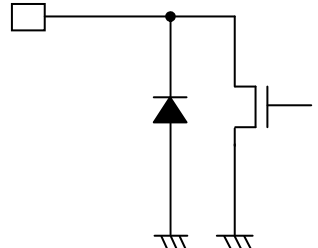
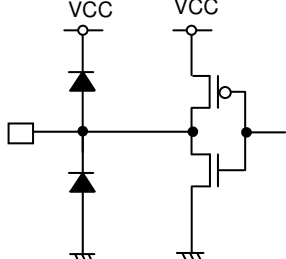
| | | |
|---|---|---|
| <p>1PIN(LATCH) 2PIN(RST_B) 3PIN(SDWN) 17PIN(SERIN) 18PIN(CLK)</p> | <p>4PIN(D11),5PIN(D10) 6PIN(D9),7PIN(D8) 8PIN(D7),9PIN(D6) 11PIN(D5),12PIN(D4) 13PIN(D3),14PIN(D2) 15PIN(D1),16PIN(D0)</p> | <p>20PIN(SEROUT)</p> |
|  |  |  |

Fig.18

●Notes for use

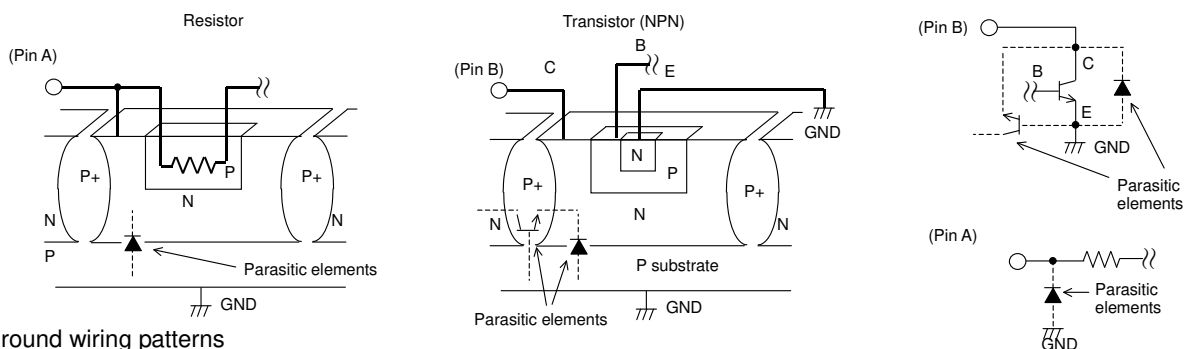
- (1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.
- (2) Reverse connection of a power supply connector
If the connector of power is wrong connected, it may result in IC breakage. In order to prevent the breakage from the wrong connection, the diode should be connected between external power and the power terminal of IC as protection solution.
- (3) GND potential
Ensure a minimum GND pin potential in all operating conditions.
- (4) Setting of heat
Use a setting of heat that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
- (5) Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage.
- (6) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.
- (7) Thermal shutdown circuit(TSD)
This IC built-in a Thermal shutdown circuit (TSD circuit). If Chip temperature becomes 175°C(TYP.), make the output an Open state. Eventually, warmly clearing the circuit is decided by the condition of whether the heat excesses over the assigned limit, resulting the cutoff of the circuit of IC, and not by the purpose of preventing and ensuring the IC. Therefore, the warm switch-off should not be applied in the premise of continuous employing and operation after the circuit is switched on.
- (8) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process
- (9) IC terminal input
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when a resistor and transistor are connected to pins. (See the chart below.)

○The P/N junction functions as a parasitic diode when

GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).

○Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

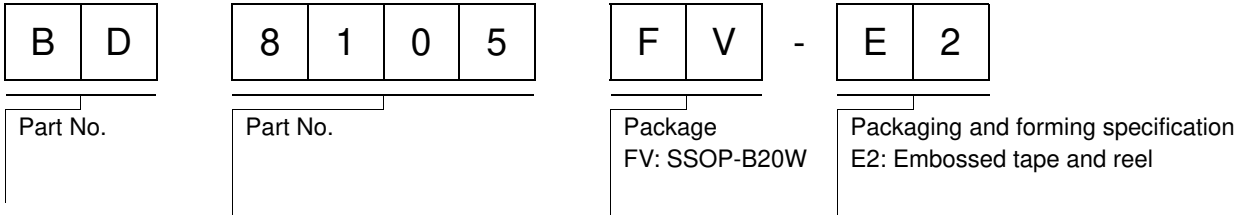
The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input pins.



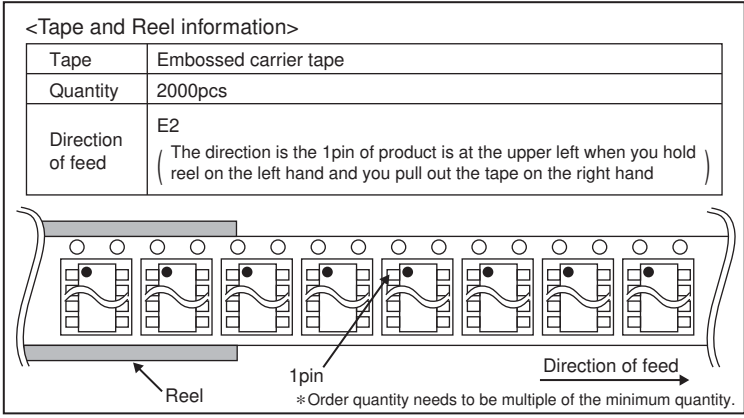
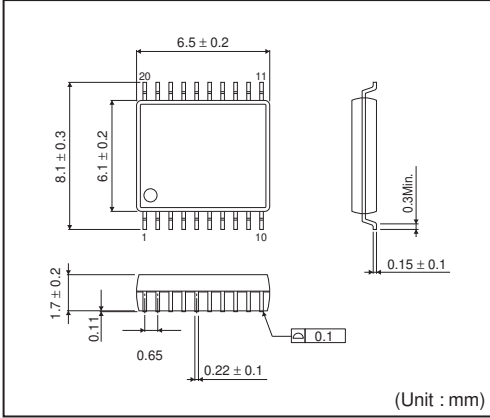
- (10) Ground wiring patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

●Ordering part number



SSOP-B20W



Notes

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