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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Single-chip Type with Built-in FET Switching Regulators

High-efficiency Step-up Switching Regulators with Built-in Power MOSFET



BD8152FVM, BD8158FVM

No.11027ECT20

●Description

BD8152FVM, BD8158FVM are the 1-channel step-up switching regulator which builds in the low voltage FET. Input voltage is 2.5 V to 5.5 V (BD8152FVM), 2.1V to 5.5V (BD8158FVM) realizing the low consumption power. High accuracy feedback voltage $\pm 1\%$ is established and the brightness dispersion of TFT-LCD panel is suppressed.

●Features

- 1) Current mode PWM system
- 2) Input voltage is 2.5 V to 5.5 V (BD8152FVM), 2.1 V to 5.5 V (BD8158FVM, providing the low power input)
- 3) Switching frequency is variable as 600 kHz/1,200 kHz.
- 4) Built-in 0.25Ω power switch
- 5) Feedback voltage $1.245 \pm 1\%$
- 6) Built-in under-voltage lockout protection circuit
- 7) Built-in overcurrent protection circuit
- 8) Built-in thermal shutdown circuit

●Applications

7 to 17 inches panels for the satellite navigation system, laptop PC
TFT-LCD panels

●Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limit	Unit
Power supply voltage		Vcc	7	V
Power dissipation		Pd	588*	mW
Operating temperature range	BD8152FVM	Topr	-40 to +85	°C
	BD8158FVM		-40 to +125	
Storage temperature range		Tstg	-55 to +150	°C
Switch pin current		Isw	1.5**	A
Switch pin voltage		Vsw	15	V
Maximum junction temperature		Tjmax	150	°C

* Reduced by 4.7 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

** Must not exceed Pd.

●Recommended Operating Ranges (Ta = 25°C)

Parameter	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Power supply voltage (BD8152FVM)	Vcc	2.5	3.3	5.5	V
Power supply voltage (BD8158FVM)	Vcc	2.1	2.5	4.0(5.5)*	V
Switch current	ISW	-	-	1.4	A
Switch pin voltage	VSW	-	-	14	V

*Specified at 600kHz switching operating.

●Electrical Characteristics BD8152FVM (Unless otherwise specified, Ta = 25°C; Vcc = 3.3 V; ENB = 3.3 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[triangular waveform oscillator]						
Oscillating frequency 1	FOSC1	540	600	660	kHz	FCLK = 0 V
Oscillating frequency 2	FOSC2	1.08	1.20	1.32	MHz	FCLK = Vcc
[Overcurrent protection circuit]						
Overcurrent limit	ISW	-	2	-	A	
[Soft start circuit]						
SS source current	ISO	6	10	14	μA	Vss = 0.5 V
[Under-voltage lockout protection circuit]						
Off threshold voltage	VUTOFF	2.1	2.2	2.3	V	
On threshold voltage	VUTON	2.0	2.1	2.2	V	
[Error amp]						
Input bias current	IB	-	0.1	0.5	μA	
Feedback voltage	VFB	1.232	1.245	1.258	V	Buffer
[Output]						
ON resistance	RON	-	250	380	mΩ	*Isw = 1 A
Max. duty ratio	DMAX	72	80	88	%	RL = 100 Ω
[ENB]						
ENB on voltage	VON	Vcc×0.7	Vcc	-	V	
ENB off voltage	VOFF	-	0	Vcc×0.3	V	
[Overall]						
Standby current	ISTB	-	0	10	μA	VENB = 0 V
Average consumption current	ICC	-	1.2	2.4	mA	no switching

○ This product is not designed for protection against radio active rays.

* Design guarantee (No total shipment inspection is made.)

●Electrical Characteristics BD8158FVM (Unless otherwise specified, Ta = 25°C; Vcc = 2.5 V; ENB = 2.5 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[triangular waveform oscillator]						
Oscillating frequency 1	FOSC1	480	600	720	kHz	FCLK = 0 V
Oscillating frequency 2	FOSC2	0.96	1.20	1.44	MHz	FCLK = Vcc
[Overcurrent protection circuit]						
Overcurrent limit	ISW	-	2	-	A	
[Soft start circuit]						
SS source current	ISO	6	10	14	μA	Vss = 0.5 V
[Under-voltage lockout protection circuit]						
Off threshold voltage	VUTOFF	1.7	1.8	1.9	V	
On threshold voltage	VUTON	1.6	1.7	1.8	V	
[Error amp]						
Input bias current	IB	-	0.1	0.5	μA	
Feedback voltage	VFB	1.232	1.245	1.258	V	Buffer
[Output]						
ON resistance	RON	-	250	-	mΩ	*Isw = 1 A
Max. duty ratio	DMAX	-	85	-	%	RL = 100 Ω
[ENB]						
ENB on voltage	VON	Vcc×0.7	Vcc	-	V	
ENB off voltage	VOFF	-	0	Vcc×0.3	V	
[Overall]						
Standby current	ISTB	-	0	10	μA	VENB = 0 V
Average consumption current	ICC	-	1.2	2.4	mA	no switching

○ This product is not designed for protection against radio active rays.

* Design guarantee (No total shipment inspection is made.)

●Reference Data (Unless otherwise specified, Ta = 25°C)

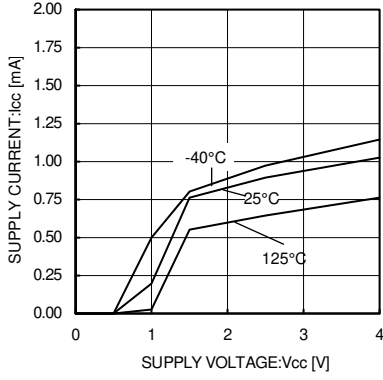


Fig. 1 Total Supply Current

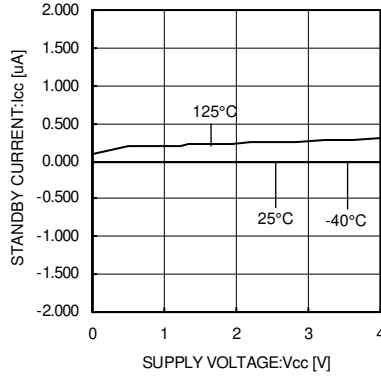


Fig. 2 Standby Current

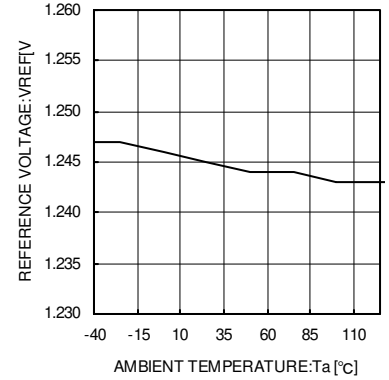


Fig. 3 Reference Voltage vs Temperature

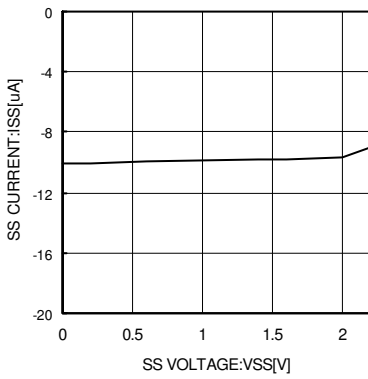


Fig. 4 SS Source Current

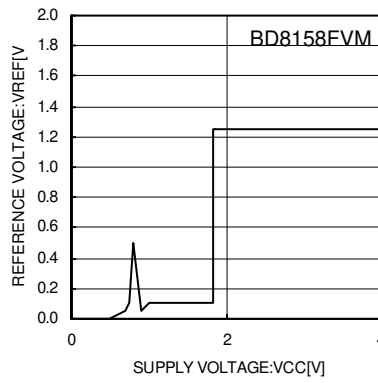


Fig. 5 Reference Voltage vs Power Supply Voltage

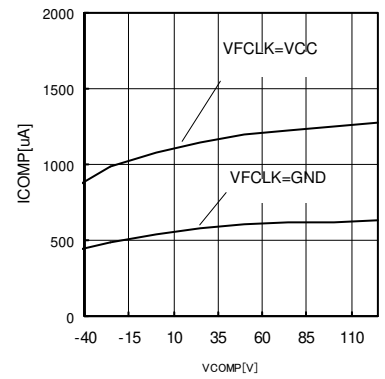


Fig. 6 Switching Frequency Temperature

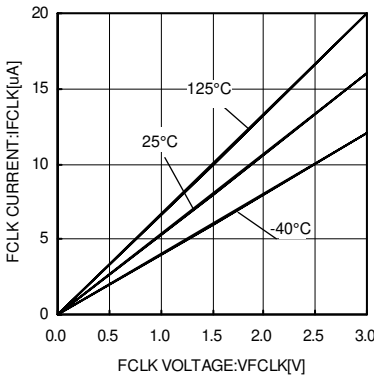


Fig. 7 FCLK Pin Current

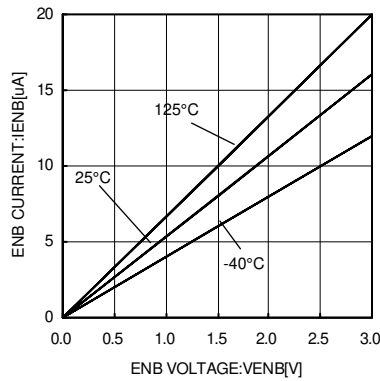


Fig. 8 ENB Pin Current

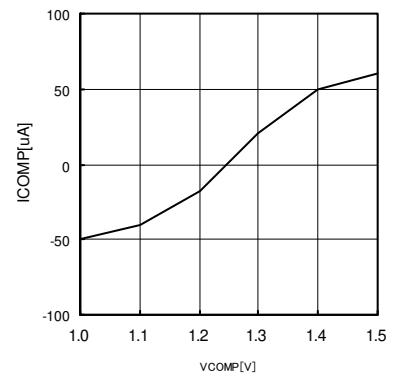


Fig. 9 COMP Sinking vs Source Current

●Reference Data (Unless otherwise specified, Ta = 25°C)

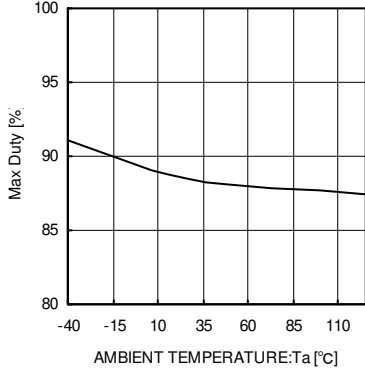


Fig. 10 Max. Duty Ratio Temperature

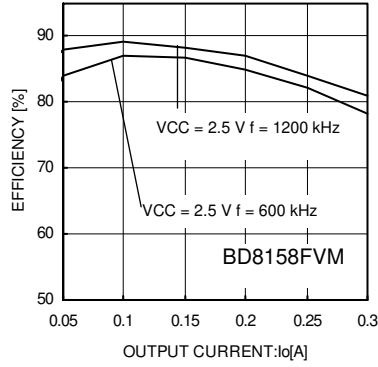


Fig. 11 Vcc = 2.5V Power Efficiency

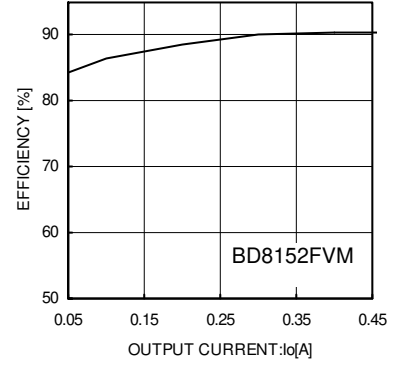


Fig. 12 Vcc = 5V Power Efficiency

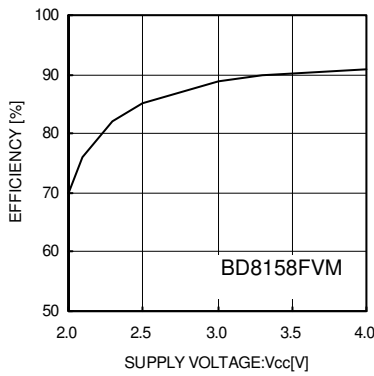


Fig. 13 Power Efficiency vs Power Supply Voltage

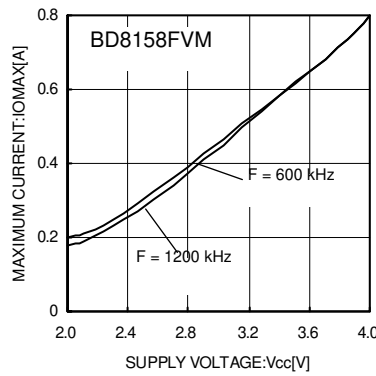


Fig. 14 Max. Load Current vs Power Supply Voltage

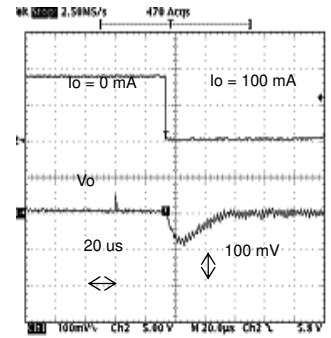


Fig. 15 Load Response Waveform

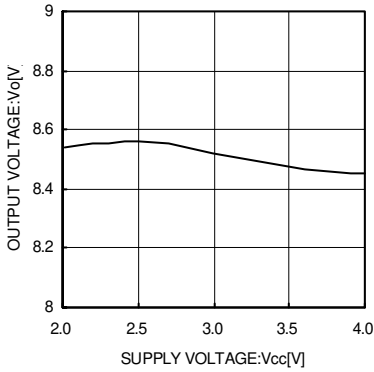


Fig. 16 Output Voltage Line Regulation

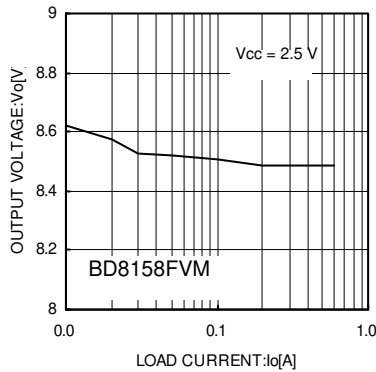


Fig. 17 Output Voltage Load Regulation 1

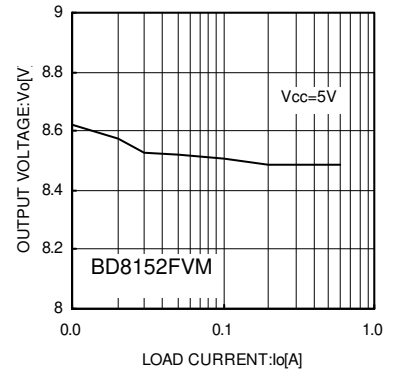


Fig. 18 Output Voltage Load Regulation 2

●Block Diagram

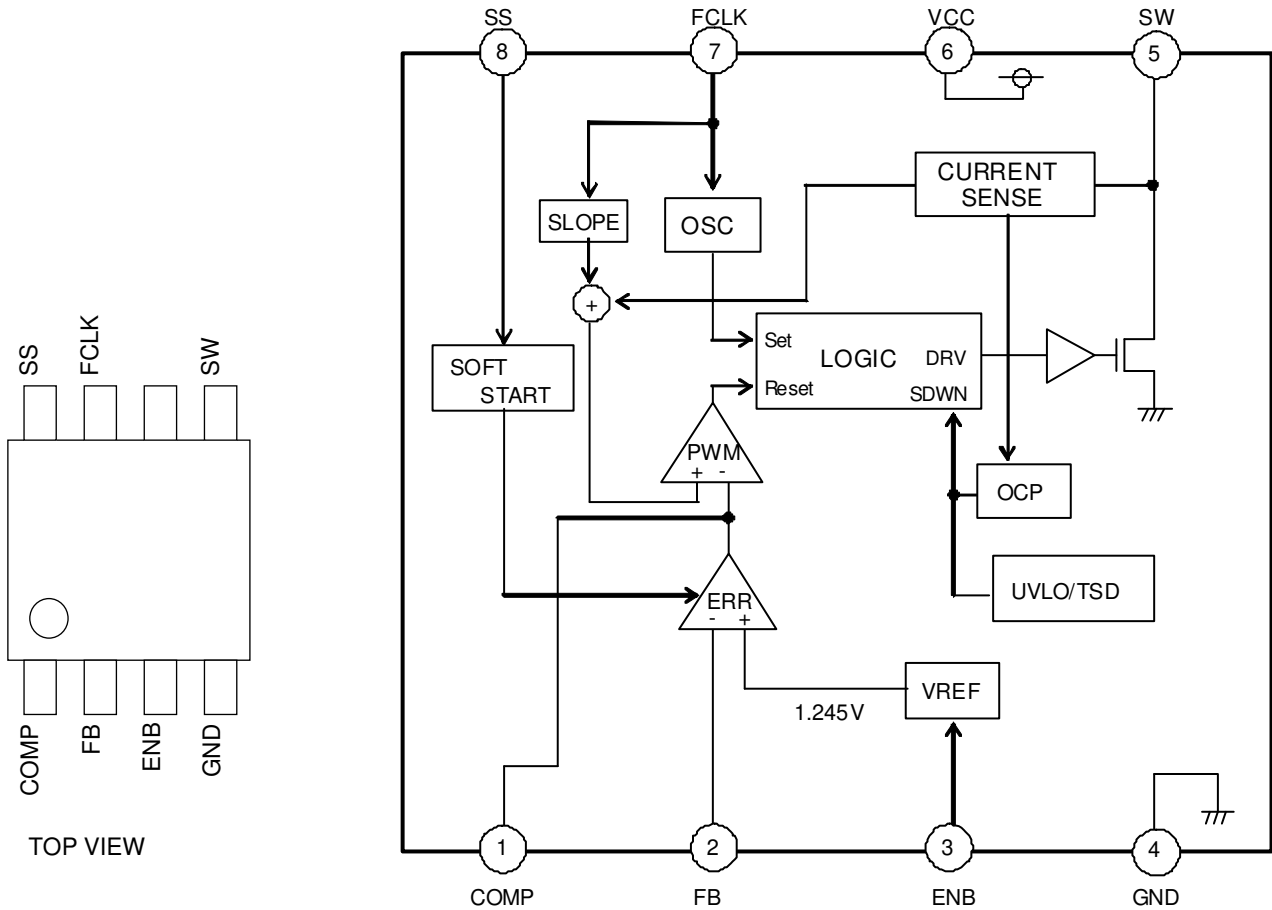


Fig. 19 Pin Arrangement Diagram and Block Diagram

●Pin Assignment Diagram and Function

Pin No.	Pin name	Function
2	FB	Error amp inversion input pin
3	ENB	Control input pin
4	GND	Ground pin
5	SW	N-channel power FET drain output
6	Vcc	Power supply input pin
7	FCLK	Frequency switching pin
8	SS	Soft start current output pin

●Timing Chart

Startup sequence

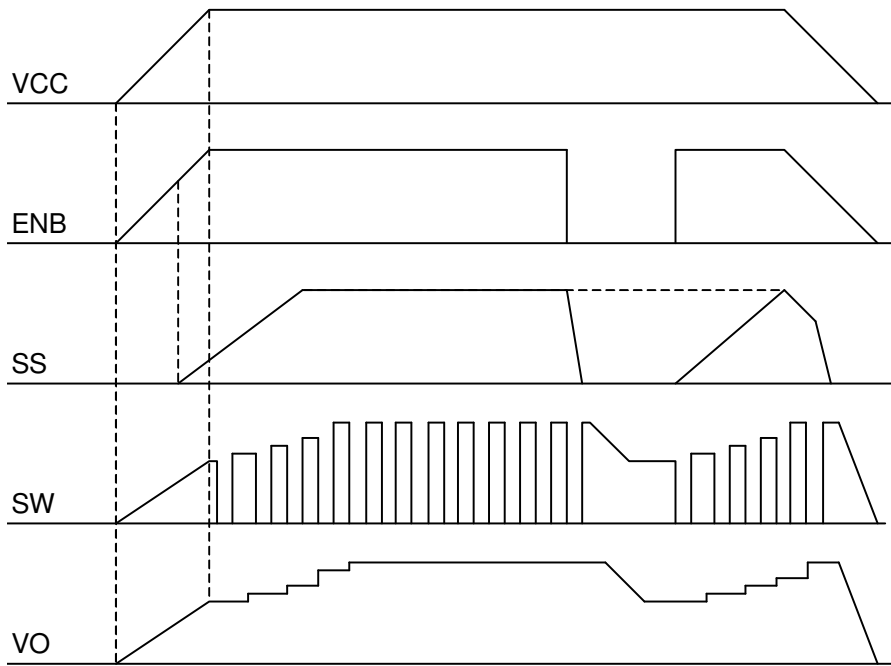


Fig. 21 Startup Sequence Waveform

Overcurrent protection operating

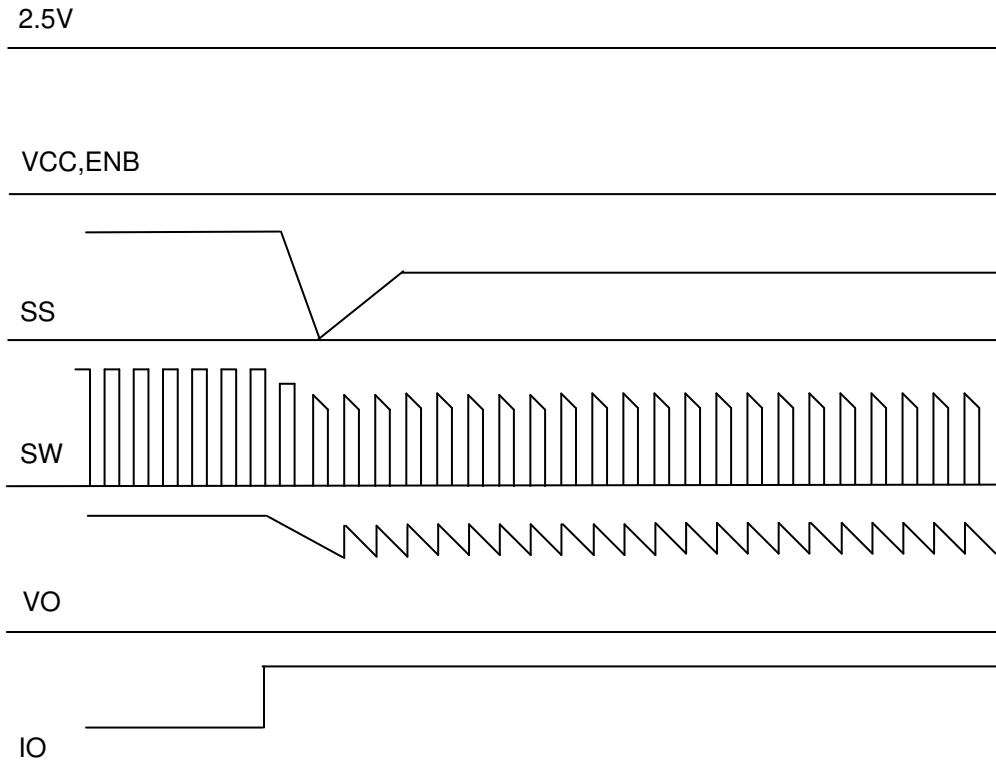


Fig. 22 Overcurrent Protection Operating Waveform

●Selecting Application Components

(1) Setting the output L constant

The coil L to use for output is decided by the rating current I_{LR} and input current maximum value I_{INMAX} of the coil.

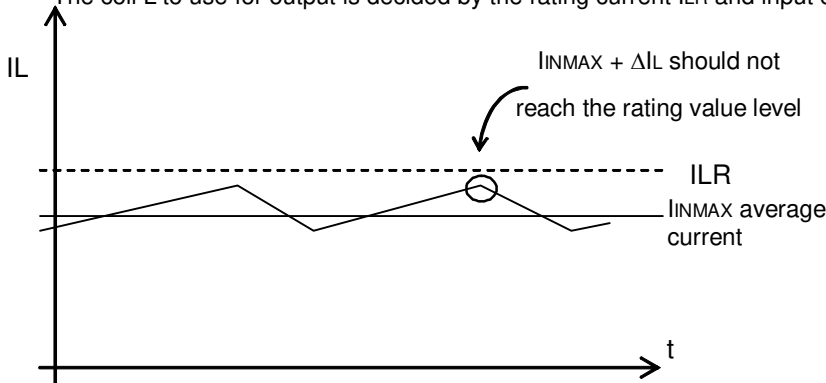


Fig. 23 Coil current waveform

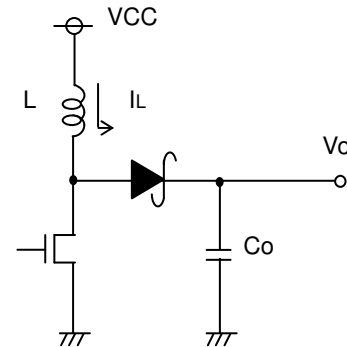


Fig. 24 Output Application Circuit Diagram

Adjust so that $I_{INMAX} + \Delta I_L$ does not reach the rating current value I_{LR} . At this time, ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times V_{CC} \times \frac{V_o - V_{CC}}{V_o} \times \frac{1}{f} \quad [A] \quad \text{Where, } f \text{ is the switching frequency.}$$

Set with sufficient margin because the coil L value may have the dispersion of approx. $\pm 30\%$. If the coil current exceeds the rating current I_{LR} of the coil, it may damage the IC internal element.

BD8152FVM, BD8158FVM use the current mode DC/DC converter control and has the optimized design at the coil value. The following coil values are recommended from the aspects of power efficiency, response and safety. When the coil out of this range is selected, the stable continual operation is not guaranteed such as the switching waveform becomes irregular. Please pay attention to it.

Switching frequency: L = 10 μ H to 22 μ H at 600 kHz

Switching frequency: L = 4.7 μ H to 15 μ H at 1,200 kHz

(2) Setting the output capacitor

For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} allowance value and the drop voltage allowance value at the time of sudden load change. Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = I_{LMAX} \times RESR + \frac{1}{fC_o} \times \frac{V_{CC}}{V_o} \times \left(I_{LMAX} - \frac{\Delta I_L}{2} \right) \quad [V] \quad \text{Where, } f \text{ is the switching frequency.}$$

Perform setting so that the voltage is within the allowable ripple voltage range.

For the drop voltage during sudden load change; V_{DR} , please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{C_o} \times 10 \mu \text{sec} \quad [V]$$

However, 10 μ s is the rough calculation value of the DC/DC response speed. Please set the capacitance considering the sufficient margin so that these two values are within the standard value range.

(3) Selecting the input capacitor

Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the input side. For this reason, the low ESR capacitor is recommended as an input capacitor which has the value more than 10 μ F and less than 100 m Ω . If a capacitor out of this range is selected, the excessive ripple voltage is superposed on the input voltage, accordingly it may cause the malfunction of IC.

However these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform the margin check using the actual product.

(4) Selecting the output rectification diode

Schottky barrier diode is recommended as the rectification diode to use at the DC/DC converter output stage. Select the diode paying attention to the max. inductor current and max. output voltage.

$$\begin{aligned} \text{Max. Inductor current} & \quad I_{INMAX} + \Delta I_L < \text{Rating current of diode} \\ \text{Max. output voltage } V_{OMAX} & < \text{Rating voltage of diode} \end{aligned}$$

Since each parameter has 30% to 40% of dispersion, be sure to design providing sufficient margins.

(5) Design of the feedback resistor constant

Refer to the following equation to set the feedback resistor. As the setting range, 10 kΩ to 330 kΩ is recommended. If the resistor is set to 10 kΩ or lower, it causes the reduction of power efficiency. If it is set to 330 kΩ or larger, the offset voltage becomes larger by the input bias current 0.4 μA (Typ.) in the internal error amp.

$$V_o = \frac{R_8 + R_9}{R_9} \times 1.245 \quad [V]$$

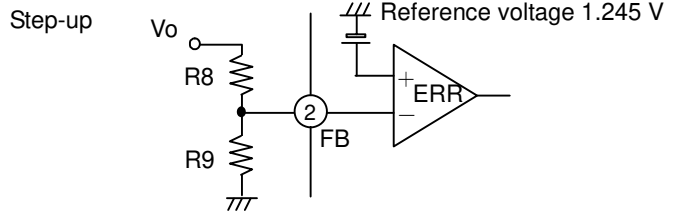


Fig. 25 Feedback Resistor Setting

(6) Setting the soft start time

Soft start is required to prevent the coil current at the time of startup from increasing and the overshoot of the output voltage at the starting time. Fig.26 shows the relation between the capacitance and soft start time. Please refer to it to set the capacitance.

As the capacitance, 0.001 μF to 0.1 μF is recommended. If the capacitance is set to 0.001 μF or lower, the overshooting may occur on the output voltage. If the capacitance is set to 0.1 μF or larger, the excessive back current flow may occur in the internal parasitic elements when the power is turned off and it may damage IC. When the capacitor to 0.1 μF or larger is used, be sure to insert a diode to VCC in series, or a bypass diode between the SS pin and VCC.

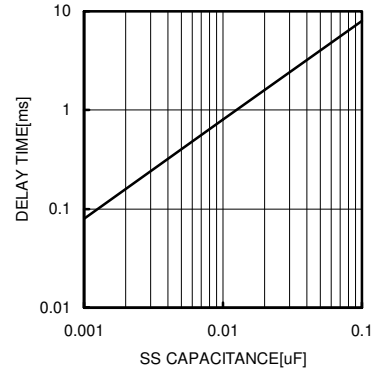


Fig. 26 SS Pin Capacitance vs Delay Time

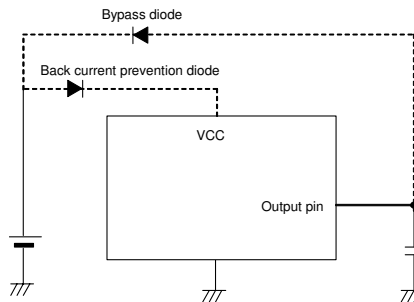


Fig. 27 Bypass Diode Example

When there is the startup relation (sequences) with other power supplies, be sure to use the high accuracy product (such as X5R). Soft start time may vary according to the input voltage, output voltage, loads, coils and output capacity. Be sure to verify the operation using the actual product.

(7) Setting the ENB pin

When the ENB pin is set to Hi, the internal circuit becomes active and the DC/DC converter starts operating. When it is set to Low, the shut down is activated and all circuits will be turned off.

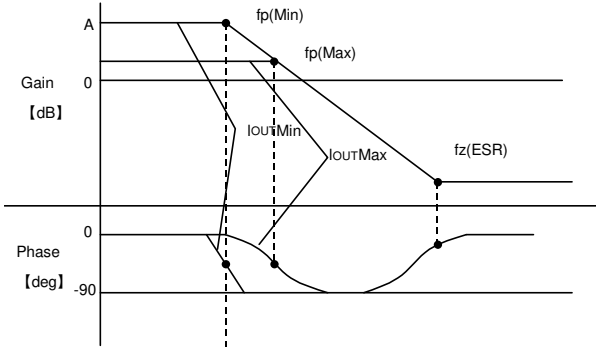
(8) Setting the frequency by FCLK

It is possible to change the switching frequency by setting the FCLK pin to Hi or Low. When it is set to Low, the product operates at 600 kHz (Typ.). When it is set to Hi, the product operates at 1,200 kHz (Typ.).

(9) Setting R_c, C_c of the phase compensation circuit

In the current mode control, since the coil current is controlled, a pole (phase lag) made by the CR filter composed of the output capacitor and load resistor will be created in the low frequency range, and a zero (phase lead) by the output capacitor and ESR of capacitor will be created in the high frequency range. In this case, to cancel the pole of the power amplifier, it is easy to compensate by adding the zero point with C_c and R_c to the output from the error amp as shown in the illustration.

Open loop gain



$$f_p = \frac{1}{2\pi \times R_o \times C_o} \quad [\text{Hz}]$$

$$f_z(\text{ESR}) = \frac{1}{2\pi \times \text{ESR} \times C_o} \quad [\text{Hz}]$$

Pole at the power amplification stage

When the output current reduces, the load resistance R_o increases and the pole frequency lowers.

$$f_p(\text{Min}) = \frac{1}{2\pi \times R_{o\text{Max}} \times C_o} \quad [\text{Hz}] \leftarrow \text{At light-load}$$

$$f_z(\text{Max}) = \frac{1}{2\pi \times R_{o\text{Min}} \times C_o} \quad [\text{Hz}] \leftarrow \text{At heavy-load}$$

Zero at the power amplification stage

When the output capacitor is set larger, the pole frequency lowers but the zero frequency will not change. (This is because the capacitor ESR becomes 1/2 when the capacitor becomes 2 times.)

$$f_p(\text{Amp.}) = \frac{1}{2\pi \times R_c \times C_c} \quad [\text{Hz}]$$

Error amp phase compensation

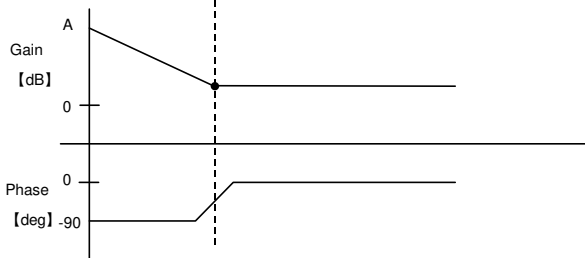


Fig. 28 Gain vs Phase

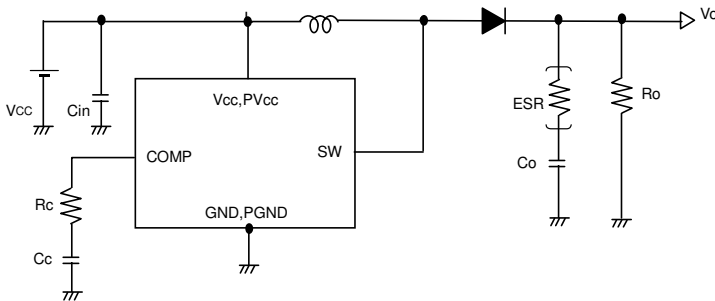


Fig. 29 Application Circuit Diagram

It is possible to realize the stable feedback loop by canceling the pole f_p (Min.), which is created by the output capacitor and load resistor, with CR zero compensation of the error amp as shown below.

$$f_z(\text{Amp.}) = f_p(\text{Min.})$$

$$\longrightarrow \frac{1}{2\pi \times R_c \times C_c} = \frac{1}{2\pi \times R_{o\text{max}} \times C_o} \quad [\text{Hz}]$$

As the setting range for the resistor, 1 kΩ to 10 kΩ is recommended. When the resistor is set to 1 kΩ or lower, the effect by phase compensation becomes low and it may cause the oscillation of output voltage. When it is set to 10 kΩ or larger, the COMP pin becomes Hi-Z and the switching noise becomes easy to superpose. Therefore the stable switching pulse cannot be generated and the irregular ripple voltage may be generated on the output voltage.

As the setting range for the capacitance, 3,300 pF to 10,000 pF is recommended. When the capacitance is set to 3,300 pF or lower, the irregular ripple voltage may be generated on the output voltage due to the effect of switching noise. When it is set to 10,000 pF or larger, the response becomes worse and the output voltage fluctuation becomes large. Accordingly it may require the output capacitor which is larger than the necessary value.

●Application Examples

Although ROHM is sure that the application examples are recommendable ones, further check the characteristics of components that require high precision before using them.

When a circuit is used modifying the externally connected circuit constant, be sure to decide allowing sufficient margins considering the dispersion of values by external parts as well as our IC including not only the static but also the transient characteristic. For the patent, we have not acquired the sufficient confirmation. Please acknowledge the status.

(1) When the charge pump is removed from the DC/DC converter to make it 3-channel output mode:

It is possible to create the charge pump by using the switching operation of DC/DC converter. When the application shown in the following diagram is used, 1-channel DC/DC converter output, 1-channel positive side charge pump and 1-channel negative side charge pump can be output as a total of 3-channels.

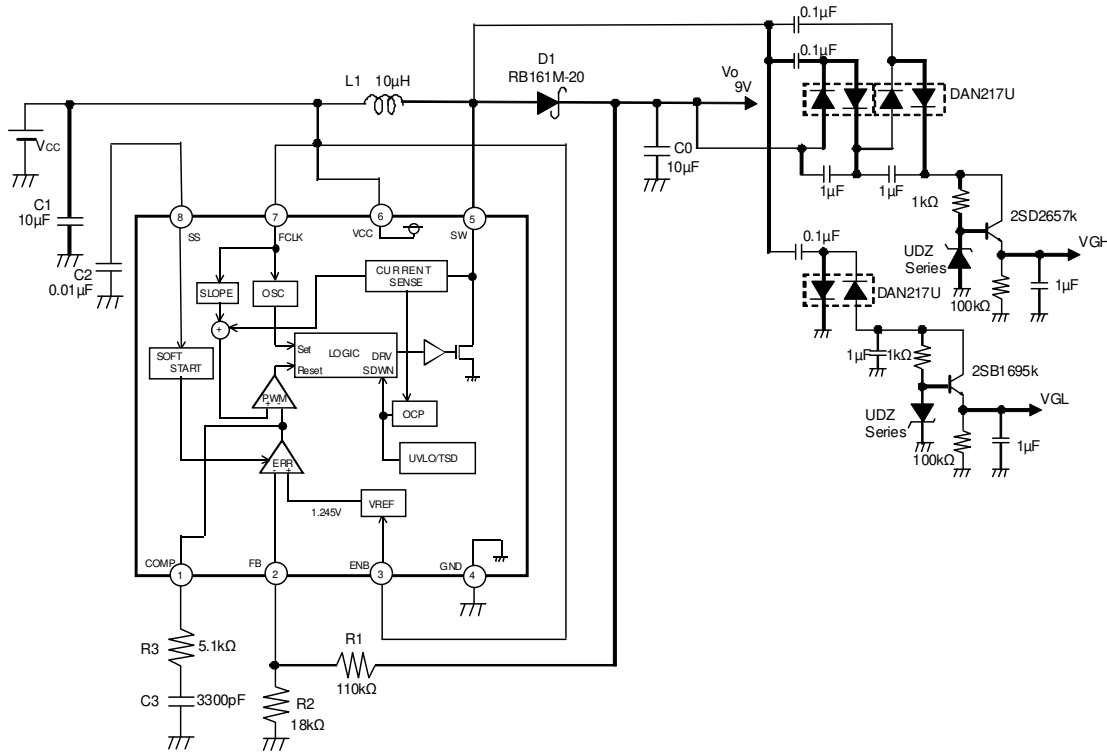


Fig. 30 3ch Application Circuit Diagram Example

(2) When the output voltage is set to 0 V:

Since the switch does not exist between the input and output in the application using the step-up type DC/DC converter, the output voltage is generated even if the IC is turned off. When it is intended to keep the output voltage 0 V until IC operates, insert the switch as shown in the following circuit diagram.

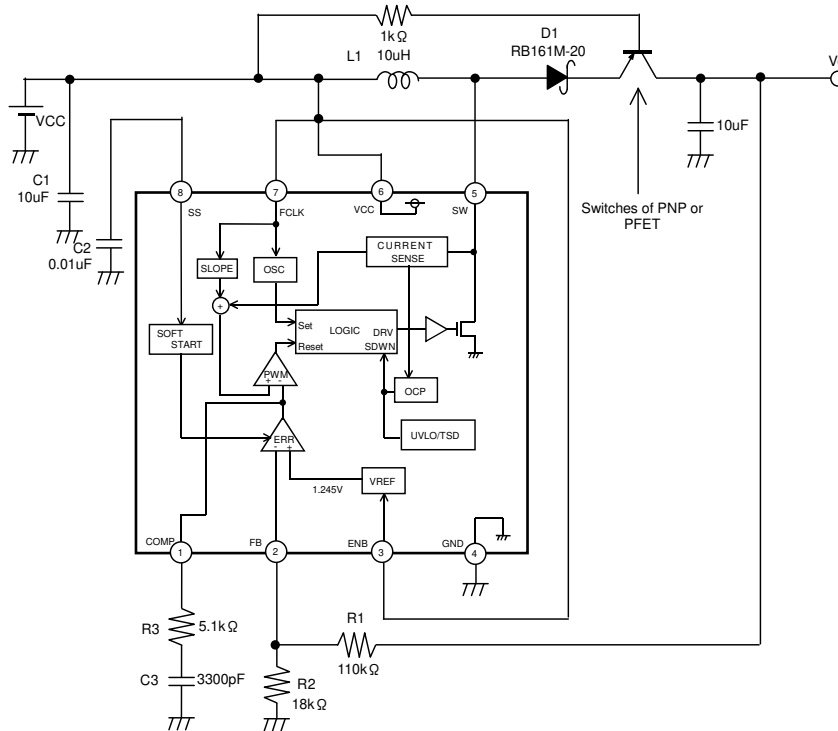


Fig. 31 Switch Application Circuit Diagram Example

● Application Examples

(3) When the circuit is intended to operate at the lower voltage than the IC operating range:

Although the recommended operating range of IC starts from 2.5 V / 2.1 V (BD8152FVM, BD8158FVM), it is possible to continue operating by composing the self-energizing type step-up DC/DC converter application even if the input voltage lowered than 2.1 V. This example is recommended for the application with battery input.

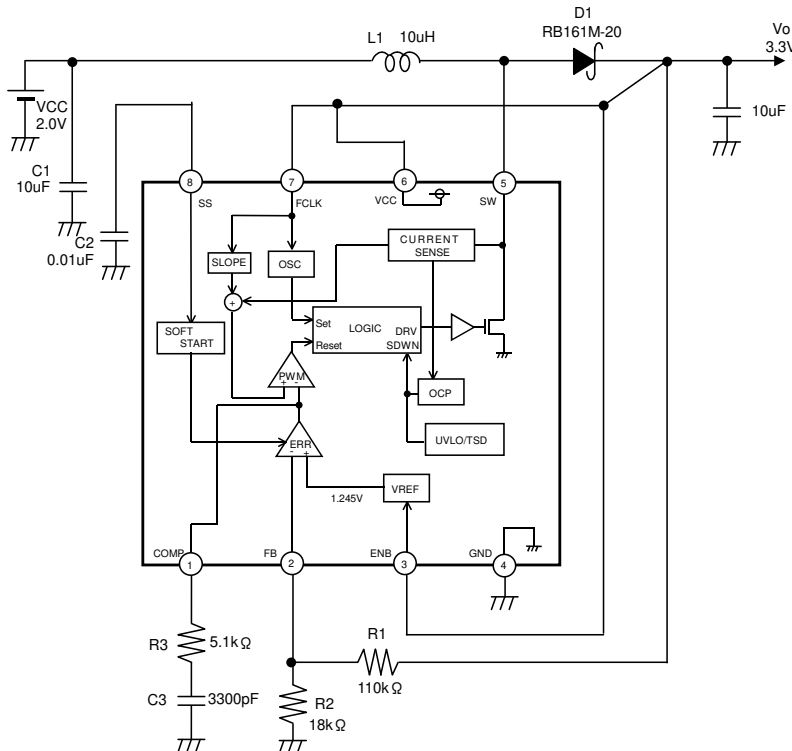


Fig. 32 Self-Energizing Application Circuit Diagram Example

(4) SEPIC type application

When it is intended to compose the step-up type DC/DC converter, the SEPIC type application is recommended. Since the switching voltage is generated by the value of input voltage + output voltage, pay utmost attention to the withstand voltage of SW pin.

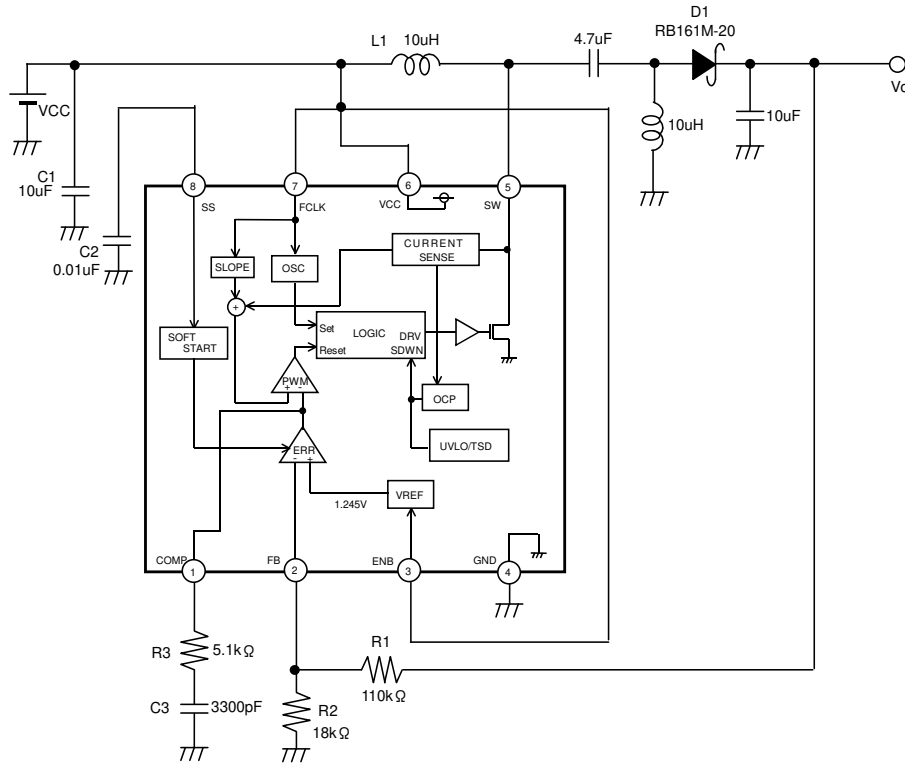


Fig. 33 SEPIC Application Circuit Diagram Example

(5) When the Supply Voltage is over 4.0 V (BD8158FVM only)

The Capacitor C4 is inserted to COMP pin, and it operates when the Supply Voltage is over 4.0 V. In this case, Switching Frequency is limited to 600kHz.

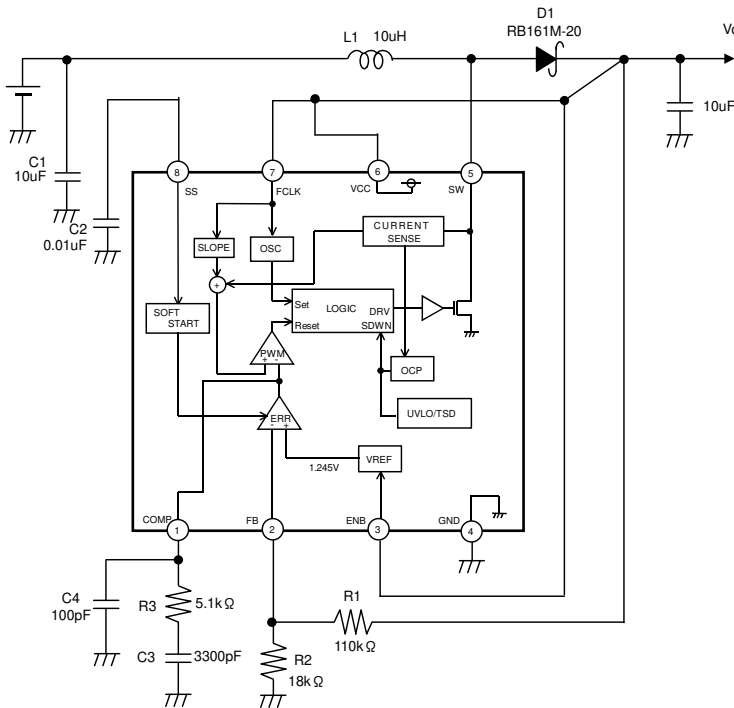


Fig.34 Circuit Diagram Example(Supply Voltage over 4.0 V)

● I/O Equivalent Circuit Diagrams

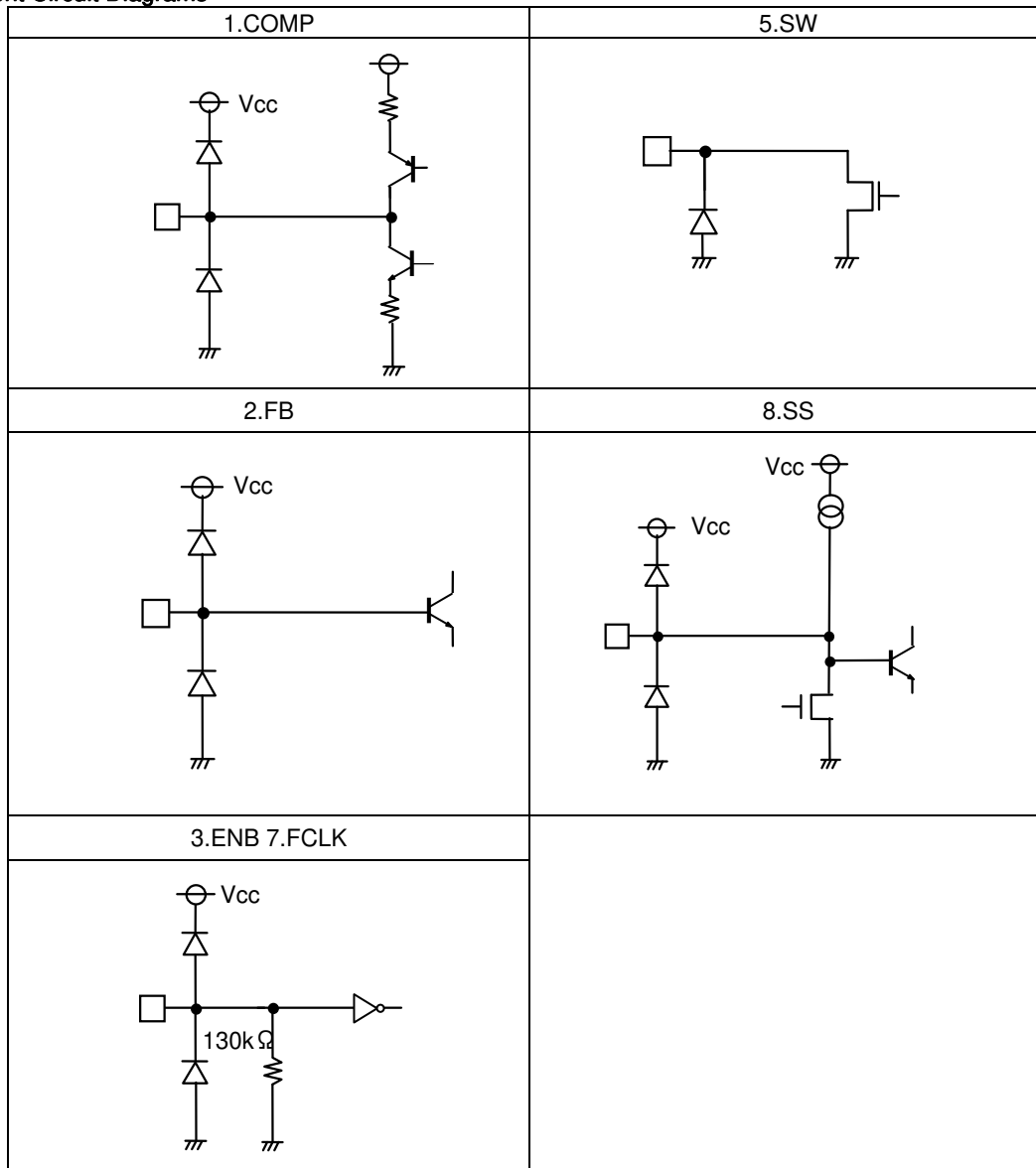


Fig. 34 I/O Equivalent Circuit Diagram

● Notes of Use

- 1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.
- 2) GND potential
Ensure a minimum GND pin potential in all operating conditions.
- 3) Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
- 4) Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on an application board. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.
- 5) Action in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, when the resistors and transistors are connected to the pins as shown in Fig. 35, a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as the application of voltages lower than the GND (P substrate) voltage to input and output pins.

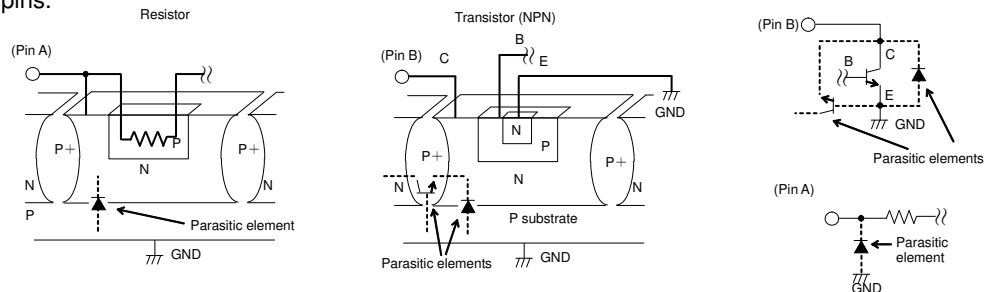


Fig.35 Example of a Simple Monolithic IC

9) Overcurrent protection circuits

An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC destruction that may result in the event of load shortening. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capability has negative characteristics to temperatures.

10) Thermal shutdown circuit (TSD)

This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's temperature T_j will trigger the temperature protection circuit to turn off all output power elements. The circuit automatically resets once the chip's temperature T_j drops. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11) Testing on application boards

At the time of inspection of the installation boards, when the capacitor is connected to the pin with low impedance, be sure to discharge electricity per process because it may load stresses to the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

● Power Dissipation Reduction

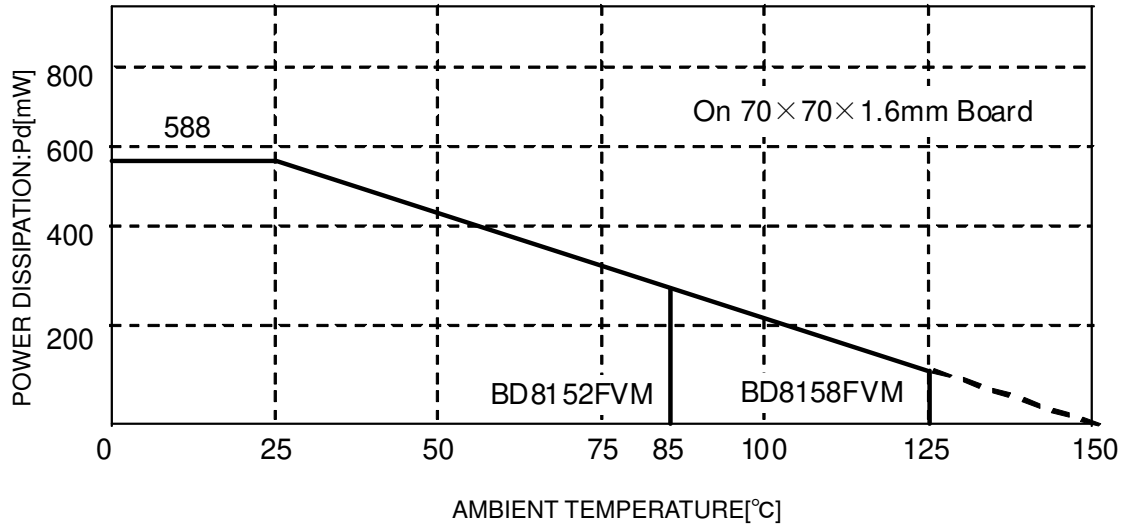
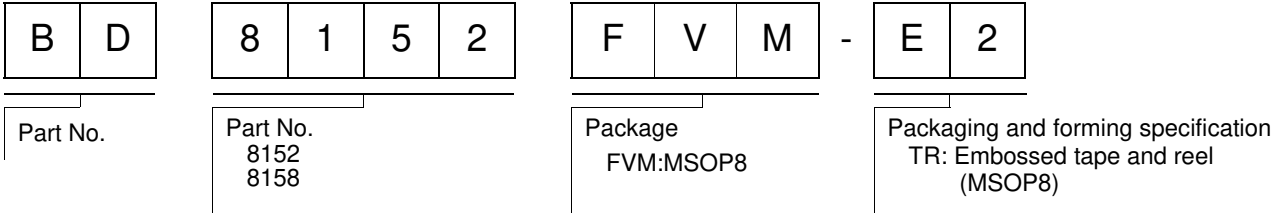
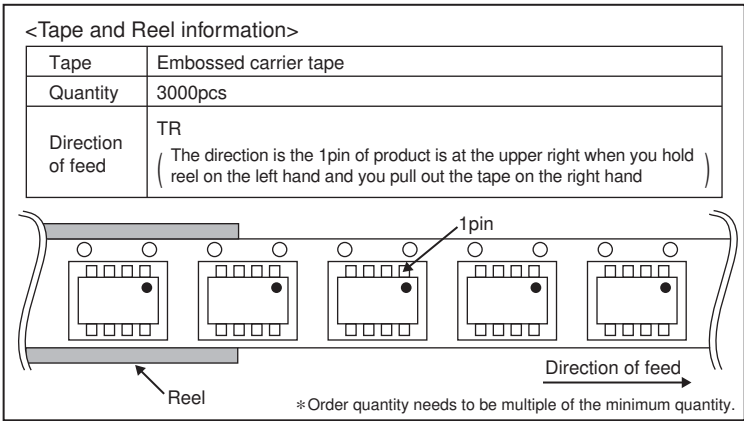
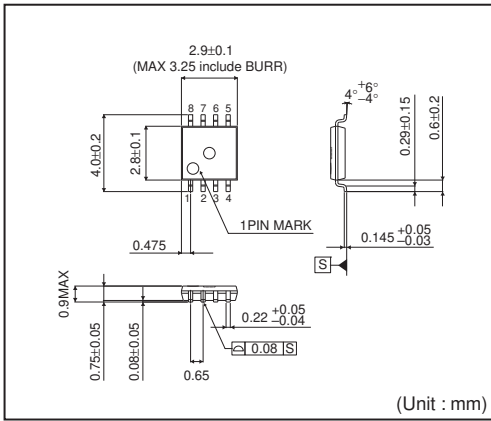


Fig. 36 Power Dissipation Reduction

●Ordering part number



MSOP8



Notes

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