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Power Supply IC Series for TFT-LCD Panels

5V Input Multi-channel System Power Supply IC


BD8153EFV

No.09035JBT09

●Description

The BD8153EFV is a system power supply IC for TFT panels. A 1-chip IC providing a total of four voltages required for TFT panels, i.e., logic voltage, source voltage, gate high-level, and gate low-level voltage, thus constructing a TFT panel power supply with minimal components required.

●Features (BD8153EFV)

- 1) Operates in an operating voltage range as low as 2.1 V to 6.0 V.
- 2) Incorporates a step-up DC/DC converter.
- 3) Incorporates a 3.3-V regulator.
- 4) Incorporates positive and negative-side charge pumps.
- 5) Switching frequency of 1100 kHz
- 6) DC/DC converter feedback voltage of $1.24\text{ V} \pm 1\%$
- 7) Incorporates a gate shading function
- 8) Under-voltage lockout protection circuit
- 9) Thermal shutdown circuit
- 10) Overcurrent protection circuit
- 11) HTSSOP-B24 package

●Applications

Liquid crystal TV, PC monitor, and TFT-LCD panel

●Absolute maximum ratings (Ta = 25°C)

| Parameter | Symbol | Limit | Unit |
|------------------------------|--------|------------|------|
| Power supply voltage | VCC | 7 | V |
| Vo1 voltage | Vo1 | 19 | V |
| Vo2 voltage | Vo2 | 32 | V |
| SW voltage | Vsw | 19 | V |
| Maximum junction temperature | Tjmax | 150 | °C |
| Power dissipation | Pd | 1100* | mW |
| Operating temperature range | Topr | -40 to 125 | °C |
| Storage temperature range | Tstg | -55 to 150 | °C |

* Reduced by 4.7 mW/°C over 25°C, when mounted on a glass epoxy board.
(70 mm × 70 mm × 1.6 mm).

●Recommended Operating Ranges

| Parameter | Symbol | Limit | | Unit |
|----------------------|--------|-------|-----|------|
| | | MIN | MAX | |
| Power supply voltage | VCC | 2.1 | 6 | V |
| Vo1 voltage | Vo1 | 8 | 18 | V |
| SW voltage | Vsw | — | 18 | V |
| SW Current | Isw | — | 1.8 | A |
| Vo2 voltage | Vo2 | — | 30 | V |

● Electrical Characteristics (Unless otherwise specified, VCC = 5 V; Vo1 = 15 V; Vo2 = 25 V; Ta = 25°C)

1 DC/DC Converter Block

| Parameter | Symbol | Limit | | | Unit | Conditions |
|--------------------------|--------------------|-------|-------|-------|------|---|
| | | Min. | Typ. | Max. | | |
| [Soft start] | | | | | | |
| Source current | I _{so} | 6 | 10 | 14 | μA | V _{ss} = 0.5 V |
| Sinking current | I _{si} | 0.1 | 0.2 | 1.0 | mA | V _{ss} = 0.5 V, VDD = 1.65 V |
| [Error amp] | | | | | | |
| Input bias current 1 | I _{FB1} | — | 0.1 | 0.5 | μA | |
| Feedback voltage 1 | V _{FB1} | 1.227 | 1.240 | 1.253 | V | Buffer |
| Voltage gain | A _V | — | 200 | — | V/V | * |
| Sinking current | I _{ol} | 25 | 50 | 100 | μA | V _{FB} = 1.5 V V _{COMP} = 0.5 V |
| Source current | I _{oo} | -100 | -50 | -25 | μA | V _{FB} = 1.0 V V _{COMP} = 0.5 V |
| [SW] | | | | | | |
| ON resistance N-channel | R _{ON_N} | 50 | 200 | 600 | mΩ | * |
| Leak current N-channel | I _{LEAKN} | — | — | 10 | μA | V _{sw} = 18 V |
| Maximum duty cycle | D _{MAX} | 75 | 85 | 95 | % | |
| [Overcurrent protection] | | | | | | |
| Saw current limit | I _{sw} | 2 | 3 | — | A | * |

2. Regulator controller

| Parameter | Symbol | Limit | | | Unit | Conditions |
|------------------------------------|-------------------|-------|------|------|------|----------------------------------|
| | | Min. | Typ. | Max. | | |
| [Error amp] | | | | | | |
| VDD voltage | VDD | 3.2 | 3.3 | 3.4 | V | |
| Maximum base current | I _{BMAX} | 4 | 7 | 11 | mA | |
| Line regulation | Reg _I | — | 10 | 30 | mV | VCC = 4.5 V to 5.5 V |
| Load regulation | Reg _L | — | 10 | 50 | mV | I _o = 10 mA to 100 mA |
| [Under-voltage lockout protection] | | | | | | |
| Off threshold voltage | V _{ROFF} | 1.7 | 1.8 | 1.9 | V | |
| On threshold voltage | V _{RON} | 1.6 | 1.7 | 1.8 | V | |

○ This product is not designed for protection against radio active rays.

* Design guarantee (No total shipment inspection is made.)

●Electrical Characteristics (Unless otherwise specified, VCC = 5 V; Vo1 = 15 V; Vo2 = 25 V; Ta = 25°C)

3.Charge pump

| Parameter | Symbol | Limit | | | Unit | Conditions |
|-------------------------|-----------------------|-----------|-------|-----------|------|---------------|
| | | Min. | Typ. | Max. | | |
| [Error amp] | | | | | | |
| Input bias current 2 | IFB2 | — | 0.1 | 0.5 | μA | |
| Input bias current 3 | IFB3 | — | 0.1 | 0.5 | μA | |
| Feedback voltage 2 | VFB2 | 1.183 | 1.240 | 1.307 | V | |
| Feedback voltage 3 | VFB3 | 0.15 | 0.2 | 0.25 | V | |
| [Delay start block] | | | | | | |
| Source current | IDSO | 3 | 5 | 7 | μA | VDLS = 0.5V |
| Sinking current | IDSI | 0.1 | 0.5 | 1.0 | mA | VDLS = 0.5V |
| Startup voltage | VST | 0.45 | 0.60 | 0.75 | V | |
| [Switch] | | | | | | |
| ON resistance N-channel | RON_NC | 0.5 | 2 | 4 | Ω | Io = 10 mA * |
| ON resistance P-channel | RON_PC | 0.5 | 4 | 8 | Ω | Io = -10 mA * |
| [Diode] | | | | | | |
| Voltage of diode | Vf | 600 | 710 | 800 | mV | Io = 10 mA |
| [Gate shading block] | | | | | | |
| ON resistance N-channel | RON_NGS | 2 | 10 | 20 | Ω | Io = 10 mA * |
| ON resistance P-channel | RON_PGS | 2 | 10 | 20 | Ω | Io = -10 mA * |
| Leak current N-channel | I _{LEAK_NGS} | — | — | 10 | μA | |
| Leak current P-channel | I _{LEAK_PGS} | — | — | 10 | μA | |
| High voltage | IGH | VDD × 0.7 | VDD | — | V | |
| Low voltage | IGL | — | 0 | VDD × 0.3 | V | |
| Input current | IIG | 8 | 16.5 | 30 | μA | IG = 3.3 V |

4.Overall

| Parameter | Symbol | Limit | | | Unit | Conditions |
|-----------------------------|--------|-------|-------|-------|------|--------------|
| | | Min. | Typ. | Max. | | |
| [Reference block] | | | | | | |
| Reference voltage | VREF | 1.215 | 1.240 | 1.265 | V | |
| Drive current | IREF | — | 23 | — | mA | VREF = 0 V |
| Load regulation | ΔV | — | 1 | 10 | mV | IREF = -1 mA |
| [Oscillator] | | | | | | |
| Oscillating frequency | Fosc | 0.94 | 1.1 | 1.265 | MHz | |
| [Oscillator] | | | | | | |
| DET 1 On threshold voltage | VDON1 | 1.7 | 1.8 | 1.9 | V | |
| DET 1 Off threshold voltage | VDOFF1 | 1.6 | 1.7 | 1.8 | V | |
| DET 2 On threshold voltage | VDON2 | 1.02 | 1.12 | 1.22 | V | |
| DET 2 Off threshold voltage | VDOFF2 | 0.90 | 1.00 | 1.10 | V | |
| DET 3 On threshold voltage | VDON3 | 0.25 | 0.30 | 0.35 | V | |
| DET 3 Off threshold voltage | VDOFF3 | 0.35 | 0.41 | 0.47 | V | |
| DET 4 On threshold voltage | VDON4 | 1.02 | 1.12 | 1.22 | V | |
| DET 4 Off threshold voltage | VDOFF4 | 0.90 | 1.00 | 1.10 | V | |
| [Device] | | | | | | |
| Average circuit current | Icc | 0.5 | 2 | 5 | mA | No switching |

○This product is not designed for protection against radio active rays.

* Design guarantee (No total shipment inspection is made.)

● Reference Data (Unless otherwise specified, Ta = 25°C)

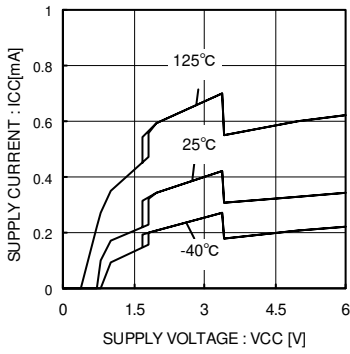


Fig. 1 Total Supply Current 1

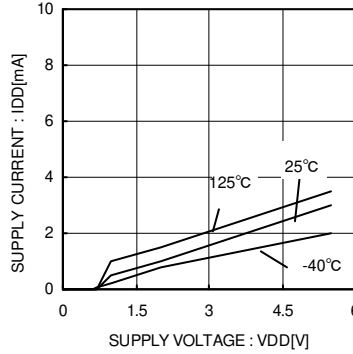


Fig. 2 Total Supply Current 2

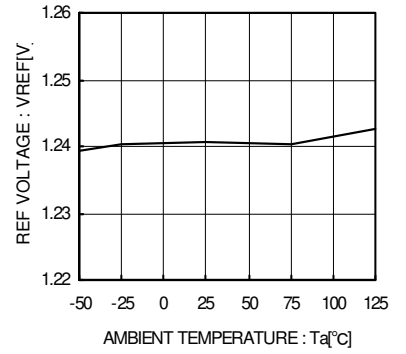


Fig. 3 Internal Reference Temperature

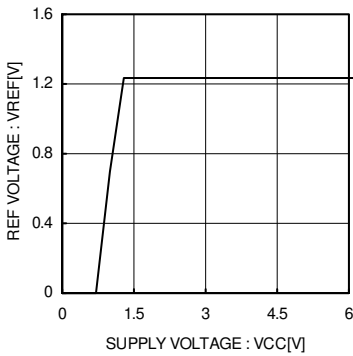


Fig. 4 Internal Reference Line Regulation

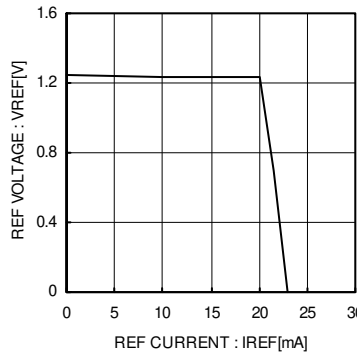


Fig. 5 Internal Reference Load Regulation

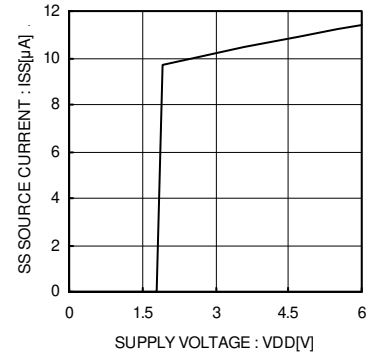


Fig. 6 SS Source Current

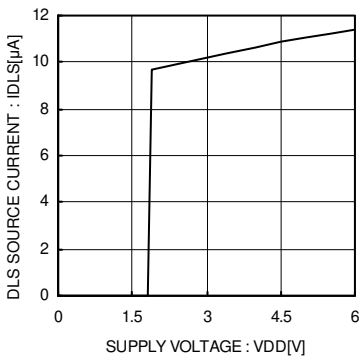


Fig. 7 DLS Source Current

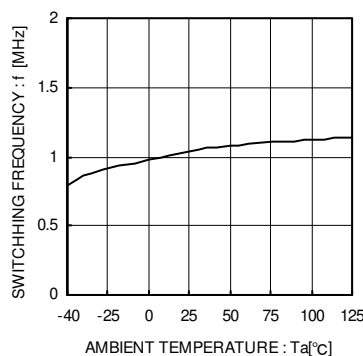


Fig. 8 Switching Frequency Temperature

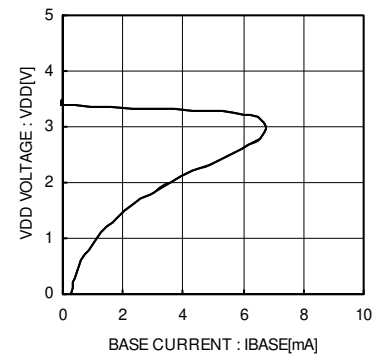


Fig. 9 REG Current Capacity

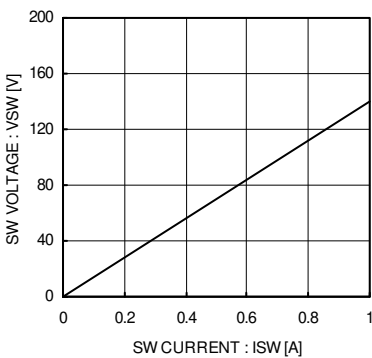


Fig. 10 SW On Resistance

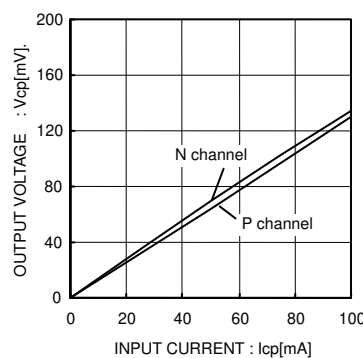


Fig. 11 Charge Pump On Voltage

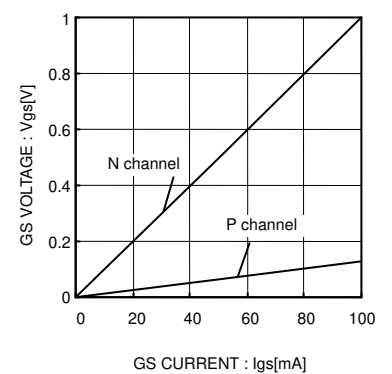


Fig. 12 Gate Shading On Voltage

●Reference Data (Unless otherwise specified, Ta = 25°C)

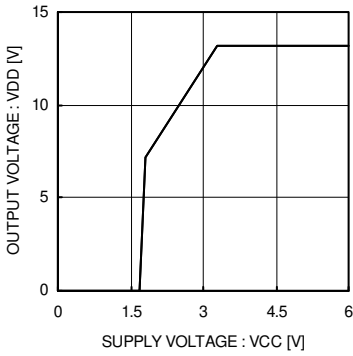


Fig. 13 Vo1 Line Regulation

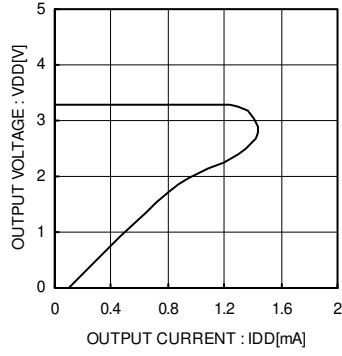


Fig. 14 VDD Load Regulation

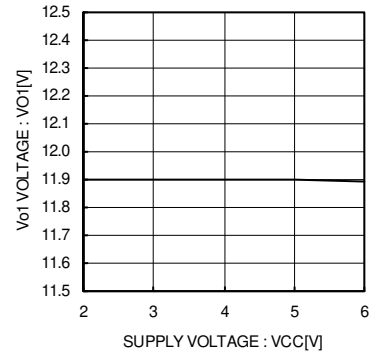


Fig. 15 Vo1 Line Regulation

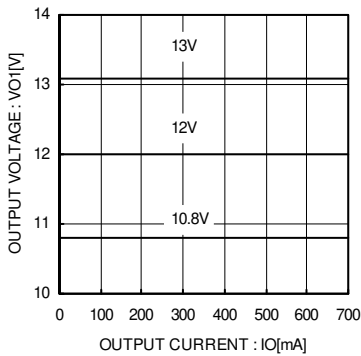


Fig. 16 Vo1 Load Regulation

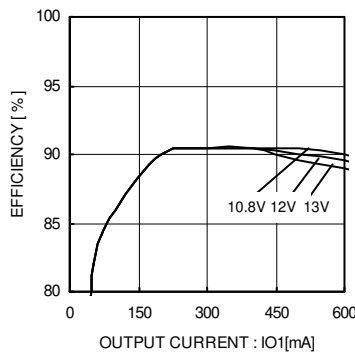


Fig. 17 Efficiency vs Output Current

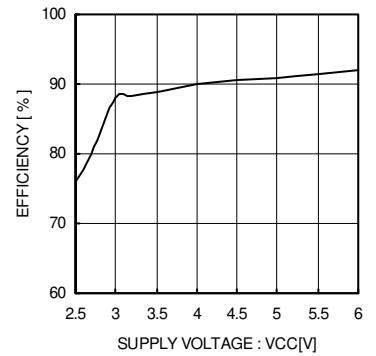


Fig. 18 Efficiency vs Power Supply Voltage

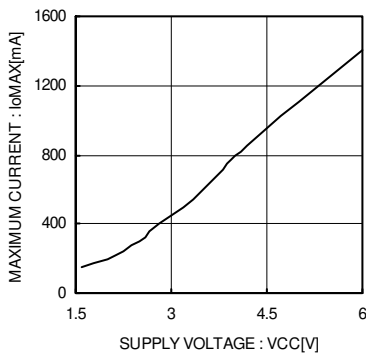


Fig. 19 Power Supply Voltage vs Max. Output Current Capacity

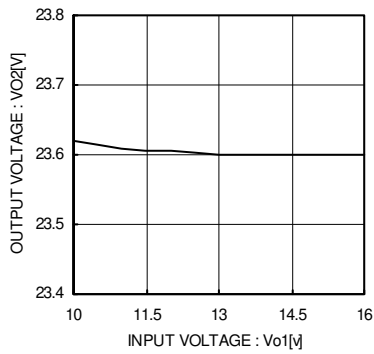


Fig. 20 Vo2 Line Regulation

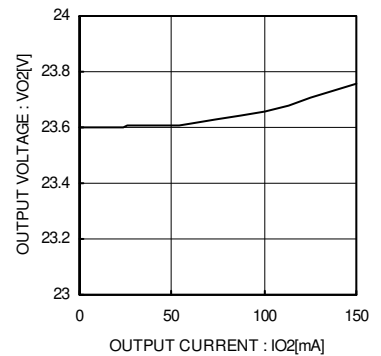


Fig. 21 Vo2 Load Regulation

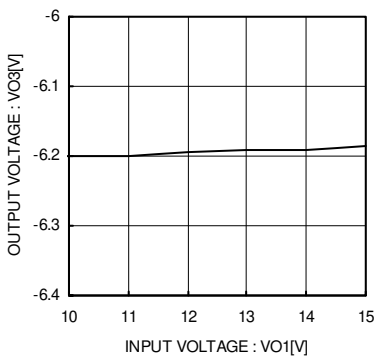


Fig. 22 Negative-side Charge Pump Line Regulation

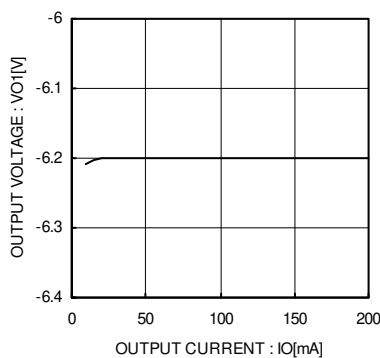


Fig. 23 Negative-side Charge Pump Load Regulation

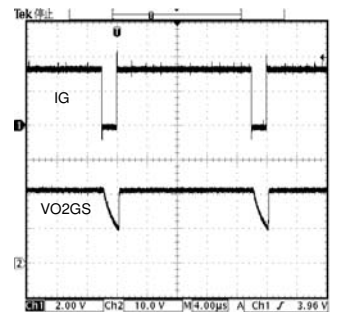
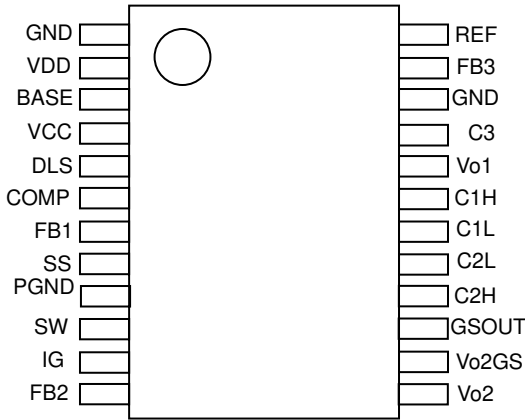


Fig. 24 Gate Shading Output Waveform

● Pin Assignments Diagram



● Block Diagram

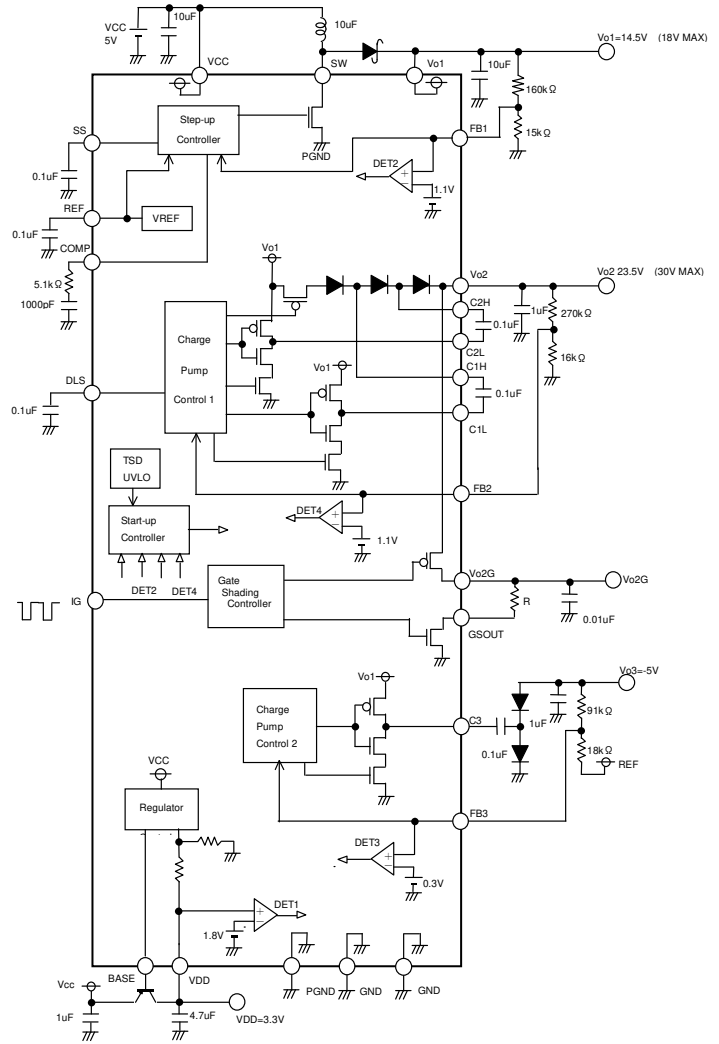


Fig. 25 Pin Arrangements and Block Diagram

● Pin Assignments and Function

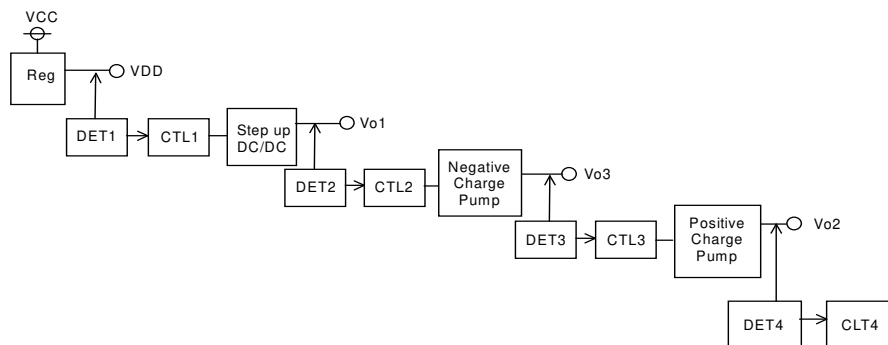
| PIN NO. | Pin name | Function | PIN NO. | Pin name | Function |
|---------|----------|--|---------|----------|--|
| 1 | GND | Ground pin | 13 | Vo2 | Positive-side charge pump output |
| 2 | VDD | LDO feedback input pin | 14 | Vo2GS | Gate shading source output pin |
| 3 | BASE | LDO base drive output pin | 15 | GSOUT | Gate shading sink output pin |
| 4 | VCC | Power supply input pin | 16 | C2H | Flying capacitor connection pin |
| 5 | DLS | Capacity connection pin for delay start | 17 | C2L | Flying capacitor connection pin |
| 6 | COMP | DC/DC difference amplifier output | 18 | C1L | Flying capacitor connection pin |
| 7 | FB1 | DC/DC feedback input | 19 | C1H | Flying capacitor connection pin |
| 8 | SS | Soft start capacitor connection pin | 20 | Vo1 | Negative-side charge pump power supply input pin |
| 9 | PGND | Ground pin | 21 | C3 | Negative-side charge pump driver output |
| 10 | SW | Switch output | 22 | GND | Ground pin |
| 11 | IG | Gate shading input | 23 | FB3 | Negative-side charge pump feedback input |
| 12 | FB2 | Positive-side charge pump feedback input | 24 | REF | Internal standard output pin |

●Block Function

- Step-up Controller
A controller circuit for DC/DC boosting.
The switching duty is controlled so that the feedback voltage FB1 is set to 1.24 V (typ.).
A soft start operates at the time of starting. Therefore, the switching duty is controlled by the SS pin voltage.
- Charge Pump Control 1
A controller circuit for the positive-side charge pump.
The switching amplitude is controlled so that the feedback voltage FB2 will be set to 1.24 V (typ.).
The start delay time can be set in the DLS terminal at the time of starting.
When the DLS voltage reaches 0.6 V (Typ.), switching waves will be output from the C1L and C2L pins.
- Charge Pump Control 2
A controller circuit for the negative-side charge pump.
The switching amplitude is controlled so that the feedback voltage FB2 will be set to 0.6 V (Typ.).
- Gate Shading Controller
A controller circuit of gate shading.
The Vo2GS and GSOUT are in on/off control according to IG pin input.
- Regulator Control
A regulator controller circuit for V_{DD} voltage generation.
The base pin current is controlled so that V_{DD} voltage will be set to 3.3 V (typ.).
- DET 1 to DET 4
A detection circuit of each output voltage. This detected signal is used for the starting sequential circuit.
- Start-up Controller
A control circuit for the starting sequence.
Controls to start in order of V_{CC} → V_{DD} → Vo₁ → Vo₃ → Vo₂.
- VREF
A block that generates internal reference voltage. 1.24V (Typ.) is output.
- TSD/UVLO
Thermal shutdown/Under-voltage lockout protection/circuit blocks.
The thermal shutdown circuit is shut down at an IC internal temperature of 175°C and reset at 160°C.
The under-voltage lockout protection circuit shuts down the IC when the V_{CC} is 1.8 V (typ.) or below.

●Starting sequence

For malfunction prevention, starting logic control operates so that each output will rise in order of V_{CC} → V_{DD} → Vo₁ → Vo₃ → Vo₂. As shown below, detectors DET1 to DET3 detect that the output on the detection side has reached 90% (typ.) of the set voltage, and starts the next block.



Starting sequence model

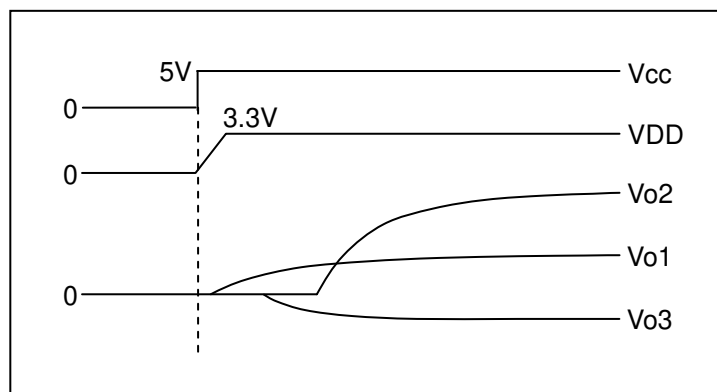


Fig. 26 Starting Timing Chart

●Selecting Application Components

(1) Setting the Output L Constant

The coil to use for output is decided by the rating current I_{LR} and input current maximum value I_{INMAX} of the coil.

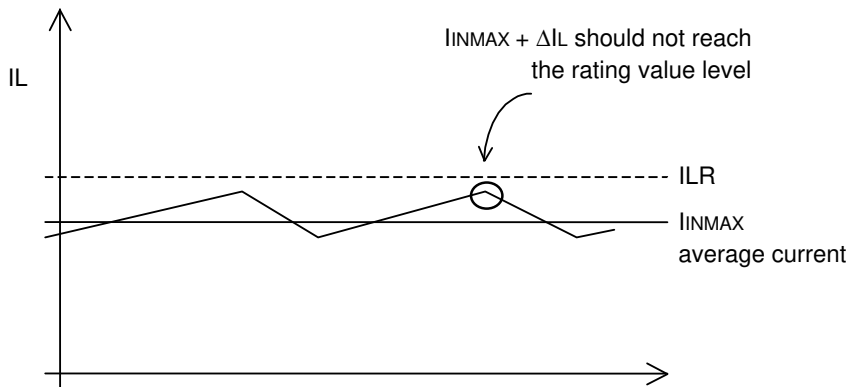


Fig. 27 Coil Current Waveform

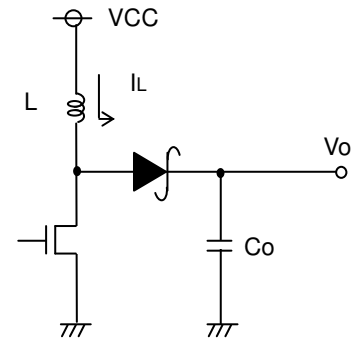


Fig. 28 Output Application Circuit Diagram

Adjust so that $I_{INMAX} + \Delta I_L$ does not reach the rating current value I_{LR} . At this time, ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} V_{CC} \times \frac{V_o - V_{CC}}{V_{CC}} \times \frac{1}{f} \quad [A] \quad \text{Here, } f \text{ is the switching frequency.}$$

Set with sufficient margin because the coil value may have the dispersion of $\pm 30\%$. If the coil current exceeds the rating current I_{LR} of the coil, it may damage the IC internal element.

BD8153EFV uses the current mode DC/DC converter control and has the optimized design at the coil value. A coil inductance (L) of 4.7 μH to 15 μH is recommended from viewpoints of electric power efficiency, response, and stability.

(2) Output Capacity Settings

For the capacitor to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} allowance value and the drop voltage allowance value at the time of sudden load change. Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = I_{LMAX} \times RESR + \frac{1}{f C_o} \times \frac{V_{CC}}{V_o} \times \left(I_{LMAX} - \frac{\Delta I_L}{2} \right) \quad [V] \quad \text{Here, } f \text{ is the switching frequency.}$$

Perform setting so that the voltage is within the allowable ripple voltage range.

For the drop voltage during sudden load change; V_{DR} , please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{C_o} \times 10 \text{ us} \quad [V]$$

However, 10 μs is the rough calculation value of the DC/DC response speed. Please set the capacitance considering the sufficient margin so that these two values are within the standard value range.

(3) Selecting the Input Capacitor

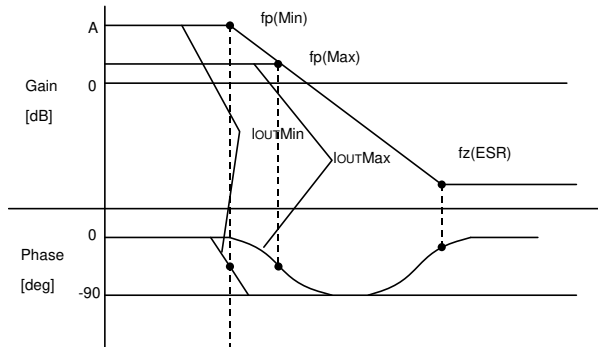
Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the input side. For the reason, the low ESR capacitor is recommended as an input capacitor which has the value more than 10 μF and less than 100 $\text{m}\Omega$. If a capacitor out of this range is selected, the excessive ripple voltage is superposed on the input voltage, accordingly it may cause the malfunction of IC.

However these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform the margin check using the actual product.

(4) Setting Rc, Cc of the Phase Compensation Circuit

In the current mode control, since the coil current is controlled, a pole (phase lag) made by the CR filter composed of the output capacitor and load resistor will be created in the low frequency range, and a zero (phase lead) by the output capacitor and ESR of capacitor will be created in the high frequency range. In this case, to cancel the pole of the power amplifier, it is easy to compensate by adding the zero point with Cc and Rc to the output from the error amp as shown in the illustration.

Open loop gain characteristics



$$F_p = \frac{1}{2 \pi \times R_o \times C_o} \text{ [Hz]}$$

$$f_z(\text{ESR}) = \frac{1}{2 \pi \times \text{ESR} \times C_o} \text{ [Hz]}$$

Pole at the power amplification stage

When the output current reduces, the load resistance R_o increases and the pole frequency lowers.

$$f_p(\text{Min}) = \frac{1}{2 \pi \times R_{o\text{Max}} \times C_o} \text{ [Hz]} \leftarrow \text{at light load}$$

$$f_p(\text{Max}) = \frac{1}{2 \pi \times R_{o\text{Min}} \times C_o} \text{ [Hz]} \leftarrow \text{at heavy load}$$

Zero at the power amplification stage

When the output capacitor is set larger, the pole frequency lowers but the zero frequency will not change. (This is because the capacitor ESR becomes 1/2 when the capacitor becomes 2 times.)

$$f_p(\text{Amp.}) = \frac{1}{2 \pi \times R_c \times C_c} \text{ [Hz]}$$

Error amp phase compensation characteristics

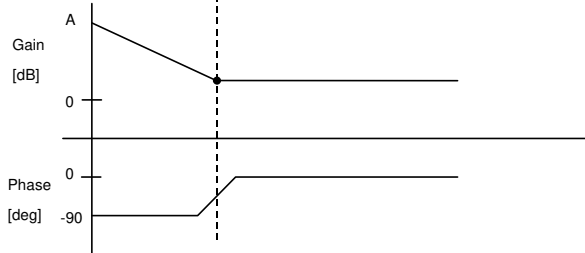


Fig. 29 Gain vs Phase

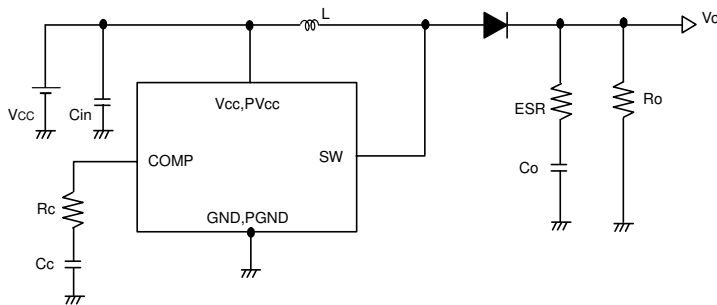


Fig. 30 Application Circuit Diagram

It is possible to realize the stable feedback loop by canceling the pole $f_p(\text{Min.})$, which is created by the output capacitor and load resistor, with CR zero compensation of the error amp as shown below.

$$f_z(\text{Amp.}) = f_p(\text{Min.})$$

$$\longrightarrow \frac{1}{2 \pi \times R_c \times C_c} = \frac{1}{2 \pi \times R_{o\text{max}} \times C_o} \text{ [Hz]}$$

(5) Regulator Controller Settings

The IC incorporates a 3.3-V regulator controller, and a regulator can be formed by using an external PNP transistor. Design the current capability of the regulator with a margin according to the following formula.

$$I_{MAX} = 7\text{mA} \times h_{fe} \quad [\text{A}]$$

The h_{fe} is the current gain of the external PNP transistor.
7 mA is the sinking current of the internal transistor.

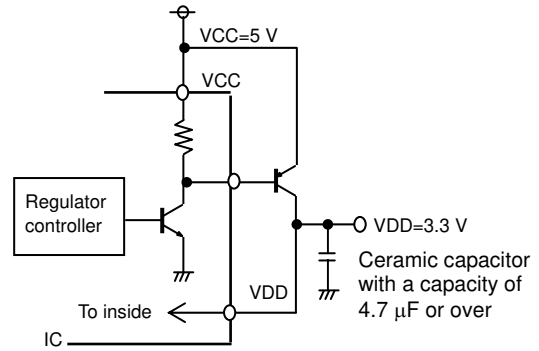


Fig.31

It is not necessary to use the regulator if the input voltage is 3.3 V. In that case, input 3.3 V to both VCC and VDD.

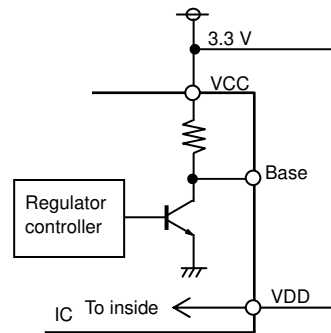


Fig.32

When incorporating a regulator into the external transistor, input the output voltage into the regulator.

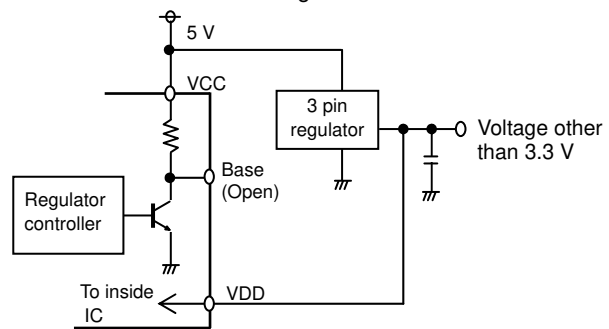


Fig.33

(6) Setting the Soft Start Time

Soft start is required to prevent the coil current at the time of start from increasing and the overshoot of the output voltage at the starting time. The relation between the capacity and soft start time is shown in the following figure. Refer to the figure and set capacity C1. Soft start is required to prevent the coil current at the time of start from increasing and the overshoot of the output voltage at the starting time. Fig. 34 shows the relation between the capacitance and soft start time. Please refer to it to set the capacitance.

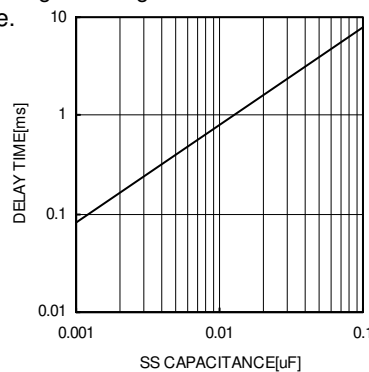


Fig. 34 SS Pin Capacitance vs Delay Time

As the capacitance, 0.001μF to 0.1μF is recommended. If the capacitance is set lower than 0.001μF, the overshooting may occur on the output voltage. If the capacitance is set larger than 0.1μF, the excessive back current flow may occur in the internal parasitic elements when the power is turned OFF and it may damage IC. When there is the activation relation (sequences) with other power supplies, be sure to use the high accuracy product (such as X5R). Soft start time may vary according to the input voltage, loads, coils and output capacity. Be sure to verify the operation using the actual product.

(7) Design of the Feedback Resistor Constant

Refer to the following equation to set the feedback resistor. As the setting range, 10 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 10 kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.4 μA(Typ.) in the internal error amplifier.

$$V_o = \frac{R8 + R9}{R9} \times 1.24 \quad [V]$$

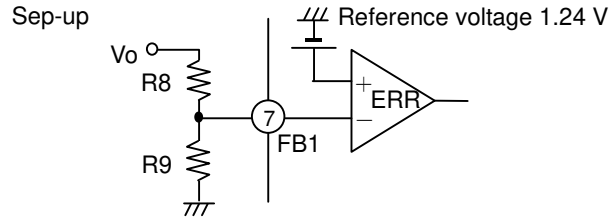


Fig. 35

(8) Positive-side Charge Pump Settings

BU8153EFV incorporates a charge pump controller, thus making it possible to generate stable gate voltage. The output voltage is determined by the following formula. As the setting range, 10 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 10kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.4 μA (Typ.) in the internal error amp.

$$V_o = \frac{R8 + R9}{R9} \times 1.24 \quad [V]$$

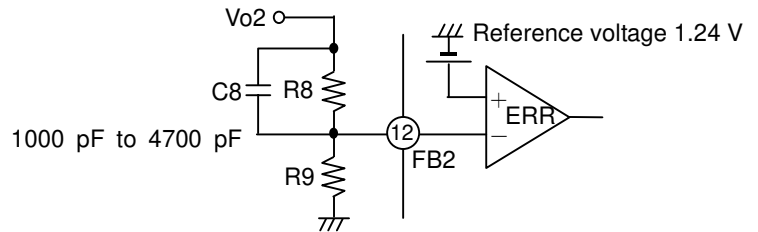


Fig. 36

In order to prevent output voltage overshooting, add capacitor C8 in parallel with R8. The recommended capacitance is 1000 pF to 4700 pF. If a capacitor outside this range is inserted, the output voltage may oscillate. By connecting capacitance to the DLS, a rising delay time can be set for the positive-side charge pump. The delay time is determined by the following formula.

- Delay time of charge pump block t_{DELAY}
 $t_{DELAY} = (C_{DLS} \times 0.6) / 5 \mu A [s]$
 where, C_{DLS} is the external capacitance.

(9) Negative-side Charge Pump Settings

BU8153EFV incorporates a charge pump controller for negative voltage, thus making it possible to generate stable gate voltage. The output voltage is determined by the following formula. As the setting range, 10 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 10 kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.4 μA (Typ.) in the internal error amp.

$$V_{o3} = - \frac{R6}{R7} \times 1.04 + 0.2 V \quad [V]$$

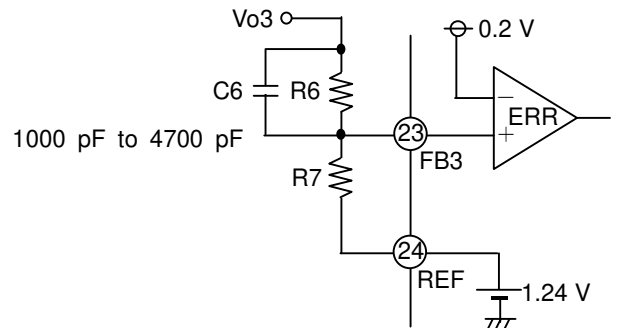


Fig.37

The delay time is internally fixed at 200 us.

In order to prevent output voltage overshooting, insert capacitor C6 in parallel with R6. The recommended capacitance is 1000 pF to 4700 pF. If a capacitor outside this range is inserted, the output voltage may oscillate.

●Gate Shading Setting Method

The IG input signal allows the high-level and low-level control of the positive-side gate voltage. The slope of output can be set by the external RC. The recommended resistance set value is 200 Ω to 5.1 kΩ and the recommended capacitor set value is 0.001 μF to 0.1 μF. The aggravation of efficiency may be caused if settings outside this range are made. Determine ΔV by referring to the following value. The following calculation formula is used for ΔV.

$$\Delta V = V_{o2GS} \left(1 - \exp \left(- \frac{t_{WL}}{CR} \right) \right) \quad [V]$$

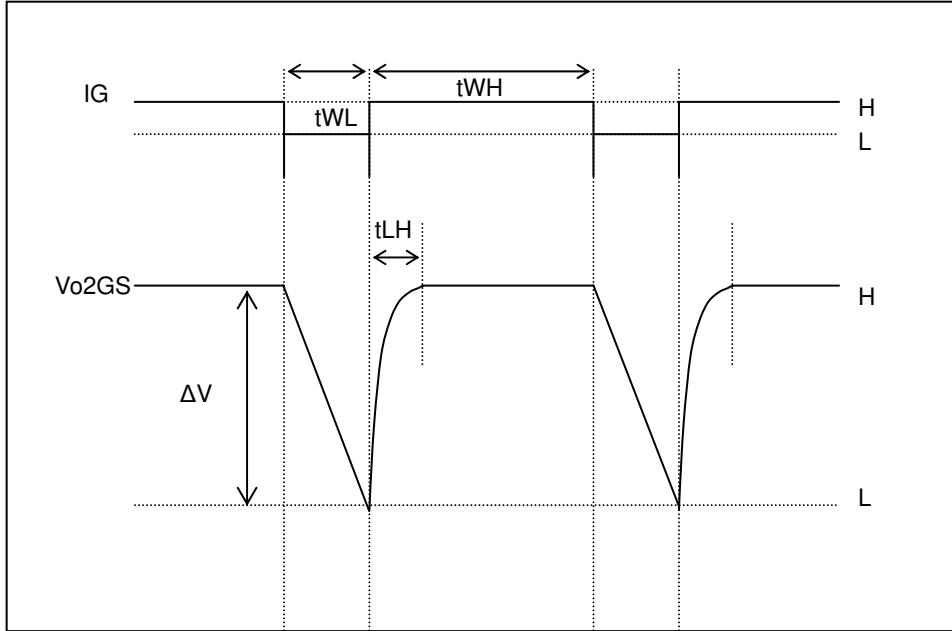


Fig. 38

| PARAMETER | SYMBOL | LIMIT | | | UNIT | CONDITION |
|-------------------------------------|--------|-------|-----|-----|------|--------------------------|
| | | MIN | TYP | MAX | | |
| IG "L" Time | tWL | 1 | 2 | - | μs | - |
| IG "H" Time | tWH | 1 | 18 | - | μs | - |
| Vo2GS "H" to "L" Voltage difference | ΔV | - | 10 | - | V | TWL = 2 μs , R = 500 Ω * |
| Vo2GS "L" to "H" Time | tLH | - | 0.1 | - | μs | ΔV = 10 V * |

TIMING STANDARD VALUE

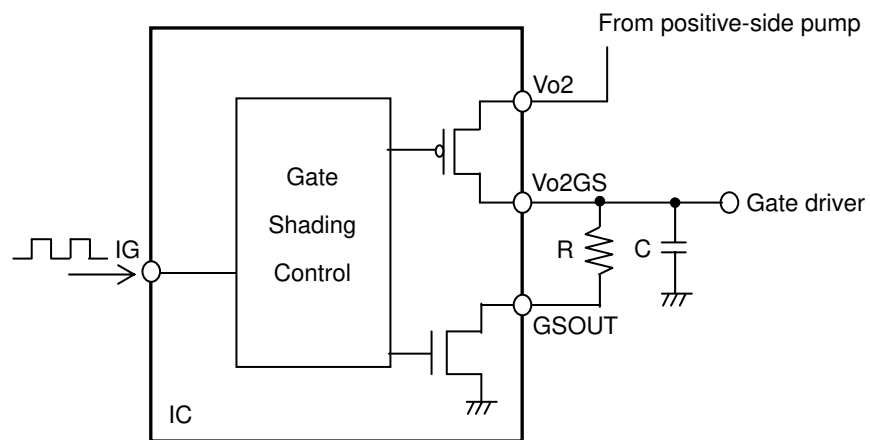


Fig. 39

●Application Examples

*Although we are confident that the application circuit diagram reflects the best possible recommendations, be sure to verify circuit characteristics for your particular application.

When a circuit is used modifying the externally connected circuit constant, be sure to decide allowing sufficient margins considering the dispersion of values by external parts as well as our IC including not only the static but also the transient characteristic. For the patent, we have not acquired the sufficient confirmation. Please acknowledge the status.

(a) Input voltage
5 V

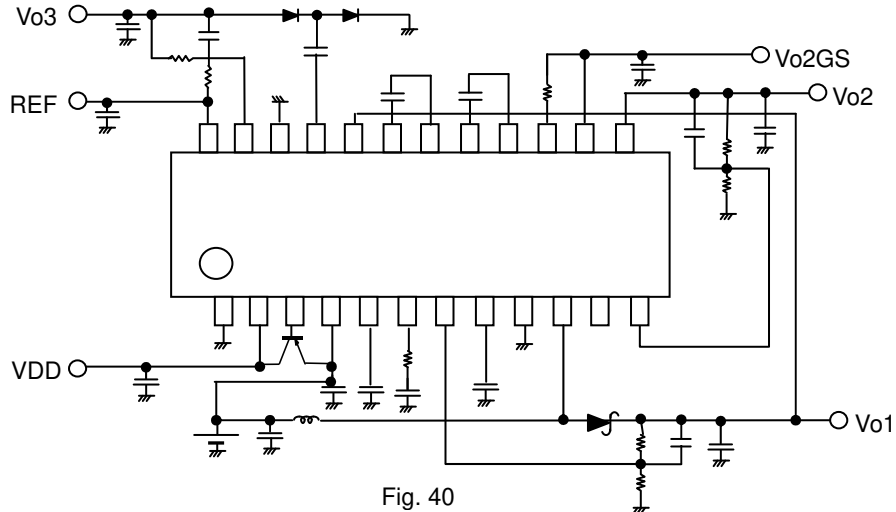


Fig. 40

(b) Input voltage
3.3 V

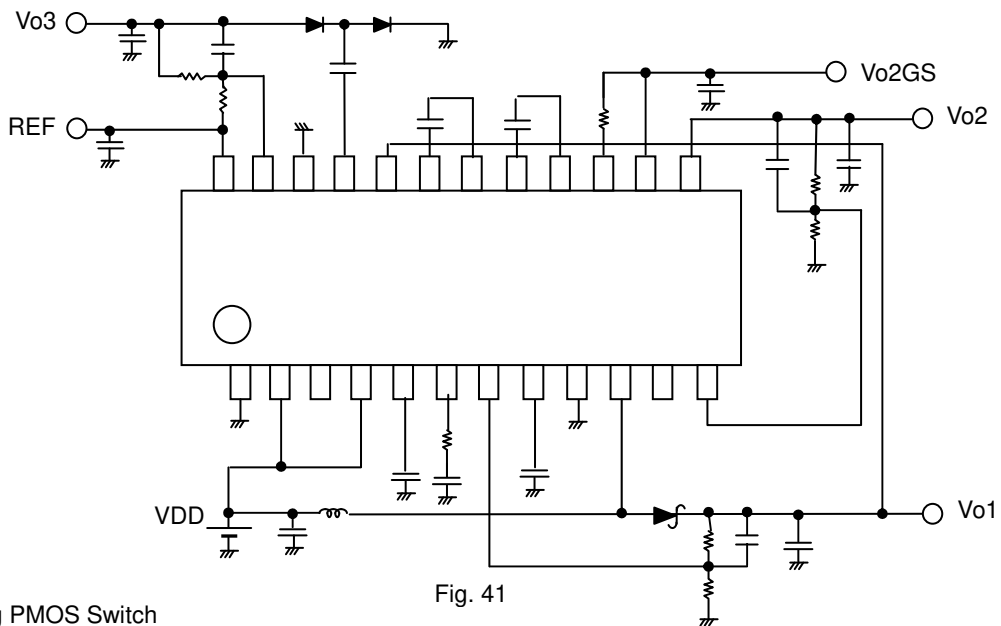


Fig. 41

(c) When Inserting PMOS Switch

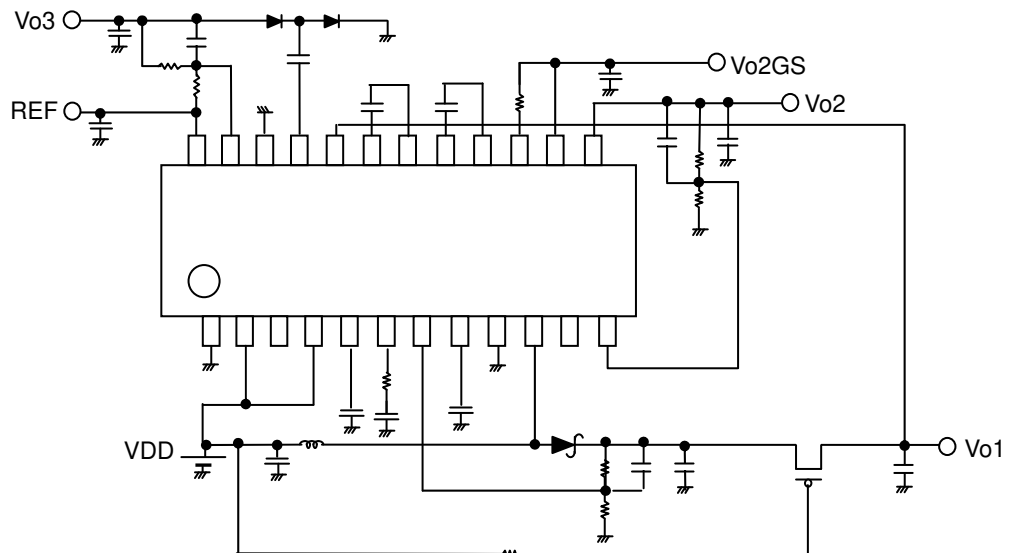


Fig. 42

● I/O Equivalent Circuits

| | | |
|-----------------|----------------------|----------------------------|
| <p>2.VDD</p> | <p>3.BASE</p> | <p>5.DLS,8.SS</p> |
| <p>6.COMP</p> | <p>7.FB1,12.FB2</p> | <p>10.SW</p> |
| <p>11.IG</p> | <p>13.Vo2</p> | <p>14.Vo2GS</p> |
| <p>15.GSOUT</p> | <p>16.C2H,19.C1H</p> | <p>17.C2L,18.C1L,21.C3</p> |
| <p>23.FB3</p> | <p>24.REF</p> | |

Fig.43

● Operation Notes

- 1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.
- 2) GND potential
Ensure a minimum GND pin potential in all operating conditions.
- 3) Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
- 4) Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.
- 5) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.
- 6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.
- 7) Ground wiring patterns
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.
- 8) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, when the resistors and transistors are connected to the pins as shown in Fig. 44, a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.
The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as the application of voltages lower than the GND (P board) voltage to input and output pins.

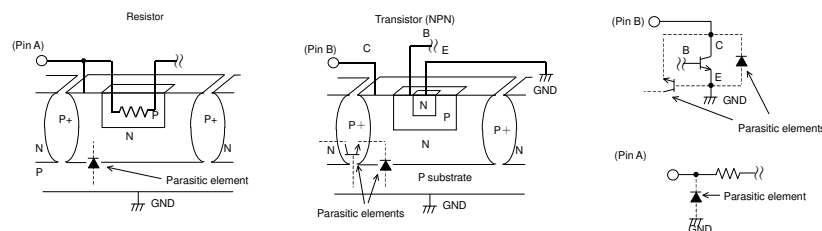


Fig.44 Example of a Simple Monolithic IC Architecture

- 9) Overcurrent protection circuits
An over current protection circuit designed according to the output current is incorporated for the prevention of IC destruction that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capability has negative characteristics to temperatures.

10) Thermal shutdown circuit

This IC incorporates a built-in thermal shutdown circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's temperature T_j will trigger the thermal shutdown circuit to turn off all output power elements. The circuit automatically resets once the chip's temperature T_j drops.

Operation of the thermal shutdown circuit presumes that the IC's absolute maximum ratings have been exceeded.

Application designs should never make use of the thermal shutdown circuit.

11) Testing on application boards

At the time of inspection of the installation boards, when the capacitor is connected to the pin with low impedance, be sure to discharge electricity per process because it may load stresses to the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

●Power Dissipation Reduction

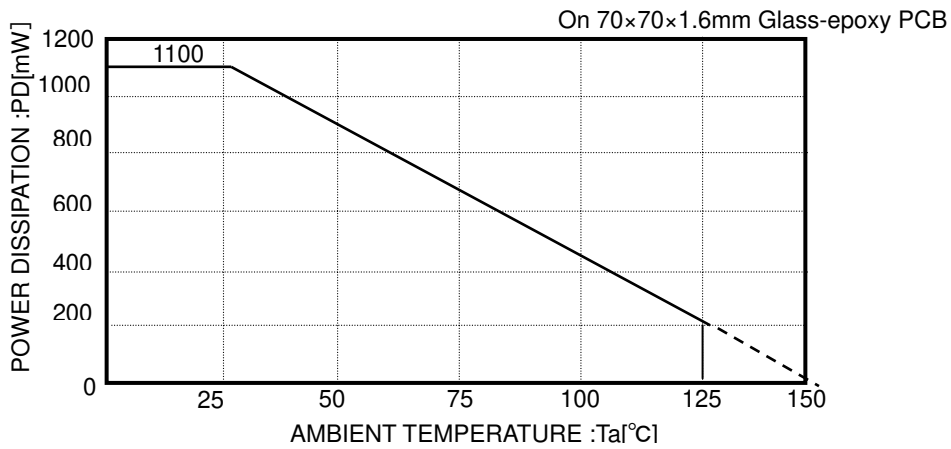


Fig.45

● Ordering part number

| | |
|---|---|
| B | D |
|---|---|

Part No.

| | | | |
|---|---|---|---|
| 8 | 1 | 5 | 3 |
|---|---|---|---|

Part No.

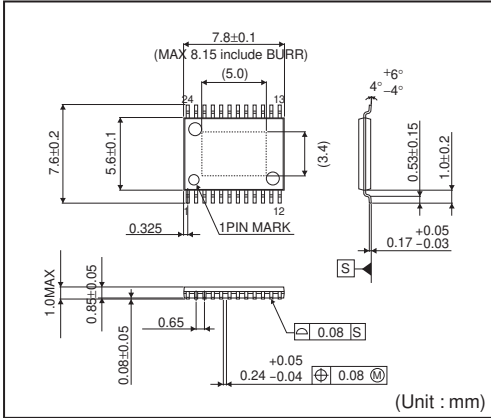
| | | |
|---|---|---|
| E | F | V |
|---|---|---|

Package
EFV:HTSSOP-B24

| | |
|---|---|
| E | 2 |
|---|---|

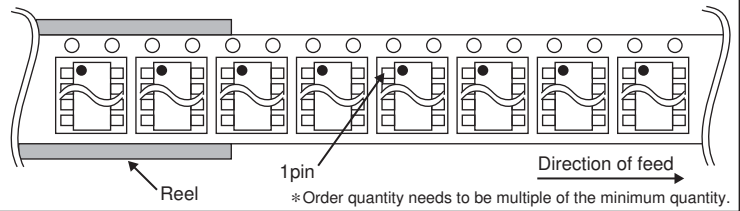
Packaging and forming specification
E2: Embossed tape and reel

HTSSOP-B24



<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape (with dry pack) |
| Quantity | 2000pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |



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