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Power Supply IC Series for TFT-LCD Panels

Automotive Panel Power Management IC

BD81842MUV-M

●General Description

The BD81842MUV-M is a power management IC for TFT-LCD panels which are used in car navigation, in-vehicle center panel, and instrument cluster. Incorporates high-power FET with low on resistance for large currents that employ high-power packages, thus driving large current loads while suppressing the generation of heat. A charge pump controller is incorporated as well, thus greatly reducing the number of application components. Also Gate Shading Function is included.

●Key Specifications

- Input voltage range : 2.0V to 5.5V
- AVDD Output voltage range : 6.0V to 18V
- SRC Output voltage range : 12V to 34V
- VCOM Output current : 200mA (Typ.)
- Oscillator Frequency : 2.1MHz (Typ.)
- Operating temperature range : -40°C to +105°C

●Special Characteristics

- FB Regulation voltage : ±3% (Ta=-40~105°C)
- Oscillator Frequency : ±10.5% (Ta=-40~105°C)

●Typical Application Circuit (TOP VIEW)

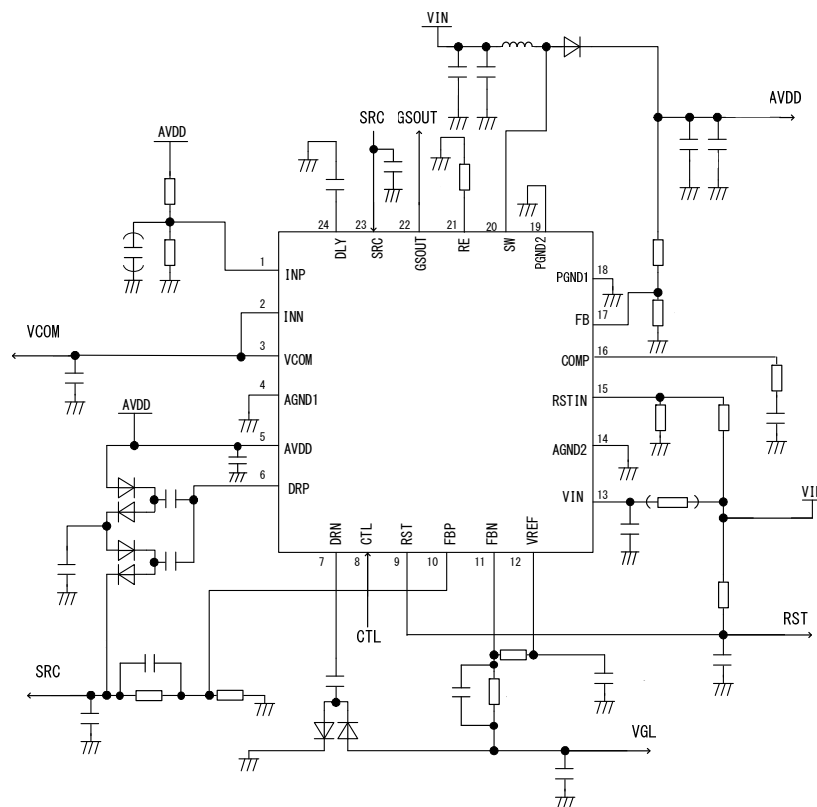


Figure 1. Application Circuit

●Applications

TFT-LCD Panels which are used in car navigation, in-vehicle center panel, and instrument cluster.

●Features

- AEC-Q100 Qualified^(Note 1)
- Boost DC/DC converter; 18 V / 2.5 A switch current.
- Switching frequency: 2.1 MHz
- Operational Amplifier (short current 200mA)
- Incorporates Positive / Negative Charge-pump Controllers.
- Gate Shading Function
- Protection circuits:
 - Under Voltage Lockout Protection Circuit
 - Thermal Shutdown Circuit (Latch Mode)
 - Over Current Protection Circuit (AVDD)
 - Timer Latch Mode Short Circuit Protection (AVDD SRC /VGL)
 - Over / Under Voltage Protection Circuit for Boost DC/DC Output
 - No SCP time included (185ms from UVLO-off)

(Note1: Grade 2)

●Package

VQFN24SV4040

W(Typ.) x D(Typ.) x H(Max.)
4.0mm x 4.0mm x 1.0mm

○Product structure : Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays

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● Pin Configuration (TOP VIEW)

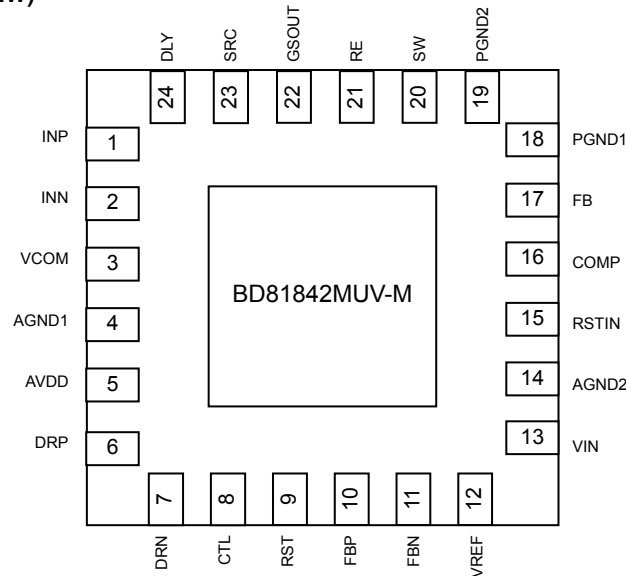


Figure 2. Pin Configuration

● Pin Descriptions

Pin No.	Pin Name	Function
1	INP	VCOM Amplifier input +
2	INN	VCOM Amplifier input -
3	VCOM	VCOM Amplifier output
4	AGND1	Ground
5	AVDD	Supply voltage input for VCOM, charge pump
6	DRP	Drive pin of the positive charge pump
7	DRN	Drive pin of the negative charge pump
8	CTL	High voltage switch control pin
9	RST	Open drain reset output
10	FBP	Positive charge pump feed back
11	FBN	Negative charge pump feed back
12	VREF	Internal Reference voltage output
13	VIN	Supply voltage input for PWM
14	AGND2	Ground
15	RSTIN	Reset comparator input
16	COMP	BOOST Error amplifier output
17	FB	BOOST Error amplifier input
18	PGND1	BOOST FET ground
19	PGND2	BOOST FET ground
20	SW	BOOST FET Drain
21	RE	Gate High voltage Fall set pin
22	GSOUT	Gate High voltage output set pin
23	SRC	Gate High voltage input set pin
24	DLY	GSOUT Delay Adjust pin

● Block Diagram

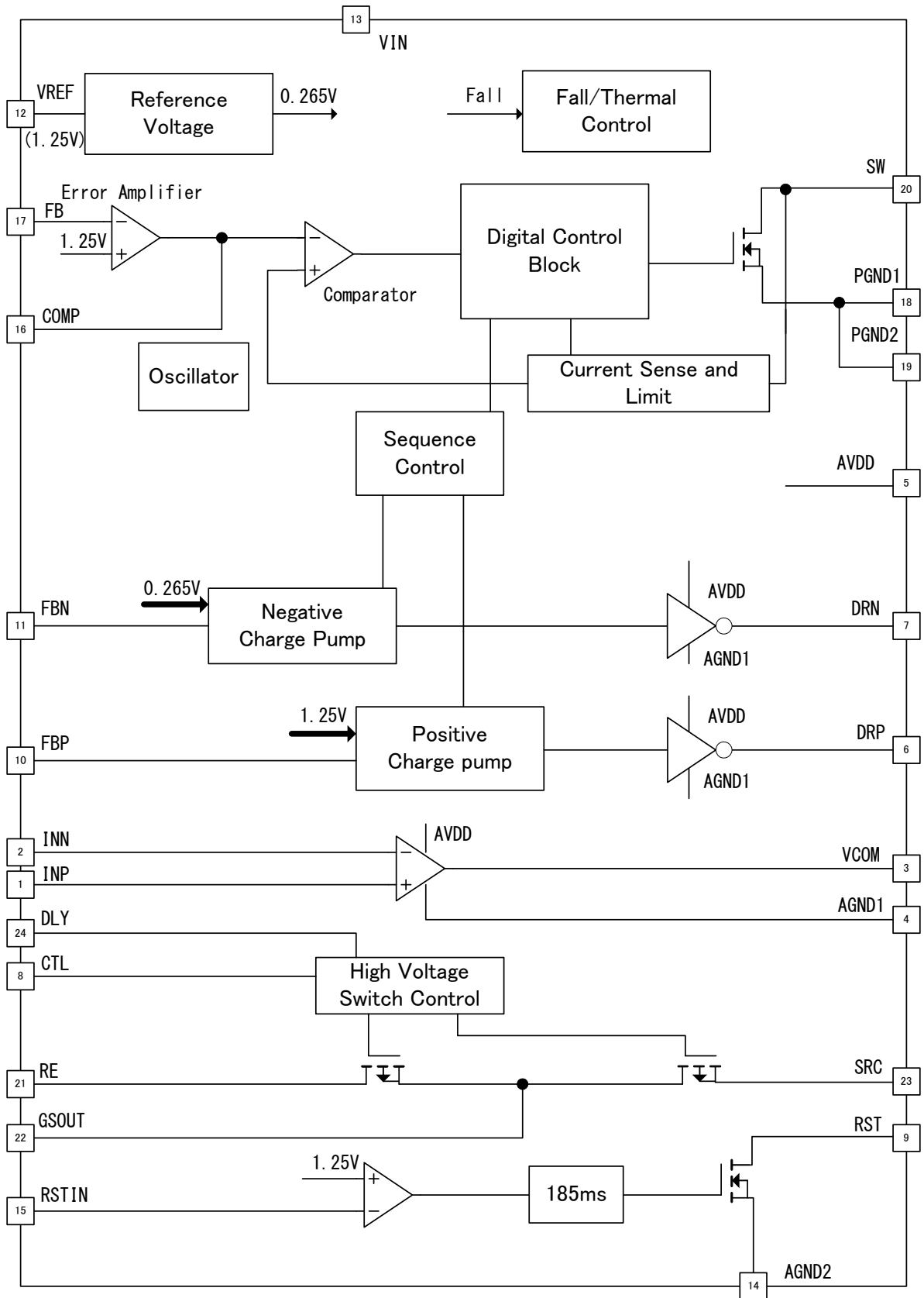


Figure 3. Block Diagram

●Main Block Function

- Boost Converter
 - A controller circuit for DC/DC boosting.
 - The switching duty is controlled so that the feedback voltage FB is set to 1.25 V (typ.).
 - A soft start operates at the time of starting.
- Positive Charge Pump
 - A controller circuit for the positive-side charge pump.
 - The switching amplitude is controlled so that the feedback voltage FBP will be set to 1.25 V (typ.).
- Negative Charge Pump
 - A controller circuit for the negative-side charge pump.
 - The switching amplitude is controlled so that the feedback voltage FBN will be set to 0.265 V (Typ.).
- Gate Shading Controller
 - A controller circuit for P-MOS FET Switch
 - The GSOUT switching synchronize with CTL input.
 - Please input voltage below VIN to CTL.
 - When VIN drops below UVLO threshold or RST=Low(=RSTIN<1.25V), GSOUT is pulled High(=SRC).
- VCOM
 - 1-channel operational amplifier block.
- Reset
 - An open-drain output(RST) refer from RSTIN voltage(up to threshold voltage 1.25V).
 - RST keeps High(need a pull-up resistor connected to VIN) dulling to 185ms from start-up.
- VREF
 - A block that generates internal reference voltage of 1.25V (Typ.).
 - VREF is keep High when the thermal/short-current-protection shutdown circuit.
- TSD/UVLO/OVP/UVP
 - The thermal shutdown circuit is shut down at an IC internal temperature of 160°C.
 - The under-voltage lockout protection circuit shuts down the IC when the VIN is 1.85 V (Typ.) or below.
 - The over-voltage protection circuit when the AVDD is 20 V (Typ.) or over.
 - The under-voltage protection circuit when the AVDD is 1.3 V (Typ.) or under
- Start-up Controller
 - A control circuit for the starting sequence.
 - Controls to start in order of VIN →VGL →AVDD→SRC
 - (Please refer to Fig.27 of 16 page for details.)

● Absolute Maximum Ratings(Ta= 25°C)

PARAMETER	SYMBOL	LIMITS			Unit
		MIN	TYP	MAX	
Power Supply Voltage	VIN	-0.3	-	7	V
Output Pin	AVDD, SW, DRP, DRN, VCOM	-0.3	-	20	V
	SRC, GSOUT, RE	-0.3	-	36	V
	RST, COMP, VREF	-0.3	-	7	V
	SRC – GSOUT	-0.3	-	40	V
Input Pin	FB, FBP, FBN	-0.3	-	VIN+0.3	V
	INN, INP	-0.3	-	20	V
Function Pin Voltage	RSTIN, DLY, CTL	-0.3		VIN+0.3	V
Maximum Junction Temperature	Tjmax	-	-	150	°C
Operating Temperature Range	Topr	-40	-	105	°C
Storage Temperature Range	Tstg	-55	-	150	°C

● Thermal Resistance^(Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 4)	2s2p ^(Note 5)	
VQFN24SV4040				
Junction to Ambient	θ_{JA}	150.6	37.9	°C/W
Junction to Top Characterization Parameter ^(Note 3)	Ψ_{JT}	20	9	°C/W

(Note 2)Based on JESD51-2A(Still-Air).

(Note 3)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 5)Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via ^(Note 6)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 6) This thermal via connects with the copper pattern of all layers.

● Recommended Operating Range

Parameter	Symbol	MIN	TYP	MAX	Unit
Power Supply Voltage	VIN	2.0	-	5.5	V
Output Pin	AVDD	6	-	18	V
	SRC	12	-	34	V

● **Electrical characteristics** (unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25°C)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
GENERAL						
Circuit Current	I _{VIN}	-	1.2	3	mA	No Switching Ta=-40~105°C
Under Voltage Lockout Threshold	V _{UVLO}	1.75	1.85	1.95	V	VIN rising Ta=-40~105°C
Internal Reference Output Voltage	V _{REF}	1.225	1.25	1.275	V	No load Ta=25°C
		1.2125	1.25	1.2875	V	No load Ta=-40~105°C
Thermal Shutdown (rising)	T _{SD}	-	160	-	°C	Junction Temp
Duration to Trigger Fault Condition	T _{SCP}	51	63	75	ms	FB, FBP or FBN below threshold
BOOST CONVERTER (AVDD)						
FB Regulation Voltage	V _{FB}	1.2375	1.25	1.2625	V	Ta=25°C
		1.2125	1.25	1.2875	V	Ta=-40~105°C
FB Fault Trip Level	V _{TL_FB}	0.9	1.0	1.1	V	FB falling
FB Input Bias Current	I _{FB}	-	0.1	2	μA	FB= 1.5V Ta=-40~105°C
SW Leakage Current	I _{SW_L}	-	0	10	μA	SW=20V Ta=-40~105°C
Maximum switching Duty Cycle	M _{DUTY}	85	90	95	%	FB= 1.0V
SW ON-Resistance	R _{SW}	-	200	250	mΩ	SW= 200mA
SW Current Limit	I _{SWLIM}	2.5	4.5	6.5	A	Ta=-40~105°C
Over Voltage Protection	V _{OV}	18	20	22	V	AVDD rising
Under Voltage Protection	V _{UV}	1	1.3	3	V	AVDD falling
BOOST Soft Start Time	T _{SS_FB}	12.5	15.5	18.5	ms	Ta=-40~105°C
Oscillator frequency	F _{SW}	1.9	2.1	2.3	MHz	Ta=25°C
		1.88	2.1	2.32	MHz	Ta=-40~105°C
RESET						
RST Output Low Voltage	V _{RST}	-	0.05	0.2	V	RST = 1.2mA
RSTIN Threshold Voltage	V _{TH_L}	1.18	1.25	1.32	V	RSTIN rising Ta=-40~105°C
RSTIN Input Current	I _{RSTIN}	-	0	6	μA	RSTIN=0 to VIN-0.3 Ta=-40~105°C
RST Blanking Time	T _{NO_SCP}	165	185	205	ms	No SCP Zone Ta=-40~105°C
Operational Amp rifer						
Input Range	V _{RANGE}	0	-	AVDD	V	
Offset Voltage	V _{OS}	-	2	15	mV	INP= 5.0V
Input Current	I _{INP}	-	0	3	μA	INP= 5.0V Ta=-40~105°C
Output Swing Voltage (INP= 5.0V)	V _{OH}	-	5.03	5.06	V	VCOM = +50mA
	V _{OL}	4.94	4.97	-	V	VCOM = -50mA
Short Circuit Current	I _{SHT_VCOM}	-	200	400	mA	INP= 5.0V
Slew Rate	SR	10	40	250	V/us	

● **Electrical characteristics** (unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25°C) (Continued)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Negative Charge pump driver (VGL)						
FBN Regulation Voltage	V _{FBN}	242	265	288	mV	Ta=25°C
		239	265	291	mV	Ta=-40~105°C
FBN Fault Trip Level	V _{TL_FBN}	400	450	500	mV	FBN rising
FBN Input Bias Current	I _{FBN}	-	0.1	15	μA	FBN= 0.1V Ta=-40~105°C
Oscillator frequency	F _{CPN}	425	525	625	kHz	Ta=-40~105°C
DRN Leakage Current	I _{DRN_L}	-	0	10	μA	FBN=1.0V Ta=-40~105°C
Positive Charge pump driver (SRC)						
FBP Regulation Voltage	V _{FBP}	1.2325	1.25	1.2675	V	Ta=25°C
		1.2125	1.25	1.2875	V	Ta=-40~105°C
FBP Fault Trip Level	V _{TL_FBP}	0.95	1.0	1.05	V	FBP falling
FBP Input Bias Current	I _{FBP}	-	0.1	15	μA	FBP= 1.5V Ta=-40~105°C
Oscillator frequency	F _{CPP}	425	525	625	kHz	Ta=-40~105°C
DRP Leakage Current	I _{DRP_L}	-	0	10	μA	FBP= 1.5V Ta=-40~105°C
Soft-Start Time	T _{SSP}	3.2	3.9	4.6	ms	Ta=-40~105°C
Gate Shading Function (GSOUT)						
DLY Source Current	I _{DLY}	3.5	5	6.5	μA	Ta=-40~105°C
DLY Threshold Voltage	V _{TL_DLY}	0.85	1.25	1.65	V	DLY falling Ta=-40~105°C
CTL Input Voltage High	V _{IN_H}	V _{IN} × 0.65	-	V _{IN}	V	Depend on V _{IN} Ta=-40~105°C
CTL Input Voltage Low	V _{IN_L}	0	-	V _{IN} × 0.25	V	Depend on V _{IN} Ta=-40~105°C
CTL Input Bias Current	I _{CTL}	-	0	6	μA	R _{STIN} =0 to V _{IN} -0.3 Ta=-40~105°C
Propagation delay time (Rising)	T _{GS_R}	-	100	200	ns	SRC= 25V
Propagation delay time (Falling)	T _{GS_F}	-	100	200	ns	SRC= 25V
SRC -GSOUT ON Resistance	R _{GS_H}	-	15	30	Ω	DLY = 1.5V
GSOUT-RE ON Resistance	R _{GS_M}	-	30	100	Ω	DLY = 1.5V
GSOUT-GND ON Resistance	R _{GS_L}	-	2.5	5.0	kΩ	DLY = 1.0V

○ This product is not designed for protection against radio active rays.

● Electrical characteristic curves (Reference data)

(Unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25°C)

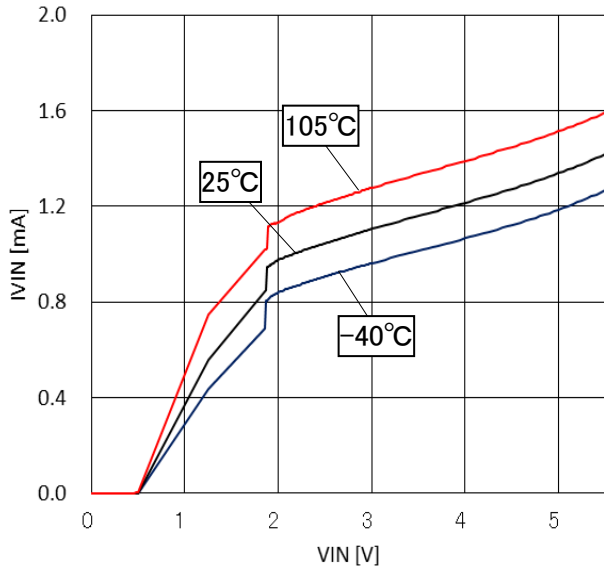


Figure 4. Circuit Current (No switching)

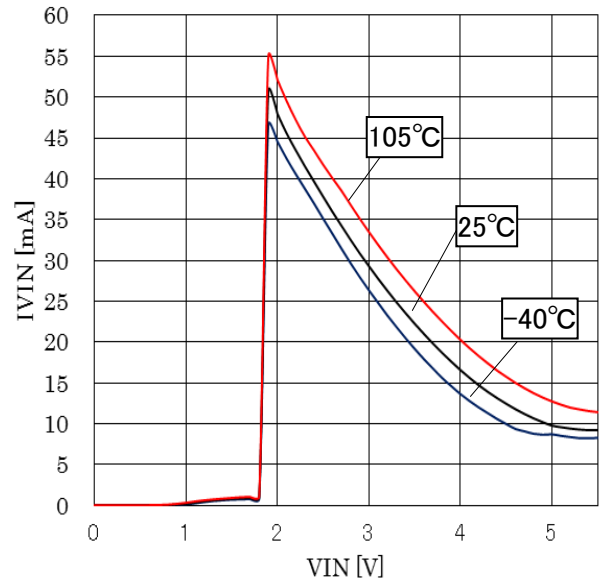


Figure 5. Circuit Current (Switching)

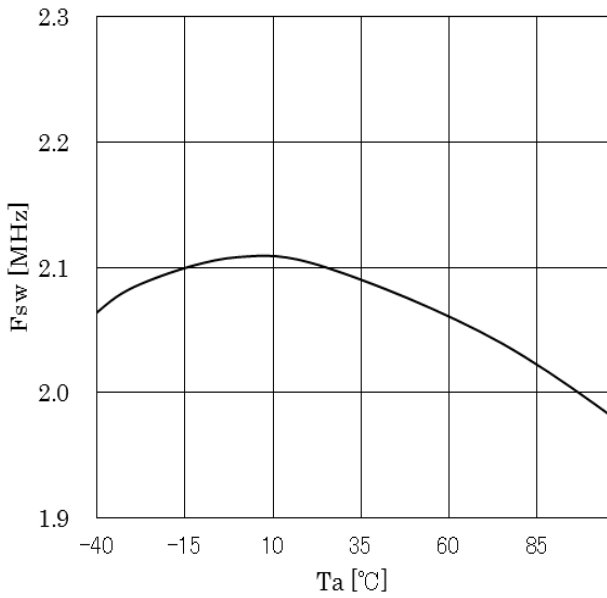


Figure 6. Dependent on Temperature Frequency

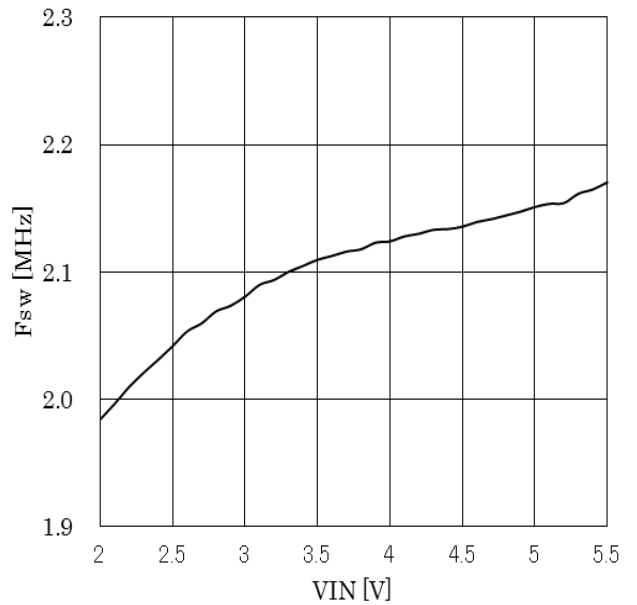


Figure 7. Dependent on Input Voltage Frequency

● Electrical characteristic curves (Reference data)

(Unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25°C)

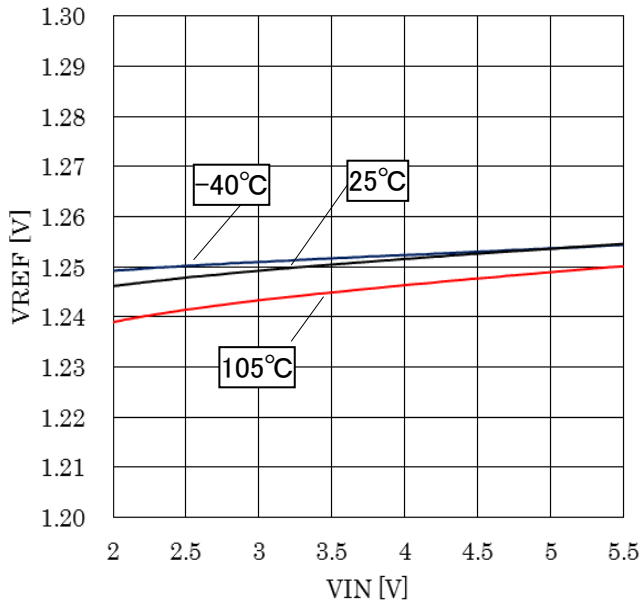


Figure 8. VREF Line Regulation

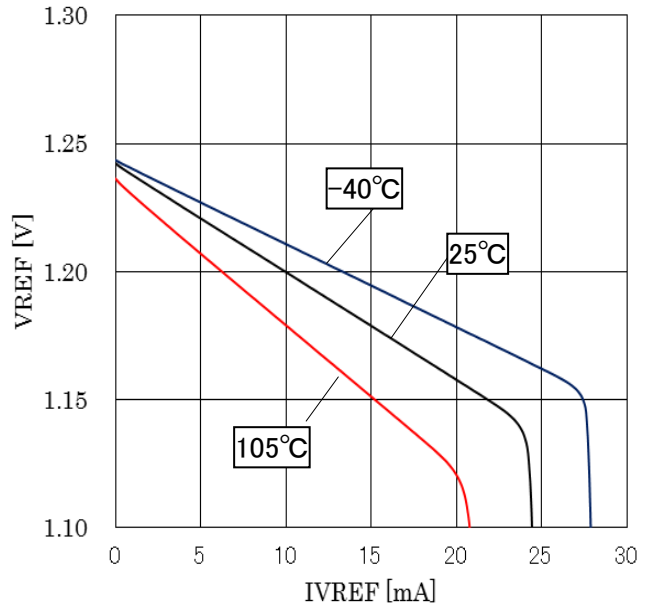


Figure 9. VREF Load Regulation

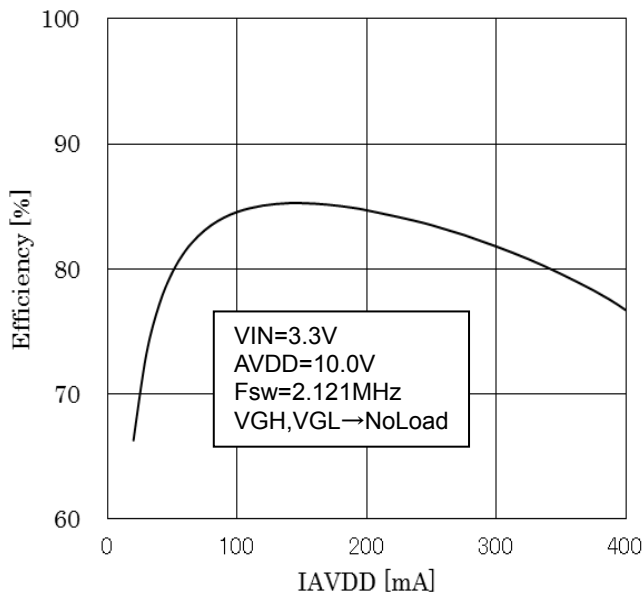


Figure 10. Boost Converter Efficiency

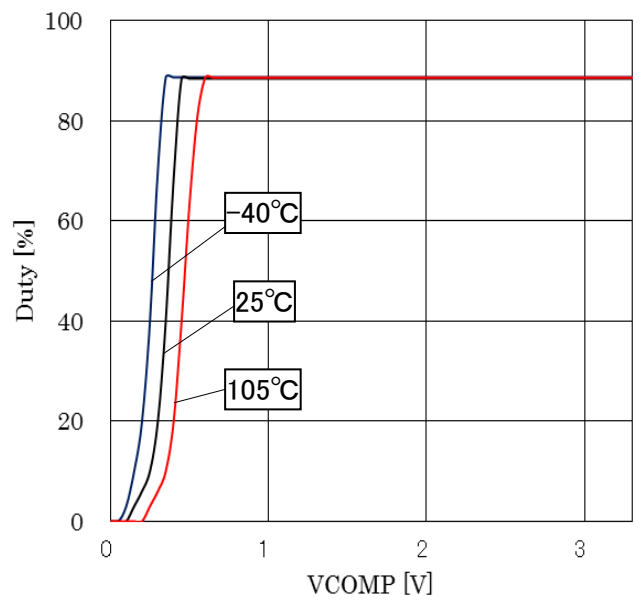


Figure 11. COMP V.S. DUTY

●Electrical characteristic curves (Reference data)

(Unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25°C)

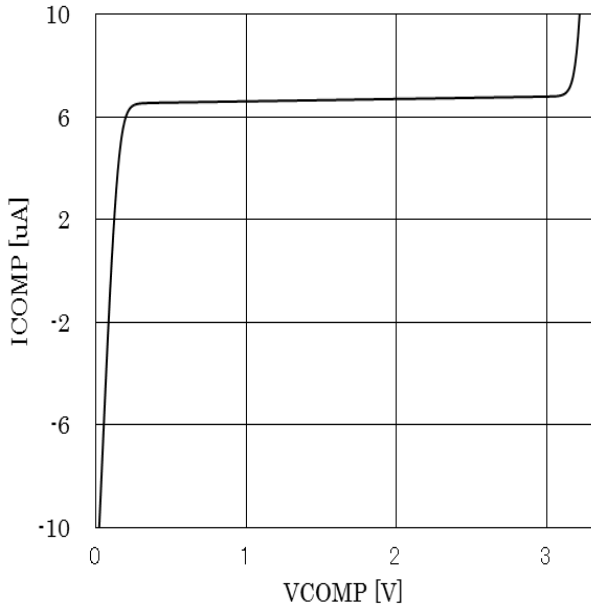


Figure 12. COMP Sink Current

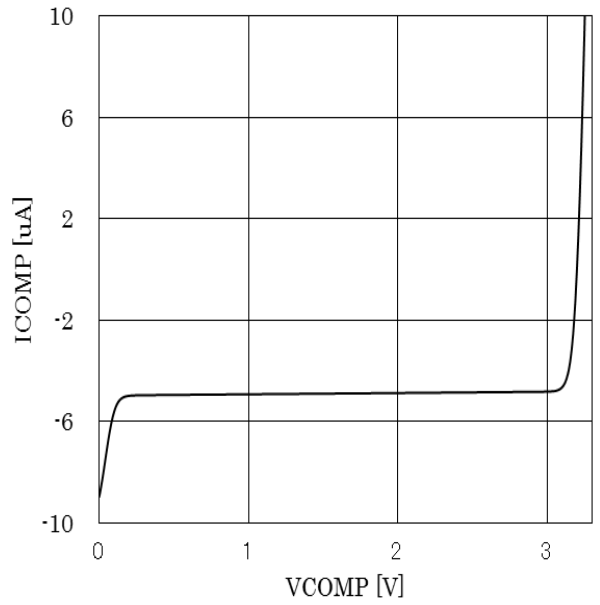


Figure 13. COMP Source Current

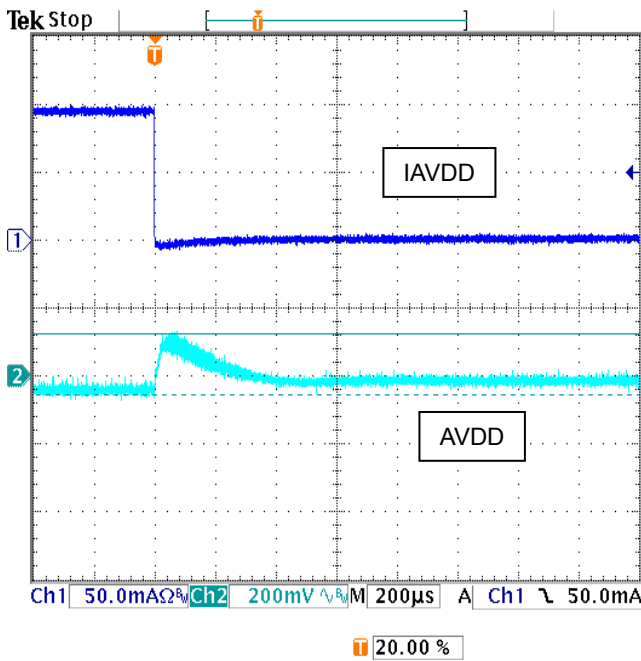


Figure 14. Load Transient Response Falling

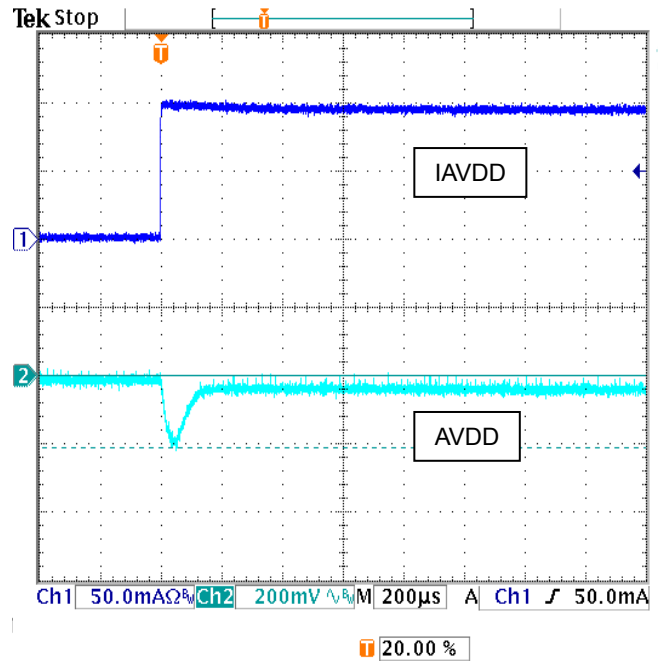


Figure 15. Load Transient Response Rising

●Electrical characteristic curves (Reference data) – Continued
 (Unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25°C)

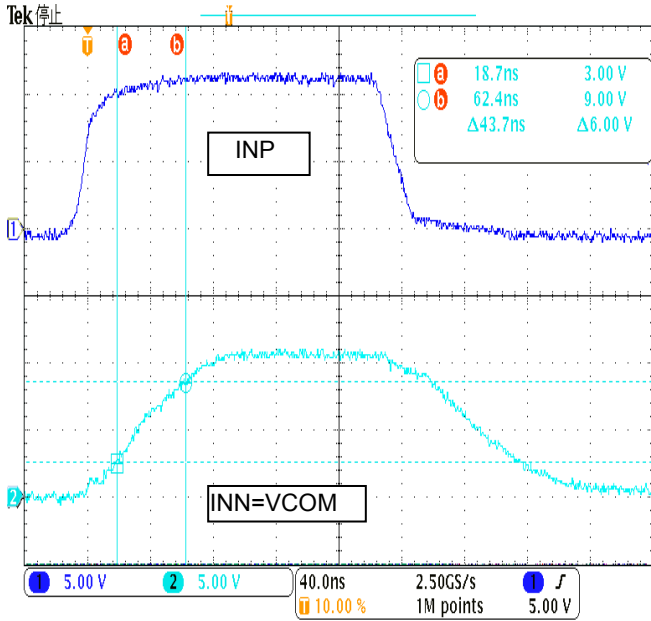


Figure 16. VCOM Slew Rate (Rising)

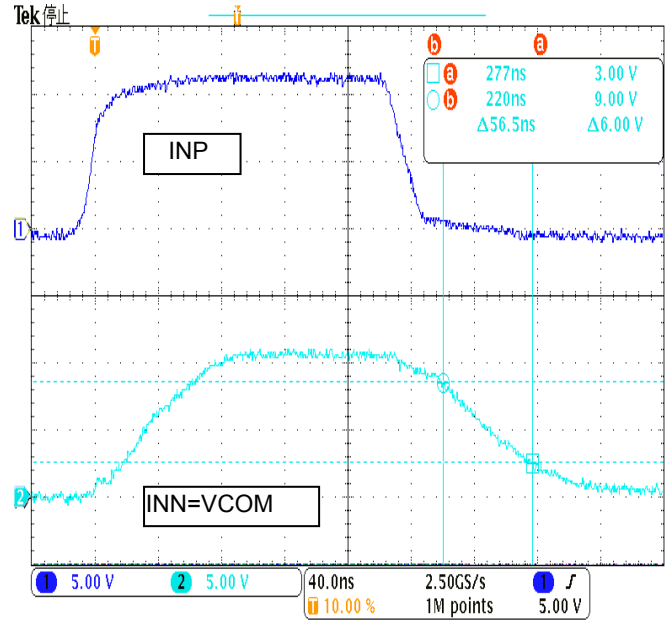


Figure 17. VCOM Slew Rate (falling)

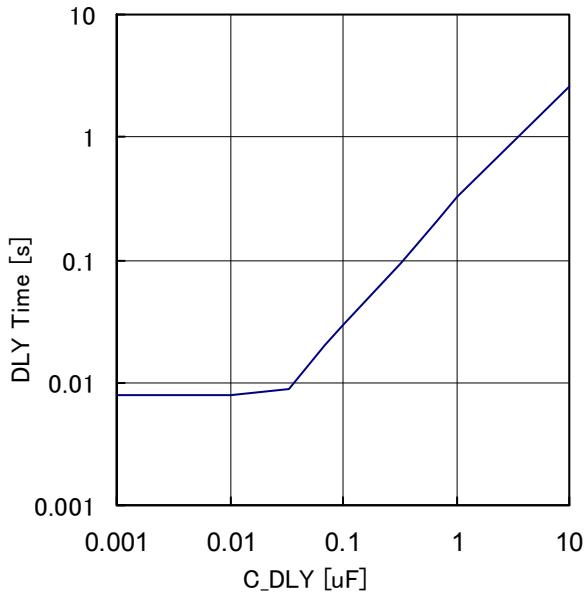


Figure 18. C_DLY vs. delay time

●Electrical characteristic curves (Reference data) – Continued
 (Unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25°C)

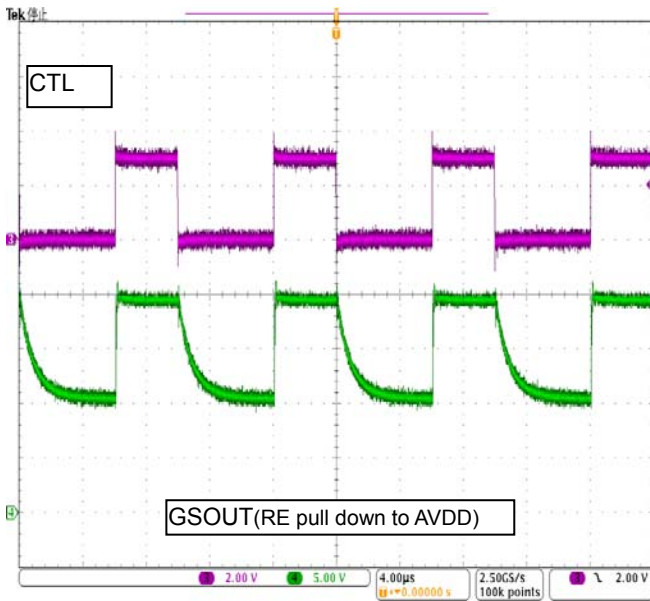


Figure 19. Gate Shading Wave form1

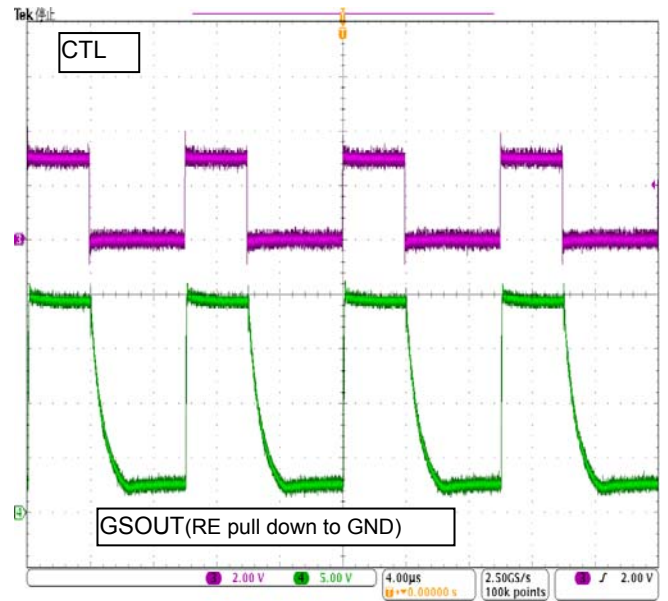


Figure 20. Gate Shading Wave form2

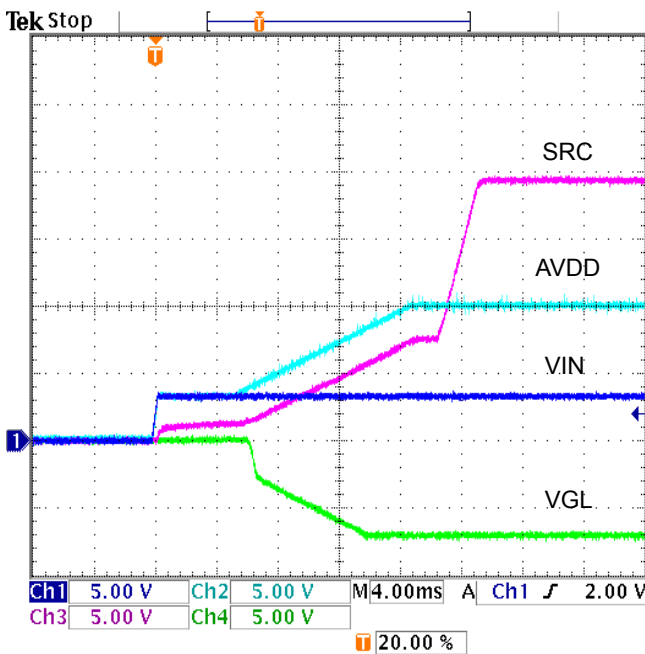


Figure 21. Power On Sequence1
 (Main Output)

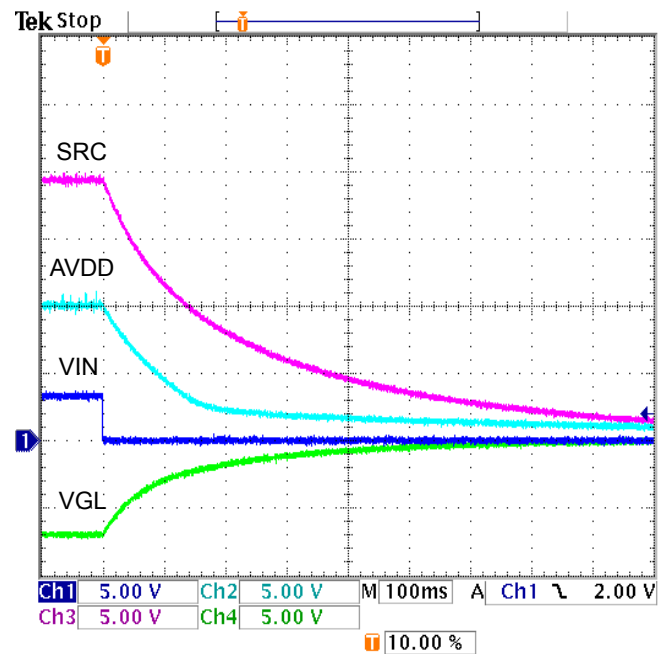


Figure 22. Power Off Sequence1
 (Main Output)

●Electrical characteristic curves (Reference data) – Continued
 (Unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25°C)

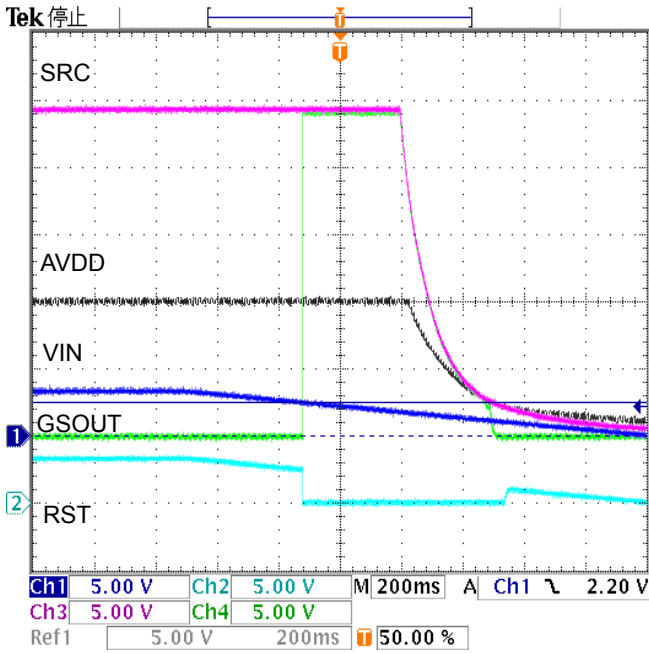


Figure 23. Power Off Sequence2
 (R_RST_U=10k,R_RST_D=10k)

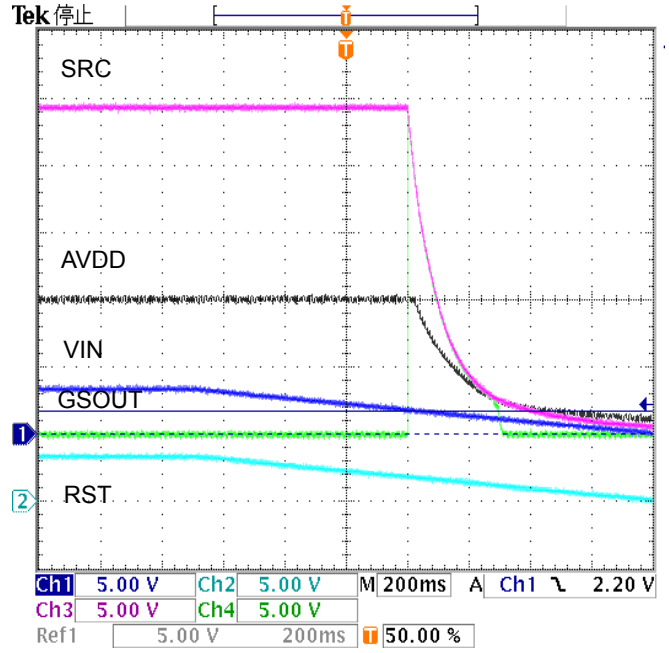


Figure 24. Power Off Sequence3
 (R_RST_U=10k,R_RST_D=OPEN)

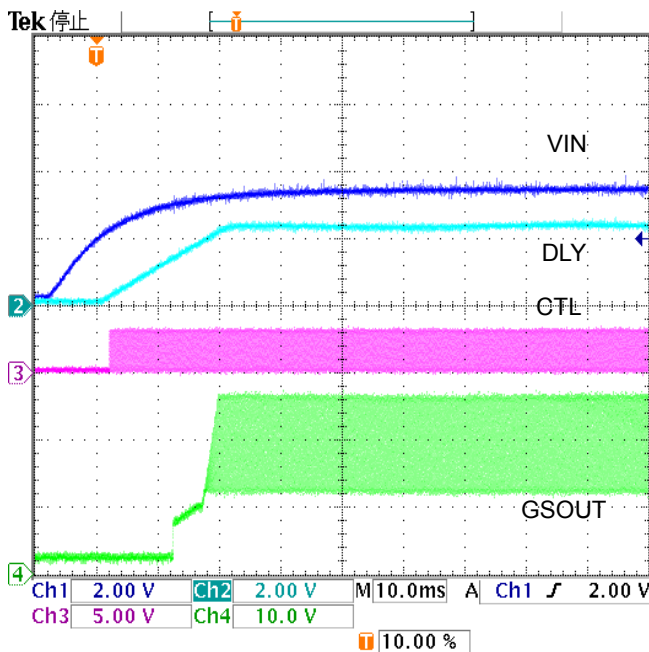


Figure 25. Power On Sequence2
 (CTL=signal, RE pull down to AVDD)

● Application Example

When resistor cannot be put near the INP, and concerned about the noise, please insert a capacitor. (0.1uF-1uF)

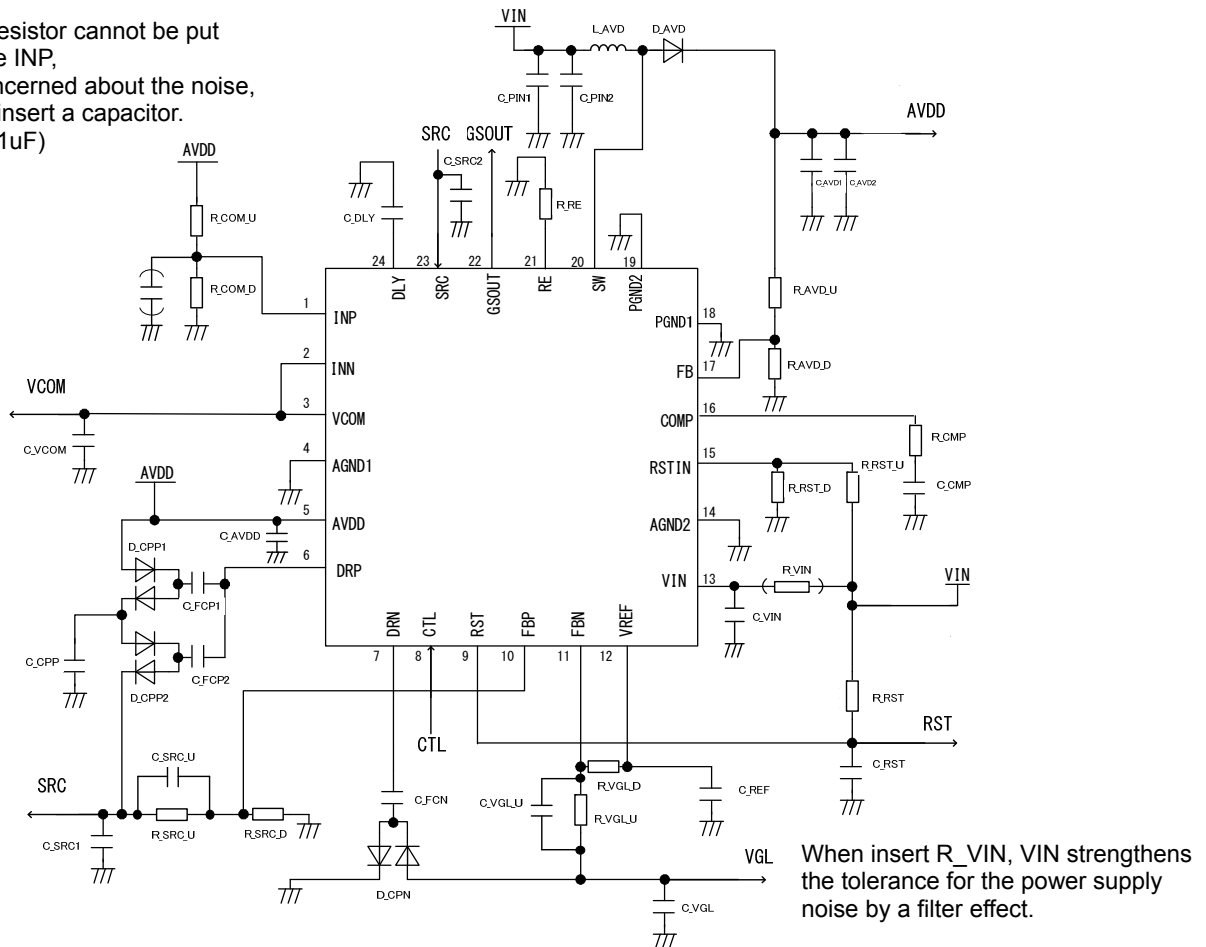


Figure 26. Application Example

Application circuit components list (VIN=3.3V, AVDD=10V, SRC=20V, VGL=-7.1V, VCOM=5V)

Parts name	Value			Unit	Company	Parts Number
	Min	Typ	Max			
C_VIN	0.47	1.0	-	uF	TDK	CGA3E1X7R1C105M
R_VIN	1	10	20	Ω	ROHM	MCR03
C_PIN1	4.7	10	-	uF	TDK	CGA5L1X7R1C106M
C_PIN2	4.7	10	-	uF	TDK	CGA5L1X7R1C106M
C_AVD1	4.7	10	22	uF	TDK	CGA5L1X7R1E106M
C_AVD2	4.7	10	22	uF	TDK	CGA5L1X7R1E106M
L_AVD	4.7	10	22	uH	TDK	LTF5022T-100M1R3-H
D_AVD	-	30/5	-	V/A	ROHM	RB080L-30DD
R_AVD_U	6.8	91	330	kΩ	ROHM	MCR03
R_AVD_D	6.8	13	330	kΩ	ROHM	MCR03
R_CMP	-	24	-	kΩ	ROHM	MCR03
C_CMP	-	2200	-	pF	TDK	CGA3E2X7R1H222M
R_RST_U	-	10	-	kΩ	ROHM	MCR03
R_RST_D	-	10	-	kΩ	ROHM	MCR03
R_RST	-	10	-	kΩ	ROHM	MCR03
C_RST	-	1.0	-	uF	TDK	CGA3E1X7R1C105M
C_DLY	10	33	100	nF	TDK	CGA3E2X7R1H333M
R_RE	0.2	1.0	5.1	kΩ	ROHM	MCR03
C_AVDD	0.047	0.1	-	uF	TDK	CGA3E2X7R1H104M
C_REF	0.1	0.22	0.47	uF	TDK	CGA3E2X7R1C224M

Parts name	Value			Unit	Company	Parts Number
	Min	Typ	Max			
C_VGL	0.47	1.0	10	uF	TDK	CGA3E1X7R1C105M
C_FCN	0.047	0.1	1.0	uF	TDK	CGA3E2X7R1H104M
D_CPN	-	80/100	-	V/mA	ROHM	DAN217UMFH
R_VGL_U	6.8	120	330	kΩ	ROHM	MCR03
R_VGL_D	6.8	16	330	kΩ	ROHM	MCR03
C_VGL_U	10	100	4700	pF	TDK	CGA3E2NP01H101J
C_SRC1	0.47	1.0	10	uF	TDK	CGA4J3X7R1H105M
C_FCP1	0.047	0.1	1.0	uF	TDK	CGA3E2X7R1H104M
C_FCP2	0.047	0.1	1.0	uF	TDK	CGA3E2X7R1H104M
C_CPP	0.047	0.1	1.0	uF	TDK	CGA3E2X7R1H104M
D_CPP1	-	80/100	-	V/mA	ROHM	DAN217UMFH
D_CPP2	-	80/100	-	V/mA	ROHM	DAN217UMFH
R_SRC_U	6.8	150	330	kΩ	ROHM	MCR03
R_SRC_D	6.8	10	330	kΩ	ROHM	MCR03
C_SRC_U	10	100	4700	pF	TDK	CGA3E2NP01H101J
C_SRC2	0.47	1.0	10	uF	TDK	CGA4J3X7R1H105M
R_COM_U	6.8	51	330	kΩ	ROHM	MCR03
R_COM_D	6.8	51	330	kΩ	ROHM	MCR03
C_VCOM	0.1	1.0	10	uF	TDK	CGA3E1X7R1E105M

※Please set in consideration of temperature properties and DC bias properties not to become less than the minimum.
 COMP parts and the coil need adjustment by output voltage and load. Please consider it based on enough evaluations with the actual model.

●Power Sequence

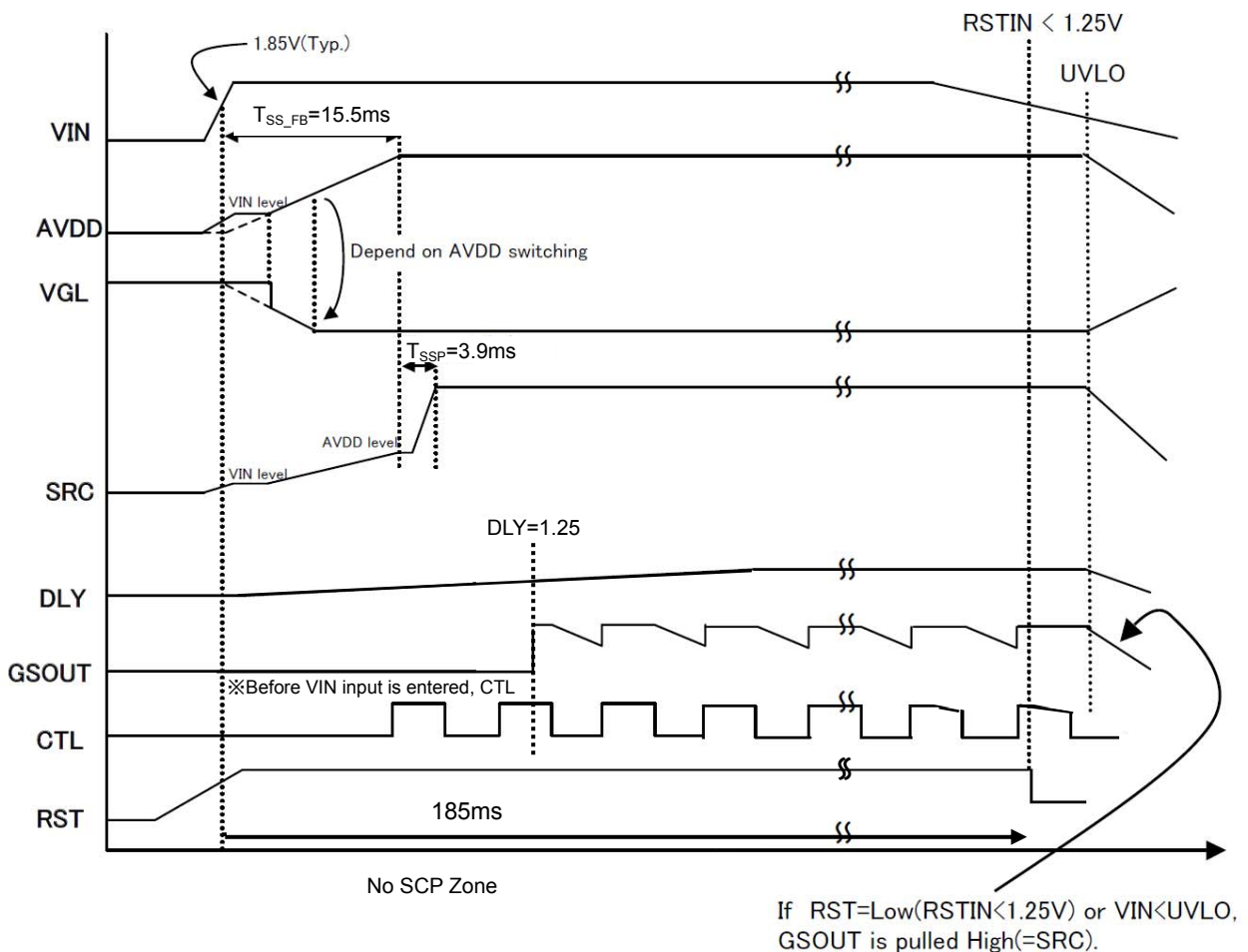


Figure 27. Power Sequence

●Protect Operation

• VIN UVLO

	AVDD	SRC	VGL
Falling (Typ.)		1.65V	
Rising (Typ.)		1.85V	
Action	All channels shut-down. Start-up Sequence Resets.		

• Thermal Shutdown

	AVDD	SRC	VGL
Threshold (Typ.)		160°C	
Action	All channels are latched in shut-down condition as soon as detecting Thermal Shutdown. For Recovery, power supply should be inputted under UVLO voltage.		

• Over Voltage Protection

	AVDD
Threshold (Typ.)	20V
Action	STOP switching of AVDD.

• Under Voltage Protect

	AVDD
Threshold (Typ.)	1.3V
Action	STOP switching of AVDD.

• Over Current Protect

	AVDD
Threshold (Min.)	2.5A
Action	STOP switching of AVDD.

• Short Circuit Protect

	AVDD	SRC	VGL
Threshold (Typ.)	AVDD x 0.8	SRC x 0.8	VGL x 0.8
Action	All channels are latched in shut-down condition after 63msec(Typ.) detecting Short Circuit Protect in any channel. For Recovery, power supply should be inputted under UVLO voltage.		

●Reset Function

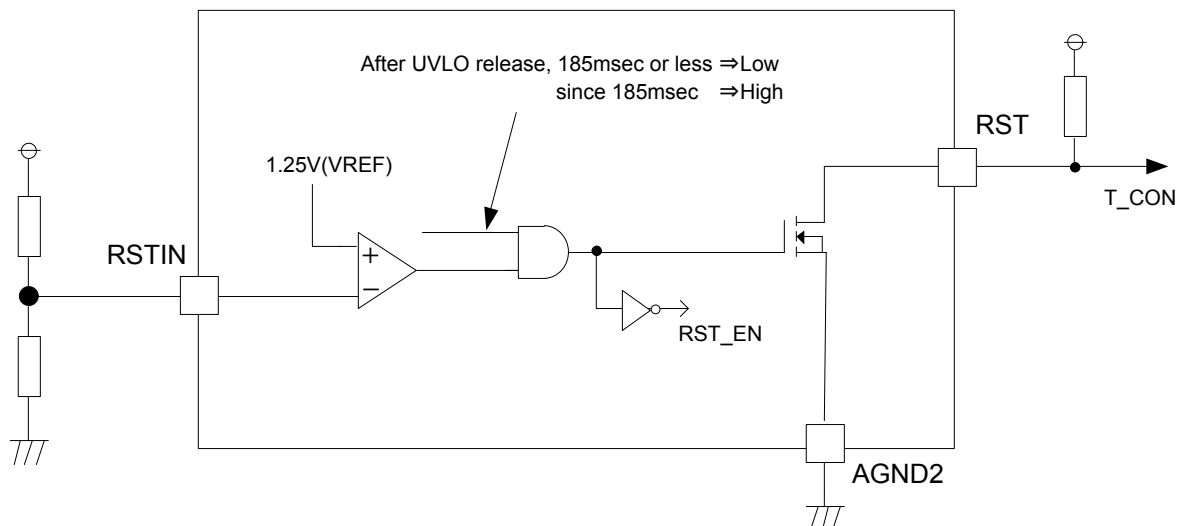


Fig.28 Reset Explanation

The RST is set to Low when the RSTIN voltage is less than 1.25V and is set to High (pulled-up by a resistor to VIN) when the RSTIN voltage is greater than or equal to 1.25V. However, during the time when power supply is ON for 185ms (Typ), RST is held High regardless of RSTIN voltage.

Gate Shading function is activated when RST_EN is High. When RSTIN is Low, the Gate Shading function cannot be used. If the Gate Shading function will not be used, the SRC, RE, and CTL must be pulled-down by a resistor or connected to GND.

● Gate Shading Function

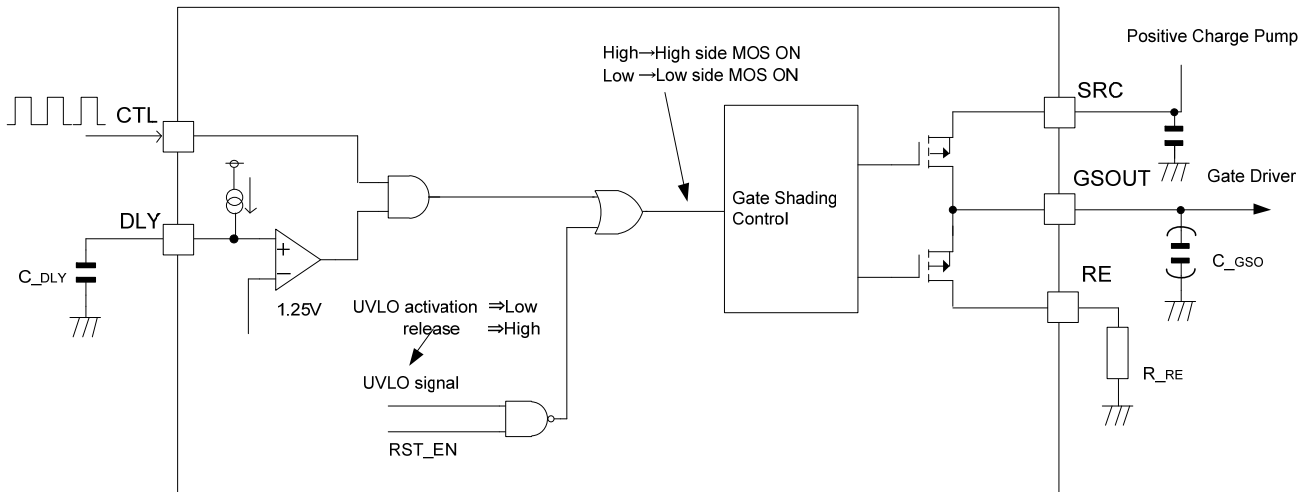


Fig.29 Gate Shading Explanation

To control the Gate Shading output (GSOUT) by the CTL input, the RSTIN and DLY pin voltages must be set greater than 1.25V. If the DLY pin is left open, the DLY voltage immediately becomes High (greater than 1.25V) when the power supply is turned ON. To add a delay time (t_DELAY) before DLY voltage becomes High, connect a capacitor (C_DLY) to the DLY pin. The delay time (t_DELAY) can be calculated using the following formula.

$$t_DELAY = (C_DLY \times 1.25V) / 5\mu A \quad [sec]$$

When the CTL input is High (0.65 × VIN to VIN), the MOS between SRC and GSOUT turns ON and sets the output voltage of GSOUT equal to SRC.

When the CTL input is Low (0 to 0.25 × VIN), the MOS between GSOUT and RE turns ON, and GSOUT will be discharged down to RE voltage by a slope decided by the external resistor (R_RE) and capacitor (C_GSO).

To adjust a slope, the following setting value is recommended; for resistor (R_RE): 200 Ω - 5.1kΩ, for capacitor (C_GSO): less than 0.1μF. It may cause the efficiency aggravation by setting out of this range.

The voltage ΔV that GSOUT discharges during the time (t_WL) when CTL input is Low can be calculated using the following formula.

$$\Delta V = SRC \times \left(1 - \exp\left(-\frac{t_WL}{C_GSO \times R_RE}\right) \right) \quad [V]$$

But the loss occurs when C_GSO is added. The loss ΔP can be calculated using the following formula.

$$\Delta P = \text{Frequency(CTL)} \times \Delta V^2 \times C_GSO \quad [W]$$

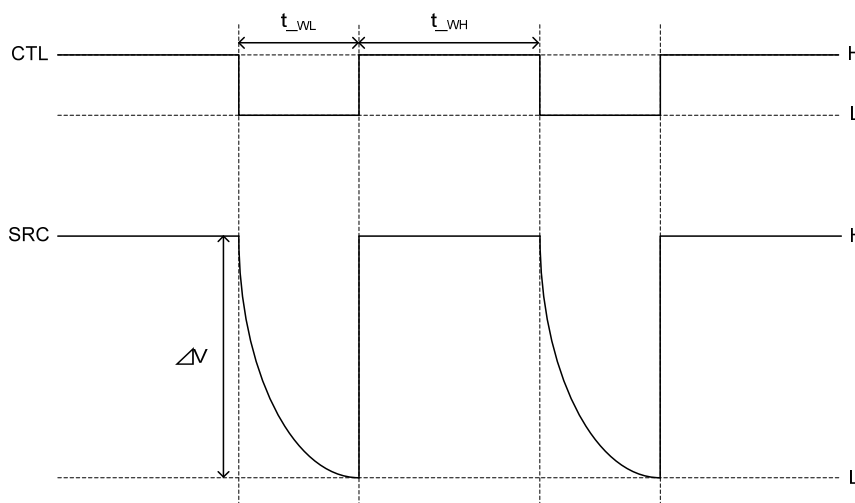


Fig.30 Gate Shading I/O Waveform

If the Gate Shading function will not be used, the SRC, RE, and CTL must be pulled-down by a resistor or connected to GND. And the DLY, please connect capacitor because there is the concern such as noises.

●How to select parts of application

(1-1) Setting the Output L Constant (Boost Converter)

The coil to use for output is decided by the rating current I_{LR} and input current maximum value I_{INMAX} of the coil.

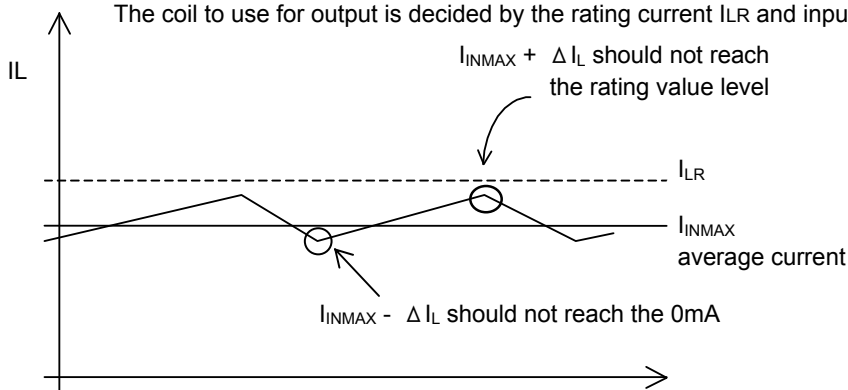


Figure 31. Coil Current Waveform

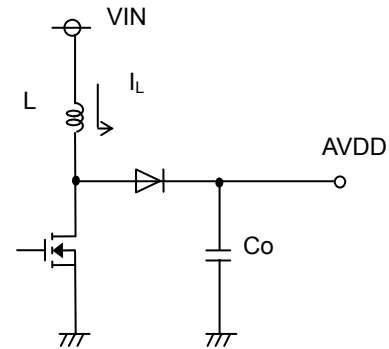


Figure 32. Output Application Circuit Diagram

Adjust so that $I_{INMAX} + \Delta I_L$ does not reach the rating current value I_{LR} . In addition, become the Discontinuous Condition Mode (DCM) when I_L reaches 0mA. As for the section which DCM and Continuous Condition Mode (CCM) are replaced by, jitter properties turn worse. Adjust the coil so that $I_{INMAX} - \Delta I_L$ does not reach the 0mA. ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times V_{IN} \times \frac{AVDD - V_{IN}}{AVDD} \times \frac{1}{f} \quad [A] \quad \text{Here, } f \text{ is the switching frequency.}$$

Set with sufficient margin because the coil value may have the dispersion of $\pm 30\%$. If the coil current exceeds the rating current I_{LR} of the coil, it may damage the IC internal element.

BD81842MUV-M uses the current mode DC/DC converter control and has the optimized design at the coil value. A coil inductance (L) of 4.7 μH to 22 μH is recommended from viewpoints of electric power efficiency, response, and stability.

(2) Output Capacity Settings

For the capacitor to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} allowance value and the drop voltage allowance value at the time of sudden load change. Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = I_{LMAX} \times RESR + \frac{1}{fCo} \times \frac{V_{IN}}{AVDD} \times \left(I_{LMAX} - \frac{\Delta I_L}{2} \right) [V]$$

Here, f is the switching frequency and RESR is ESR of output capacitor.

Perform setting so that the voltage is within the allowable ripple voltage range.

For the drop voltage during sudden load change; V_{DR} , please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{Co} \times 10 \text{ us} \quad [V]$$

However, 10 μs is the rough calculation value of the DC/DC response speed. Please set the capacitance considering the sufficient margin so that these two values are within the standard value range.

(3) Selecting the Input Capacitor

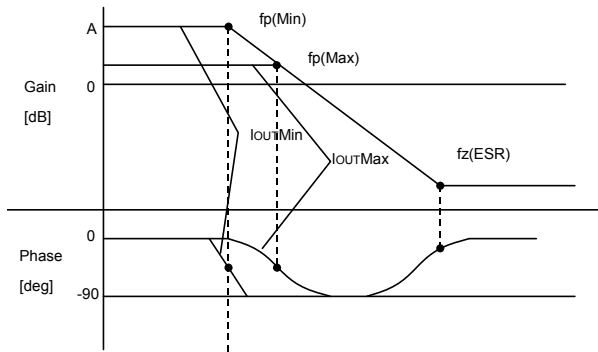
Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the input side. For the reason, the low ESR capacitor is recommended as an input capacitor which has the value more than 10 μF and less than 100 $m\Omega$. If a capacitor out of this range is selected, the excessive ripple voltage is superposed on the input voltage, accordingly it may cause the malfunction of IC.

However these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform the margin check using the actual product.

(4) Setting Rc, Cc of the Phase Compensation Circuit

In the current mode control, since the coil current is controlled, a pole (phase lag) made by the CR filter composed of the output capacitor and load resistor will be created in the low frequency range, and a zero (phase lead) by the output capacitor and ESR of capacitor will be created in the high frequency range. In this case, to cancel the pole of the power amplifier, it is easy to compensate by adding the zero point with Cc and Rc to the output from the error amp as shown in the illustration.

Open loop gain characteristics



Error amp phase compensation characteristics

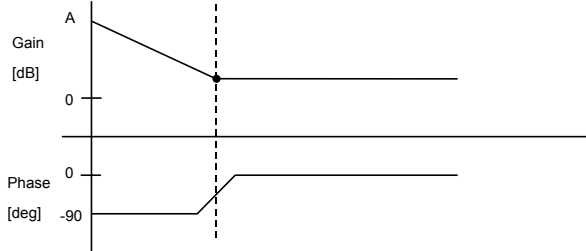


Figure 33. Gain vs Phase

$$F_p = \frac{1}{2 \pi \times R_o \times C_o} \text{ [Hz]}$$

$$f_z(\text{ESR}) = \frac{1}{2 \pi \times \text{ESR} \times C_o} \text{ [Hz]}$$

Pole at the power amplification stage

When the output current reduces, the load resistance R_o increases and the pole frequency lowers.

$$f_p(\text{Min}) = \frac{1}{2 \pi \times R_{O\text{Max}} \times C_o} \text{ [Hz]} \leftarrow \text{at light load}$$

$$f_p(\text{Max}) = \frac{1}{2 \pi \times R_{O\text{Min}} \times C_o} \text{ [Hz]} \leftarrow \text{at heavy load}$$

Zero at the power amplification stage

When the output capacitor is set larger, the pole frequency lowers but the zero frequency will not change. (This is because the capacitor ESR becomes 1/2 when the capacitor becomes 2 times.)

$$f_p(\text{Amp.}) = \frac{1}{2 \pi \times R_c \times C_c} \text{ [Hz]}$$

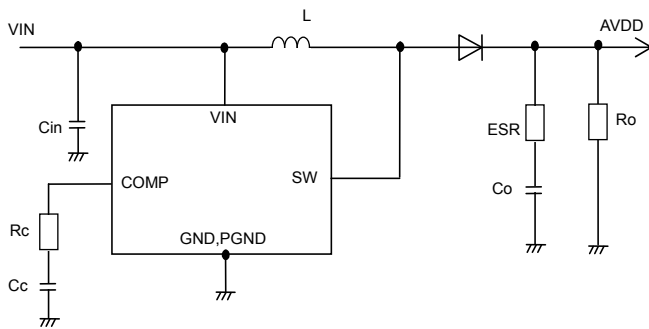


Figure 34. Application Circuit Diagram

It is possible to realize the stable feedback loop by canceling the pole $f_p(\text{Min.})$, which is created by the output capacitor and load resistor, with CR zero compensation of the error amp as shown below.

$$f_z(\text{Amp.}) = f_p(\text{Min.}) \rightarrow \frac{1}{2 \pi \times R_c \times C_c} = \frac{1}{2 \pi \times R_{o\text{max}} \times C_o} \text{ [Hz]}$$

(5) Design of the Feedback Resistor Constant

Refer to the following equation to set the feedback resistor. As the setting range, 6.8 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 6.8 kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.1 μA(Typ.) in the internal error amplifier.

$$AVDD = \frac{R_AVD_U + R_AVD_D}{R_AVD_D} \times FB \quad [V]$$

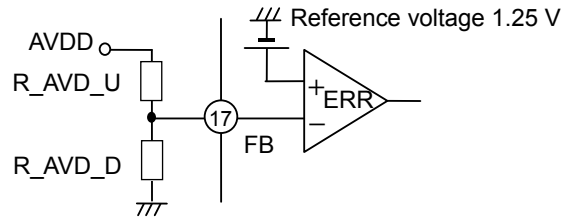


Figure 35. Application Circuit Diagram

(6) Positive-side Charge Pump Settings

The IC incorporates a charge pump controller, thus making it possible to generate stable gate voltage. The output voltage is determined by the following formula. As the setting range, 6.8 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 6.8kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.1 μA (Typ.) in the internal error amp.

$$SRC = \frac{R_SRC_U + R_SRC_D}{R_SRC_D} \times FBP \quad [V]$$

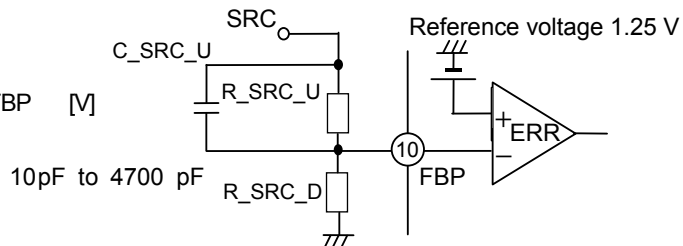


Figure 36. Application Circuit Diagram

In order to prevent output voltage overshooting, add capacitor C_SRC_U in parallel with R_SRC_U. The recommended capacitance is 10 pF to 4700 pF. But please enough evaluate with the actual model because adjustments in the application may be necessary.

Please meet the following condition about the number of the steps of the charge pump. In addition, confirm with an actual model for the last time. Because the loss is increase when a calculation result is the small, please be careful.

$$\frac{SRC}{(n + 1) \times AVDD - 2n \times Vf} < 1 \quad \text{Here, } n \text{ is the steps of charge pump, } Vf \text{ is the forward voltage of diode.}$$

(7) Negative-side Charge Pump Settings

This IC incorporates a charge pump controller for negative voltage, thus making it possible to generate stable gate voltage.

The output voltage is determined by the following formula. As the setting range, 6.8 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 6.8 kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.1 μA (Typ.) in the internal error amp.

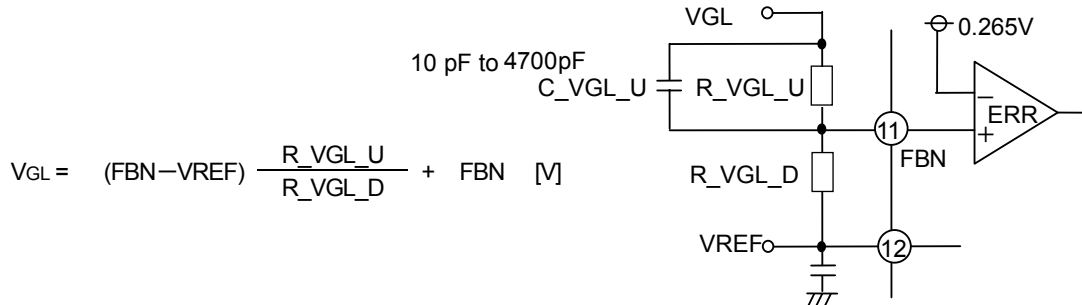


Figure 37. Application Circuit Diagram

In order to prevent output voltage overshooting, insert capacitor C_VGL_U in parallel with R_VGL_U. The recommended capacitance is 10 pF to 4700 pF. But please enough evaluate with the actual model because adjustments in the application may be necessary.

Please meet the following condition about the number of the steps of the charge pump. In addition, confirm with an actual model for the last time. Because the loss is increase when a calculation result is the small, please be careful.

$$\frac{-VGL}{-(n \times AVDD - 2n \times Vf)} < 1$$

Here, n is the steps of charge pump, Vf is the forward voltage of diode.

(8) VCOM Amplifier block

VCOM Amplifier is a rail-to-rail high slew rate Operational Amplifier which has 0V - AVDD voltage (the 1pin (INP) input voltage) as an input and output voltage range.

When add a capacitor to output, 0.1μF – 10μF is recommended for the reason of stability.

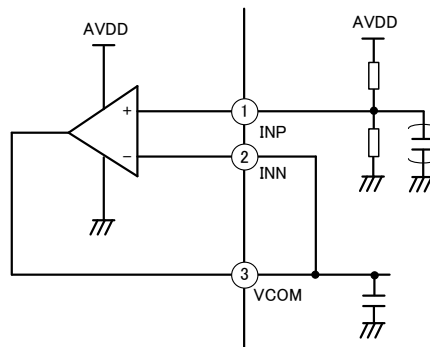


Figure 38. Application Circuit Diagram

(9) Process of unused function

When Gate Shading Function is not used, please proceed each pin (SRC, RE, CTL, DLY) as follows.

- ※The SRC, RE, and CTL must be pulled-down by a resistor (0Ω-10kΩ) or connected to GND.
- The DLY, please connect capacitor because there is the concern such as noises.

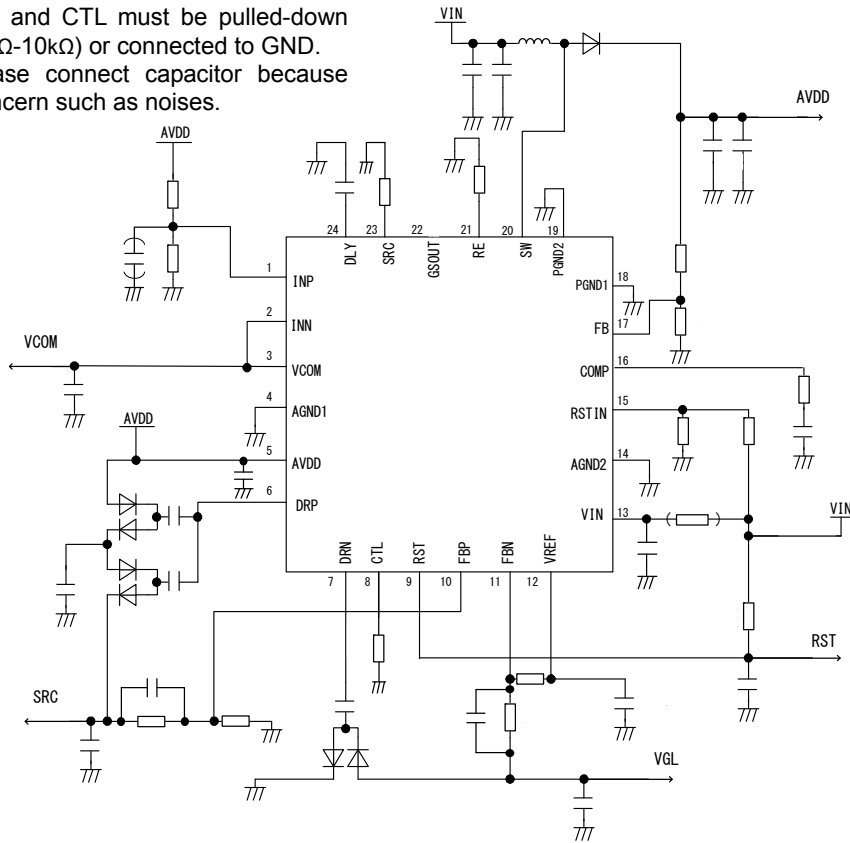


Figure 39. Application Circuit

When VCOM function is not used, please proceed each pin (INP, INN, VCOM) as follows.

- ※The INP must be pulled-down by a resistor (0Ω-10kΩ) or connected to GND.

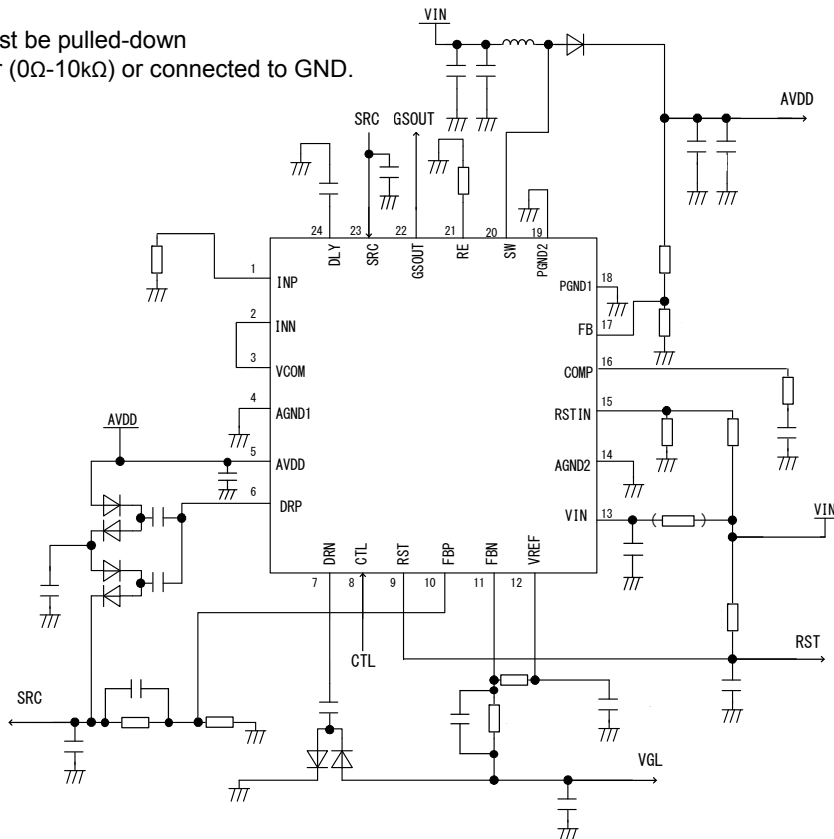


Figure 40. Application Circuit

●PCB Layout Guide

GND Wiring Pattern

The high current GND (PGND) should be wired thick. To reduce line impedance, the GND lines must be as short and thick as possible and uses few via. Therefore design at PCB board four layers or above is recommended. (Please use the middle layer as GND shielding and directly connect each GND.) In the case of two layers or less at PCB board designs, please enough confirm with the actual model about the heat and the noise with care to a GND wiring.

Switching-Line Wiring Pattern

The wiring from switching line (SW pin) of DC/DC converter to inductor and diode must be as short and thick as possible. If a wiring is long, ringing by switching increases, and the voltage over the resistance of this IC might be generated. Please note that switching line does not vary PCB layer. Switching line and wiring easily affected by noise such as feedback line or COMP line must be placed separately. Switching noise spread may cause the lack of operation stability. In case the multi-layer PCB board, please note that a switching line and a line easily affected by noise or the external components are not adjacent between layers. Drawing GND shield line between switching line and these lines easily affected by noise is recommended if these lines are placed close.

Power Supply Voltage Line Wiring Pattern

For power supply voltage (VIN) and internal reference voltage (VREF), place smooth capacitor nearby IC pin. Especially, VIN is a power supply line of internal MOSFET for Boost DC/DC, placing capacitor at distance within 2mm from pin is needed. In addition, wire the VIN line by thickness more than 3mm. Furthermore, insert the resistance (RC filter formation) on VIN line and become stronger in a power supply change. Please note that smooth capacitor does not vary PCB layer.

The figure 41 shows an application circuit on the basis of the basic PCB layout pattern guideline mentioned above.

- ◆ Bold line: High current line
- ◆ Blue line(two dots and dashed line): Wiring easily affected by noise
- ◆ Red line (dashed line): Noise source line such as switching line

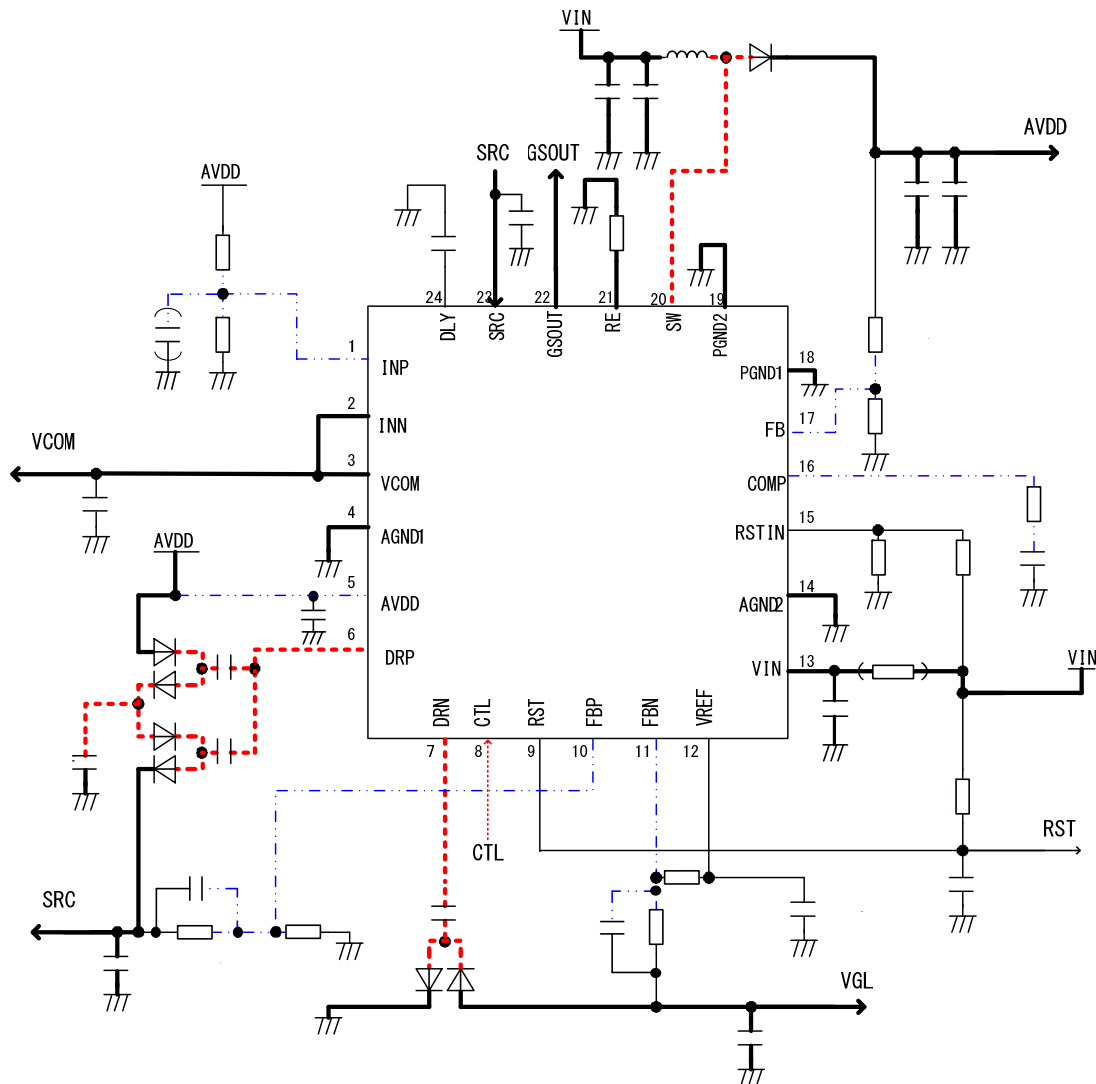


Figure 41. Application Circuit

Recommended Layout Pattern

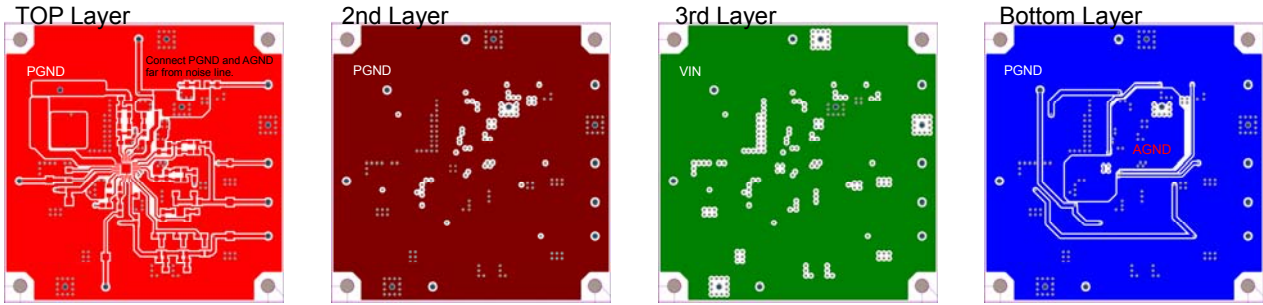


Figure 42. Recommended Layout Pattern

EMC Layout Guide

Introduce the plan that can design on the PCB as EMC measures.

Measures by the board pattern

- ① Wire AVDD line briefly thickly.
- ② Wire the current loop of Boost DC/DC briefly thickly.

Measures by the external component

- ③ Insert a common mode filter or a beads coil in the AVDD line and form the EMC filter.
- ④ Place output capacitor and small capacitor (10pF - 1,000pF) in parallel.
- ⑤ Insert the snubber circuit in SW pin. (Assumed the efficiency becomes worse)

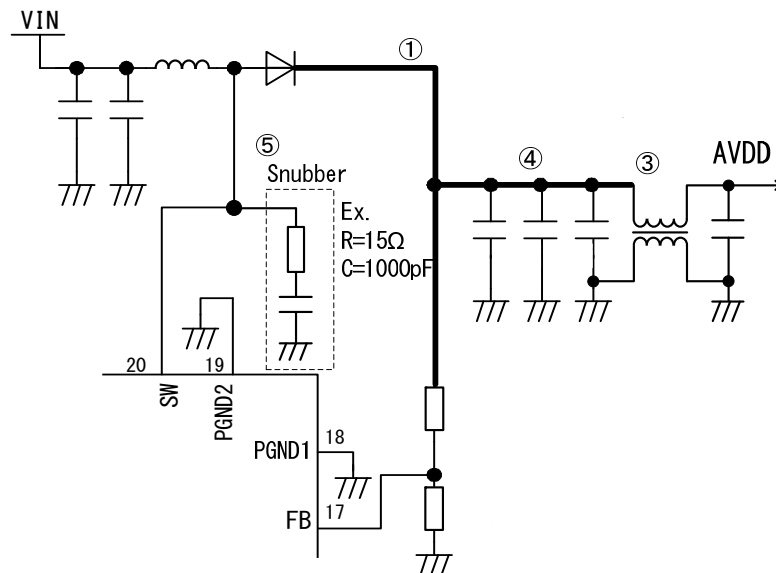


Figure 43. Application Circuit

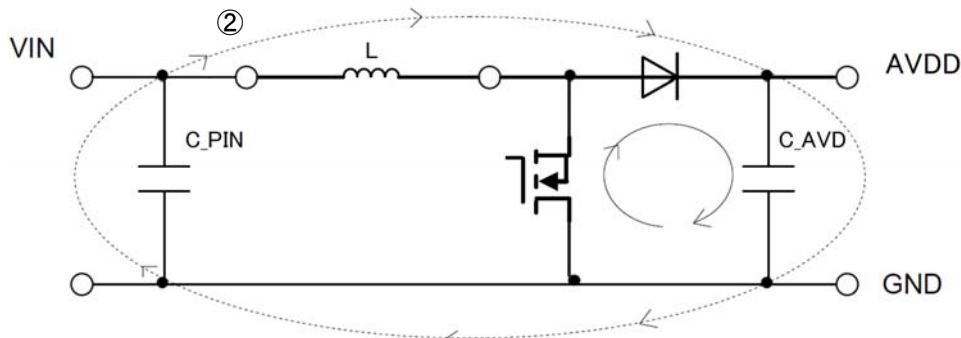


Figure 44. Current loop